PHU78NQ03LT

N-channel TrenchMOS logic level FET

Rev. 06 — 15 June 2009 Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Suitable for high frequency applications due to fast switching characteristics
- Suitable for logic level gate drive sources

1.3 Applications

- Computer motherboards
- DC-to-DC convertors

1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	-	25	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see Figure 1; see Figure 3	-	-	75	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2	-	-	107	W
Dynamic characteristics						
Q_{GD}	gate-drain charge	V_{GS} = 4.5 V; I_D = 25 A; V_{DS} = 12 V; T_j = 25 °C; see Figure 9; see Figure 10	-	4	-	nC
Static characteristics						
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 7; see Figure 8	-	7.65	9	mΩ

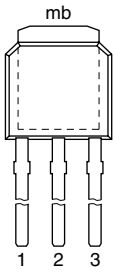
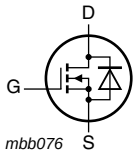
2. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PHU78NQ03LT	IPAK	plastic single-ended package (IPAK); 3 leads (in-line)	SOT533

3. Pinning information

Table 3. Pinning information

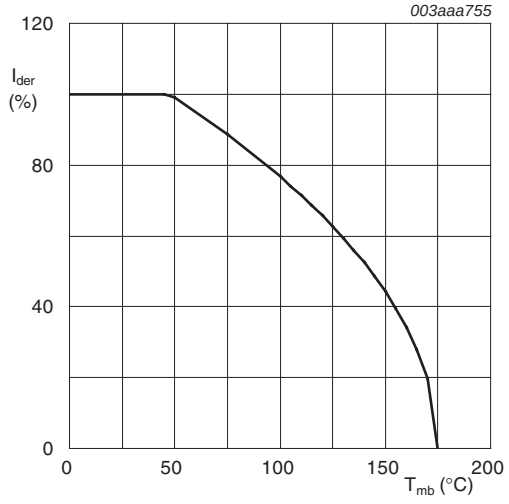
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 **SOT533 (IPAK)**	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

4. Limiting values

Table 4. Limiting values

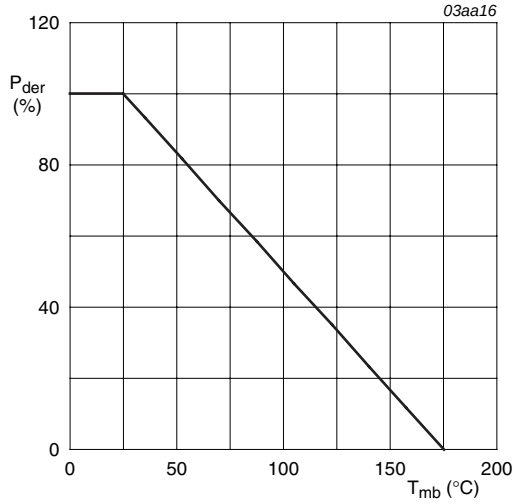
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	25	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20$ kΩ; $T_{mb} \geq 25$ °C; $T_{mb} \leq 175$ °C	-	25	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 5$ V; $T_{mb} = 100$ °C	-	46.9	A
		$V_{GS} = 10$ V; $T_{mb} = 100$ °C; see Figure 1	-	57.5	A
		$V_{GS} = 10$ V; $T_{mb} = 25$ °C; see Figure 1; see Figure 3	-	75	A
		$V_{GS} = 5$ V; $T_{mb} = 25$ °C	-	66.4	A
I_{DM}	peak drain current	$t_p \leq 10$ µs; pulsed; $T_{mb} = 25$ °C; see Figure 3	-	240	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2	-	107	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25$ °C	-	75	A
I_{SM}	peak source current	$t_p \leq 10$ µs; pulsed; $T_{mb} = 25$ °C	-	240	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $I_D = 32$ A; $V_{sup} \leq 25$ V; unclamped; $t_p = 0.17$ ms; $R_{GS} = 50$ Ω	-	100	mJ



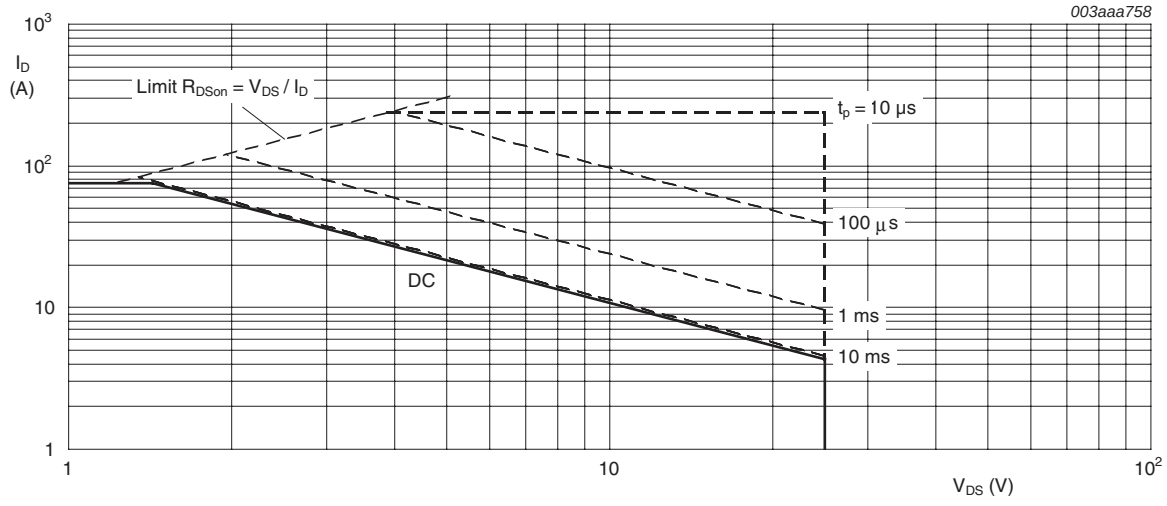
$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25°C; I_{DM}$ is single pulse; $V_{GS} = 10V$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	1.4	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	vertical in free air	-	70	-	K/W

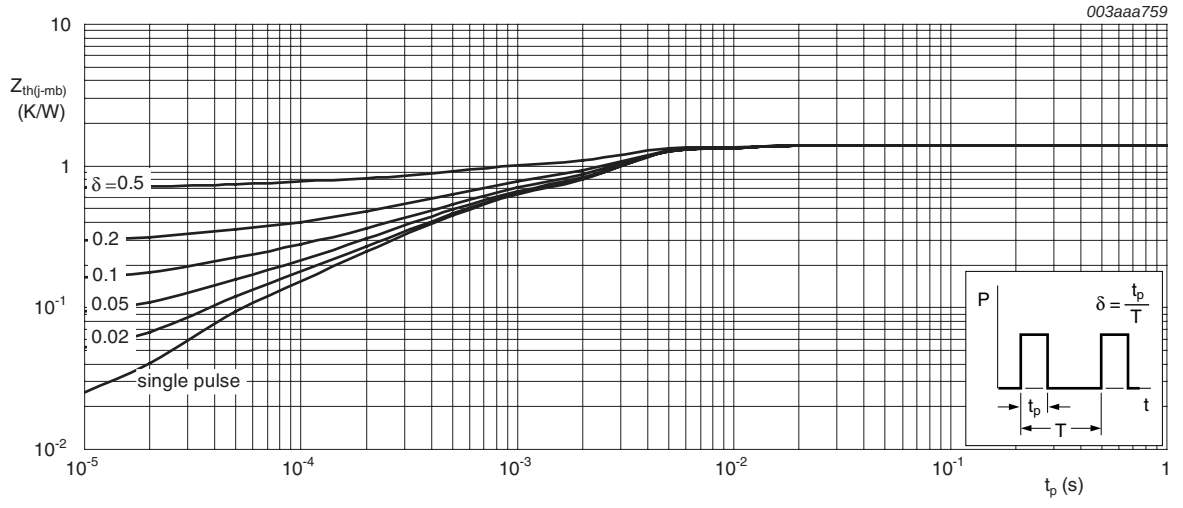


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

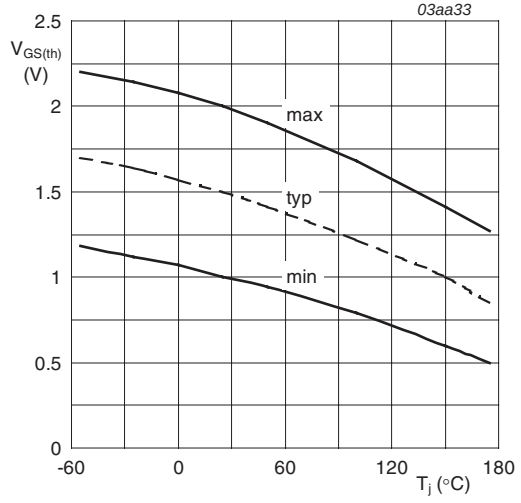
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	22	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	25	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 5; see Figure 6	-	-	2.2	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 5; see Figure 6	0.5	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 5; see Figure 6	1	1.5	2	V
I_{DSS}	drain leakage current	V_{DS} = 25 V; V_{GS} = 0 V; T_j = 25 °C	-	-	1	µA
		V_{DS} = 25 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = 15 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
		V_{GS} = -15 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 7; see Figure 8	-	7.65	9	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 175 °C; see Figure 7; see Figure 8	-	18.9	24.3	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 25 °C; see Figure 7; see Figure 8	-	10.5	13.5	mΩ
R_G	internal gate resistance (AC)	f = 1 MHz; T_j = 25 °C	-	1	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 0 A; V_{DS} = 0 V; V_{GS} = 4.5 V; T_j = 25 °C	-	8.6	-	nC
		I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; T_j = 25 °C; see Figure 9; see Figure 10	-	11	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; T_j = 25 °C; see Figure 10; see Figure 10	-	3.6	-	nC
Q_{GS1}	pre-threshold gate-source charge		-	1.8	-	nC
Q_{GS2}	post-threshold gate-source charge		-	1.8	-	nC
Q_{GD}	gate-drain charge		-	4	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 12 V; T_j = 25 °C; see Figure 9; see Figure 10	-	3	-	V
C_{iss}	input capacitance	V_{DS} = 12 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 11	-	970	-	pF
			-	1460	-	pF
C_{oss}	output capacitance		-	415	-	pF
C_{rss}	reverse transfer capacitance		-	170	-	pF

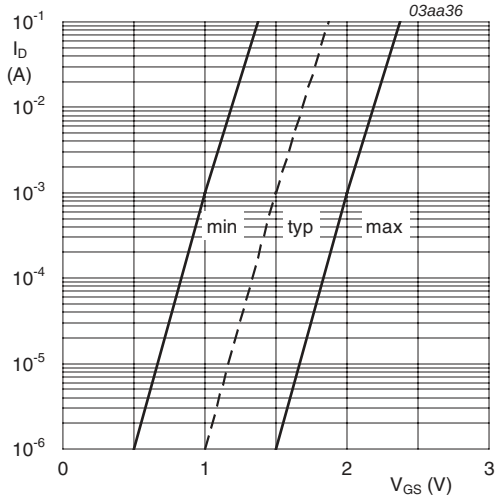
Table 6. Characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	V_{DS} = 12 V; R_L = 0.5 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 5.6 Ω; T_j = 25 °C	-	13	-	ns
t_r	rise time		-	46	-	ns
$t_{d(off)}$	turn-off delay time		-	20	-	ns
t_f	fall time		-	15	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 12	-	0.78	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V; T_j = 25 °C	-	35	-	ns
Q_r	recovered charge		-	20	-	nC



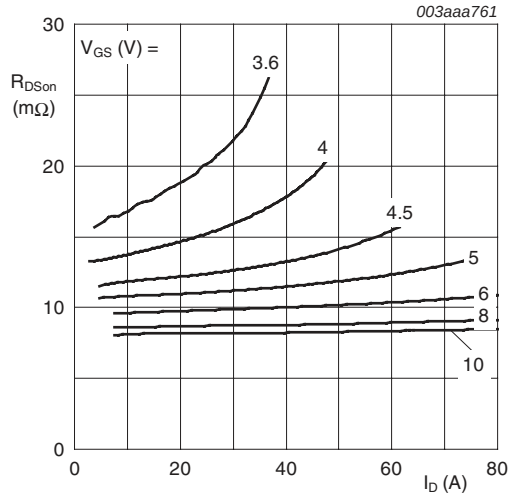
$I_D = 1\,mA; V_{DS} = V_{GS}$

Fig 5. Gate-source threshold voltage as a function of junction temperature



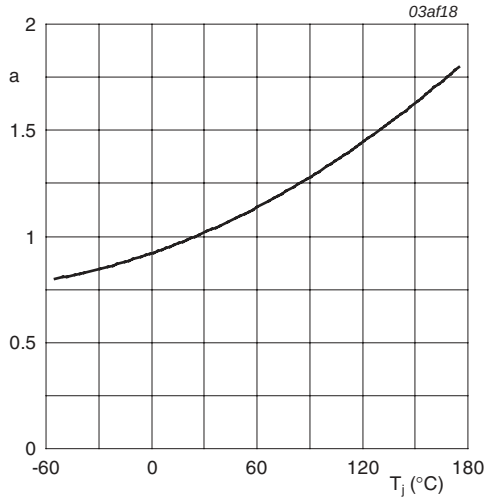
$T_j = 25\,°C; V_{DS} = V_{GS}$

Fig 6. Sub-threshold drain current as a function of gate-source voltage



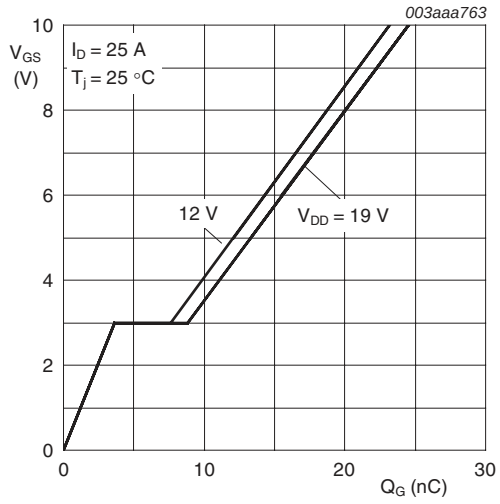
$$T_j = 25°C$$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



$$I_D = 25A; V_{Ds} = 12V \text{ and } 19V$$

Fig 9. Gate-source voltage as a function of gate charge; typical values

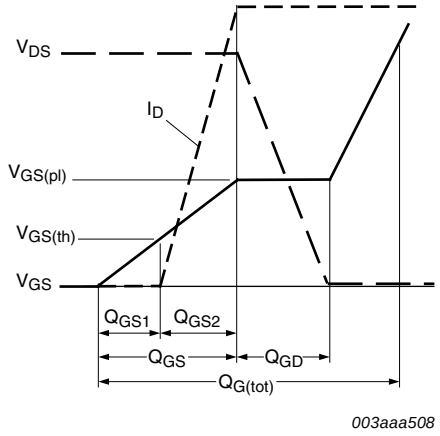
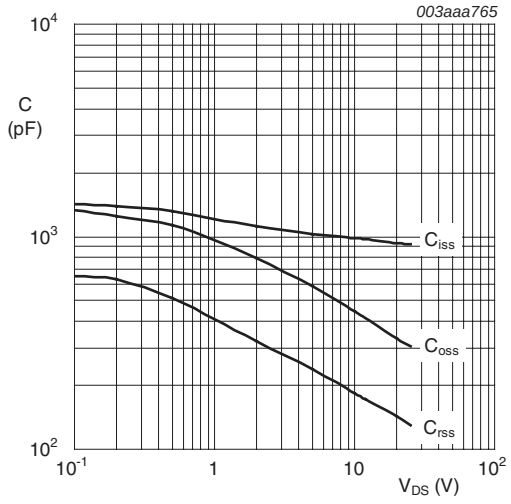
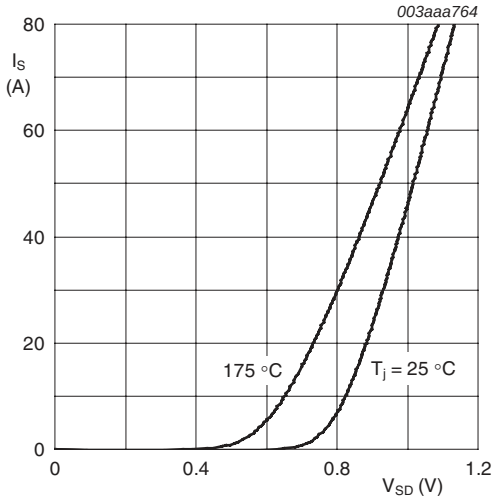


Fig 10. Gate charge waveform definitions



$V_{GS} = 0V; f = 1MHz$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

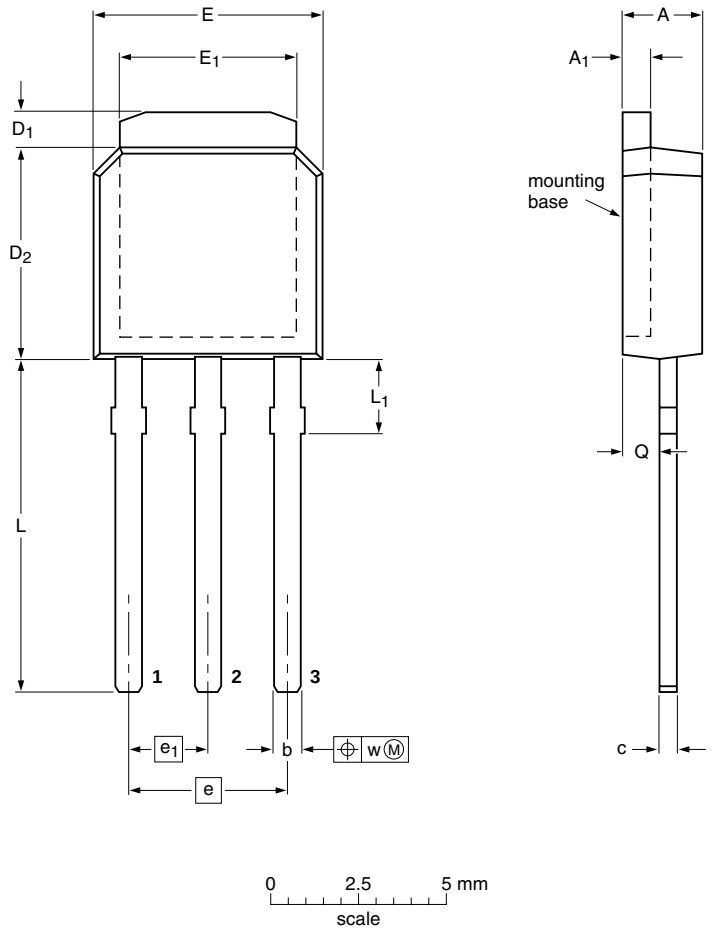


$T_j = 25°C \text{ and } 175°C; V_{GS} = 0V$

Fig 12. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended package (IPAK); 3 leads (in-line) **SOT533**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D_1	D_2	E	E_1	e	e_1	L	L_1 (2) max	Q	w
mm	2.38 2.22	0.93 0.46	0.89 0.71	0.56 0.46	1.10 0.96	6.22 5.98	6.73 6.47	5.21 5.00	4.57 BSC (1)	2.285 BSC (1)	9.6 9.2	2.7	1.1 1.0	0.3

Notes

1. Basic spacing between centers.
2. Terminal dimensions are uncontrolled within zone L_1.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT533		TO-251				~~05-02-11~~ 06-02-14

Fig 13. Package outline SOT533 (IPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHU78NQ03LT_6	20090615	Product data sheet	-	PHU_PHD78NQ03LT_5
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type number PHU78NQ03LT separated from data sheet PHU_PHD78NQ03LT_5.			
PHU_PHD78NQ03LT_5 (9397 750 15084)	20050727	Product data sheet	-	PHP_PHU78NQ03LT_4
PHP_PHU78NQ03LT_4 (9397 750 13431)	20040726	Product data sheet	-	PHP_PHB_PHD78NQ03 LT-03
PHP_PHB_PHD78NQ03 LT-03 (9397 750 09667)	20020626	Product data	-	PHP_PHB_PHD78NQ03 LT-02
PHP_PHB_PHD78NQ03 LT-02 (9397 750 09418)	20020322	Product data	-	PHP_PHB_PHD78NQ03 LT-01
PHP_PHB_PHD78NQ03 LT-01 (9397 750 08916)	20011114	Product data	-	-

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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10. Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

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