ADS5560/62EVM

Contents

List of Figures

List of Tables

1 Overview

This user's guide gives a general overview of the ADS556xEVM evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module. This manual is applicable to the ADS556x. The ADS556xEVM provides a platform for evaluating the 16-bit, 40-/80-MSPS, analog-to-digital converter (ADC) parallel and DDR data output.

Use this document in combination with the respective ADC data sheet.

1.1 ADS556xEVM Quick-Start Procedure

Using the quick-start procedure, many users can begin evaluating the ADC in a short time. The quick-start procedure uses the default conditions of the EVM as shipped from the factory.

1. Five power supply connectors (banana jack), J11 (3.3 V), J13 (3.3 V), J16 (Vss– for amplifier), J20 (5 V), and J12 (GND) on the EVM are used to connect the EVM with offboard dc power supply. It provides supply voltage for all devices on the board. A few options for using supply pairs are shown in Table 1. The default option uses J20 (+5 V) and J12 (GND) to connect with the power supply because 3.3-V and 3.3-V supply voltages are generated on the board for the LDO solution (from 5-V supply voltage).
2. Connector J9 (SMA) is connected to the path of the ADC clock input. It is used to connected ADC clock input with the offboard clock source. A sine-wave clock source is recommended for the default EVM setting.
3. Connectors J6 (SMA) and J8 (SMA) are used to connect the ADC with the offboard analog signal source. At default, J8 is not installed as it is connected to GND. A single-ended analog signal, for example a sine wave, is input to J6. Then, it is converted into a differential signal through transformers T1 and T2 or through T5 and THS4509 to the ADC's differential analog input pins. A few configurations are possible for the analog input path; the default one is the transformer-coupling configuration through T1 and T2.
4. By default the DDR LVDS digital output is brought to connector J10 (Samtec).
5. If using TSW1200 capture board from TI, connect TSW1200 to J10 of the ADS556x EVM and follow the instructions found in Section 4.

2 Circuit Description

2.1 Schematic Diagram

The schematic diagram for the EVM is in Section 5.3.

2.2 EVM Circuit Function

The following sections describe the functions of individual circuits. See the relevant data sheet for device operating characteristics.

2.2.1 EVM Power Connections

Five power supply connectors (banana jack) J11 (3.3 V), J13 (3.3 V), J16 (Vss– for amplifier), J20 (5 V), and J12 (GND) on the EVM are used to connect the EVM to offboard dc power supply to support all devices onboard. A few options for supply connection are shown in Table 1. The default one is using J20 (5 V) and J12 (GND) as well as J16 (for OPA) to connect the EVM with the offboard supply. Two 3.3-V supply voltages can be generated on board from 5 V through U3(TPS79633DCQ), U8 (TPS79633DCQ), and U9 (TPS79601DCQ) as the EVM default setting. Two 3.3-V supply voltages can also be provided from the offboard power supplies through J13 and J11 (see Table 1).

Table 1. EVM Power Supply Connections

	Shorted 1 and 2	Shorted 2 and 3	Default Setting
JP16	3.3 Va is from LDO solution	external 3.3-V supply connects to J13	Shorted 2 and 1
JP17	3.3 Vd is from LDO solution	external 3.3-V supply connects to J11	Shorted 2 and 1

ADS556x EVM also can be powered from the TSW1200EVM (optional). On the TSW1200EVM, J7 is a 6-V wall power supply connector; connect it to 6 V with JP8 (1 to 2 short) and J22 open. The TSW1200EVM can provide a 5-V output at the J15 connector. Connect J15 to the 5-V banana jack on the ADS556xEVM to provide a 5-V supply for the ADS556xEVM.

2.2.2 ADC Analog Input

Connectors J6 (SMA) and J8 (SMA) are used to connect the ADC with the offboard analog signal source. At default, J8 is not installed as it is connected to GND. A single-ended analog signal, for example a sine wave, is input to J6; then, it is converted into a differential signal through transformers T1 and T2 or through T5 and THS4509 to the ADC's differential analog input pins. A few configurations are possible for the analog input path. The default one is a transformer-coupling configuration through T1 and T2. The total ratio of transformers T1 and T2 is 1:1. This configuration gives an equivalent load of 50 Ω to the signal source in a certain frequency range, and it is a default setting from the factory. The common-mode voltage Vcm for the analog input of ADC is provided from the ADC's CM pin. R81, C74, and R68 form a low-pass filter to filter the glitch from the sample and hold stage.

Another analog input configuration for the ADC input is through the fully differential THS4509 amplifier. To receive an analog signal from the THS4059, it needs to switch the connection on SJP5 and SJP3, and SJP1 and SJP2 (see Table 2); the analog source signal is connected to J6 for a signal-ended signal source. The source signal is coupled by the 1:1 transformer T5 to THS4509. It is gained by 10 dB through the amplifier and filtered by a LC low-pass or band-pass filter (users can configure it through a flexible layout), then through transformers T1 and T2 to the ADC differential input. The ADC's CM pin provides the common-mode voltage Vcm for the THS4509. By default, the THS4509 path is not connected to the input of ADS556x. To use THS4509 driving the analog input of ADS556x, JP1, JP2, JP3, and JP5 need to be reconnected from the default position as shown in the Table 2.

Table 2. Analog Input Selection Through Surface-Mount Jumpers

	SJP3	SJP5	SJP1	SJP2
Transformer single-ended (SE) input through J6	Short 1 to 2	Short 1 to 2	Short 1 to 2	Short 1 to 2
OPA SE input through J6	Short 2 to 3	Short 2 to 3	Short 2 to 3	Short 2 to 3

2.2.3 ADC Clock Input

The ADC clock input is from connector J9, a single-ended (SE) clock source connector. The SE clock is converted into a differential clock through the 1:4 transformer to the ADC clock input pins. The resistor R29 is a 50-Ω source termination. A sine wave with a 1.5-V amplitude can be used for the evaluation test.

2.2.4 ADC Digital Output

The digital output of ADS556x is brought to the 40-pin IDC connector J5 for CMOS parallel output; it is also brought to a high-density Samtec connector J10 for DDR LVDS output as a default setting (interface to TSW1200). The connectors J5 and J10 can be accessed by a logic analyzer and other CMOS digital interface directly, for example, the TSW1200 data capture board (through J10). The connector J10 can be extended by the TI ADC breakout board to interface with the LVDS receiver including the logic analyzer. If the CMOS parallel output is used, the U7 (SN74AVC16244DGGR) must be installed.

2.2.5 Jumper Selections for ADS556x Configuration

The EVM features different models of the ADS556x for evaluation. The model selection is based on an internal control register setting. To access the internal control registers, the ADS556x provides three access interfaces, parallel interface, serial interface, and parallel and serial mixed interface. The default

setting for the EVM is parallel interface, where the RESET pin is tied to high (AVdd) through JP12. The interface includes six pins: SCLK, SEN, SDATA, DFS, and MODE plus a RESET pin. The detail functions of these pins are described in the data sheet. On the EVM, these control pins are connected to jumpers JP9, JP11, J12, and J1 to J3. Table 3 to Table 5 describe all possible settings of these jumpers. For the function of each setting, see the data sheet.

Table 3. Jumper Setting for Control Interface

	Parallel interface (default setting)	Serial interface
JP12 (RESET)	Short 1 to 2	Short 2 to 3
JP11 (SDATA)	Floating 2 (normal) or Short 1 to 2	Short 2 to 3
JP9 (SEN)	Short 1 to 2	Short 2 to 3

Table 4. Jumper Setting for Control Pins SEN, DFS, and MODE at Parallel Interface

	AVdd	**(5/8)AVdd**	**(3/8)AVdd**	**GND**
J1 (SEN: short 1 to 2 on JP9)	Short 7 to 8	Short 5 to 6	Short 3 to 4	Short 1 to 2
J2 (DFS)	Short 7 to 8	Short 5 to 6	Short 3 to 4	Short 1 to 2
J3 (MODE)	Short 7 to 8	Short 5 to 6	Short 3 to 4	Short 1 to 2

Table 5. Jumper Setting for Control Pins SDATA and SCLK at Parallel Interface

	3.3 V	**GND (default setting)**
JP11 (SDATA)	Short 2 to 1	Pin 2 is float
SCLK		Float

3 Serial Interface Control

For serial interface access, SEN, SDATA, and SCLK function as serial interface pins and are used to access the internal registers of the ADC. Their relative jumper settings are shown in Table 3. The pins DFS and MODE must be set to GND through jumpers J2 (short 1 to 2) and J3 (short 1 to 2) at serial interface control. The serial interface control is implemented by an ADC SPI control software installed on the PC and a USB port (J17) on the EVM. For evaluating the ADC, it is unnecessary for users to use a serial interface. Users only need the serial interface software when the desired feature is inaccessible by the parallel interface mode.

3.1 Installing the AD SPI Control Software

The ADC SPI control software can be installed on a personal computer by running the setup.exe file located on the CD. This file installs the graphical user interface (GUI) along with the USB drivers needed to communicate to the USB port that resides on the EVM. After the software is installed and the USB cable has been plugged in for the first time, the user is prompted to complete the installation of the USB drivers. When prompted, allow the Windows™ operating system to search for device drivers. It automatically finds the TI ADC SPI Interface drivers. Figure 1 shows the SPI interface. Click the right top button to select the ADS556x device.

Note: Before plugging in the USB cable for the first time, install the TI ADC SPI software. The software installs the necessary drivers for USB communication.

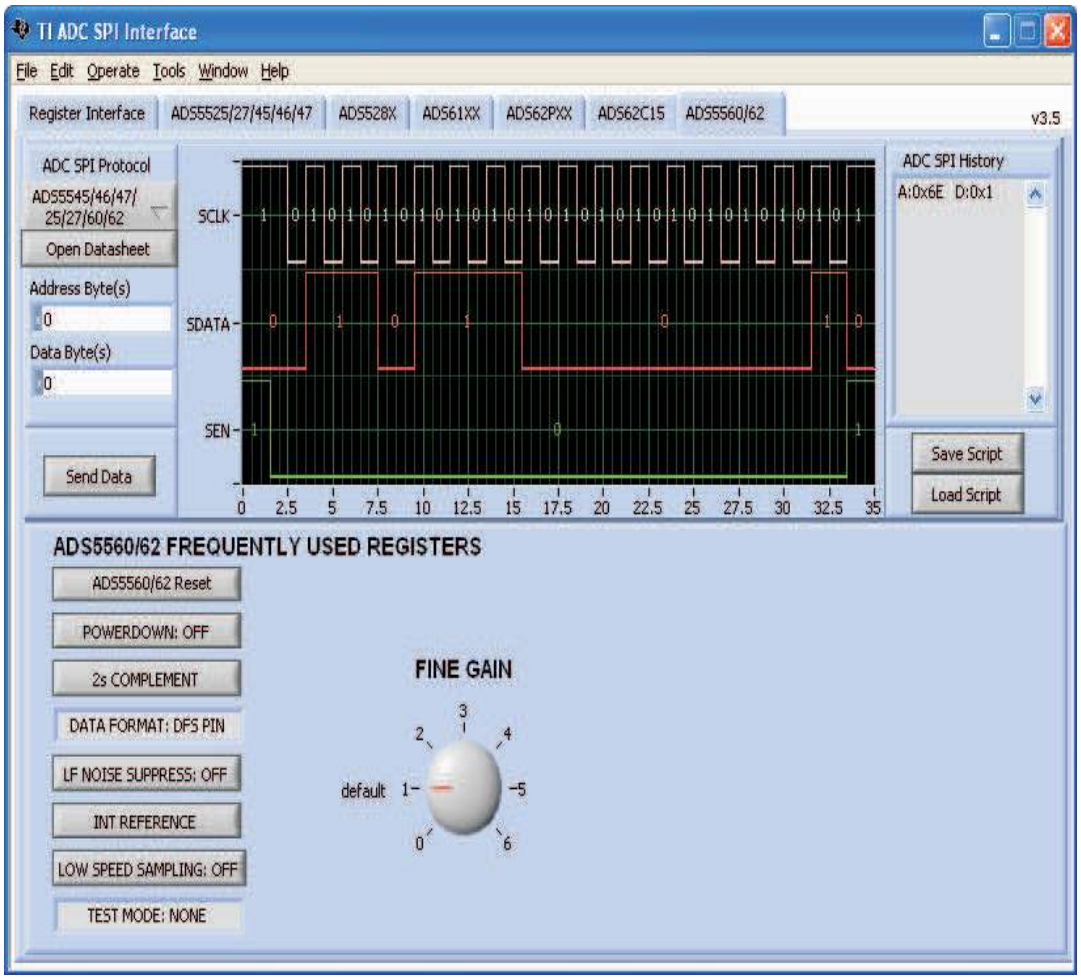


Figure 1. TI ADC SPC Interface Screen

3.2 Using the ADC SPI Interface Software

Once the software is installed and the USB cable is connected, three primary modes of operating the software are available: SPI Register Writes, SPI Register Write Using a Script File, and ADC Frequently Used Registers.

3.2.1 SPI Register Writes

The most basic mode of operation allows full control of writing to individual register addresses. In the top left corner of the interface screen, select the ADS5545/46/47/25/27/60/62 from the ADC SPI Protocol drop-down list. Next, type the Address Bytes(s) in hexadecimal (hex) and Data Byte(s) in hex which can be found in the device data sheet. When you are ready to send this command to the ADC, press "Enter" on your keyboard, or press "Send Data". The graph indicator is updated with the patterns sent to the ADC. The default inputs to both the Address Byte(s) and Data Byte(s) fields are hex inputs as designated by the small "x" in the control. Users can change the default input style by clicking on the "x" to binary, decimal, octal, or hex. Multiple register writes can be written simply by changing the contents of the Address Byte(s) and Data Byte(s) field, and pressing Enter again.

3.2.2 SPI Register Write Using a Script File

For situations where the same multiple registers need to be written on a frequent basis, users can easily create a script file using a test editor containing all ADC register writes. An example Script File is located in the \\Install Directory\Script Files\ADS6145_LVDS_CourseGain.txt. Users who wish to take advantage of writing their own script files can start by using the ADS6145_LVDS_CourseGain.txt as a template file. When ready to write the contents of the script file to the ADC, users can press the Load Script button, and they are prompted for the file location of their script file. The commands are sent to the ADC when the user acknowledges the selection of the file.

3.2.3 ADS556x Frequently Used Registers

For ease of use, several buttons have been added that allow one-click register writes of commonly used features found in Table 6. The software writes to the ADC both the contents of the associated address and data when the button is clicked. When the ADSxxxx Reset button is pressed, it issues a software reset to the ADC, and it resets the button values to match the contents inside of the ADC. The graph indicator plots the SPI commands written to the ADC when a button has been depressed.

Table 6. Frequently Used Registers

Default Value	Alternate Value
ADSxxxx Reset	
2s Complement	Straight binary
CMOS/LVDS : DFS pin determines	DDR LVDS/CMOS
Powerdown: OFF	Powerdown on
Fine gain: 1	Up to 6-dB gain
INT reference	EXT reference
LVDS current: 3.5 mA	Multiple options
Test mode: None	Multiple options
Low sampling speed: off	Low sampling speed: on
LF noise suppression: off	LF noise suppression: on

3.2.4 Using Both Serial Interface and Parallel Controls

For increased flexibility, a combination of serial interface registers and parallel pin controls (DFS, MODE) also can be used to configure the device. For more details, see the data sheet .

3.3 TSW1200 Capture Board

The TSW1200 board can be used to analyze the performance of the EVM. The TSW1200EVM is a circuit board that assists designers in prototyping and evaluating the performance of high-speed ADCs that feature parallel or serialized LVDS outputs. The TSW1200 has the LVDS 100-Ω termination resistor on the input interface for ADC outputs. For more information, see the TSW1200EVM user's guide (SLAU212).

To start the TSW1200 software, note the following points.

1. Select the ADC type to be used before capturing.
2. For test, select Single Tone FFT plot.
3. For the ADC Sampling Rate, type in the value.
4. Type in the ADC Input Frequency. Auto calculation of the input frequency depends on the FFT record length. As soon as the number is entered, the software calculates the coherent input frequency corresponding to that FFT length. This frequency signal must be supplied through the signal generator.
5. Select the FFT Record Length.
6. Select Capture to obtain the plot.
7. The Continuous Capture option is used if the user wants to continuously capture the FFT.

Adjust the input level signal to attain the dBFs of approximately –1.

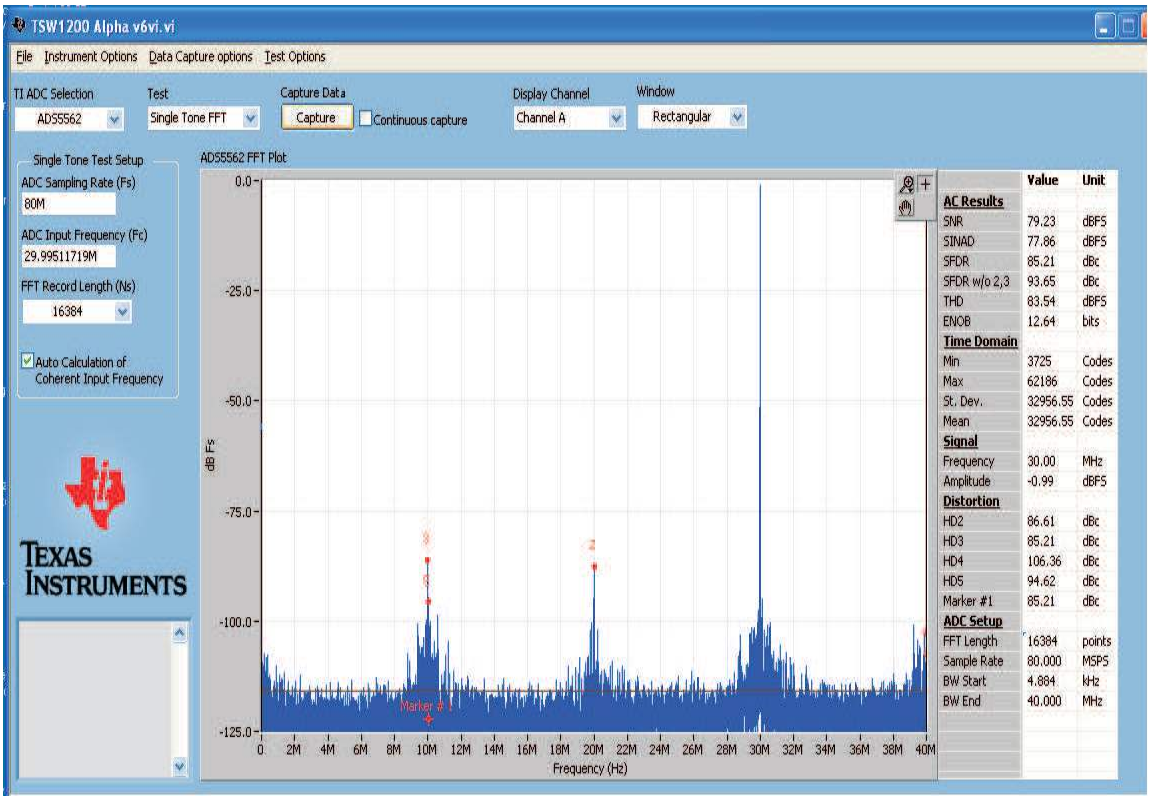


Figure 2. TSW1200 GUI Introduction

4 ADC Evaluation

This section describes how to set up a typical ADC evaluation system that is similar to what TI uses to perform testing for data-sheet generation. Consequently, the information in this section is generic in nature and is applicable to all high-speed, high-resolution ADC evaluations. This section covers signal tone analysis, which yields ADC data-sheet figures of merit such as signal-to-noise ratio (SNR) and spurious free dynamic range (SFDR).

4.1 Hardware Selection

To reveal the true performance of the ADC under evaluation, take great care in selecting both the ADC signal source and the ADC clocking source.

4.1.1 Analog Input Signal Generator

When choosing the quality of the ADC analog input source, consider both harmonic distortion performance of the signal generator and the noise performance of the source. In many cases, the harmonic distortion performance of the signal generator is inferior to that of the ADC, and additional filtering is needed if users expect to reproduce the ADC SFDR numbers found in the data sheet. Users can easily evaluate the harmonic distortion of their signal generator by hooking it directly to a spectrum analyzer and measuring the power of the output signal and comparing that to the power of the integer multiples of the output signal's frequency. If the harmonic distortion is worse than the ADC under evaluation, the ADC digitizes the performance of the signal generator and the true SFDR of the ADC is masked. To avoid this, TI recommends that users provide additional LC filtering (BPF) after the signal generator output. Another important metric when deciding on a signal generator is its noise performance. As with the distortion performance, if the noise performance is worse than that of the ADC under evaluation, the ADC digitizes

the performance of the source. Noise can be broken into two components, broadband noise and close-in phase noise. Broadband noise can be improved by the LC filter added to improve distortion performance. The close-in phase noise, however, typically cannot be improved by additional filtering. Therefore, when selecting an analog signal source, it is important to review the manufacturer's phase noise plots and take care to choose a signal generator with the best phase-noise performance.

4.1.2 Clock Signal Generator

Equally important in the high-performance ADC evaluation setup is the selection of the clocking source. Most modern ADCs accept either a sinusoidal or a square-wave clock input. The key metric in selecting a clocking source is selecting a source with the lowest jitter. This becomes increasingly important as the ADC input frequency (Fin) increases, because the ADC SNR evaluation setups can become jitter-limited (To) as shown by the following equation.

$$SNR\ (dBc) = 20 \log [2\pi \times Fin \times Tj(rms)]$$

In theory, a square-wave source with femtosecond jitter is ideal for an ADC evaluation setup. However, in practical terms, most commercially available square-wave generators offer jitter measured in picoseconds, which is too great for high-resolution ADC evaluation setups. Therefore, most evaluation setups rely on the ADC's internal clock buffer to convert a sinusoidal input signal into a ultralow-jitter square wave. When selecting a sinusoidal clocking source, it has been shown that phase noise has a direct impact on jitter performance. Consequently, great scrutiny must be applied to the phase-noise performance of the clocking signal generator. TI has found that high-Q monolithic crystal filters can improve the phase noise of the signal generator, and these filters become essential elements of the evaluation setup when high ADC input frequencies are being evaluated.

4.2 Coherent Input Frequency Selection

Typical ADC analysis requires users to collect the resulting time-domain data and perform a Fourier transform to analyze the data in the frequency domain. A stipulation of the Fourier transform is that the signal must be continuous-time. However, this is impractical when looking at a finite set of ADC samples, usually collected from a logic analyzer. Consequently, users typically apply a window function to minimize the time-domain discontinuities that arise when analyzing a finite set of samples. For ADC analysis, window functions have their own frequency signatures or lobes that distort both SNR and SFDR measurements of the ADC. TI uses the concept of coherent sampling to work around the use of a window function. The central premise of coherent sampling entails that the input signal into the ADC is carefully chosen such that when a continuous-time signal is reconstructed from a finite sample set, no time-domain discontinuities exist. To achieve this, the input frequency must be an integer multiple of the ratio of the ADC's sample rate (f_s) and the number of samples collected from the logic analyzer (N_s). The ratio of f_s to N_s is typically referred to as the fundamental frequency (f_f). Determining the ADC input frequency is a two-step process. First, users select the frequency of interest for evaluating the ADC; then, they divide this by the fundamental frequency. This typically yields a noninteger value, which must be rounded to the nearest odd, preferably prime, integer. Once that integer, or frequency bin (f_{bin}), has been determined, users multiply this with the fundamental frequency to obtain a coherent frequency to program into their ADC input signal generator. The procedure is summarized as follows.

$f_f = f_s/N_s$
$f_{bin} = Odd\_round(f_{desired}/f_f)$
Coherent frequency = $f_f \times f_{bin}$

5 Physical Description

This section describes the physical characteristics and PCB layout of the EVM.

5.1 PCB Layout

The EVM is constructed on a 6-layer, 0.062-inch thick PCB using FR-4 material. The individual layers are shown in Figure 3 through Figure 6. The layout features a split ground plane; however, similar performance can be had with a careful layout using a common ground plane.

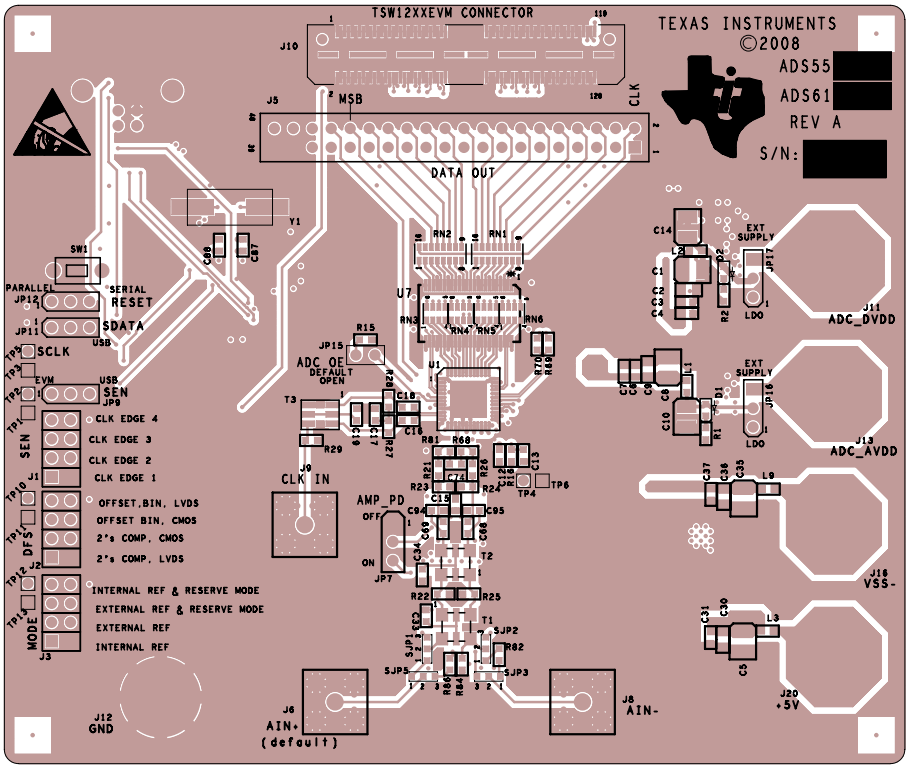


Figure 3. Top Silkscreen

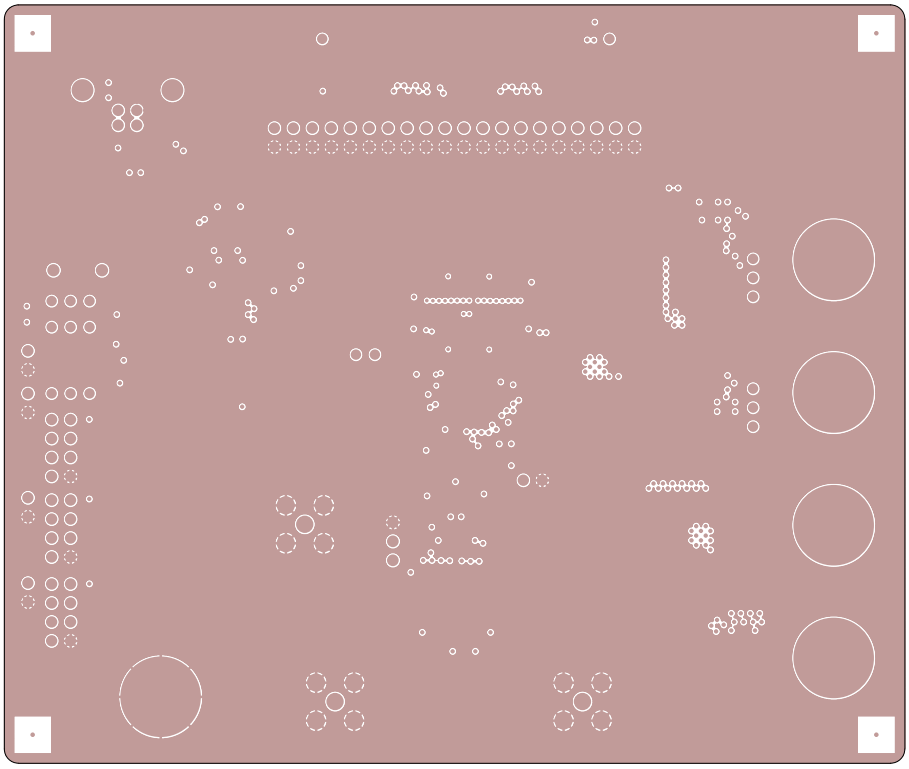


Figure 4. Ground Plane

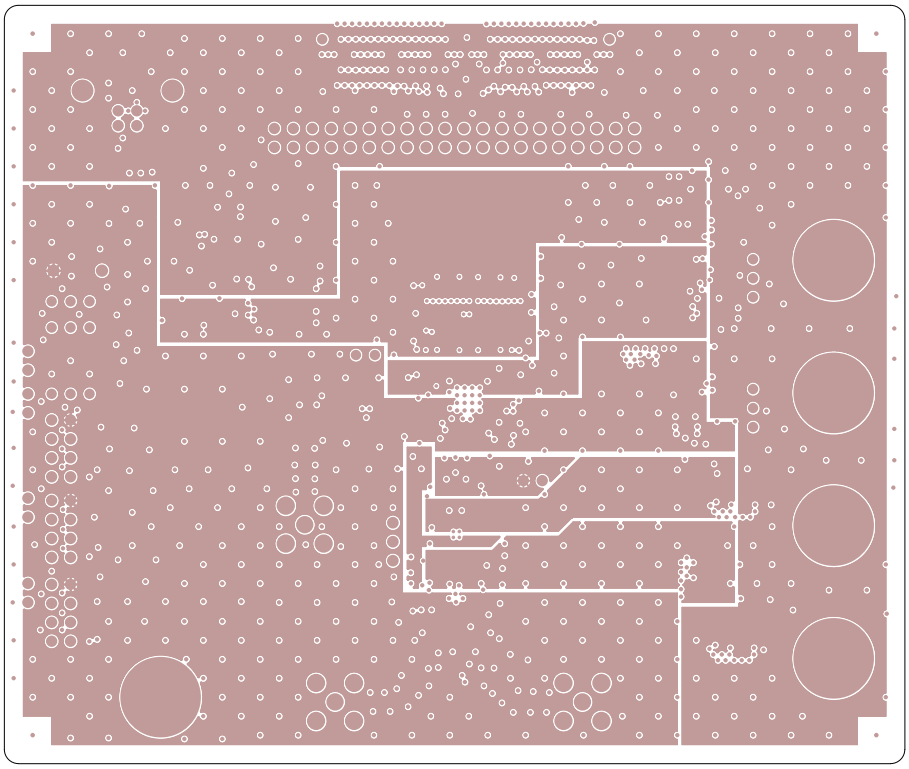


Figure 5. Power Plane

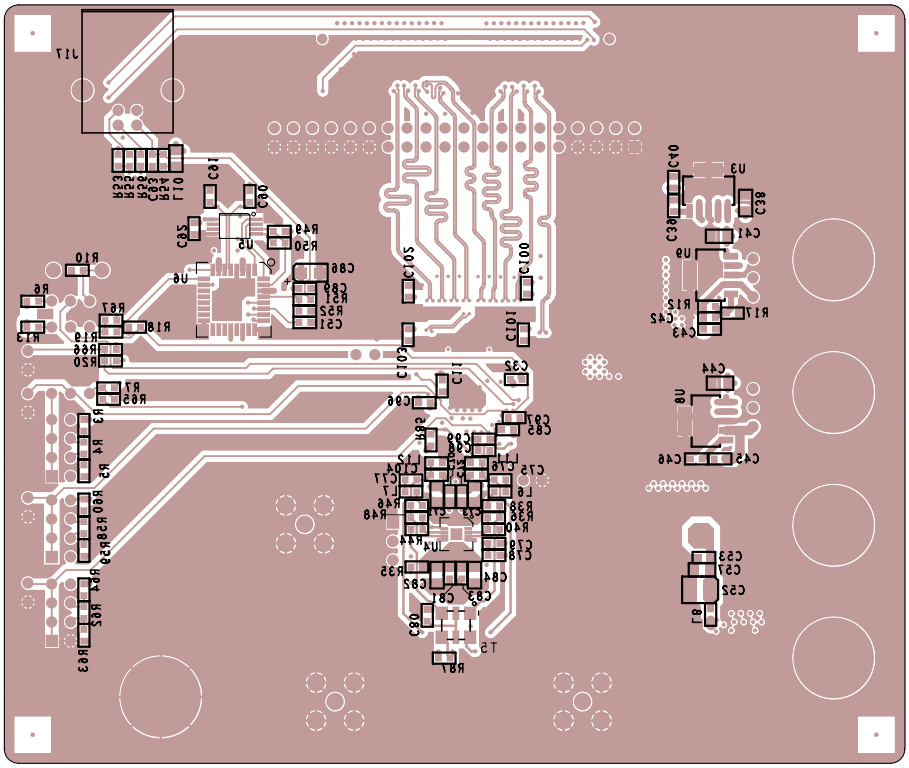


Figure 6. Bottom Silkscreen

5.2 Bill of Materials

Table 7. ADS61B49EVM Bill of Materials

QTY	Reference	Not Installed	Part	Foot Print	Part Number	Manufacturer	Tolerance	Volt	Watt
5	C1, C5, C8, C35, C52		33 µF	TANT_B	B45196H2336M209	Kemet	20%	10V	
5	C2, C9, C30, C36, C57		10 µF	805	ECJ-2FB0J106K	Panasonic	10%	6.3V	
2	C3, C6		1 µF	603	ECJ-1VB1A105K	Panasonic	10%	10V	
32	C4, C7, C11–C13, C16–C19, C32, C37, C53, C70, C72, C78–C81, C83, C85, C87–C89, C92, C96–C103		0.1 µF	603	ECJ-1VB1C104K	Panasonic	10%	16V	
2	C10, C14		22 µF	TANT_B	T491B226M016AT	KEMET	20%	16V	
5	C15, C33, C34, C68, C69		0.1 µF	603	GRM188R71H104KA93D	Murata	5%	50V	
4	C31, C40, C43, C45		1 µF	603	GRM188R61E105KA12D	Murata	10%	25V	
3	C38, C41, C44		2.2 µF	805	GRM21BR71E225KA73L	Murata	10%	25V	
2	C39, C46		0.01 µF	603	GCM188R71H103KA37D	Murata	10%	50V	
1	C42		33 pF	603	06031A330FAT2A	AVX	1%	100V	
1	C51		33 nF	603	06035C333KAT2A	AVX	10%	50V	
4	C71, C73, C82, C84		10uF	805	ECJ-2FB1A106K	Panasonic	10%	10V	
1	C74		3.3 pF	603	GRM1885C1H3R3CZ01D	Murata	±0.25 pF	50V	
0	C75, C77	Not Installed	47 pF	603	ECJ-1VC1H470J	Panasonic	5%	50V	
0	C76, C104	Not Installed	5 pF	603	ECJ-1VC1H050C	Panasonic	±0.25 pF	50V	
1	C86		10 µF	TANT_A	T491A106M010AT	Kemet	20%	10V	
2	C90, C91		27 pF	603	GRM1885C2A270JA01D	Murata	5%	100V	
1	C93		0.01 µF	603	C0603C103K1RACTU	Kemet	10%	100V	
2	C94, C95		5.6 pF	603	GRM1885C1H5R6DZ01D	Murata	±0.5 pF	50V	
1	D1		Green	diode_0603	LNJ312G8TRA	Panasonic			
1	D2		Yellow	diode_0603	SML-311YTT86	ROHM			
1	JP11		Jumper_1x3	HDR_THVT_1x3_100	22-28-4030	Molex			
5	JP9,JP7, JP12, JP16, JP17		Header 3POS 0.1 CTR	JUMPER3	22-28-4030	Molex	Short pins 1-2 with shunt connector DigiKey # S9000-ND (see Figure 7)		
1	JP15		Header 2/SM	JUMPER2	22-28-4020	Molex			
3	J1, J2, J3		Header 4x2	hdr4X2_100ctr	90131-0124	Molex	Short pins 1-2 with shunt connector DigiKey # S9000-ND (see Figure 7)		
1	J5		Header male 20x2 POS 0.100 VERT	CON20X2_100ctr_M_tsw1100_mate	PBC20DAAN	Samtec			
2	J6, J9		SMA	SMA_THVT_320x320	142-0701-201	Johnson Components			
0	J8	Not Installed	SMA	SMA_THVT_320x320	142-0701-201	Johnson Components			
1	J10		CONN_QTH_30X2-D-A	conn_QTH_30X2-D-A	QTH-060-02-F-D-A	Samtec			
4	J11, J13, J16, J20		RED	BANANA_JACK	ST-351A	Allied Electronics			
1	J12		BLK	BANANA_JACK	ST-351B	Allied Electronics			
1	J17		CONN USB TYP B FEM	conn_usb_typb_fem	897-43-004-90-000	Milmax			
5	L1–L3, L8, L9		68	603	MI0603J680R-10	Steward			
0	L6, L7	Not Installed	150nH	603	0603-151J	API Delavan Inc.	5%		
1	L10		1K at 100 MHz	805	BLM21AG102SN1D	Murata			
0	L11, L12	Not Installed	47 nH	603	PE-0603CD470JTT	Pulse	5%		
2	RN1, RN2		22	rnet8_16_0603	MNR18E0APJ220	ROHM	5%		62.5mW
4	RN3–RN6		0 Ω	rnet4_8_0603	TC164-JR-070RL				
1	R1		750	603	ERJ-3EKF7500V	Panasonic	1%		
1	R2		402	603	MCR03EZPFX4020	ROHM	1%		
9	R3–R5, R58–R60, R62–R64		1K	603	ERJ-3EKF1001V	Panasonic	1%		1/10W
5	R6, R10, R15, R18, R35		10K	603	ERJ-3EKF1002V	Panasonic	1%		1/10W

Table 7. ADS61B49EVM Bill of Materials (continued)

QTY	Reference	Not Installed	Part	Foot Print	Part Number	Manufacturer	Tolerance	Volt	Watt
6	R7, R65–R67, R69, R70		0 Ω	603	ERJ-3GEY0R00V	Panasonic	5%		1/10W
1	R12		14K	603	RC0603FR-0714KL	Yageo	1%		1/10W
5	R13, R19, R20, R40, R44		100	603	ERJ-3EKF1000V	Panasonic	1%		1/10W
1	R16	Not Installed	10	603	ERJ-3EKF10R0V	Panasonic	1%		1/10W
1	R17		30.1K	603	MCR03EZPFX3012	ROHM	1%		1/10W
2	R21, R26		4.99	603	CRCW06034R99FNEA	Dale/Vishay	1%		1/10W
0	R22 ,R25	Not Installed	49.9	603	ERJ-3EKF49R9V	Panasonic	1%		1/10W
2	R23, R24		24.9	603	ERJ-3EKF24R9V	Panasonic	1%		1/10W
0	R27, R28	Not Installed	121	603	ERJ-3EKF1210V	Panasonic	1%		1/10W
3	R29, R68, R81		49.9	603	ERJ-3EKF49R9V	Panasonic	1%		1/10W
2	R36, R48		348	603	ERJ-3EKF3480V	Panasonic	1%		1/10W
0	R38, R46	Not Installed	68	603	MCR03EZPFX68R0	ROHM	1%		1/10W
1	R49		10K	603	ERJ-3GEYJ103V	Panasonic	5%		1/10W
1	R50		2.21K	603	ERJ-3EKF2211V	Panasonic	1%		1/10W
1	R51		4.7K	603	ERJ-3EKF4R71V	Panasonic	1%		1/10W
0	R52	Not Installed	10K	603	ERJ-3EKF1002V	Panasonic	1%		1/10W
1	R53		1.5K	603	ERJ-3EKF1501V	Panasonic	5%		1/10W
0	R54	Not Installed	0 Ω	603	ERJ-3GEY0R00V	Panasonic	5%		1/10W
2	R55, R56		26.7	603	ERJ-3EKF26R7V	Panasonic	1%		1/10W
0	R82	Not Installed	ZERO	603	ERJ-3GEY0R00V	Panasonic	5%		1/10W
2	R84, R87		ZERO	603	ERJ-3GEY0R00V	Panasonic	5%		1/10W
1	R85		ZERO	603	ERJ-3GEY0R00V	Panasonic	5%		1/8W
0	R86	Not Installed	ZERO	603	ERJ-3GEY0R00V	Panasonic	5%		1/8W
4	SJP1–SJP3, SJP5		JUMPER_1x3_SMT	smd_bridge_0603			Short 1-2 using 0 Ω resistors		
1	SW1		SW Pushbutton	SW_RESET_PTS635	PTS635SL43	C & K Switch			
5	TP1, TP3, TP6, TP11, TP13		Test Point Black	testpoint	5001	Keystone			
5	TP2, TP4, TP5, TP10, TP12		Test Point White	testpoint	5002	Keystone			
3	T1, T2, T5		WBC1-1	XFMR_WBC4-1W	WBC1-1TL	Coilcraft			
1	T3		TC4-1T	XFMR_TC4-1W	TC4-1T	Mini Circuits			
1	U1		ADS61X9	QFN48		TI			
2	U3, U8		TPS79633DCQ	SOT_223_6_TG	TPS79633DCQR	TI			
1	U4		THS4509	QFN16	THS4509RGTT	TI			
1	U5		93C66B	TSSOP8	93C66B-I/ST	Microchip			
1	U6		FT245BM	PQFP32	FT245BM	Future Technology Devices			
0	U7	Not Installed	SN74AVC16244DGGR	TSSOP_48_496x244_20					
1	U9		TPS79601DCQ	SOT_223_6_TG	TPS79601DCQR	TI			
1	Y1		6.0000 MHz	smd_csm-7_xtal	ECS-60-32-5PDN-TR	ECS			
	Screw machine, ph 4-40 X 3/8		PMS 440 0038 PH	Building Fasteners	PCB legs				
	Stand-off hex 0.5/4-40THR		1902C	Keystone Electronic					

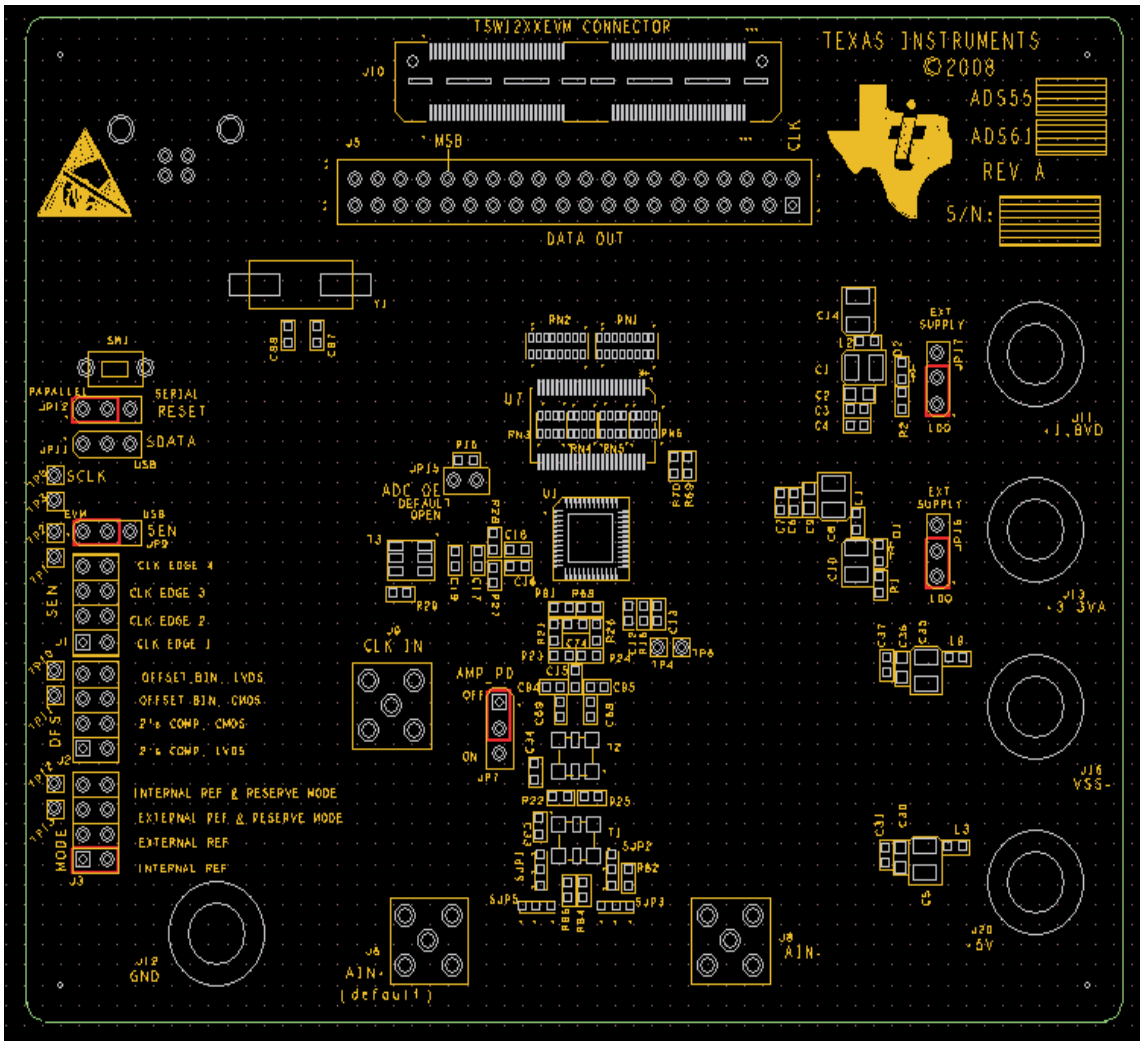
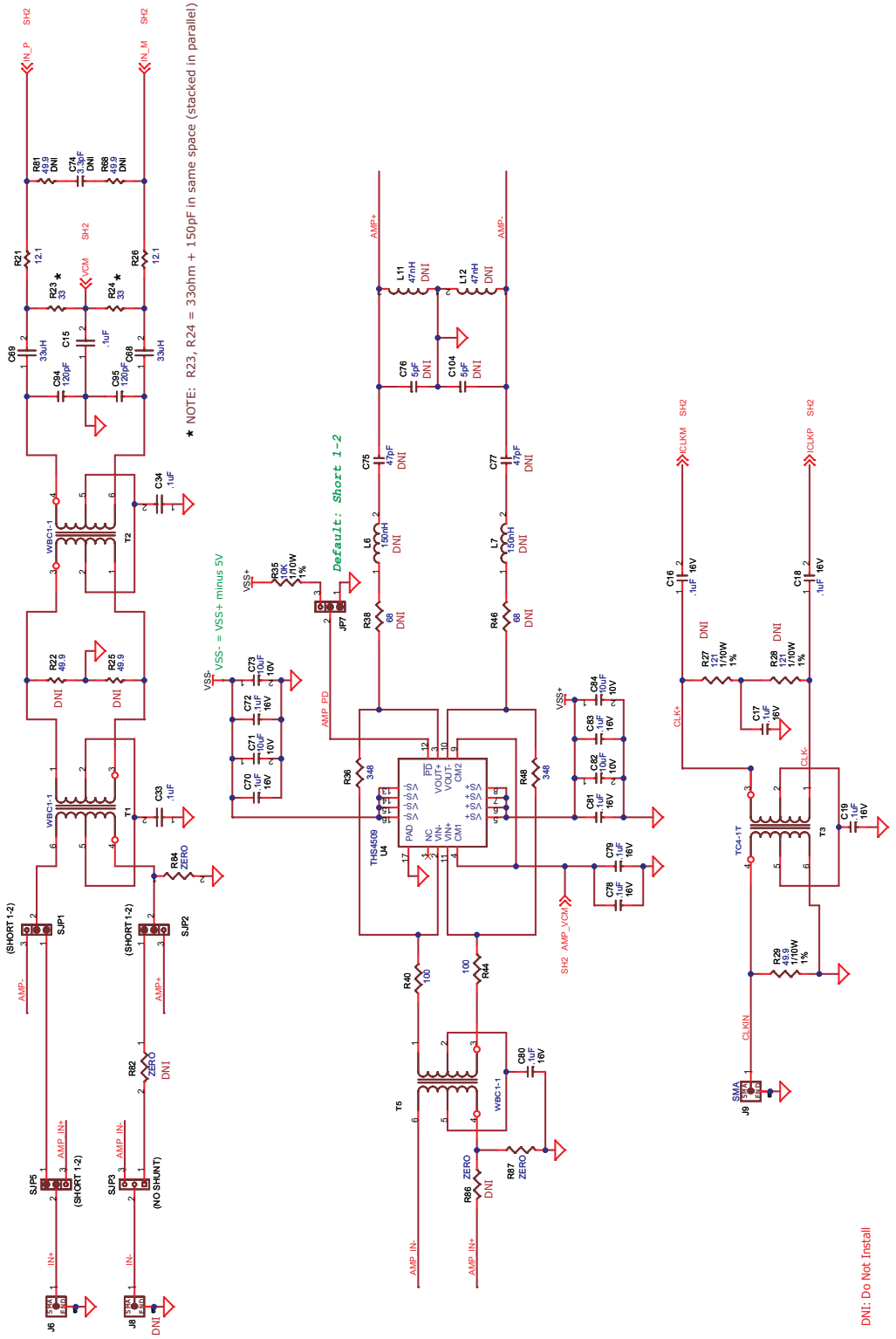
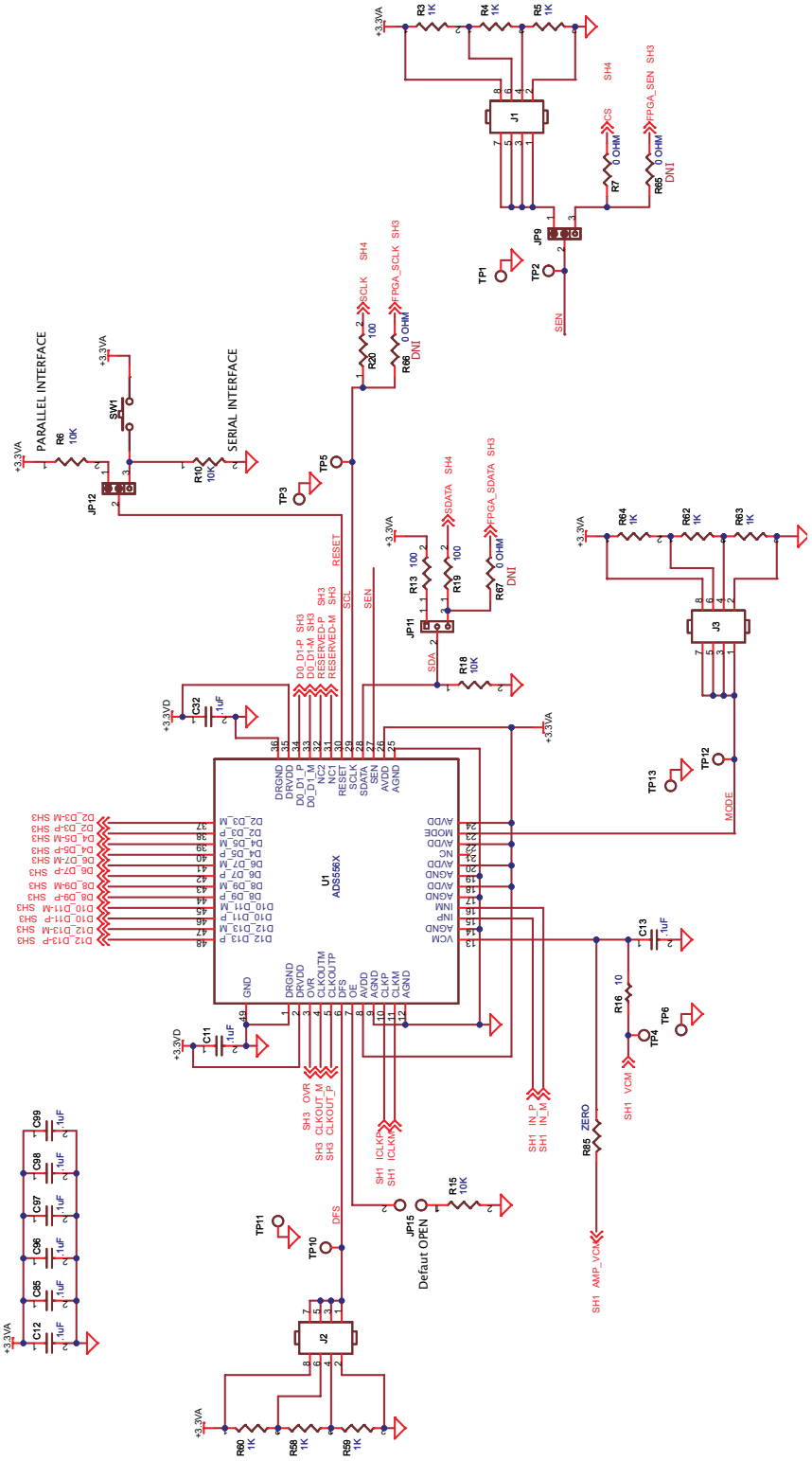
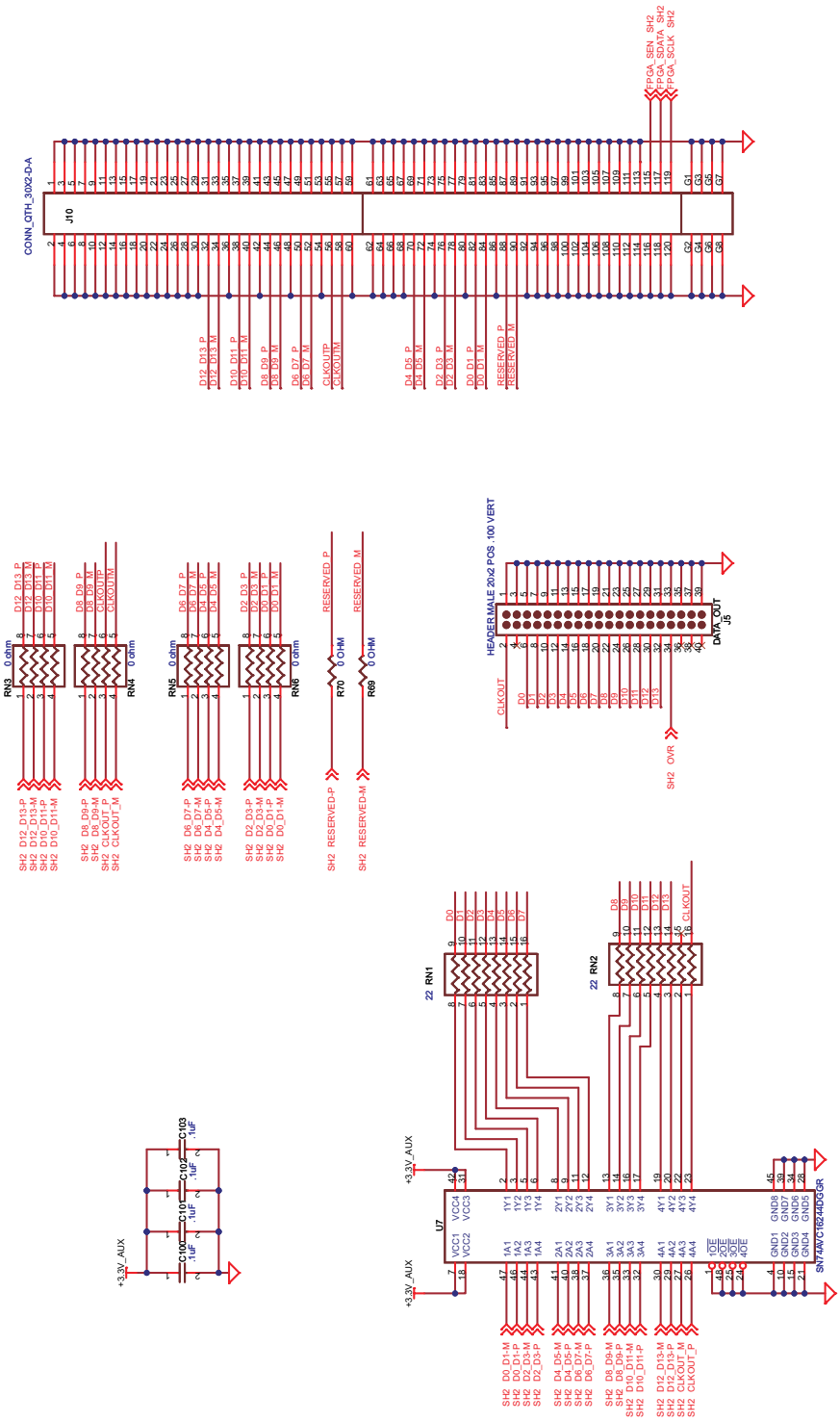


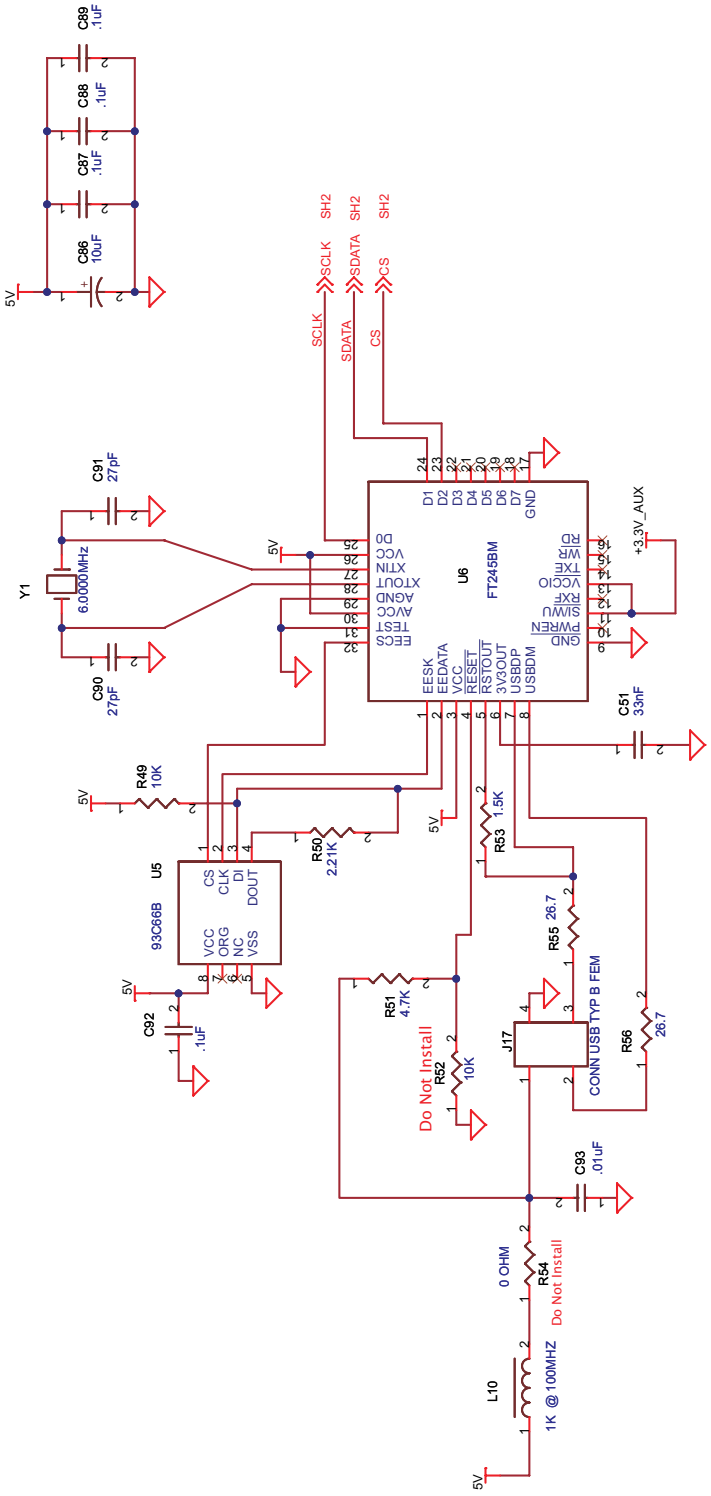
Figure 7. TSW12XXEVM – Connector

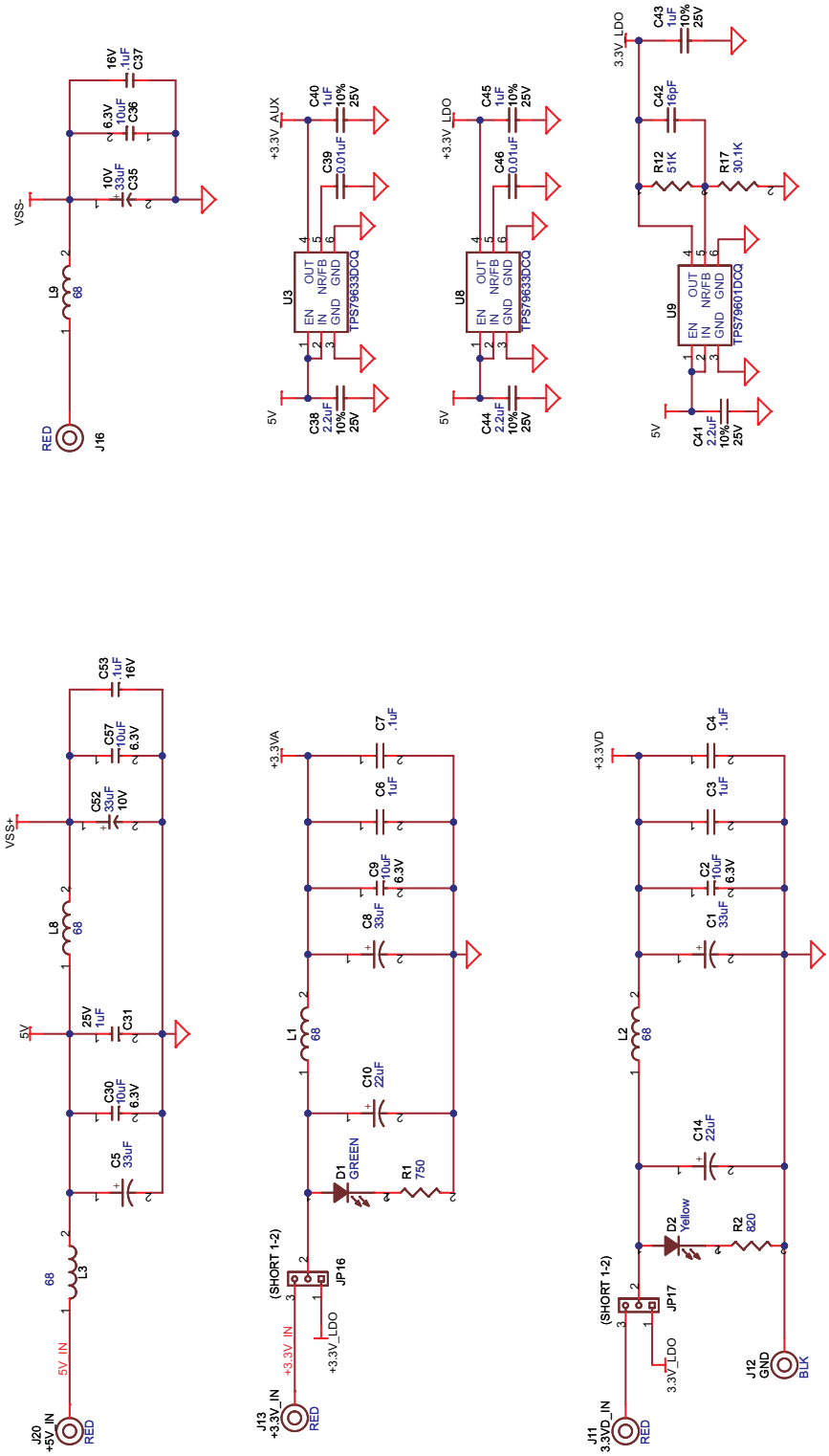
5.3 EVM Schematics




PARALLEL INTERFACE
SERIAL INTERFACE
U1
ADS556X
J1
J2
J3
JP9
JP11
JP12
JP15
Defaut OPEN
SW1
TP1
TP2
TP3
TP4
TP5
TP6
TP10
TP11
TP12
TP13
SEN
SDA
SCLK
RESET
MODE
ZERO
VCM
DFS
+3.3VA
+3.3VD




C89 .1uF
C88 .1uF
C87 .1uF
C86 10uF
5V
SCLK
SDATA
CS
SH2
C91 27pF
Y1 6.000MHz
C90 27pF
U6 FT245BM
D0 D1 D2 D3 D4 D5 D6 D7 GND
VCC XTIN XTOUT AGND AVCC TEST EECS
EESK EEDATA VCC RESET 3V3OUT USBDP USBDM
RD WR TXE VCCIO RXF SIWU PWREN GND
+3.3V_AUX
C51 33nF
R49 10K
R50 2.21K
R53 1.5K
U5 93C66B
CS CLK DI DOUT
VCC ORG NC VSS
C92 .1uF
R51 4.7K
R52 10K
Do Not Install
R55 26.7
J17 CONN USB TYP B FEM
R56 26.7
C93 .01uF
R54 0 OHM Do Not Install
L10 1K @ 100MHZ


VSS-
16V
.1uF
C37
6.3V
10uF
C36
10V
33uF
C35
L9
68
RED
J16
+3.3V_AUX
C40
1uF
10%
25V
C39
0.01uF
U3
EN
IN
GND
OUT
NR/FB
GND
TPS79633DCQ
5V
C38
2.2uF
10%
25V
+3.3V_LDO
C45
1uF
10%
25V
C46
0.01uF
U8
TPS79633DCQ
C44
2.2uF
10%
25V
3.3V_LDO
C43
1uF
10%
25V
C42
16pF
R12
51K
R17
30.1K
U9
TPS79601DCQ
C41
2.2uF
10%
25V
VSS+
C53
.1uF
16V
C57
10uF
6.3V
C52
33uF
10V
L8
68
5V
25V
1uF
C31
C30
10uF
6.3V
C5
33uF
L3
68
5V IN
J20
+5V_IN
RED
+3.3VA
C7
.1uF
C6
1uF
C9
10uF
6.3V
C8
33uF
L1
68
C10
22uF
D1
GREEN
R1
750
(SHORT 1-2)
JP16
+3.3V_IN
+3.3V_LDO
J13
+3.3V_IN
RED
+3.3VD
C4
.1uF
C3
1uF
C2
10uF
6.3V
C1
33uF
L2
68
C14
22uF
D2
Yellow
R2
820
(SHORT 1-2)
JP17
3.3V_LDO
J12
GND
BLK
J11
3.3VD_IN
RED

EVALUATION BOARD/KIT IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive.**

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the analog input voltage range of -0.3 V to AVDD + 0.3 V and the analog output voltage range of -0.3 V to DRVDD. AVDD and DRVDD voltage range is -0.3 V to 3.9 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 25°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Clocks and Timers	www.ti.com/clocks	Digital Control	www.ti.com/digitalcontrol
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265