+3.3 V to +5 V Quad/Octal 10-Bit DACs

AD7804/AD7805/AD7808/AD7809

FEATURES

Four 10-Bit DACs in One Package
Serial and Parallel Loading Facilities Available
- **AD7804 Quad 10-Bit Serial Loading**
- **AD7805 Quad 10-Bit Parallel Loading**
- **AD7808 Octal 10-Bit Serial Loading**
- **AD7809 Octal 10-Bit Parallel Loading**

+3.3 V to +5 V Operation
Power-Down Mode
Power-On Reset
Standby Mode (All DACs/Individual DACs)
Low Power All CMOS Construction
10-Bit Resolution
Double Buffered DAC Registers
Dual External Reference Capability

APPLICATIONS

Optical Disk Drives
Instrumentation and Communication Systems
Process Control and Voltage Setpoint Control
Trim Potentiometer Replacement
Automatic Calibration

GENERAL DESCRIPTION

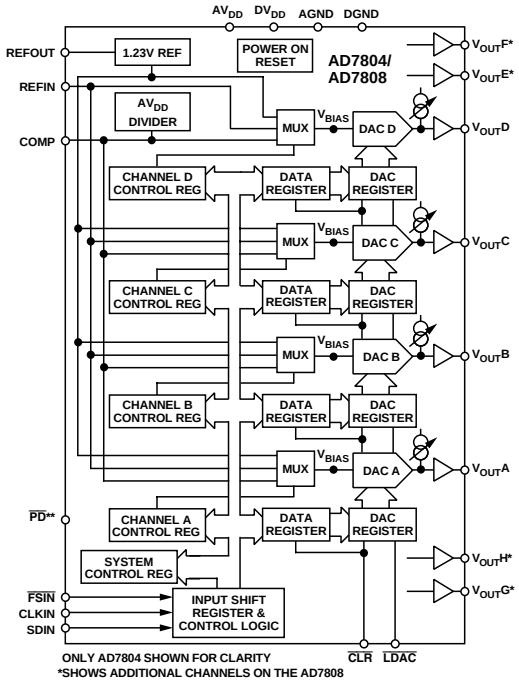
The AD7804/AD7808 are quad/octal 10-bit digital-to-analog converters, with serial load capabilities, while the AD7805/AD7809 are quad/octal 10-bit digital-to-analog converters with parallel load capabilities. These parts operate from a +3.3 V to +5 V (±10%) power supply and incorporates an on-chip reference. These DACs provide output signals in the form of $V_{BIAS} \pm V_{SWING}$. V_{SWING} is derived internally from V_{BIAS}. On-chip control registers include a system control register and channel control registers. The system control register has control over all DACs in the package. The channel control registers allow individual control of DACs. The complete transfer function of each individual DAC can be shifted around the V_{BIAS} point using an on-chip Sub DAC. All DACs contain double buffered data inputs, which allow all analog outputs to be simultaneously updated using the asynchronous LDAC input.

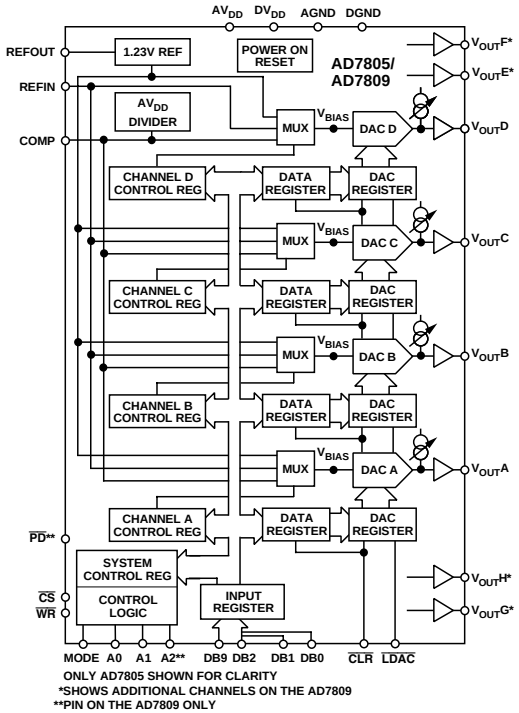
Control Features	Channels Controlled	Main DAC	Sub DAC
Hardware Clear	All	√	√
System Control			
Power Down[1]	All	√	√
System Standby[2]	All	√	√
System Clear	All	√	
Input Coding	All	√	√
Channel Control			
Channel Standby[2]	Selective	√	√
Channel Clear	Selective	√	
V_{BIAS}	Selective	√	√

NOTES
[1]Power-down function powers down all internal circuitry including the reference.
[2]Standby functions power down all circuitry except for the reference.

REV. A

FUNCTIONAL BLOCK DIAGRAMS





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AD7804/AD7805–SPECIFICATIONS

(AV_{DD} and DV_{DD} = 3.3 V ± 10% to 5 V ± 10%; AGND = DGND = 0 V; Reference = Internal Reference; C_L = 100 pF; R_L = 2 kΩ to GND. Sub DAC at Midscale. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Grade[1]	C Grade[1]	Units	Comments
STATIC PERFORMANCE				
MAIN DAC				
Resolution	10	10	Bits	
Relative Accuracy	±3	±3	LSB max	
Gain Error	±3	±3	% FSR max	
Bias Offset Error[2]	–80/+40	–80/+40	mV max	DAC Code = 0.5 Full Scale
Zero-Scale Error[3]	$\frac{-V_{BIAS}}{16}$ / +40	$\frac{-V_{BIAS}}{16}$ / +40	mV max	DAC Code = 000H for Offset Binary
Monotonicity	9	10	Bits	and 200H for Twos Complement Coding
Minimum Load Resistance	2	2	kΩ min	
SUB DAC				
Resolution	8	8	Bits	
Differential Nonlinearity	±0.125	±0.125	LSB typ	Refers to an LSB of the Main DAC
	±0.5	±0.5	LSB max	
OUTPUT CHARACTERISTICS				
Output Voltage Range[3]	$V_{BIAS} \pm 15/16 \times V_{BIAS}$	$V_{BIAS} \pm 15/16 \times V_{BIAS}$	V	Twos Complement Coding
	$V_{BIAS}/16$ to $31/16 \times V_{BIAS}$	$V_{BIAS}/16$ to $31/16 \times V_{BIAS}$	V	Offset Binary Coding
Voltage Output Settling Time to 10 Bits	4	4	µs max	Typically 1.5 µs
Slew Rate	2.5	2.5	V/µs typ	
Digital-to-Analog Glitch Impulse	1	1	nV-s typ	1 LSB Change Around the Major Carry
Digital Feedthrough	0.5	0.5	nV-s typ	
Digital Crosstalk	0.5	0.5	nV-s typ	
Analog Crosstalk	±0.2	±0.2	LSB typ	
DC Output Impedance	2	2	Ω typ	
Power Supply Rejection Ratio	0.002	0.002	%/% typ	ΔV_{DD} ± 10%
DAC REFERENCE INPUTS				
REF IN Range	1.0 to $V_{DD}/2$	1.0 to $V_{DD}/2$	V min to V max	
REF IN Input Leakage	±1	±1	µA max	Typically ±1 nA
DIGITAL INPUTS				
Input High Voltage, V_{IH} @ V_{DD} = 5 V	2.4	2.4	V min	
Input High Voltage, V_{IH} @ V_{DD} = 3.3 V	2.1	2.1	V min	
Input Low Voltage, V_{IL} @ V_{DD} = 5 V	0.8	0.8	V max	
Input Low Voltage, V_{IL} @ V_{DD} = 3.3 V	0.6	0.6	V max	
Input Leakage Current	±10	µA max		
Input Capacitance	10	10	pF max	
Input Coding	Twos Comp/Binary	Twos Comp/Binary		
REFERENCE OUTPUT				
REF OUT Output Voltage	1.23	1.23	V nom	
REF OUT Error	±8	±8	% max	
REF OUT Temperature Coefficient	–100	–100	ppm/°C typ	
REF OUT Output Impedance	5	5	kΩ nom	
POWER REQUIREMENTS				
V_{DD} (AV_{DD} and DV_{DD})	3/5.5	3/5.5	V min to V max	
I_{DD} (AI_{DD} Plus DI_{DD})				Excluding Load Currents
Normal Mode	12	12	mA max	$V_{IH} = V_{DD}$, V_{IL} = DGND
System Standby (SSTBY) Mode	250	250	µA	$V_{IH} = V_{DD}$, V_{IL} = DGND
Power-Down ($\overline{PD}$) Mode				
@ +25°C	0.8	0.8	µA max	$V_{IH} = V_{DD}$, V_{IL} = DGND
T_{MIN}–T_{MAX}	1.5	1.5	µA max	
Power Dissipation				Excluding Power Dissipated in Load
Normal Mode	66	66	mW max	
System Standby (SSTBY) Mode	1.38	1.38	mW max	
Power-Down ($\overline{PD}$) Mode				
@ +25°C	4.4	4.4	µW max	
T_{MIN}–T_{MAX}	8.25	8.25	µW max	

NOTES

[1]Temperature range is –40°C to +85°C.

[2]Can be minimized using the Sub DAC.

[3]V_{BIAS} is the center of the output voltage swing and can be $V_{DD}/2$, Internal Reference or REFIN as determined by MX1 and MX0 in the channel control register.

Specifications subject to change without notice.

AD7808/AD7809–SPECIFICATIONS (AV_{DD} and DV_{DD} = 3.3 V ± 10% to 5 V ± 10%; AGND = DGND = 0 V; Reference = Internal Reference; C_L = 100 pF; R_L = 2 kΩ to GND. Sub DAC at Midscale. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Grade[1]	Units	Comments
STATIC PERFORMANCE			
MAIN DAC			
Resolution	10	Bits	
Relative Accuracy	±4	LSB max	
Gain Error	±3	% FSR max	
Bias Offset Error[2]	±60	mV max	DAC Code = 0.5 Full Scale
Zero-Scale Error	±35	mV max	DAC Code = 000H for Offset Binary
Monotonicity	9	Bits	and 200H for Twos Complement
Minimum Load Resistance	2	kΩ min	Coding
SUB DAC			
Resolution	8	Bits	
Differential Nonlinearity	±0.125	LSB typ	Refers to an LSB of the Main DAC
	±0.5	LSB max	
OUTPUT CHARACTERISTICS			
Output Voltage Range[3]	V_{BIAS} ± 15/16 × V_{BIAS}	V	Twos Complement Coding
	V_{BIAS}/16 to 31/16 × V_{BIAS}	V	Offset Binary Coding
Voltage Output Settling Time to 10 Bits	4	µs max	Typically 1.5 µs
Slew Rate	2.5	V/µs typ	
Digital-to-Analog Glitch Impulse	1	nV-s typ	1 LSB Change Around the Major Carry
Digital Feedthrough	0.5	nV-s typ	
Digital Crosstalk	0.5	nV-s typ	
Analog Crosstalk	±0.2	LSB typ	
DC Output Impedance	2	Ω typ	
Power Supply Rejection Ratio	0.002	%/% typ	ΔV_{DD} ± 10%
DAC REFERENCE INPUTS			
REF IN Range	1.0 to V_{DD}/2	V min to V max	
REF IN Input Leakage	±1	µA max	Typically ±1 nA
DIGITAL INPUTS			
Input High Voltage, V_{IH} @ V_{DD} = 5 V	2.4	V min	
Input High Voltage, V_{IH} @ V_{DD} = 3.3 V	2.1	V min	
Input Low Voltage, V_{IL} @ V_{DD} = 5 V	0.8	V max	
Input Low Voltage, V_{IL} @ V_{DD} = 3.3 V	0.6	V max	
Input Leakage Current	±10	µA max	
Input Capacitance	8	pF max	
Input Coding	Twos Comp/Binary		
REFERENCE OUTPUT			
REF OUT Output Voltage	1.23	V nom	
REF OUT Error	±8	% max	
REF OUT Temperature Coefficient	–100	ppm/°C typ	
REF OUT Output Impedance	5	kΩ nom	
POWER REQUIREMENTS			
V_{DD} (AV_{DD} and DV_{DD})	3/5.5	V min to V max	
I_{DD} (AI_{DD} Plus DI_{DD})			Excluding Load Currents
Normal Mode	18	mA max	V_{IH} = V_{DD}, V_{IL} = DGND
System Standby (SSTBY) Mode	250	µA max	V_{IH} = V_{DD}, V_{IL} = DGND
Power-Down ($\overline{PD}$) Mode			
@ +25°C	1	µA max	V_{IH} = V_{DD}, V_{IL} = DGND
T_{MIN}–T_{MAX}	3	µA max	
Power Dissipation			Excluding Power Dissipated in Load
Normal Mode	99	mW max	
System Standby (SSTBY) Mode	1.38	mW max	
Power-Down ($\overline{PD}$) Mode			
@ +25°C	5.5	µW max	
T_{MIN}–T_{MAX}	16.5	µW max	

NOTES
[1]Temperature range is –40°C to +85°C.
[2]Can be minimized using the Sub DAC.
[3]V_{BIAS} is the center of the output voltage swing and can be V_{DD}/2, Internal Reference or REFIN as determined by MX1 and MX0 in the channel control register.
Specifications subject to change without notice.

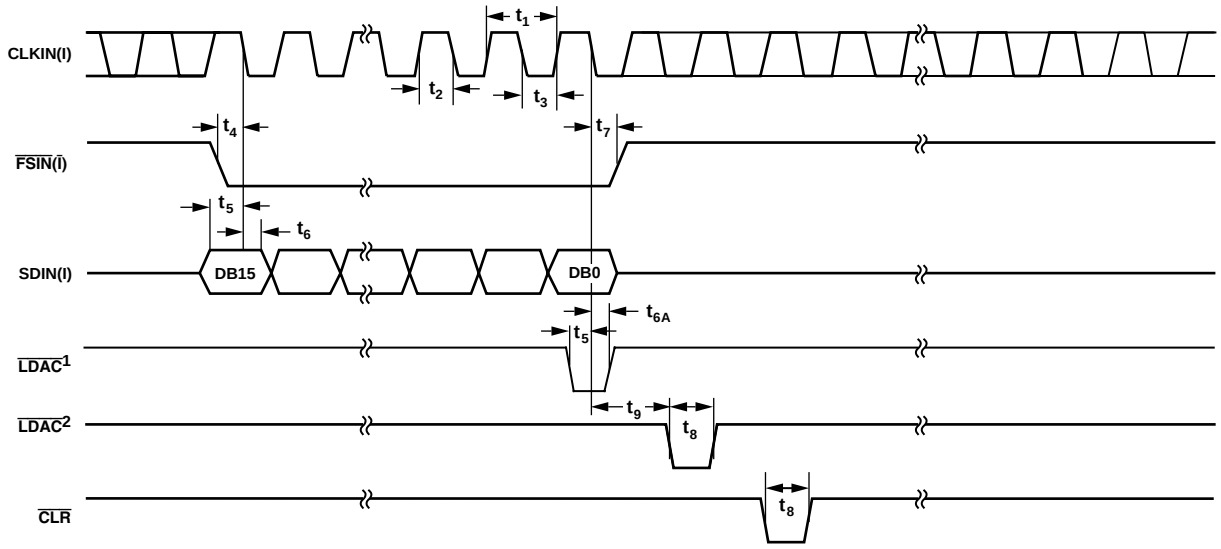
AD7804/AD7808 TIMING CHARACTERISTICS[1] (V_{DD} = 3.3 V ± 10% to 5 V ± 10%; AGND = DGND = 0 V; Reference = Internal Reference. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} All Versions	Units	Description
t_1	100	ns min	CLKIN Cycle Time
t_2	40	ns min	CLKIN High Time
t_3	40	ns min	CLKIN Low Time
t_4	30	ns min	$\overline{\text{FSIN}}$ Setup Time
t_5	30	ns min	Data Setup Time
t_6	5	ns min	Data Hold Time
t_{6A}	6	ns min	$\overline{\text{LDAC}}$ Hold Time
t_7	90	ns max	$\overline{\text{FSIN}}$ Hold Time
	20	ns min	
t_8	40	ns min	$\overline{\text{LDAC}}$, $\overline{\text{CLR}}$ Pulsewidth
t_9	100	ns min	$\overline{\text{LDAC}}$ Setup Time

NOTES

[1]Sample tested during initial release and after any redesign or process change that may affect this parameter. All input signals are specified with tr = tf = 5 ns and timed from a voltage of $(V_{IL} + V_{IH})/2$.

Specifications subject to change without notice.



[1]TIMING REQUIREMENTS FOR SYNCHRONOUS $\overline{\text{LDAC}}$ UPDATE OR $\overline{\text{LDAC}}$ MAY BE TIED PERMANENTLY LOW IF REQUIRED.
[2]TIMING REQUIREMENTS FOR ASYNCHRONOUS $\overline{\text{LDAC}}$ UPDATE.

Figure 1. Timing Diagram for AD7804 and AD7808

AD7805/AD7809 TIMING CHARACTERISTICS[1] (V_{DD} = 3.3 V ± 10% to 5 V ± 10%; AGND = DGND = 0 V; Reference = Internal Reference. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} All Versions	Unit	Description
t_1	25	ns min	Mode Valid to Write Setup Time
t_2	4.5	ns min	Mode Valid to Write Hold Time
t_3	25	ns min	Address Valid to Write Setup Time
t_4	4.5	ns min	Address Valid to Write Hold Time
t_5	25	ns min	Data Setup Time
t_6	4.5	ns min	Data Hold Time
t_{6A}	6	ns min	$\overline{\text{LDAC}}$ Valid to Write Hold Time
t_7	40	ns min	Chip Select to Write Setup Time
t_8	0	ns min	Chip Select to Write Hold Time
t_9	40	ns min	Write Pulsewidth
t_{10}	100	ns min	Time Between Successive Writes
t_{11}	40	ns min	$\overline{\text{LDAC}}$, $\overline{\text{CLR}}$ Pulsewidth
t_{12}	100	ns min	Write to $\overline{\text{LDAC}}$ Setup Time

NOTE
[1]Sample tested during initial release and after any redesign or process change that may affect this parameter. All input signals are specified with tr = tf = 5 ns and timed from a voltage of $(V_{IL} + V_{IH})/2$.

Specifications subject to change without notice.

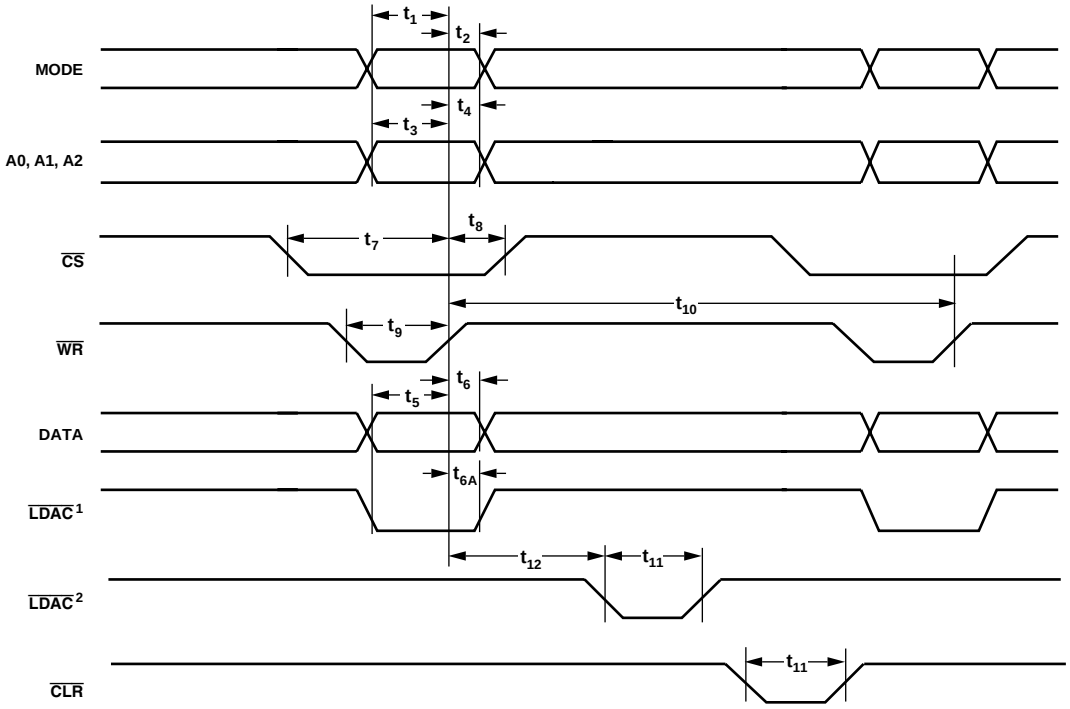


Figure 2. Timing Diagram for AD7805/AD7809 Parallel Write

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

DV_{DD} to DGND ..... –0.3 V to +7 V
AV_{DD} to AGND ..... –0.3 V to +7 V
AGND to DGND ..... –0.3 V + 0.3 V
Digital Input Voltage to DGND ..... –0.3 V to DV_{DD} + 0.3 V
Analog Input Voltage to AGND ..... –0.3 V to AV_{DD} + 0.3 V
COMP to AGND ..... –0.3 V to AV_{DD} + 0.3 V
REF OUT to AGND ..... –0.3 V to + AV_{DD}
REF IN to AGND ..... –0.3 V to AV_{DD} + 0.3 V
V_{OUT} to AGND[2] ..... –0.3 V to AV_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[3] ..... ±10 mA
Operating Temperature Range
  AD7804/AD7805 Commercial Plastic
    (B, C Versions) ..... –40°C to +85°C
  AD7808/AD7809 Commercial Plastic
    (B, C Versions) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
SOIC (R-16) Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 75°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C
PDIP (N-16) Package, Power Dissipation ..... 670 mW
  θ_{JA} Thermal Impedance ..... 116°C/W
  Lead Temperature, Soldering (10 sec) ..... +260°C
SOIC (R-24) Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 75°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C
PDIP (N-24) Package, Power Dissipation ..... 670 mW
  θ_{JA} Thermal Impedance ..... 105°C/W
  Lead Temperature, Soldering (10 sec) ..... +260°C
SOIC (R-28) Package, Power Dissipation ..... 875 mW
  θ_{JA} Thermal Impedance ..... 70°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C
PDIP (N-28) Package, Power Dissipation ..... 875 mW
  θ_{JA} Thermal Impedance ..... 75°C/W
  Lead Temperature, Soldering (10 sec) ..... +260°C
SSOP (RS-28) Package, Power Dissipation ..... 875 mW
  θ_{JA} Thermal Impedance ..... 110°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C
TQFP (SU-44) Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 116°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]The outputs may be shorted to voltages in this range provided the power dissipation of the package is not exceeded.

[3]Transient currents of up to 100 mA will not cause SCR latch-up.

ORDERING GUIDE

Model	Supply Voltage	Temperature Range	Relative Accuracy	Package Descriptions	Package Options
AD7804BN	3.3 V to 5 V	–40°C to +85°C	±3 LSB	16-Lead Plastic DIP	N-16
AD7804BR	3.3 V to 5 V	–40°C to +85°C	±3 LSB	16-Lead Small Outline IC	R-16
AD7805BN	3.3 V to 5 V	–40°C to +85°C	±3 LSB	28-Lead Plastic DIP	N-28
AD7805BR	3.3 V to 5 V	–40°C to +85°C	±3 LSB	28 Lead Small Outline IC	R-28
AD7805BRS	3.3 V to 5 V	–40°C to +85°C	±3 LSB	28-Lead Shrink Small Outline Package	RS-28
AD7805CR	3.3 V to 5 V	–40°C to +85°C	±3 LSB	28-Lead Small Outline IC	R-28
AD7808BN	3.3 V to 5 V	–40°C to +85°C	±4 LSB	24-Lead Plastic DIP	N-24
AD7808BR	3.3 V to 5 V	–40°C to +85°C	±4 LSB	24 Lead Small Outline IC	R-24
AD7809BST	3.3 V to 5 V	–40°C to +85°C	±4 LSB	44-Lead Thin Plastic Quad Flatpack (TQFP)	SU-44

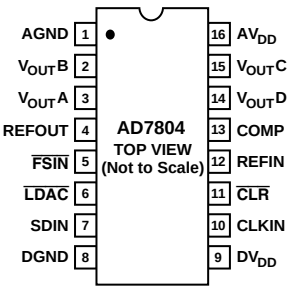
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

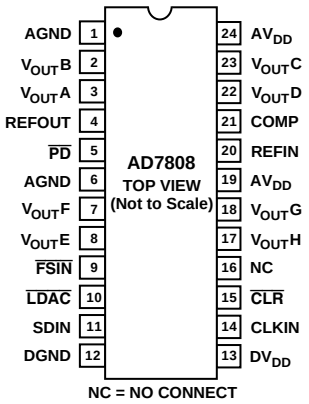
AD7804/AD7808 PIN FUNCTION DESCRIPTION

AD7804 Pin No.	AD7808 Pin No.	Mnemonic	Description
1	1, 6	AGND	Ground reference point for analog circuitry.
2, 3	2, 3	$V_{OUT}B$, $V_{OUT}A$	Analog output voltage from the DACs.
4	4	REFOUT	Reference Output. This is a bandgap reference and is typically 1.23 V.
	5	$\overline{PD}$	Active low input used to put the part into low power mode reducing current consumption to 1 μA.
	7, 8	$V_{OUT}F$, $V_{OUT}E$	Analog output voltages from the DACs.
5	9	$\overline{FSIN}$	Level-triggered control input (active low). This is the frame synchronization signal for the input data. When $\overline{FSIN}$ goes low, it enables the input shift register and data is transferred on the falling edges of CLKIN.
6	10	$\overline{LDAC}$	$\overline{LDAC}$ Input. When this digital input is taken low, all DAC registers are simultaneously updated with the contents of the data registers. If $\overline{LDAC}$ is tied permanently low, or is low on the sixteenth falling clock edge with timing similar to that of SDIN, an automatic update will take place.
7	11	SDIN	Serial Data Input. These devices accept a 16-bit word. Data is clocked into the input shift register on the falling edge of CLKIN.
8	12	DGND	Ground reference point for digital circuitry.
9	13	DV_{DD}	Digital Power Supply.
10	14	CLKIN	Clock Input. Data is clocked into the input shift register on the falling edges of CLKIN. Duty Cycle should be between 40% and 60%.
11	15	$\overline{CLR}$	Asynchronous $\overline{CLR}$ Input. When this input is taken low, all Main DAC outputs are cleared either to V_{BIAS} or to V_{BIAS}/16 volts. All Sub DACs are also cleared and thus the transfer function of the Main DAC will remain centered around the V_{BIAS} point.
	16	NC	No Connect. This pin should be left open circuit.
	17, 18	$V_{OUT}H$, $V_{OUT}G$	Analog output voltages from the DACs.
12	20	REFIN	This is an external reference input for the DACs. When this reference is selected for a DAC in the control register, the analog output from the selected DAC swings around this point.
13	21	COMP	Compensation Pin. This pin provides an output from the internal V_{DD}/2 divider and is provided for ac bypass purposes only. This pin should be decoupled with 1 nF capacitors to both AV_{DD} and AGND. This pin can be overdriven with an external reference, thus giving the facility for two external references on the part.
14, 15	22, 23	$V_{OUT}D$, $V_{OUT}C$	Analog output voltage from the DACs.
16	19, 24	AV_{DD}	Analog Power Supply. +3.3 V to +5 V.

AD7804 PIN CONFIGURATION



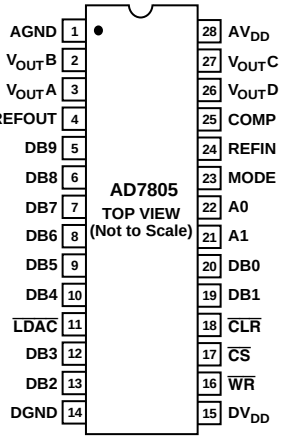
AD7808 PIN CONFIGURATION



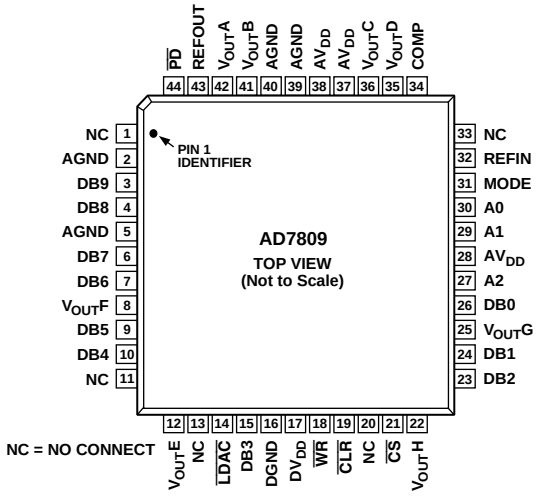
AD7805/AD7809 PIN FUNCTION DESCRIPTIONS

AD7805 Pin No.	AD7809 Pin No.	Mnemonic	Description
	1, 11, 13, 20, 33	NC	No Connect. These pins should be left open circuit.
1	2, 5, 39, 40	AGND	Ground reference point for analog circuitry.
2, 3	41, 42	$V_{OUT}B$, $V_{OUT}A$	Analog output voltages from the DACs.
4	43	REFOUT	Reference Output. This is a bandgap reference and is typically 1.23 V.
5–10, 12, 13	3, 4, 6, 7, 9, 10, 15, 23	DB9–DB2	Data Inputs. DB9 to DB2 are the 8 MSBs of the data word.
19, 20	24, 26	DB1, DB0	DB1 and DB0 function as the 2 LSBs of the 10-bit word in 10-bit parallel mode but have other functions when BYTE loading structure is used.
	8, 12	$V_{OUT}F$, $V_{OUT}E$	Analog output voltages from the DACs.
11	14	$\overline{LDAC}$	$\overline{LDAC}$ Input. When this digital input is taken low, all DAC registers are simultaneously updated with the contents of the DAC data registers. If $\overline{LDAC}$ is permanently tied low, or is low during the rising edge of $\overline{WR}$ similar to data inputs, an automatic update will take place.
14	16	DGND	Ground reference point for digital circuitry.
15	17	DV_{DD}	Digital Power Supply.
16	18	$\overline{WR}$	Write Input $\overline{WR}$ is an active low logic input which is used in conjunction with $\overline{CS}$ and the address pins to write data to the relevant registers.
17	21	$\overline{CS}$	Chip Select. Active low logic input.
18	19	$\overline{CLR}$	Asynchronous $\overline{CLR}$ Input. When this input is taken low, all Main DAC outputs are cleared either to V_{BIAS} or to $V_{BIAS}/16$ volts. All Sub DACs are also cleared and thus the transfer function of the MAIN DAC will remain centered around the V_{BIAS} point.
	22, 25	$V_{OUT}H$, $V_{OUT}G$	Analog output voltages from the DACs.
21, 22	27, 29, 30	A2, A1, A0	DAC Address Inputs. These digital inputs are used in conjunction with $\overline{CS}$ and $\overline{WR}$ to determine which DAC channel control register or DAC data register is loaded from the input register. These address bits are don't cares when writing to the system control register.
23	31	MODE	Logic Input. Logic high enables writing to the DAC data registers, a logic low enables writing to the control registers.
24	32	REFIN	This is an external reference input for the DAC. When this reference is selected for the DAC in the control register, the analog output from the selected DAC swings around this point.
25	34	COMP	Compensation Pin. This pin provides an output from the internal $V_{DD}/2$ divider and is provided for ac bypass purposes only. This pin should be decoupled with 1 nF capacitors to both AV_{DD} and AGND. This pin can be overdriven with an external reference, thus giving the facility for two external references on the part.
26, 27	35, 36	$V_{OUT}D$, $V_{OUT}C$	Analog output voltages from the DACs.
28	28, 37, 38	AV_{DD}	Analog Power Supply.
	44	$\overline{PD}$	Active low input used to put the part into low power mode reducing current consumption to 1 μA.

AD7805 PIN CONFIGURATION



AD7809 PIN CONFIGURATION



TERMINOLOGY

Relative Accuracy
For the DACs, relative accuracy or endpoint nonlinearity is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. Figures 32 and 33 show the linearity at 3 V and 5 V respectively.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity.

Bias Offset Error
If the DACs are ideal, the output voltage of any DAC with midscale code loaded will be equal to V_{BIAS} where V_{BIAS} is selected by MX1 and MX0 in the control register. The DAC bias offset error is the difference between the actual output voltage and V_{BIAS}, expressed in mV.

Gain Error
The difference between the actual and ideal analog output range, expressed as a percent of full-scale range. It is the deviation in slope of the DAC transfer characteristic from ideal.

Zero-Scale Error
The zero-scale error is the actual output minus the ideal output from any DAC when zero code is loaded to the DAC. If offset binary coding is used, the code loaded is 000Hex, and if twos complement coding is used, a code of 200HEX is loaded to the DAC to calculate the zero-scale error. Zero-scale error is expressed in mV.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the digital inputs change state with the DAC selected and the $\overline{LDAC}$ used to update the DAC. It is normally specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition. Regardless of whether offset binary or twos complement coding is used, the major carry transition occurs at the analog output voltage change of V_{BIAS} to V_{BIAS} – 1 LSB or vice versa.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital inputs of the same DAC but is measured when the DAC is not updated. It is specified in nV secs and is measured with a full-scale code change on the data bus, i.e., from all 0s to all 1s and vice versa.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one converter due to a digital code change to another DAC. It is specified in nV-s.

Analog Crosstalk
Analog crosstalk is a change in output of any DAC in response to a change in the output of one or more of the other DACs. It is measured in LSBs.

Power Supply Rejection Ratio (PSRR)
This specification indicates how the output of the DAC is affected by changes in the power supply voltage. Power-supply rejection ratio is quoted in terms of % change in output per % change in V_{DD} for full-scale output of the DAC. V_{DD} is varied ±10%.

AD7804/AD7808 INTERFACE SECTION

The AD7804 and AD7808 are serial input devices. Three lines control the serial interface, $\overline{FSIN}$, CLKIN and SDIN. The timing diagram is shown in Figure 1.

Two mode bits (MD1 and MD0) which are DB13 and DB14 of the serial word written to the AD7804/AD7808 are used to determine whether writing is to the DAC data registers or the control registers of the device. These parts contain a system control register for controlling the operation of all DACs in the package as well as a channel control register for controlling the operation of each individual DAC. Table I shows how to access these registers.

Table I. Register Selection Table for the AD7804/AD7808

MD1	MD0	Function
0	0	Write enable to system control register.
0	1	Write enable to channel control register.
1	X	Write enable to DAC data registers.

When the $\overline{FSIN}$ input goes low, data appearing on the SDIN line is clocked into the input register on each falling edge of CLKIN. Data to be transferred to the AD7804/AD7808 is loaded MSB first. Figure 4 shows the loading sequence for the AD7804/AD7808 system control register, Figure 5 shows the sequence for the channel control register write, and Figures 6 and 7 show the sequence for loading data to the Main and Sub DAC data registers. Figure 3 shows the internal registers associated with the AD7804/AD7808 serial interface DACs. Only one DAC structure is shown for clarity.

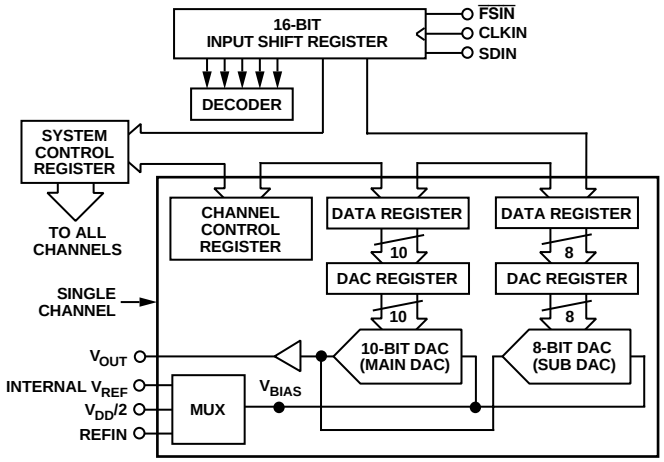


Figure 3. AD7804/AD7808 Internal Registers

MSB															LSB
X	MD0 = 0	MD1 = 0	X	X	X	X	X	0	BIN/$\overline{\text{COMP}}$	$\overline{\text{PD}}$	SSTBY	SCLR	0	X	X

X = Don't Care

Figure 4. AD7804/AD7808 System Control Register Loading Sequence

DB15 (MSB)															DB0 (LSB)
X	MD0 = 1	MD1 = 0	A2*	A1	A0	MX1	MX0	X	X	X	$\overline{\text{STBY}}$	CLR	0	X	X

X = Don't Care
*Applicable to the AD7808 Only, and Are Don't Care Conditions when Operating the AD7804.

Figure 5. AD7804/AD7808 Channel Control Register Loading Sequence

DB15 (MSB)															DB0 (LSB)
$\overline{\text{MAIN}}$/SUB	MD0 = X	MD1 = 1	A2*	A1	A0	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

X = Don't Care
*Applicable to the AD7808 Only, and Are Don't Care Conditions when Operating the AD7804.

Figure 6. AD7804/AD7808 Main DAC Data Register Loading Sequence ($\overline{\text{MAIN}}$/SUB = 0)

DB15 (MSB)															DB0 (LSB)
$\overline{\text{MAIN}}$/SUB	MD0 = X	MD1 = 1	A2*	A1	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	X	X

X = Don't Care
*Applicable to the AD7808 Only, and Are Don't Care Conditions when Operating the AD7804.

Figure 7. AD7804/AD7808 Sub DAC Data Register Loading Sequence ($\overline{\text{MAIN}}$/SUB = 1)

When the system control register is selected by writing zeros to the mode bits, MD1 and MD0 the address bits are ignored as the system control register controls all DACs in the package. When MD1 = 0 and MD0 = 1, writing is to the channel control register. Only the DAC selected by the address bits will be affected by writing to this register. Each individual DAC has a channel control register.

The DACs data registers are addressed by writing a one to MD1 (DB13); the condition of MD0 (DB14) does not matter when writing to the data registers. DB15 determines whether writing is to the Main DAC data register or to the Sub DAC data register. The Main DAC is 10 bits wide and the Sub DAC is 8 bits wide. Thus when writing to the Sub DAC DB1 and DB0 become don't cares. The Sub DAC is used to offset the complete transfer function of the Main DAC around its V_{BIAS} point. The Sub DAC has 1/8 LSB resolution and will enable the transfer function of the Main DAC to be offset by $\pm V_{BIAS}/32$.

When the $\overline{\text{LDAC}}$ line goes low, all DAC registers in the device are simultaneously loaded with the contents of their respective DAC data registers, and the outputs change accordingly.

Bringing the $\overline{\text{CLR}}$ line low resets the DAC data and DAC registers. This hardware clear affects both the Main and Sub DACs. This operation sets the analog output of the Main DAC to V_{BIAS}/16 when offset binary coding is selected and the output is set to V_{BIAS} when twos complement coding is used. V_{BIAS} is the output of the internal multiplexer as shown in Figure 3. The output of the Sub DAC is used to shift the transfer function of the Main DAC around the V_{BIAS} point and the contribution from the Sub DAC is zero following an external hardware clear. Software clears affect the Main DACs only.

AD7804/AD7808 SYSTEM CONTROL REGISTER (MD1 = 0, MD0 = 0)

The bits in this register allow control over all DACs in the package. The control bits include power down ($\overline{\text{PD}}$), DAC input coding select (BIN/$\overline{\text{COMP}}$), system standby (SSTBY) and a system clear (SCLR). The function of these bits is as follows:

Power Down ($\overline{\text{PD}}$)

This bit in the control register is used to shut down the complete device. With a 0 in this position, the reference and all DACs are put into low power mode. Writing a 1 to this bit puts the part in the normal operating mode. When in power-down mode, the contents of all registers are retained and are valid when the device is put back into normal operation.

Coding (BIN/$\overline{\text{COMP}}$)

This bit in the system control register allows the user to select one of two input coding schemes. The available schemes are Twos complement coding and offset binary coding. All DACs will be configured with the same input coding scheme. Writing a zero to the control register selects twos complement coding, while writing a 1 to this bit in the control register selects offset binary coding.

With twos complement coding selected the output voltage from the Main DAC is of the form :

$$V_{OUT} = V_{BIAS} \pm V_{SWING}$$

where

$$V_{SWING}\ is\ \frac{15}{16} \times V_{BIAS}$$

With Offset Binary coding selected the output voltage from the Main DAC ranges from:

$$V_{OUT} = \frac{V_{BIAS}}{16}\ to\ V_{OUT} = \frac{31}{16} \times V_{BIAS}$$

V_{BIAS} can be the internal bandgap reference, the internal $V_{DD}/2$ reference or the external REFIN as determined by MX1 and MX0 in the channel control register. A second external reference can be used if required by overdriving the $V_{DD}/2$ reference which appears at the COMP pin.

System Standby (SSTBY)
This bit allows all the DACs in the package to be put into low power mode simultaneously but the reference is not affected. Writing a one to the SSTBY bit in the system control register puts all DACs into standby mode. On writing a one to this bit all linear circuitry is switched off and the DAC outputs are connected through a high impedance to ground. The DACs come out of standby mode when a 0 is written to the SSTBY bit.

System Clear Function (SCLR)
This function allows the user to clear the contents of all data and DAC registers in software. Writing a one to the SCLR bit in the control register clears the DAC's outputs. A zero in this bit position puts the DAC in normal operating mode. The output of the Main DACs are cleared to one of two voltages depending on the input coding used. If twos complement coding is selected, then issuing a software clear will reset the output of the Main DAC to midscale (V_{BIAS}). If offset binary coding is selected, the Main DAC output will be reset to V_{BIAS} /16 following the execution of a software clear. This system clear function does not affect the Sub DAC; the Sub DAC data register retains its value during a system software clear (SCLR).

AD7804/AD7808 CHANNEL CONTROL REGISTER (MD1 = 0, MD0 = 1)
This register allows the user to have control over individual DACs in the package. The control bits in this register include the address bits for the selected DAC, standby ($\overline{STBY}$), individual DAC clear (CLR) and multiplexer output selection (MX1 and MX0). The function of these bits follows.

DAC Selection (A2, A1, A0)
Bits A2, A1 and A0 in the input registers are used to address a specific DAC. Table IIa shows the selection table for the DACs of the AD7804. Table IIb shows the selection table for the DACs of the AD7808.

Table IIa. DAC Selection Table for the AD7804

A2	A1	A0	Function
X	0	0	DAC A Selected
X	0	1	DAC B Selected
X	1	0	DAC C Selected
X	1	1	DAC D Selected

Table IIb. DAC Selection Table for the AD7808

A2	A1	A0	Function
0	0	0	DAC A Selected
0	0	1	DAC B Selected
0	1	0	DAC C Selected
0	1	1	DAC D Selected
1	0	0	DAC E Selected
1	0	1	DAC F Selected
1	1	0	DAC G Selected
1	1	1	DAC H Selected

Standby ($\overline{STBY}$)
This bit allows the selected DAC in the package to be put into low power mode. Writing a zero to the $\overline{STBY}$ bit in the channel control register puts the selected DAC into standby mode. On writing a zero to this bit all linear circuitry is switched off and the DAC output is connected through a high impedance to ground. The DAC is returned to normal operation by writing a one to the $\overline{STBY}$ bit.

Software Clear Function (CLR)
This function allows the user to clear the contents of the selected DAC's data in software. Writing a one to the CLR bit in the control register clears the DAC's output. A zero in the CLR bit position puts the DAC in normal operating mode. This software CLR operation clears only the Main DAC, the contents of the Sub DAC is unaffected by a CLR operation. The output of the Main DAC can be cleared to one of two places depending on the input coding used. An $\overline{LDAC}$ pulse is required to activate the channel clear function and must be applied after the bit in the channel control register is set or reset. If twos complement coding is selected, then issuing a software clear will reset the output of the Main DAC to midscale (V_{BIAS}). If offset binary coding is selected, the Main DAC output will be reset to $V_{BIAS}/16$ following the execution of a software clear.

Multiplexer Selection (MX1, MX0)
These two bits are used to select the reference input for the selected DAC. Table III shows the options available.

Table III. Multiplexer Output Selection

MX1	MX0	V_{BIAS}
0	0	$V_{DD}/2$
0	1	INTERNAL V_{REF}
1	0	REFIN
1	1	Undetermined

AD7804/AD7808 SUB DAC DATA REGISTER
Figure 7 shows the loading sequence for writing to the data registers of the DACs. DB15 determines whether writing is to the Main or Sub DAC's data register. A one in this position selects the addressed Sub DAC's data register. The Sub DAC is 8 bits wide and thus DB1 and DB0 of the 16-bit input word are don't cares when writing to the Sub DAC. This Sub DAC allows the complete transfer function of each individual DAC to be offset around the V_{BIAS} point. This is achieved by either adding or subtracting to the output of the Main DAC. This Sub DAC has a span of $\pm V_{BIAS}/32$ with 1/8-bit resolution. The coding scheme for the Sub DAC is the same as that for the Main DAC. With offset binary coding the transfer function for the Sub DAC is

$$\frac{V_{BIAS}}{16} \times \frac{(NB - 128)}{256}$$

where *NB* is the digital code written to the Sub DAC and varies from 0 to 255.

With twos complement coding the transfer function for the Sub DAC is

$$\frac{V_{BIAS}}{16} \times \left(\frac{NB}{256}\right)$$

where *NB* is the digital code written to the Sub DAC and varies from –128 to 127. V_{BIAS} can be either the internal bandgap reference, the internal $V_{DD}/2$ reference or the external REFIN as

determined by MX1 and MX0 in the channel control register as shown in Table III. The internal $V_{DD}/2$ reference is provided at the COMP pin. This internal reference can be overdriven with an external reference thus providing the facility for two external references.

AD7804/AD7808 POWER-UP CONDITIONS

When power is applied to the device, the device will come up in standby mode where all the linear circuitry excluding the reference are switched off. Figure 8 shows the relevant default values for the system control register. Since a write to the system control register is required to remove the standby condition the only bits for which default conditions are applicable are $\overline{PD}$ and SSTBY. Figure 9 details the relevant default conditions for the Channel Control Register.

$\overline{PD}$	SSTBY
1	1

Figure 8. Default Conditions for System Control Register on Power-Up

$\overline{STBY}$	CLR	MX1	MX0
1	1	0	0

Figure 9. Default Conditions for Channel Control Register on Power-Up

After power has been applied to the device the following procedure should be followed to communicate and set up the device. First, a write to the system control register is required to clear the SSTBY bit and change the input coding scheme if required.

For example, to remove standby and set up offset binary input coding 0060Hex should be written to the input register, if twos complement coding is required 0020Hex should be written to the input register. MD1 and MD0 are decoded in the input register and this allows the data to be written to the system control register.

Step two requires writing to the channel control register, which allows individual control over each DAC in the package and allows the V_{BIAS} for the DAC to be selected as well as individual DAC standby and clear functions. For example, if channel A is to be configured for normal operation with internal reference selected then 4110Hex should be written to the input register. In the input register, the MD1 and MD0 bits are decoded in association with the address bits to give access to the required channel control register. The third and final step is to write data to the selected DAC. To write half scale to channel A Main DAC, 2200Hex should be written to the input register, the MSB in the sixteen bit stream selects the Main DAC and the next three bits address the DAC and the final 10 bits contain the data. To write half scale to channel A Sub DAC, then A200 should be written to the input register. The flowchart in Figure 10 shows in graphic form the steps required in communicating with the AD7804/AD7808.

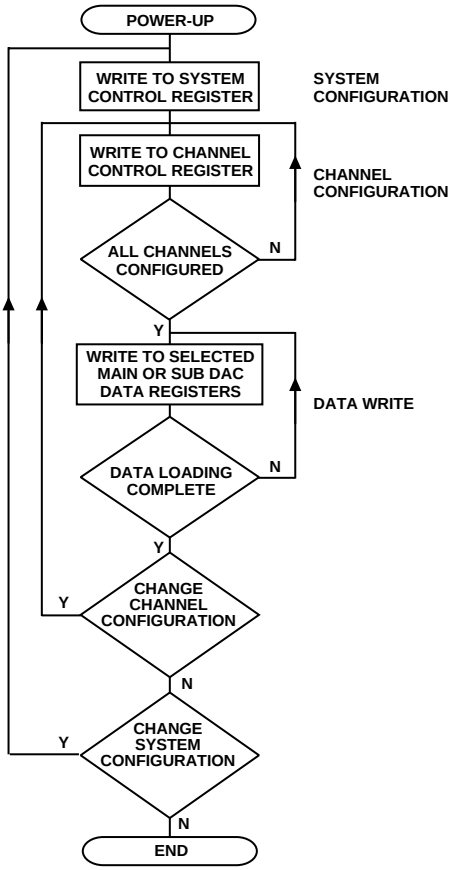


Figure 10. Flowchart for Controlling the DAC Following Power-Up

AD7805/AD7809 INTERFACE SECTION

The AD7805 and AD7809 are parallel data input devices and contain both control registers and data registers. The system control register has global control over all DACs in the package while the channel control register allows control over individual DACs in the package. Two data registers are also available, one for the 10-bit Main DAC and the second for the 8-bit Sub DAC. In the parallel mode, $\overline{CS}$ and $\overline{WR}$, in association with the address pins, control the loading of data. Data is transferred from the data register to the DAC register under the control of the $\overline{LDAC}$ signal. Only data contained in the DAC register determines the analog output of any DAC. The timing diagram for 10-bit parallel loading is shown in Figure 2. The MODE pin on the device determines whether writing is to the data registers or to the control registers. When MODE is at a logic one, writing is to the data registers. In the next write to the data registers a bit in the channel control register determines whether the Main DAC or the Sub DAC is addressed. This means that to address either the Main or the Sub DAC the $\overline{Main}$/Sub bit in the control register has to be set appropriately before the data register write. A logic zero on the mode pin enables writing to the control register. Bit MD0 determines whether writing is to the system control register or to the addressed channel control register.

Bringing the $\overline{CLR}$ line low resets the DAC registers to one of two known conditions depending on the coding scheme selected. The hardware clear affects both the Main and Sub DAC registers. With offset binary coding a clear sets the output

of the Main DAC to the bottom of the transfer function, $V_{BIAS}/16$. With twos complement coding the output of the DAC is cleared to midscale which is V_{BIAS}. A hardware clear always clears the output of the Sub DAC to midscale thus the output of the Sub DAC makes zero contribution to the output of the channel.

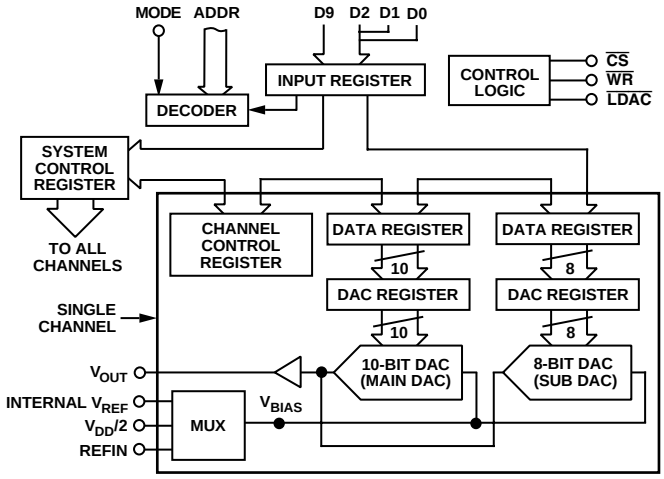


Figure 11. AD7805/AD7809 Internal Registers

AD7805/AD7809 CONTROL REGISTERS

Access to the control registers of the AD7805/AD7809 is achieved by taking the mode pin to a logic low. The control register of these DACs are configured as in Figures 12 and 13. There are two control registers associated with the part. System control register which looks after the input coding, data format, power down, system clear and system standby. The channel control register contains bits that affect the operation of the selected DAC. The external address bits are used to select the DACs. These registers are eight bits wide and the last two bits are control bits. The mode pin must be low to have access to the control registers.

DB9							DB2	DB1	DB0
X	X	$\overline{10}$/8	BIN/$\overline{COMP}$	$\overline{PD}$	SSTBY	SCLR	0	X	MD0 = 0

X = Don't Care

Figure 12. AD7805/AD7809 System Control Register Configuration, (MODE = 0)

DB9							DB2	DB1	DB0
MX1	MX0	$\overline{MAIN}$/SUB	X	X	$\overline{STBY}$	CLR	0	X	MD0 = 1

X = Don't Care

Figure 13. AD7805/AD7809 Channel Control Register Configuration (MODE = 0)

The external mode pin must be taken high to allow data to be written to the DAC data registers. Figure 14 shows the bit allocations when 10-bit parallel operation is selected in the system control register.

DB9									DB0
DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	X	X

X = Don't Care

Figure 14. AD7805/AD7809 Main DAC Data Register (Top) and Sub DAC Data Register (Bottom) Configuration (MODE = 1, $\overline{10}$/8 = 0)

Figure 15 shows the bit allocations when 8-bit parallel operation is selected in the system control register. DB9 to DB2 are retained as data bits. DB1 acts as a high byte or low byte enable. When DB1 is low, the eight MSBs of the data word are loaded to the input register. When DB1 is high, the low byte consisting of the two LSBs are loaded to the input register. DB0 is used to select either the Main or Sub DAC when in the byte mode.

DB9							DB2	DB1	DB0
DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	0	$\overline{MAIN}$/SUB
X	X	X	X	X	X	DB1	DB0	1	$\overline{MAIN}$/SUB

X = Don't Care

Figure 15. AD7805/AD7809 Main DAC Data Register Configuration (MODE = 1, $\overline{10}$/8 = 1, $\overline{MAIN}$/SUB = 0)

Figure 16 shows the bit allocations for writing to the Sub DAC.

DB9							DB2	DB1	DB0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	X	$\overline{MAIN}$/SUB

X = Don't Care

Figure 16. AD7805/AD7809 Sub DAC Data Register Configuration (MODE = 1, $\overline{MAIN}$/SUB = 1)

Each DAC has a separate channel control register. The following is a brief discussion on the bits in each of the control registers.

DAC Selection (A2, A1, A0)

The external address pins in conjunction with $\overline{CS}$, $\overline{WR}$ and MODE are used to address the various DAC data and control registers. Table IVa shows how these DAC registers can be addressed on the AD7805. Table IVb shows how these registers are addressed on the AD7809. Refer to Figures 12 to 16 for information on the registers.

Table IVa. AD7805 DAC Data/Control Register Selection Table

MODE	A1	A0	Function Selected
0	0	0	DAC A Control Registers
0	0	1	DAC B Control Registers
0	1	0	DAC C Control Registers
0	1	1	DAC D Control Registers
1	0	0	DAC A Data Registers
1	0	1	DAC B Data Registers
1	1	0	DAC C Data Registers
1	1	1	DAC D Data Registers

Table IVb. AD7809 DAC Data/Control Register Selection Table

MODE	A2	A1	A0	Function Selected
0	0	0	0	DAC A Control Register
0	0	0	1	DAC B Control Register
0	0	1	0	DAC C Control Register
0	0	1	1	DAC D Control Register
0	1	0	0	DAC E Control Register
0	1	0	1	DAC F Control Register
0	1	1	0	DAC G Control Register
0	1	1	1	DAC H Control Register
1	0	0	0	DAC A Data Register
1	0	0	1	DAC B Data Register
1	0	1	0	DAC C Data Register
1	0	1	1	DAC D Data Register
1	1	0	0	DAC E Data Register
1	1	0	1	DAC F Data Register
1	1	1	0	DAC G Data Register
1	1	1	1	DAC H Data Register

AD7805/AD7809 SYSTEM OR CHANNEL CONTROL REGISTER SELECTION

MD0

0 This enables writing to the system control register. The contents of this are shown in Figure 12. Mode must be low to access this control register.

1 This enables writing to the channel control register. The contents of this are shown in Figure 13. Mode must also be low to access this control register.

AD7805/AD7809 SYSTEM CONTROL REGISTER

The bits in this register allow control over all DACs in the package. The control bits include data format ($\overline{10}$/8), power down ($\overline{PD}$), DAC input coding select (BIN/$\overline{COMP}$), system standby (SSTBY) and a system clear (SCLR). The function of these bits is as follows:

Data Format
$\overline{10}$/8

0 10-bit parallel loading structure.

1 Byte loading structure. (8+2 loading).

Input Coding
BIN/$\overline{COMP}$

0 Twos complement coding.

1 Offset Binary Coding.

Power Down
$\overline{PD}$

0 Complete power-down of device.

1 Normal operation (default on power-up).

System Standby
SSTBY

0 Normal operation.

1 All DACs in the package put in standby mode (default on power-up).

System Clear
SCLR

0 Normal operation.

1 All DACs in the package are cleared to a known state depending on the coding scheme selected. The SCLR bit clears the Main DACs only; the Sub DACs are unaffected by the system clear function. The main DAC is cleared to different levels depending on the coding scheme. With offset binary coding the Main DAC output is cleared to the bottom of the transfer function V_{BIAS}/16. With twos complement coding the Main DAC output is cleared to midscale V_{BIAS}. The channel output will be the sum of the Main DAC and Sub DAC contributions.

AD7805/AD7809 CHANNEL CONTROL REGISTER

This register allows the user to have control over individual DACs in the package. The control bits in this register include multiplexer output selection (MX1 and MX0), Main or Sub DAC selection ($\overline{MAIN}$/SUB), standby ($\overline{STBY}$) and individual DAC clear (CLR). The function of these bits is as follows.

Multiplexer Selection (MX1, MX0)
Table V shows the V_{BIAS} selection using MX1 and MX0 bits in the channel control register.

Table V. V_{BIAS} Selection Table

MX1	MX0	V_{BIAS}
0	0	V_{DD}/2 (Default on Power-Up)
0	1	INTERNAL VREF
1	0	REFIN
1	1	Undetermined

Main DAC or Sub DAC Selection
$\overline{MAIN}$/SUB

0 Writing a 0 to this bit means that the data in the next data register write is transferred to the selected Main DAC.

1 Writing a 1 to this bit means that the data in the next data register write is transferred to the selected Sub DAC.

This applies to the 10-bit parallel load feature. In byte load mode, (Figure 15) DB0 selects the Main or Sub DAC data registers.

Standby
$\overline{STBY}$

0 Places the selected DAC and its associated linear circuitry in Standby Mode.

1 Normal operation (default on power-up).

Clear
CLR

0 Normal operation.

1 Clears the output of the selected Main DAC to one of two conditions depending on the input coding selected. With offset binary coding the Main DAC output is cleared to the bottom of the transfer function, V_{BIAS}/16 and with twos complement coding the Main DAC output is cleared to midscale V_{BIAS}. The Sub DAC is unaffected by a clear operation. An $\overline{LDAC}$ signal has to be applied to the DAC for a channel clear to be implemented.

POWER-UP CONDITIONS (POWER-ON RESET)

When power is applied to the AD7805/AD7809 the device powers up in a known condition. The device powers up in system standby (SSTBY) mode where all DACs in the package are in low power mode, the reference is active and the outputs of the DACs are connected internally through a high impedance to ground. Figure 17 show the default conditions for the system control register. Since a write to the system control register is required to remove the standby condition, relevant default conditions are only applicable for $\overline{PD}$ and SSTBY in the system control register. The following are the bits in the channel control register for which default conditions are applicable, $\overline{STBY}$, CLR, MX1 and MX0. Figure 18 shows the default conditions for the channel control register.

$\overline{PD}$	SSTBY
1	1

Figure 17. Default Conditions for the AD7805/AD7809 System Control Register on Power-Up

$\overline{STBY}$	CLR	MX1	MX0
1	1	0	0

Figure 18. Default Conditions for the AD7805/AD7809 Channel Control Register on Power-Up

The flowchart in Figure 19 shows the steps necessary to control the AD7805/AD7809 following power-on. This flowchart details the necessary steps when using the AD7805/AD7809 in its 10-bit parallel mode. The first step is to write to the system control register to clear the SSTBY bit and to configure the part for 10-bit parallel mode and select the required coding scheme. The next step is to determine whether writing is to the Main or Sub DAC. This is achieved by writing to the channel control register. Other bits that need to be configured in the channel control register are MX1 and MX0 which determine the source of the V_{BIAS} for the selected DAC and the channel $\overline{STBY}$ and channel CLR bits need to be configured as desired. Once writing to the channel control register is complete, data can now be written to the selected Main or Sub DAC.

Parallel data can also be written to the device in 8+2 format to allow interface to 8-bit processors. Eight-bit mode is invoked by writing a one to the $\overline{10}$/8 bit in the system control register. When in the 8-bit mode the two unused data bits (DB1 and DB0) are used as hardware control bits and have the same timing characteristics as the address inputs. DB1 is a don't care bit when writing to both the system and channel control registers; DB0 acts as the mode select bit and must be low to enable writing to the system control register and when high enables access to the channel control register.

When in the 8-bit data write mode, DB1 acts as a low byte and high byte enable, when low data is written to the 8 MSBs of the DAC and when high data is written to the two LSBs. DB0 acts as a bit to select writing to the Main or Sub DAC. When DB0 is low, writing is to the Main DAC, and when high, writing is to the Sub DAC data register. In the 8+2 mode the channel control register does not have to be accessed to switch between writing to the Main and Sub DACs as in the 10-bit parallel

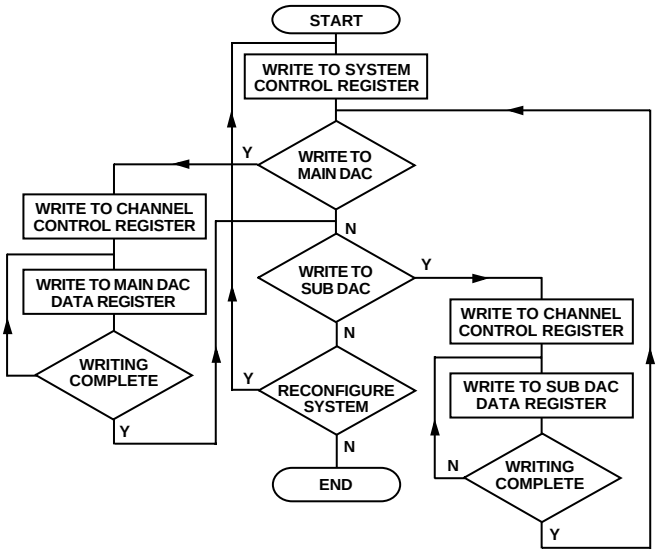


Figure 19. Flowchart for Controlling the AD7805/AD7809 DACs in 10-Bit Parallel Mode Following Power-Up

mode as the selection can be made using the hardware bit DB0 and this will reduce the software overheads when accessing the DACs.

CLEAR FUNCTIONS

There are three methods of clearing the output of the Main DAC in these devices. The first is the external hardware clear. An active low logic signal applied to this pin clears all the DACs in the package. The voltage to which the output is cleared will depend on the input coding selected. The Main DAC outputs are cleared to midscale (V_{BIAS}) in twos complement format and to the bottom of the transfer function (V_{BIAS}/16) in offset binary format. The second way of clearing the main DACs is a software clear by asserting the SCLR bit in the system control register of the part. Writing a one to this bit clears all DACs in the package. The third method of clearing a DAC is to write a one to the CLR bit in the channel control register. This differs from that of the system control register in that only the selected DACs output is cleared. The channel clear requires an $\overline{LDAC}$ pulse to activate it.

There is only one way of clearing the output of the Sub DAC and that is to use the external hardware clear. The output of the Sub DAC is cleared to midscale (0 V) regardless of the input coding being used. Figure 20 shows a simplified diagram of the implementation of the clear functions for a single DAC in the package.

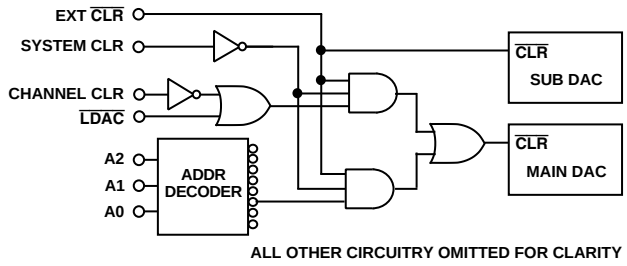


Figure 20. $\overline{CLR}$ Functions for Main and Sub DACs

POWER-DOWN AND STANDBY FUNCTIONS

There are two distinct low power modes on the device, power-down mode and standby mode. When in power-down mode all circuitry including the reference are put into low power mode and power dissipation from the package is at its minimum.

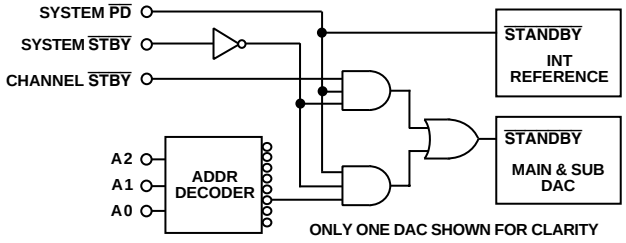


Figure 21. Implementation of Power-Down and Standby Functions

The standby functions allow either the selected DAC or all DACs in the package to be put into low power mode. The reference is not switched off when any of the standby functions are invoked.

The $\overline{PD}$ bit in the system control register is used to shut down the complete device. With a 0 in this position the reference and all DACs are put into low power mode. Writing a 1 to this bit puts the part in the normal operating mode. When in power-down mode the contents of all registers are retained and are valid when the device is taken out of power down. The SSTBY bit which resides in the system control register can be used to put all DACs and their associated linear circuitry into standby mode, the SSTBY function does not power down the reference. The $\overline{STBY}$ bit in the channel control register can be used to put a selected DAC and its associated linear circuitry into standby mode. Figure 18 shows a simplified diagram of how the power-down and standby functions are implemented for a single DAC in the package.

$\overline{LDAC}$ FUNCTION

$\overline{LDAC}$ input is a logic input that allows all DAC registers to be simultaneously updated with the contents of the DAC data registers. $\overline{LDAC}$ input has two operating modes, a synchronous mode and an asynchronous mode. The $\overline{LDAC}$ input condition is sampled on the sixteenth falling edge on the AD7804/AD7808 and is sampled on the rising edge of write on the AD7805/AD7809. If $\overline{LDAC}$ is low on the sixteenth falling clock edge or on the rising edge of $\overline{WR}$, an automatic or synchronous update will take place. $\overline{LDAC}$ input can be tied permanently low or have timing similar to that of the data inputs to operate in the synchronous mode.

If $\overline{LDAC}$ is high during the sample period, the AD7804/AD7805/AD7808/AD7809 assumes an asynchronous update. When in the asynchronous mode, an $\overline{LDAC}$ setup time has to be allowed following the sixteenth falling clock edge or the rising edge of $\overline{WR}$ before the $\overline{LDAC}$ can be activated.

ANALOG OUTPUTS

The AD7804 and AD7805 DACs contain four independent voltage output Main DACs with 10-bit resolution. The AD7808 and AD7809 contain eight independent voltage output main DACs with 10-bit resolution. Each Main DAC has an associated Sub DAC with 8-bit resolution which can be used to offset the complete transfer function of the Main DAC around the V_{BIAS} point. These DACs produce an output voltage in the form of $V_{BIAS} \pm V_{SWING}$ where V_{SWING} is 15/16 of V_{BIAS}.

The digital input code to these DACs can be in twos complement or offset binary form. All DACs will be configured with the same input coding scheme which is programmed through the system control register. The default condition on power-up is for offset binary coding.

TWOS COMPLEMENT CODING

Table VI shows the twos complement transfer function for the Main DAC.

Table VI. Twos Complement Code Table for Main DAC

Digital Input MSB . . . LSB	Analog Output
0111111111	$V_{BIAS}(1+1.875 \times 511/1024)$
0111111110	$V_{BIAS}(1+1.875 \times 510/1024)$
0000000001	$V_{BIAS}(1+1.875 \times 1/1024)$
0000000000	V_{BIAS}
1111111111	$V_{BIAS}(1-1.875 \times 1/1024)$
1000000001	$V_{BIAS}(1-1.875 \times 511/1024)$
1000000000	$V_{BIAS}(1-1.875 \times 512/1024)$

Figure 22 shows the Main DAC transfer function for twos complement coding. Any Main DAC output voltage can be expressed as:

$$V_{OUT}' = V_{BIAS} + 1.875 \times V_{BIAS} \times NA/1024$$

where NA is the decimal equivalent of the twos complement input code. NA ranges from –512 to +511.

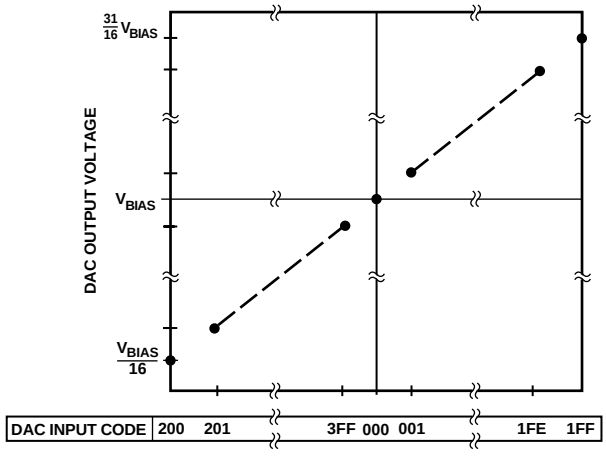


Figure 22. Main DAC Output Voltage vs. DAC Input Codes (HEX) for Twos Complement Coding

Table VII shows the twos complement transfer function for the Sub DAC. Figure 23 shows the Sub DAC transfer function for twos complement coding. Any Sub DAC output voltage can be expressed as:

$$V_{OUT}'' = V_{BIAS}/16 \times (NB/256)$$

where NB is the decimal equivalent of the twos complement input code. NB ranges from –128 to +127.

Table VII. Twos Complement Code Table for Sub DAC

Digital Input MSB . . . LSB	Analog Input
01111111	$(V_{BIAS}/16) \times (127/256)$
01111111	$(V_{BIAS}/16) \times (126/256)$
00000001	$(V_{BIAS}/16) \times (1/256)$
00000000	0
11111111	$(-V_{BIAS}/16) \times (1/256)$
10000001	$(-V_{BIAS}/16) \times (127/256)$
10000000	$(-V_{BIAS}/16) \times (128/256)$

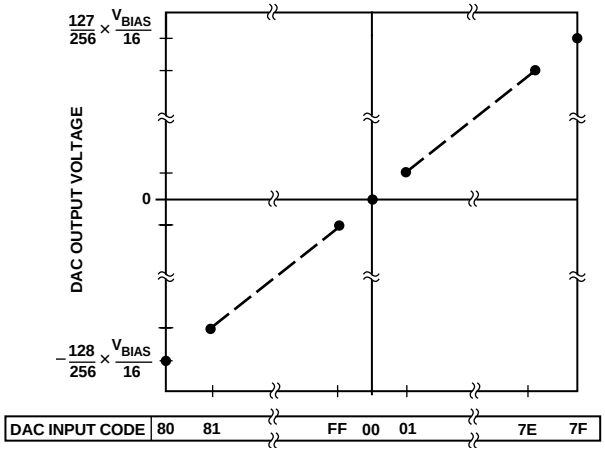


Figure 23. Sub DAC Output Voltage vs. DAC Input Codes (HEX) for Twos Complement Coding

The total output for a single channel when using twos complement coding is the sum of the voltage from the Main DAC and the Sub DAC.

$$V_{OUT} = V_{OUT}' + V_{OUT}''$$
$$= V_{BIAS} + 1.875 \times V_{BIAS} \times (NA/1024) + V_{BIAS}/16 \times (NB/256)$$
$$= V_{BIAS} \times (1 + 1.875 \times NA/1024 + NB/4096)$$

where NA ranges from –512 to +511 and NB ranges from –128 to +127. Figure 28 shows a pictorial view of the transfer function for any DAC.

Configuring the AD7805/AD7809 for Twos Complement Coding

Figure 24 shows a typical configuration for the AD7805/AD7809. The circuit can be used for either 3.3 V or 5 V operation and uses the internal $V_{DD}/2$ as the reference for the part and 10-bit parallel interfacing is used. The following are the steps required to operate the Main DACs in this part.

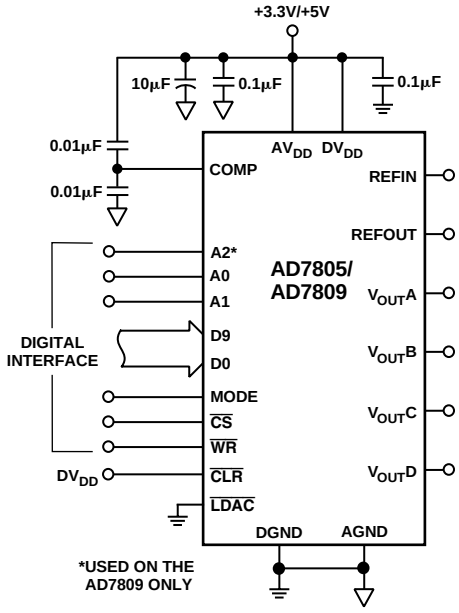


Figure 24. Typical Configuration for AD7805/AD7809

System Control Register Write:

MODE = 0, address inputs (A2, A1, A0) are don't cares.

Write 020 Hex — Configure part for 10-bit parallel, twos complement coding, normal operation

Channel Control Register Write:

MODE = 0, address inputs (A2, A1, A0) select desired channel.

Write 011 Hex — Internal $V_{DD}/2$ selected as V_{BIAS} for DAC, and any DAC data writes that follow are to the Main DAC.

DAC Data Register Write:

MODE = 1, address inputs (A2, A1, A0) select desired channel.

Write XXX Hex — With MODE = 1 all data writes are to the selected DAC. XXX is the required data. 200 Hex will give zero scale and 1FF Hex will give full scale from the DAC.

Table VI and Figure 22 show the analog outputs available for the above configuration. The following is the procedure required if the complete transfer function needs to be offset around the V_{BIAS} point. Table VII and Figure 23 show the analog output variations available from the Sub DAC.

System Control Register Write:

MODE = 0, address inputs (A2, A1, A0) are don't cares.

Write 020 Hex — Configure part for 10-bit parallel, twos complement coding, normal operation

Channel Control Register Write:

MODE = 0, address inputs (A2, A1, A0) select desired channel.

Write 091 Hex — Internal $V_{DD}/2$ selected as V_{BIAS} for DAC, and any DAC data writes that follow are to the Sub DAC.

DAC Data Register Write:

MODE = 1, address inputs (A2, A1, A0) select desired channel.

Write XX Hex — With MODE = 1 all data writes are to the selected DACs Sub DAC. XX is the required data. 7F Hex will give zero scale and 80 Hex will give full scale from the Sub DAC.

Channel Control Register Write:

MODE = 0, address inputs (A2, A1, A0) select desired channel.

Write 011 Hex — Internal $V_{DD}/2$ selected as V_{BIAS} for DAC, and any DAC data writes that follow are to the Main DAC.

DAC Data Register Write:

MODE = 1, address inputs (A2, A1, A0) select desired channel.

Write XXX Hex — With MODE = 1 all data writes are to the selected Main DAC. XXX is the required data. 1FF Hex will give zero scale and 200 Hex will give full scale from the DAC.

OFFSET BINARY CODING

Table VIII shows the offset binary transfer function for the Main DAC**.**

Table VIII. Offset Binary Code Table for Main DAC

Digital Inputs MSB . . . LSB	Analog Output
1111111111	$V_{BIAS}+1.875 \times V_{BIAS}(1023–512)/1024$
1111111110	$V_{BIAS}+1.875 \times V_{BIAS}(1022–512)/1024$
1000000001	$V_{BIAS}+1.875 \times V_{BIAS}/1024$
1000000000	V_{BIAS}
0111111111	$V_{BIAS}+1.875 \times V_{BIAS}(511–512)/1024$
0000000001	$V_{BIAS}+1.875 \times V_{BIAS}(1–512)/1024$
0000000000	$V_{BIAS}/16$

NOTE: The span range is $(30/16) \times V_{BIAS} = 1.875 \times V_{BIAS}$

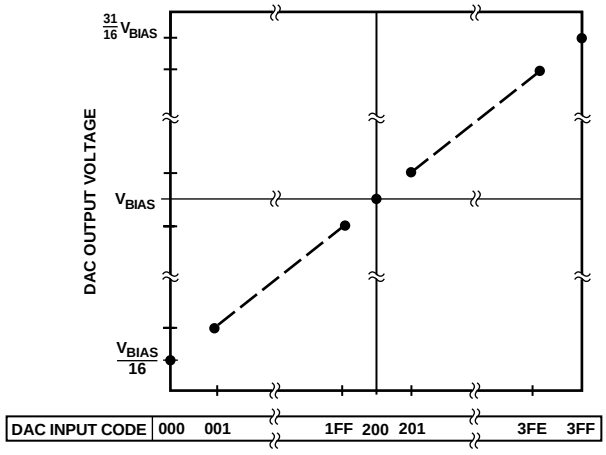


Figure 25. Main DAC Output Voltage vs. DAC Input Codes (HEX) for Offset Binary Coding

Figure 25 shows the Main DAC transfer function when offset binary coding is used. With offset binary coding selected the output voltage can be calculated as follows:

$$V_{OUT}' = V_{BIAS} + 1.875 \times V_{BIAS} \times ((NA\text{-}512)/1024)$$

where NA is the decimal equivalent of the offset binary input code. NA ranges from 0 to 1023.

Table IX shows the offset binary transfer function for the Sub DAC. Figure 26 shows the Sub DAC transfer function for offset binary coding. Any Sub DAC output voltage can be expressed as:

$$V_{OUT}'' = V_{BIAS}/16 \times [(NB\text{-}128)/256]$$

where NB is the decimal equivalent of the offset binary input code. NB ranges from 0 to 255.

Table IX. Offset Binary Code Table for Sub DAC

Digital Input MSB . . . LSB	Analog Output
11111111	$V_{BIAS}/16 \times 127/256$
11111110	$V_{BIAS}/16 \times 126/256$
10000001	$V_{BIAS}/16 \times 1/256$
10000000	0
01111111	$-V_{BIAS}/16 \times 1/256$
00000001	$-V_{BIAS}/16 \times 127/256$
00000000	$-V_{BIAS}/32$

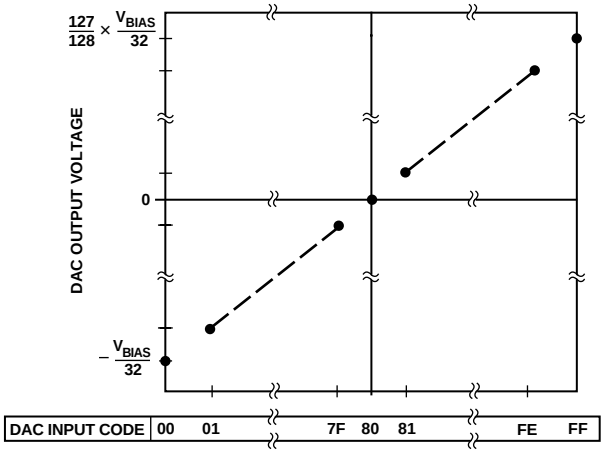


Figure 26. Sub DAC Output Voltage vs. DAC Input Codes (HEX) for Offset Binary Coding

Configuring the AD7804/AD7808 for Offset Binary Coding
Figure 27 shows a typical configuration for the AD7804/AD7808. This circuit can be used for both 3.3 V or 5 V operation and uses an external AD589 as the reference for the part and serial interfacing with offset binary coding is used. The MX1 and MX0 bits in the system control register have to be set to enable selection of the AD589 as the reference. The following are the steps required to operate the DACs in this part. Figures 4 to 7 show the contents of the registers on the AD7804/AD7808.

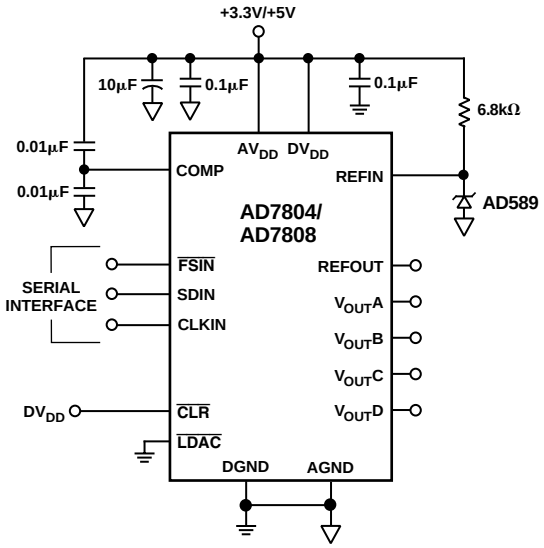


Figure 27. Typical Configuration for AD7804/AD7808 Using an AD589 1.23 V Reference for the AD7804/AD7808

System Control Register Serial Write:

Write 0060 Hex — Mode bits select system control register and configure system for offset binary coding and normal operation.

Channel Control Register Serial Write:

Write 4210 Hex — Mode bits select channel control register, channel A is configured for operation with external reference.

Main DAC Data Register Serial Write:

Write 23FF Hex — This 16-bit write selects writing to channel A and writes full scale to the Main DAC.

Sub DAC Data Register Serial Write:

Write A3FF Hex — This 16-bit write selects writing to channel A Sub DAC and writes full scale to the Sub DAC.

Table VIII and Figure 25 show the analog outputs available for the above configuration when writing to the Main DAC only while Table IX and Figure 26 show the contributions from the Sub DAC to the overall transfer function. The total output for a single channel when using offset binary coding is the sum of that from the Main DAC and the Sub DAC.

$$V_{OUT} = V_{OUT}' + V_{OUT}''$$
$$= V_{BIAS} + 1.875 \times V_{BIAS} \times ((NA\text{-}512)/1024) + V_{BIAS}/16$$
$$= \times [(NB\text{-}128)/256]$$
$$= V_{BIAS} \times (1 + 1.875 \times ((NA\text{-}512)/1024) + (NB\text{-}128)/4096)$$

where NA ranges from 0 to +1023 and NB ranges from 0 to +255. Figure 28 shows a pictorial view of the transfer function for any DAC channel.

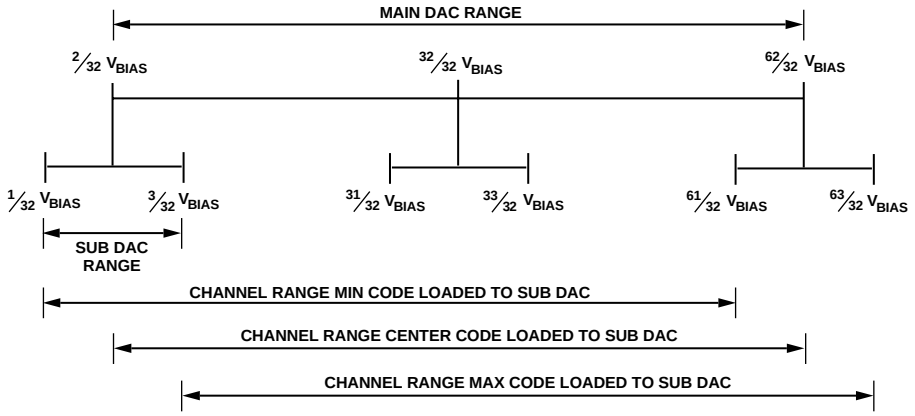


Figure 28. Pictorial View of Transfer Function for Any DAC Channel

Grounding and Layout Techniques

To obtain optimum performance from the AD7804/AD7805/AD7808/AD7809 care should be taken with the layout. Causes for concern would be feedthrough from the interface bus onto the analog circuitry particularly the reference pins and ground loops. The board should be designed such that the analog and digital sections are separated as much as possible. Ground planing and shielding should be used as much as possible. Digital and analog ground planes should only be joined in one place to avoid ground loops. The ideal place to join the ground planes is at the analog and digital ground pins of the DAC. Alternatively a star ground should be established on the board to which all other grounds are returned. Good decoupling is important in achieving optimum performance. All supplies, analog or digital, should be decoupled with 10 µF tantalum and 0.1 µF ceramic capacitors to their respective grounds, and should be as close as possible to the pins of the device. The main aim of the bypassing element is to maximize the charge stored in the bypass loop while simultaneously minimizing the inductance of this loop. Inductance in the loop acts as an impedance to high frequency transients and results in power supply spiking. By keeping the decoupling as close as possible to the device, the loop area is kept to a minimum thus reducing the possibility of power supply spikes.

On the AD7805 the REFOUT pin of the device is located next to the DB9 of the data bus, to reduce the risk of digital feedthrough and noise being coupled from the digital section onto the reference, the REFOUT pin and any trace connected to it should be shielded with analog ground. To reduce the noise on this reference it should be decoupled with a 0.01 µF capacitor to analog ground, keeping the capacitor as close as possible to the device. The comp pin which is the output from the internal $V_{DD}/2$ reference is located next to $V_{OUT}D$ on the DAC and is sensitive to noise pickup and feedthrough from the DAC output and thus should be shielded with analog ground to keep this reference point as quiet as possible. The comp pin should be decoupled both to AV_{DD} and AGND with 1–10 nF ceramic capacitors. The external REFIN pin should also be shielded with analog ground from the digital pins located next to it.

The same precautions should be taken with the reference pins on the AD7804/AD7808 to reduce the risk of noise pickup and feedthrough.

Reference Settling Time

With the REFOUT on the AD7804/AD7805/AD7808/AD7809 decoupled with a 0.01 µF capacitor to AGND it takes the REFOUT approximately 2 ms to fully settle after taking the device out of power down. When this capacitor is reduced to 1 nF the settling time reduces to 150 µs. The size of the capacitor required on the REFOUT depends to a large extent on the layout, if the REFOUT is well shielded with AGND the size of the capacitor can be reduced thus reducing the settling time for the reference. The internal $V_{DD}/2$ reference provided at the comp pin when decoupled with a 1 nF capacitor to both AV_{DD} and AGND has very fast settling time, typically less than 500 ns.

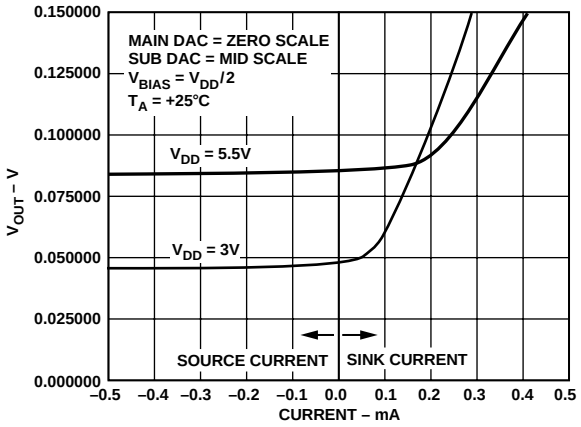


Figure 29. Sink and Source Current with Zero Scale Loaded to DAC. V_{DD} = 5 V and V_{DD} = 3 V

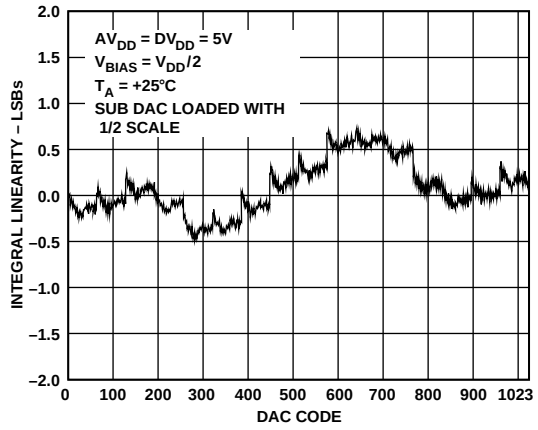


Figure 32. Integral Linearity with 5 V Operation

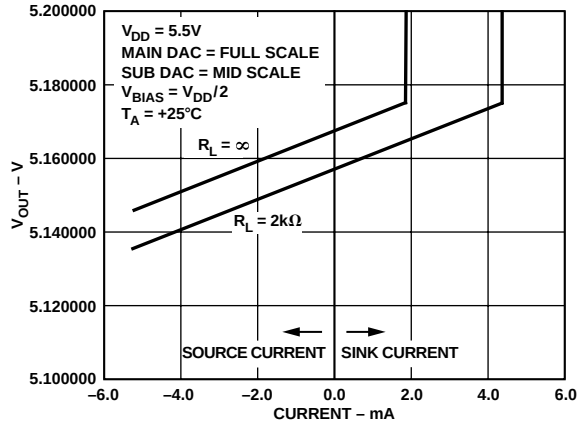


Figure 30. Sink and Source Current at Full Scale with V_{DD} = 5 V

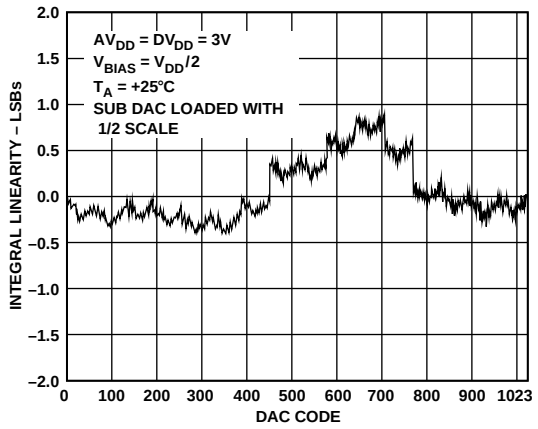


Figure 33. Integral Linearity with 3 V Operation

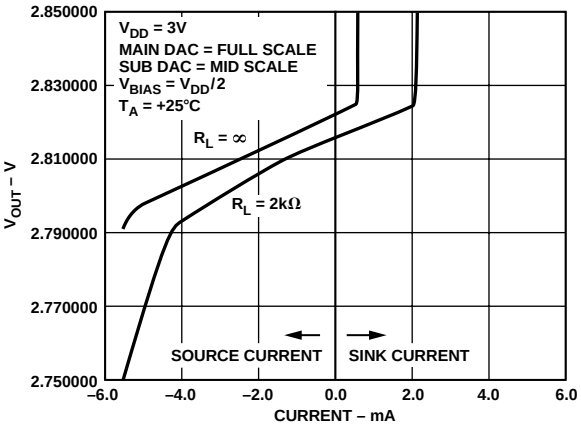


Figure 31. Sink and Source Current at Full Scale with V_{DD} = 3 V

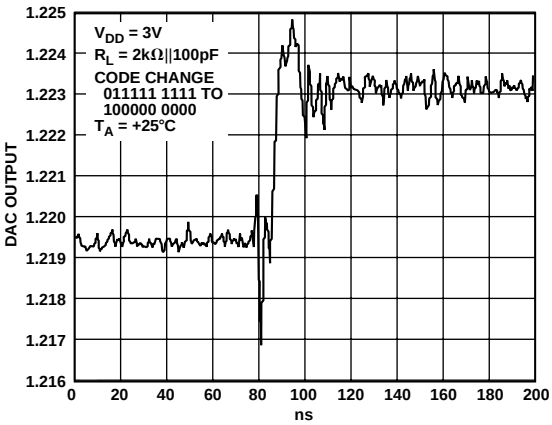


Figure 34. Digital-to-Analog Glitch Impulse

MICROPROCESSOR INTERFACING

AD7804/AD7808–ADSP-2101/ADSP-2103 Interface

Figure 35 shows a serial interface between the AD7804/AD7808 and the ADSP-2101/ADSP-2103. The ADSP-2101/ADSP-2103 should be set up to operate in the SPORT Transmit Alternate Framing Mode. The ADSP-2101/ADSP-2103 SPORT is programmed through the SPORT control register and should be configured as follows: Internal Clock Operation, Active Low Framing, 16-bit Word Length. Transmission is initiated by writing a word to the TX register after the SPORT has been enabled. The data is clocked out on each rising edge of the serial clock and clocked into the AD7804/AD7808 on the falling edge of the SCLK.

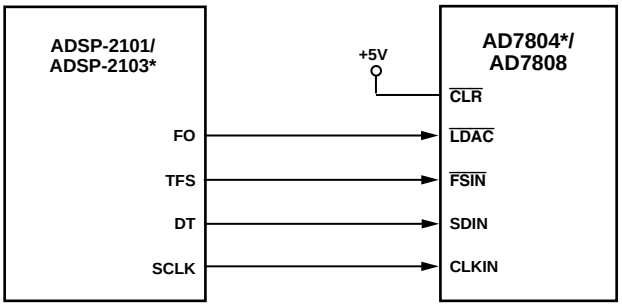


Figure 35. ADSP-2101/ADSP-2103 Interface

AD7804/AD7808–68HC11/68L11 Interface

Figure 36 shows a serial interface between the AD7804/AD7808 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the CLKIN of the AD7804/AD7808, while the MOSI output drives the serial data line of the DAC. The $\overline{\text{FSIN}}$ signal is derived from a port line (PC7). The setup conditions for correct operation of this interface are as follows: the 68HC11/68L11 should be configured so that its CPOL bit is a 0 and its CPHA bit is a 1. When data is being transmitted to the DAC the $\overline{\text{FSIN}}$ line is taken low (PC7). When the 68HC11/68L11 is configured as above, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to load data to the AD7804/AD7808, PC7 is left low after the first eight bits are transferred and a second serial write operation is performed to the DAC and then PC7 is taken high at the end of this procedure. In the diagram shown $\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$ are also controlled from the bit programmable lines of the 68HC11/68L11. The user can bring $\overline{\text{LDAC}}$ low after every two bytes have been transmitted to update that particular DAC which has been programmed or alternatively it is possible to wait until all the input registers have been loaded before updating takes place.

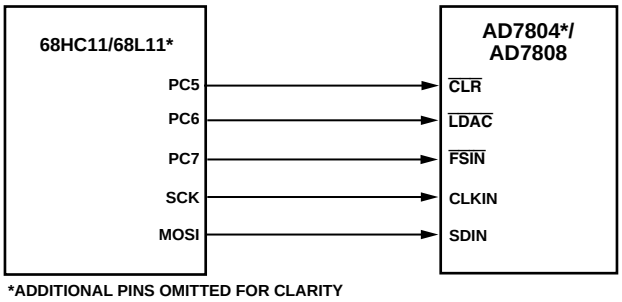


Figure 36. AD7804/AD7808–68HC11/68L11 Interface

AD7804/AD7808–80C51/80L51 Interface

Figure 37 shows a serial interface between the AD7804/AD7808 and the 80C51/80L51 microcontroller. The setup for the interface is as follows, TXD of the 80C51/80L51 drives CLKIN of the AD7804/AD7808 while RXD drives the serial data line of the part. The $\overline{\text{FSIN}}$ signal is again derived from a bit programmable pin on the port in this case port line P3.3 is used. When data is to be transmitted to the part, P3.3 is taken low. Data on RXD is valid on the falling edge of TXD. The 80C51/80L51 transmits data in eight bit bytes thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted and a second write cycle is initiated to transmit the second byte of data, P3.3 is taken high following the completion of this cycle. The 80C51/80L51 outputs the serial data in a format which has the LSB first. The AD7804/AD7808 requires its data with the MSB as the first bit received. The 80C51/80L51 transmit routine should take this into account. In the diagram shown $\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$ are also controlled from the bit programmable lines of the 80C51/80L51 port. The user can bring $\overline{\text{LDAC}}$ low after every two bytes have been transmitted to update that particular DAC which has been programmed or alternatively it is possible to wait until all the input registers have been loaded before updating takes place.

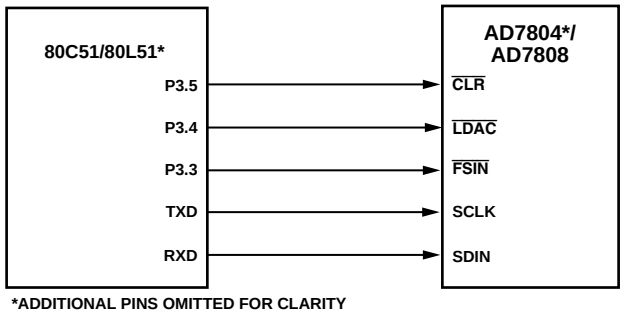


Figure 37. AD7804/AD7808–80C51/80L51 Interface

AD7805/AD7809–ADSP-2101 Interface

Figure 38 shows a parallel interface between the AD7805/AD7809 and the ADSP-2101/ADSP-2103 digital signal processor.

Fast interface timing allows the AD7805/AD7809 interface directly to the DSP. In this interface an external timer is used to update the DACs.

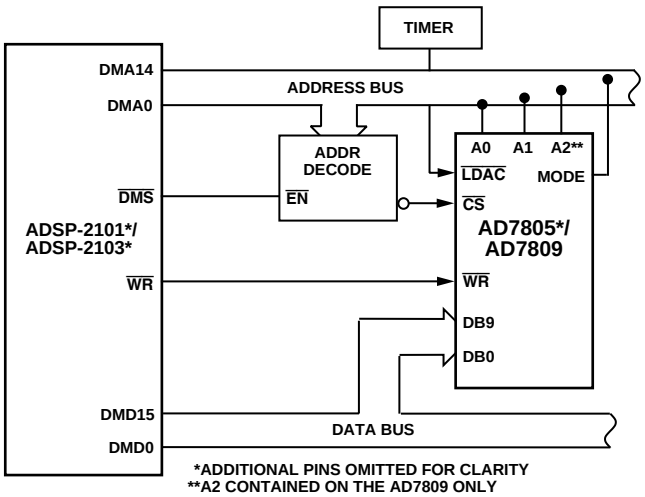


Figure 38. AD7805/AD7809–ADSP-2101/ADSP-2103 Interface

Data is loaded to the AD7805/AD7809 input register using the following instruction:

DM(DAC) = MR0,

MR0 = ADSP-2101 MR0 Register.

DAC = Decoded DAC Address.

AD7805/AD7809–TMS32020 Interface

Figure 39 shows a parallel interface between the AD7805/AD7809 and the TMS32020 processor.

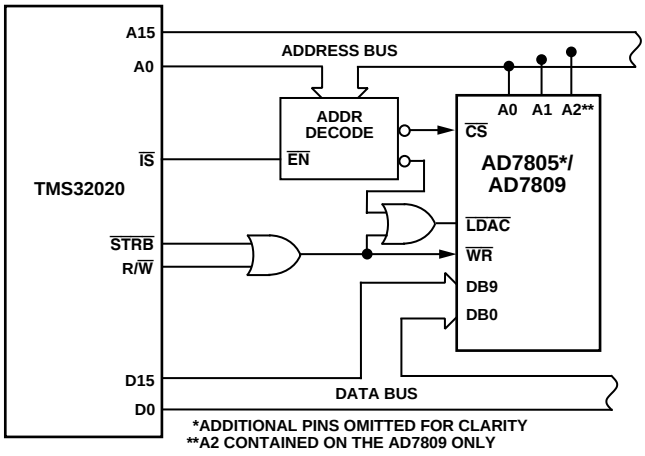


Figure 39. AD7805/AD7809–TMS32020 Interface

Again fast interface timing allows the AD7805/AD7809 interface directly to the processor. Data is loaded to the AD7805/AD7809 input latch using the following instruction:

OUT DAC, D.

DAC = Decoded DAC Address.

D = Data Memory Address.

Certain applications may require that the updating of the DAC latch be controlled by the microprocessor rather than the external timer. One option as shown in the TMS32020 interface is to decode the $\overline{\text{LDAC}}$ from the address bus so that a write operation to the DAC latch (at a separate address to the input latch) updates the output.

AD7805/AD7809–8051/8088 Interface

Figure 40 shows a parallel interface between the AD7805/AD7809 and the 8051/8088 processors.

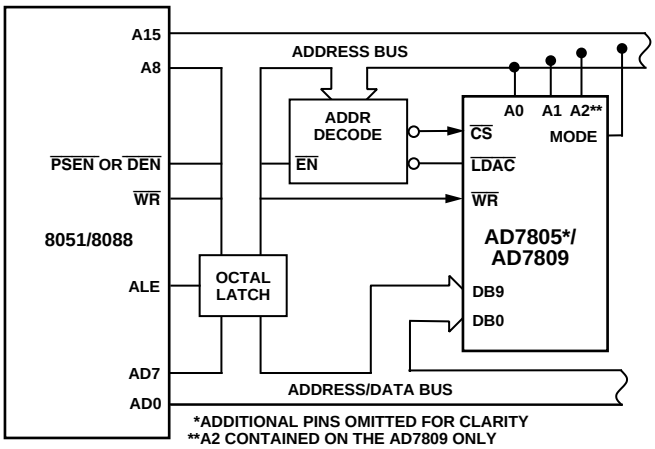


Figure 40. AD7805/AD7809–8051/8088 Interface

APPLICATIONS

Opto-Isolated Interface for Process Control Applications

The AD7804/AD7808 has a versatile serial three-wire serial interface making it ideal for generating accurate voltages in process control and industrial applications. Due to noise, safety requirements, or distance, it may be necessary to isolate the AD7804/AD7808 from the controller. This can easily be achieved by using opto-isolators which will provide isolation in excess of 3 kV. The serial loading structure of the AD7804/AD7808 makes it ideally suited for use in opto-isolated applications. Figure 41 shows an opto-isolated interface to the AD7804/AD7808 where SDIN, CLKIN and $\overline{\text{FSIN}}$ are driven from optocouplers. $\overline{\text{LDAC}}$ is hardwired low to reduce the number of interface lines and this ensures that each DAC is updated following the sixteenth serial clock of a write cycle.

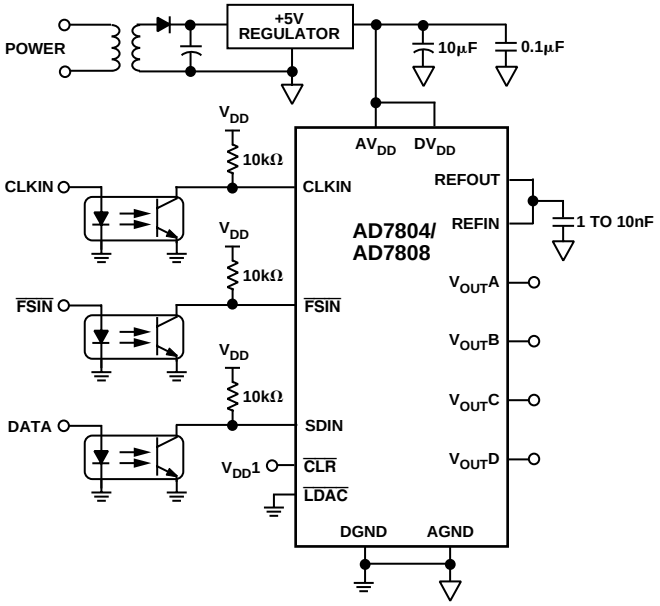


Figure 41. AD7804/AD7808 Opto-Isolated Interface

Decoding Multiple AD7808s

The $\overline{\text{FSIN}}$ pin on the AD7808s can be used in applications to decode a number of DACs. In this application all DACs in the system receive the same serial clock and serial data, but only the $\overline{\text{FSIN}}$ to one of the DACs will be active at any one time allowing access to eight channels in this thirty-two channel system. The 74HC139 is used as a 2- to 4-line decoder to address any of the DACs in the system. To prevent timing errors from occurring the enable input should be brought to its inactive state while the coded address inputs are changing state. Figure 42 shows a system decoding multiple AD7808s in a multichannel system.

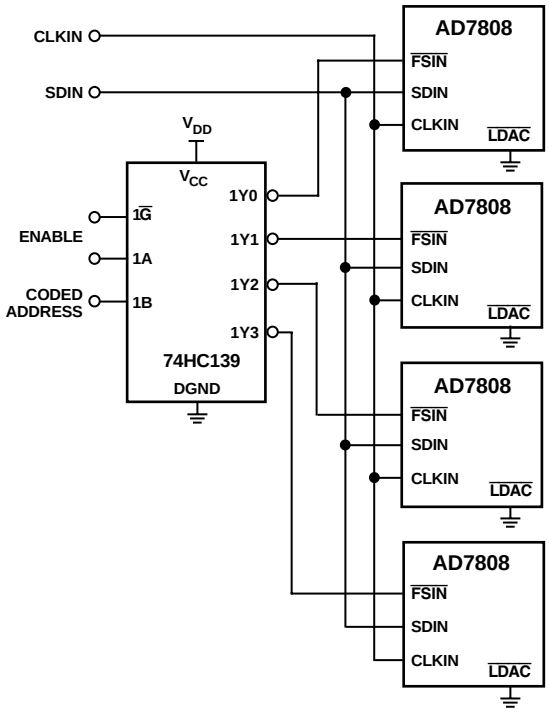


Figure 42. Decoding Multiple AD7808s Using the $\overline{\text{FSIN}}$ Pin

AD7805 As a Digitally Programmable Window Detector

A digitally programmable upper/lower limit detector using two DACs in the AD7805 is shown in Figure 43. The upper and lower limits for the test are loaded to DACs A and B that in turn set the limits on the CMP04. If a signal at the V_{IN} input is not within the programmed window an LED will indicate the fail condition. Only one limit detector is shown below but can easily be adapted for a dual channel system by using the extra DACs on the AD7805 and the two unused comparators on the CMP04.

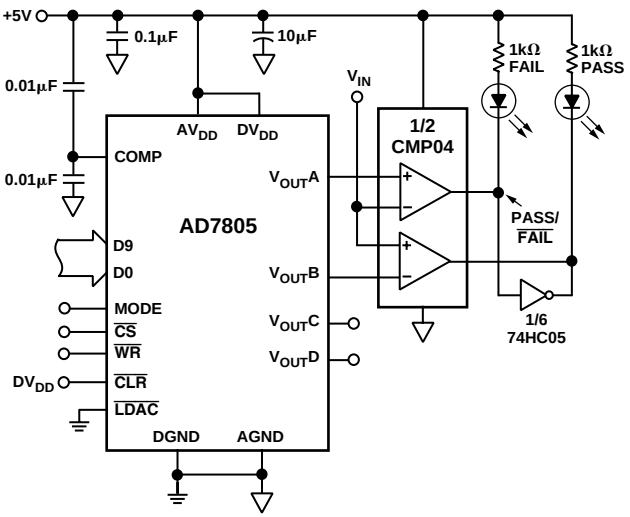


Figure 43. Digitally Programmable Window Detector

Low Cost, Two-Channel Mixer Using AD7805, SSM2164 and OP275

The SSM2164 is a quad voltage controlled amplifier (VCA) with 120 dB of gain control range. Each VCA in the package is a current in, current out device with a –33 mV/dB voltage control input port. Figure 44 shows a basic application circuit which can be used to implement a low cost stereo, two channel mixer. A 30 kΩ resistor converts the input voltage to an input current for the VCA. The 500 Ω resistor and 560 pF capacitor on the input are added to ensure stable operation of the SSM2164. The I_{OUT} pin of the SSM2164 should be maintained at virtual ground and thus the OP275 is operated in its inverting mode. Its wide bandwidth, high slew rate and low power make it ideal for a current to voltage converter. A 30 kΩ feedback resistor is chosen to match the input resistor and thus give unity gain for a zero volt control voltage input. The 100 pF capacitors reduce high frequency noise and can be increased to reduce the low pass cutoff frequency for further noise reduction. The AD7805 in the circuit is used to control the attenuation of the VCA, this application circuit only gives attenuation. The voltage output from the AD7805 provides a low impedance drive to the SSM2164 so attenuation can be controlled accurately. With a 5 V V_{DD} and a V_{BIAS} of $V_{DD}/2$ the AD7805 has an LSB size of approximately 4.5 mV. Therefore, the attenuation can be controlled with a resolution of 0.136 dB/bit and thus 750 codes are required to provide the full 100 dB of attenuation.

Dual External Reference Input Capability

It is possible to operate the AD7804/AD7805/AD7808/AD7809 with two externally applied references. Figure 45 shows the connections for the AD7804. Reference one, the AD589, is connected to the REFIN pin of the part; the second reference, the AD780, is used to overdrive the internal VDD/2 reference which is provided at the COMP pin of the device. With the circuit shown in Figure 45 it is possible to configure two of the channels for operation with the AD780 2.5 V reference and the other two with the AD589 1.23 V reference. The channel control register allows the user to select the reference for the individual channels.

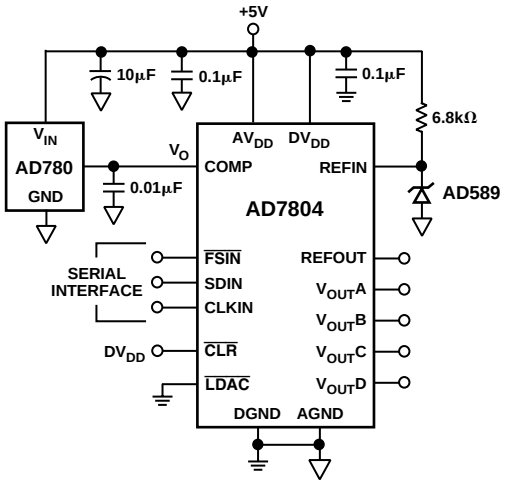


Figure 45. Two Externally Applied References

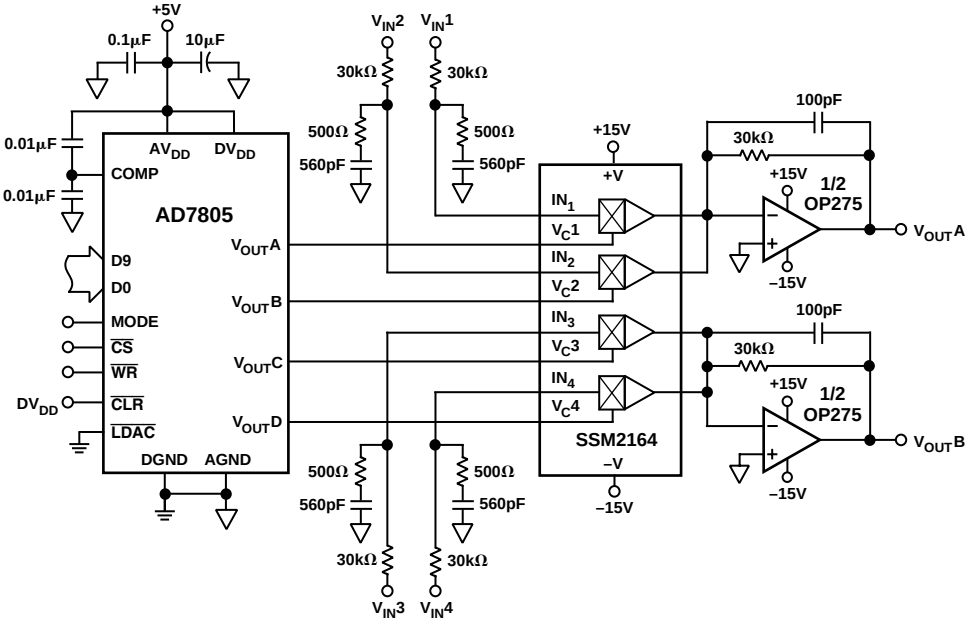


Figure 44. Low Cost, Two-Channel Mixer

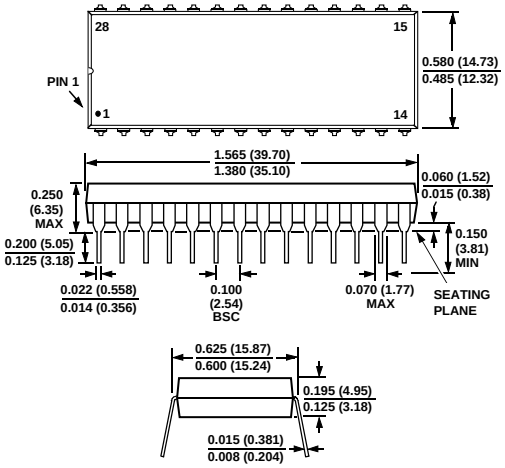
PAGE INDEX
(AD7804/AD7808 SERIAL INTERFACE PART)

PAGE INDEX
(AD7805/AD7809 PARALLEL INTERFACE PART)

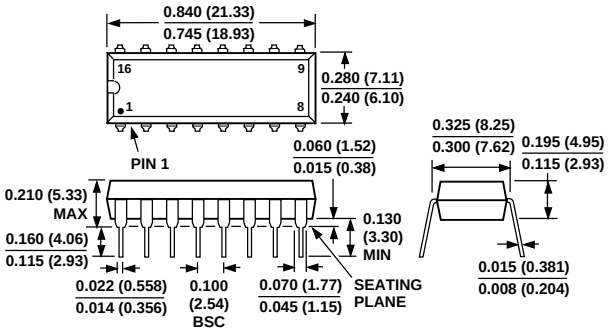
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

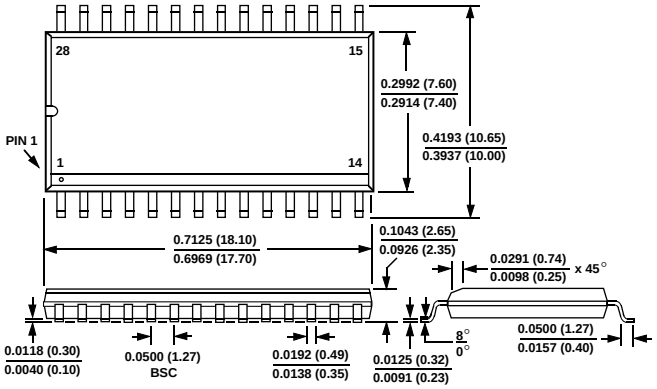
Plastic DIP (N-28)



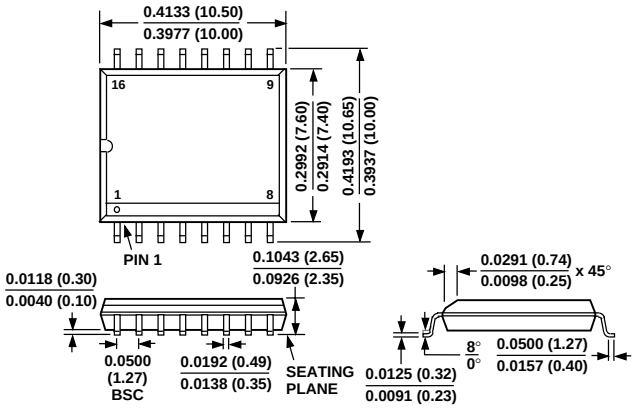
Plastic DIP (N-16)



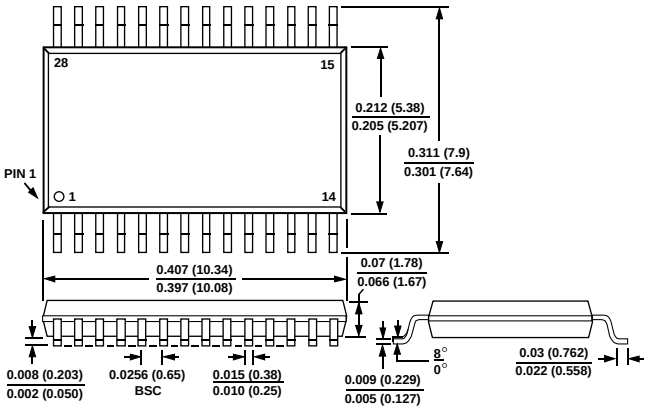
SOIC (R-28)



SOIC (R-16)



SSOP (RS-28)

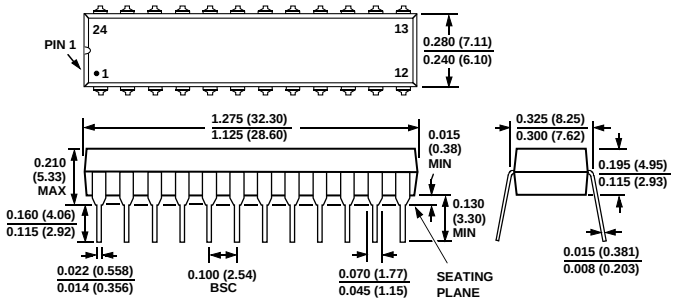


1. LEAD NO. 1 IDENTIFIED BY A DOT.
2. LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS

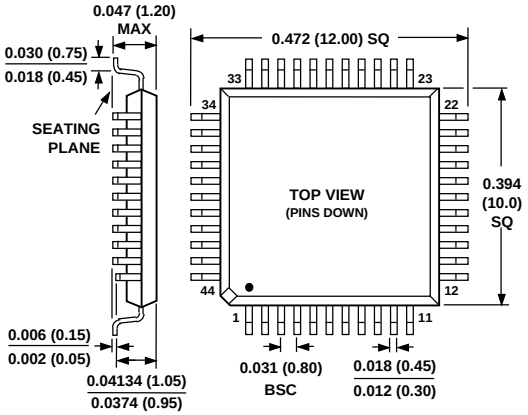
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

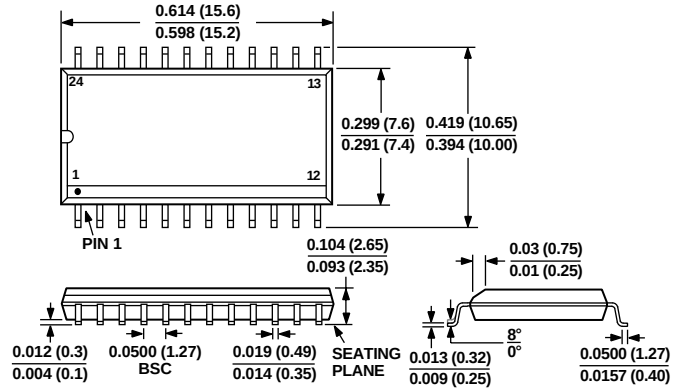
Plastic DIP (N-24)



TQFP (SU-44)



SOIC (R-24)



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