

## FEATURES

- Ultralow voltage noise (0.1 Hz to 10 Hz): 1.2  $\mu$ V p-p**
- Superb temperature drift: 5 ppm/ $^{\circ}$ C**
- Low dropout operation (supply voltage headroom): 500 mV**
- Supply voltage operating range: 3 V to 18 V**
- High output source and sink current**  
+10 mA and -5 mA, respectively

## ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)**
- Military temperature range (-55 $^{\circ}$ C to +125 $^{\circ}$ C)**
- Controlled manufacturing baseline**
- 1 assembly/test site**
- 1 fabrication site**
- Product change notification**
- Qualification data available on request**

## APPLICATIONS

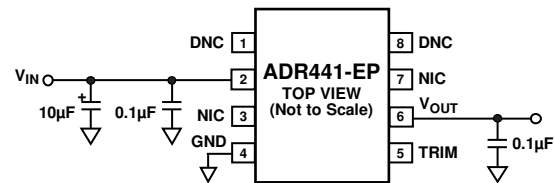
- Precision data acquisition systems**
- High resolution data converters**
- Battery-powered instrumentation**
- Precision instruments**
- Military communication**
- Unmanned systems**
- Avionics**

## GENERAL DESCRIPTION

The ADR441-EP<sup>1</sup> is a XFET<sup>®</sup> voltage reference featuring ultralow noise, high accuracy, and low temperature drift performance. Using Analog Devices, Inc., temperature drift curvature correction and extra implanted junction FET (XFET) technology, voltage change vs. temperature nonlinearity in the ADR441-EP is greatly minimized.

The XFET reference offers better noise performance than buried Zener references, and the XFET reference operates off low supply voltage headroom (500 mV). This combination of features makes the ADR441-EP ideally suited for precision signal conversion applications in high end data acquisition systems, military communication, and avionics applications.

## TYPICAL APPLICATION CIRCUIT



### NOTES

1. NIC = NOT INTERNALLY CONNECTED. THIS PIN IS NOT CONNECTED INTERNALLY.
2. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

Figure 1.

17030-001

The ADR441-EP has the capability to source up to +10 mA of output current and sink up to -5 mA. The device also comes with a trim terminal to adjust the output voltage over a 0.5% range without compromising performance.

The ADR441-EP is available in an 8-lead, narrow SOIC package. The ADR441-EP is specified over the military temperature range of -55 $^{\circ}$ C to +125 $^{\circ}$ C. Additional application and technical information can be found in the [ADR441](#) data sheet.

<sup>1</sup> Protected by U.S. Patent Number 5,838,192.

### Rev. 0

### Document Feedback

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

**TABLE OF CONTENTS**

Features .....	1	Absolute Maximum Ratings .....	4
Enhanced Product Features .....	1	Thermal Resistance .....	4
Applications .....	1	ESD Caution.....	4
Typical Application Circuit .....	1	Pin Configuration and Function Descriptions.....	5
General Description .....	1	Typical Performance Characteristics .....	6
Revision History .....	2	Outline Dimensions .....	8
Specifications.....	3	Ordering Guide .....	8
Electrical Characteristics .....	3		

**REVISION HISTORY**

7/2018—Revision 0: Initial Version

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS

$V_{IN} = 3\text{ V to }18\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , and input capacitance ( $C_{IN}$ ) = output capacitance ( $C_{OUT}$ ) =  $0.1\ \mu\text{F}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	$V_{OUT}$		2.499	2.500	2.501	V
INITIAL ACCURACY	$V_{OERR}$				$\pm 1$ 0.04	mV %
TEMPERATURE DRIFT	$TCV_{OUT}$	$-55^\circ\text{C} < T_A < +125^\circ\text{C}$		1	5	ppm/ $^\circ\text{C}$
REGULATION						
Line	$\Delta V_{OUT}/\Delta V_{IN}$	$-55^\circ\text{C} < T_A < +125^\circ\text{C}$		10	20	ppm/V
Load	$\Delta V_{OUT}/\Delta I_{LOAD}$	Load current ( $I_{LOAD}$ ) = 0 mA to 10 mA, $V_{IN} = 4\text{ V}$ , $-55^\circ\text{C} < T_A < +125^\circ\text{C}$	-50		+50	ppm/mA
	$\Delta V_{OUT}/\Delta I_{LOAD}$	$I_{LOAD} = 0\text{ mA to }-5\text{ mA}$ , $V_{IN} = 4\text{ V}$ , $-55^\circ\text{C} < T_A < +125^\circ\text{C}$	-50		+50	ppm/mA
OUTPUT CURRENT CAPACITY	$I_{LOAD}$					
Sourcing				10		mA
Sinking				-5		mA
QUIESCENT CURRENT	$I_{IN}$	No load, $-55^\circ\text{C} < T_A < +125^\circ\text{C}$		3	3.75	mA
VOLTAGE NOISE	$e_N$ p-p	0.1 Hz to 10 Hz		1.2		$\mu\text{V p-p}$
Density	$e_N$	1 kHz		48		nV/ $\sqrt{\text{Hz}}$
TURN-ON SETTLING TIME	$t_R$			10		$\mu\text{s}$
LONG-TERM STABILITY <sup>1</sup>	$\Delta V_{OUT}$	1000 hours		50		ppm
OUTPUT VOLTAGE HYSTERESIS	$V_{OUT\_HYS}$			70		ppm
RIPPLE REJECTION RATIO	RRR	Input frequency ( $f_{IN}$ ) = 1 kHz		-80		dB
SHORT CIRCUIT TO GND	$I_{SC}$			27		mA
SUPPLY VOLTAGE						
Operating Range	$V_{IN}$		3		18	V
Headroom	$V_{IN} - V_{OUT}$		500			mV

<sup>1</sup> The long-term stability specification is noncumulative. The drift in the subsequent 1000 hour period is significantly lower than in the first 1000 hour period.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Rating
Supply Voltage	20 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Operating Temperature Range	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
Junction Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature, Soldering (60 sec)	$300^\circ\text{C}$

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JA}$  is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

$\theta_{JC}$  is the junction to case thermal resistance.

Table 3. Thermal Resistance

Package Type <sup>1</sup>	$\theta_{JA}$	$\theta_{JC}$	Unit
R-8	130	43	$^\circ\text{C}/\text{W}$

<sup>1</sup> Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board. See JEDEC JESD-51.

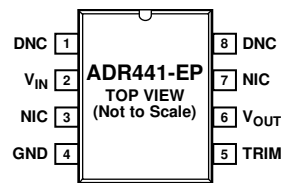
## ESD CAUTION



### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



### NOTES

1. NIC = NOT INTERNALLY CONNECTED.  
THIS PIN IS NOT CONNECTED INTERNALLY.
2. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

17030-101

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8	DNC	Do Not Connect. Do not connect to these pins.
2	V <sub>IN</sub>	Input Voltage Connection.
3, 7	NIC	Not Internally Connected. These pins are not connected internally.
4	GND	Ground.
5	TRIM	Output Voltage Trim.
6	V <sub>OUT</sub>	Output Voltage.

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 7\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , and  $C_{IN} = C_{OUT} = 0.1\ \mu\text{F}$ , unless otherwise noted.

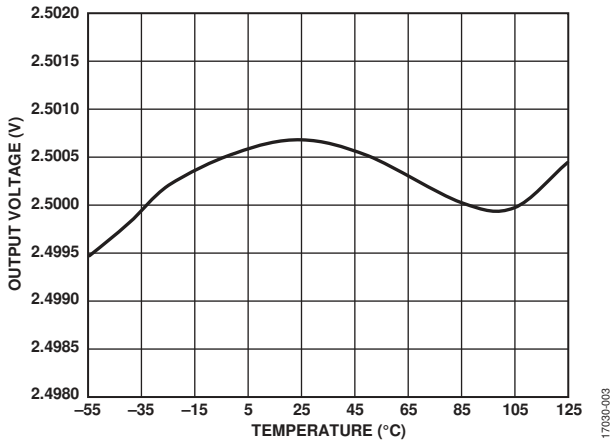


Figure 3. Output Voltage vs. Temperature

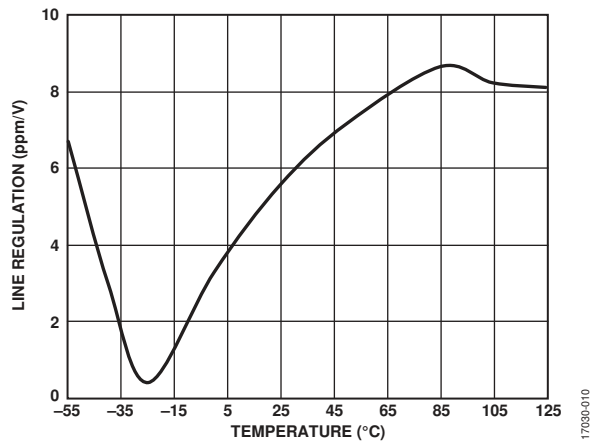


Figure 6. Line Regulation vs. Temperature

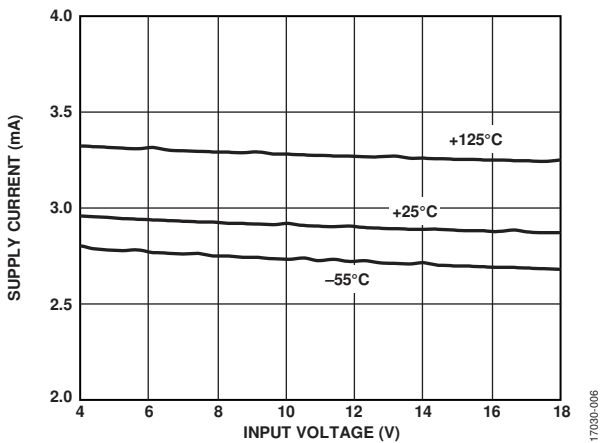


Figure 4. Supply Current vs. Input Voltage for Various Temperatures

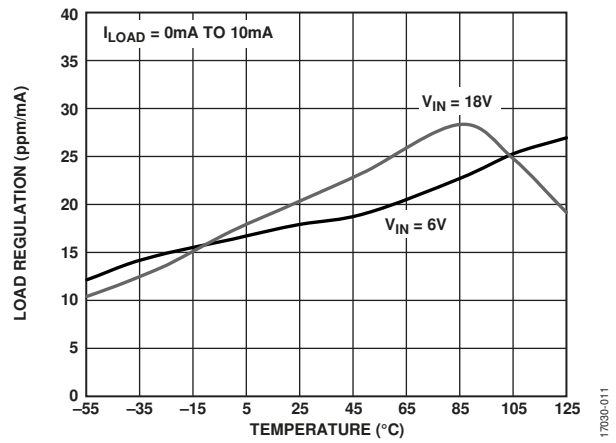


Figure 7. Load Regulation vs. Temperature for Various Input Voltages

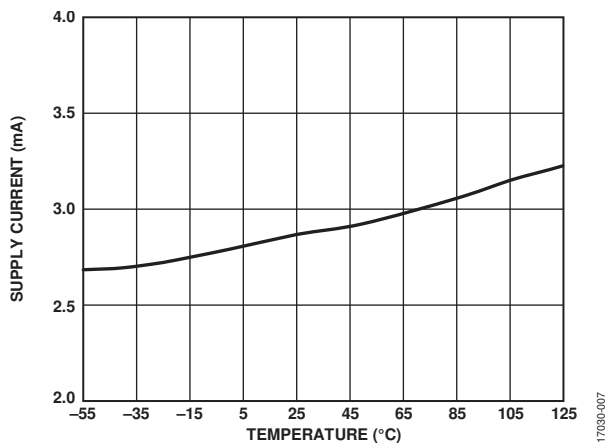


Figure 5. Supply Current vs. Temperature

17030-003

17030-010

17030-006

17030-011

17030-007

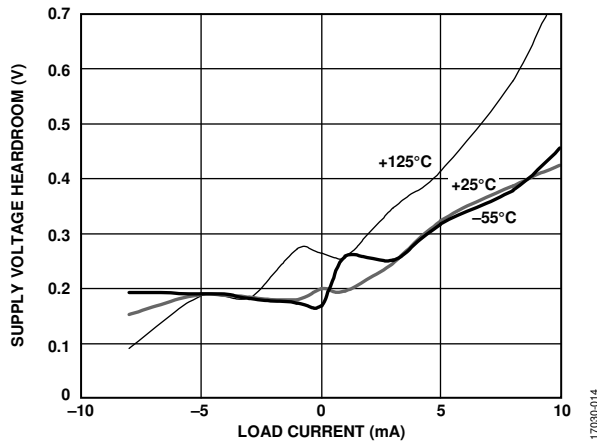


Figure 8. Supply Voltage Headroom vs. Load Current for Various Temperatures

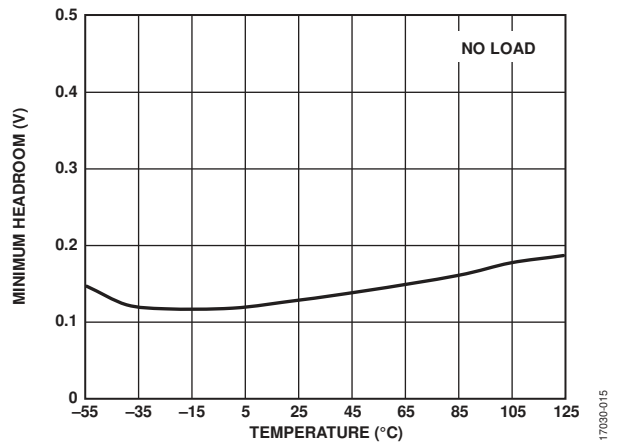
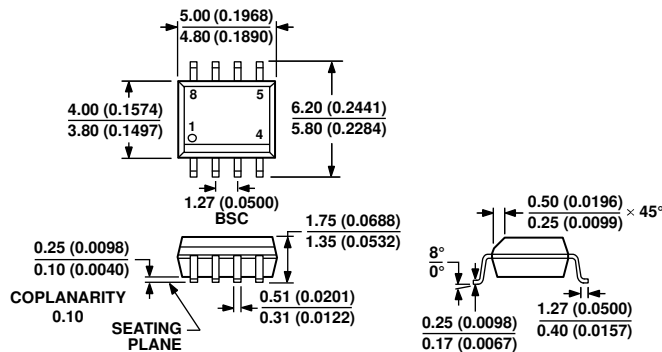


Figure 9. Minimum Headroom vs. Temperature

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 10. 8-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body  
 (R-8)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model <sup>1</sup>	Output Voltage (V)	Initial Accuracy		Temperature Drift (ppm/°C)	Temperature Range	Package Description	Package Option
		±mV	%				
ADR441TRZ-EP	2.500	1	0.04	5	-55°C to +125°C	8-Lead SOIC_N	R-8
ADR441TRZ-EP-R7	2.500	1	0.04	5	-55°C to +125°C	8-Lead SOIC_N	R-8

<sup>1</sup> Z = RoHS Compliant Part.