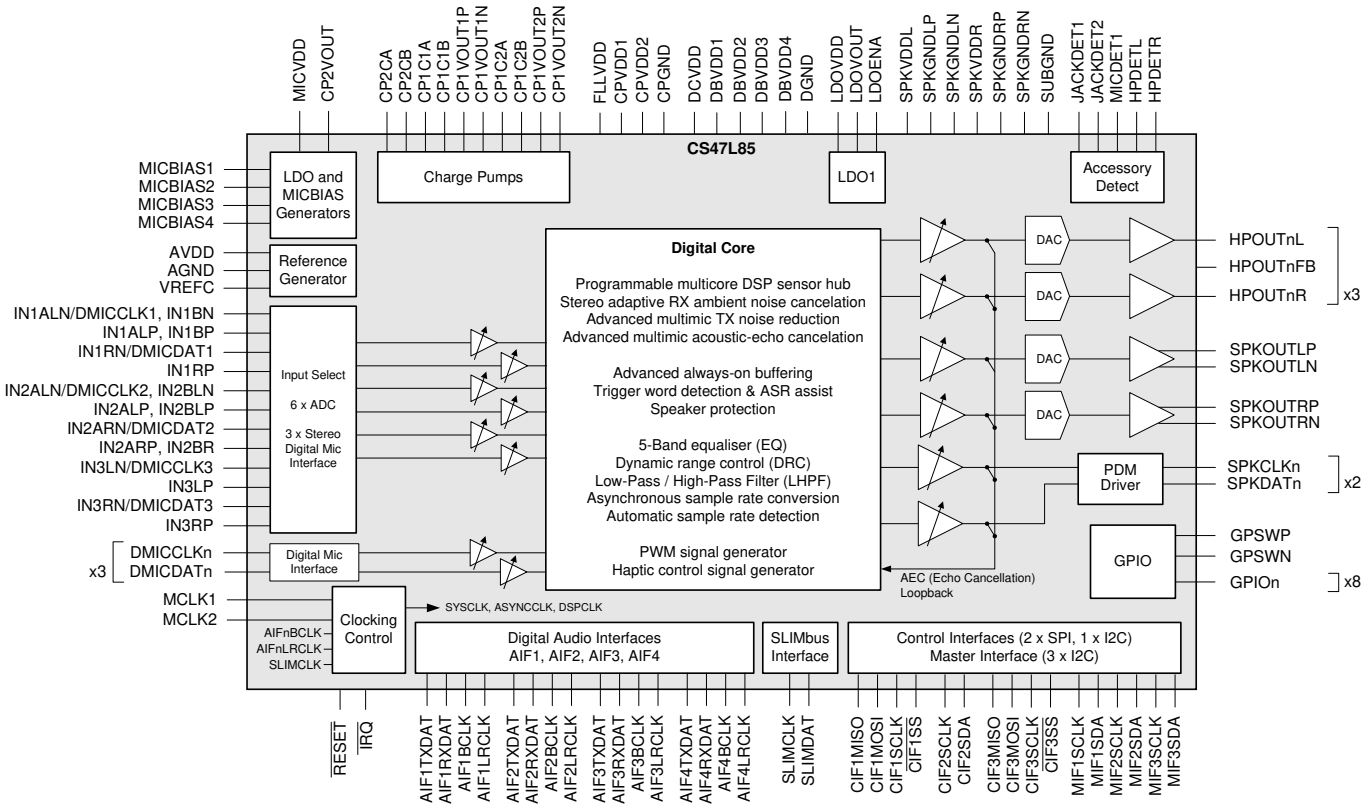
Low-Power Smart Codec with Seven DSP Cores, Voice and Media Enhancement, and Integrated Sensor Hub

Features

- 900 MIPS, 900MMAC multicore audio-signal processor
- Sensor hub capability, with event time-stamp functions
- Programmable wideband, multimic audio processing
  - — Cirrus Logic® adaptive ambient noise cancelation
  - — Transmit-path noise reduction and echo cancelation
  - — Wind noise, sidetone, and other programmable filters
- Multichannel asynchronous sample rate conversion
- Integrated multichannel 24-bit hi-fi audio hub codec
  - — Six ADCs, 100-dB SNR mic input (48 kHz)
  - — Eight DACs, 121-dB SNR headphone playback (48 kHz)
- Up to 9 analog or 12 digital microphone inputs
- Multipurpose headphone/earpiece/line output drivers
  - — 30 mW into 32-Ω load at 0.1% THD+N
- Class D speaker, and digital (PDM) output interfaces
- SLIMbus® audio and control interface
- Four full digital audio interfaces
  - — Standard sample rates from 8 to 192 kHz
  - — Multichannel TDM support on AIF1 and AIF2
- Flexible clocking, derived from MCLKn, AIFn, or SLIMbus
- Low-power frequency-locked loops (FLLs) support reference clocks down to 32 kHz
- Configurable functions on up to 40 GPIO pins
- Integrated regulators and charge pumps
- Small W-CSP package, 0.4-mm staggered ball array

Applications

- Smartphones and multimedia handsets
- Tablets and Mobile Internet Devices (MIDs)



Description

The CS47L85 is a highly integrated, low-power audio and sensor hub system for smartphones, tablets and other portable audio devices. It combines an advanced DSP feature set with a flexible, high-performance audio hub codec. The CS47L85 combines seven programmable DSP cores with a variety of power-efficient fixed-function audio processors. Extensive GPIO and I²C master interfaces enable powerful sensor fusion functions to be integrated.

The DSP cores support multiple concurrent audio features, including multimic wideband noise reduction, high-performance acoustic-echo cancellation (AEC), stereo ambient noise cancellation (ANC), speech enhancement, advanced media enhancement, and many more. The CS47L85 sensor hub technology enables applications to support increased contextual awareness, including advanced motion sensing and pedestrian navigation functionality. The DSP cores are supported by a fully flexible, all-digital mixing and routing engine with sample rate converters, for wide use-case flexibility. Support for third-party DSP programming provides far-reaching opportunities for product differentiation.

A SLIMbus interface supports multi-channel audio paths and host control register access. Four further digital audio interfaces are provided, each supporting a wide range of standard audio sample rates and serial interface formats. Automatic sample rate detection enables seamless wideband/narrowband voice-call handover.

Three stereo headphone drivers each provide stereo ground-referenced or mono BTL outputs. 121dB SNR, and noise levels as low as 0.8 µVRMS, offer hi-fi quality line or headphone output. The CS47L85 also features a stereo pair of 2.5-W Class D outputs, four channels of stereo PDM output, and an IEC-60958-3–compatible S/PDIF transmitter. A signal generator for controlling haptics devices is included; vibe actuators can connect directly to the Class D speaker output or via an external driver on the PDM output interface. All inputs, outputs, and system interfaces can function concurrently.

The CS47L85 supports up to 9 analog inputs, and up to 12 PDM digital inputs. Microphone activity detection with interrupt is available. A smart accessory interface supports most standard 3.5mm accessories. Impedance sensing and measurement is provided for external accessory and push-button detection.

The CS47L85 is configured using the SLIMbus, SPI™, or I²C interfaces. Three integrated FLLs provide support for a wide range of system clock frequencies. The device is powered from 1.8- and 1.2-V supplies. (A separate 4.2-V battery supply is typically required for the Class D speaker drivers). The power, clocking and output driver architectures are all designed to maximise battery life in voice, music and standby modes. Low-power (10µA) ‘Sleep’ is supported, with configurable wake-up events.

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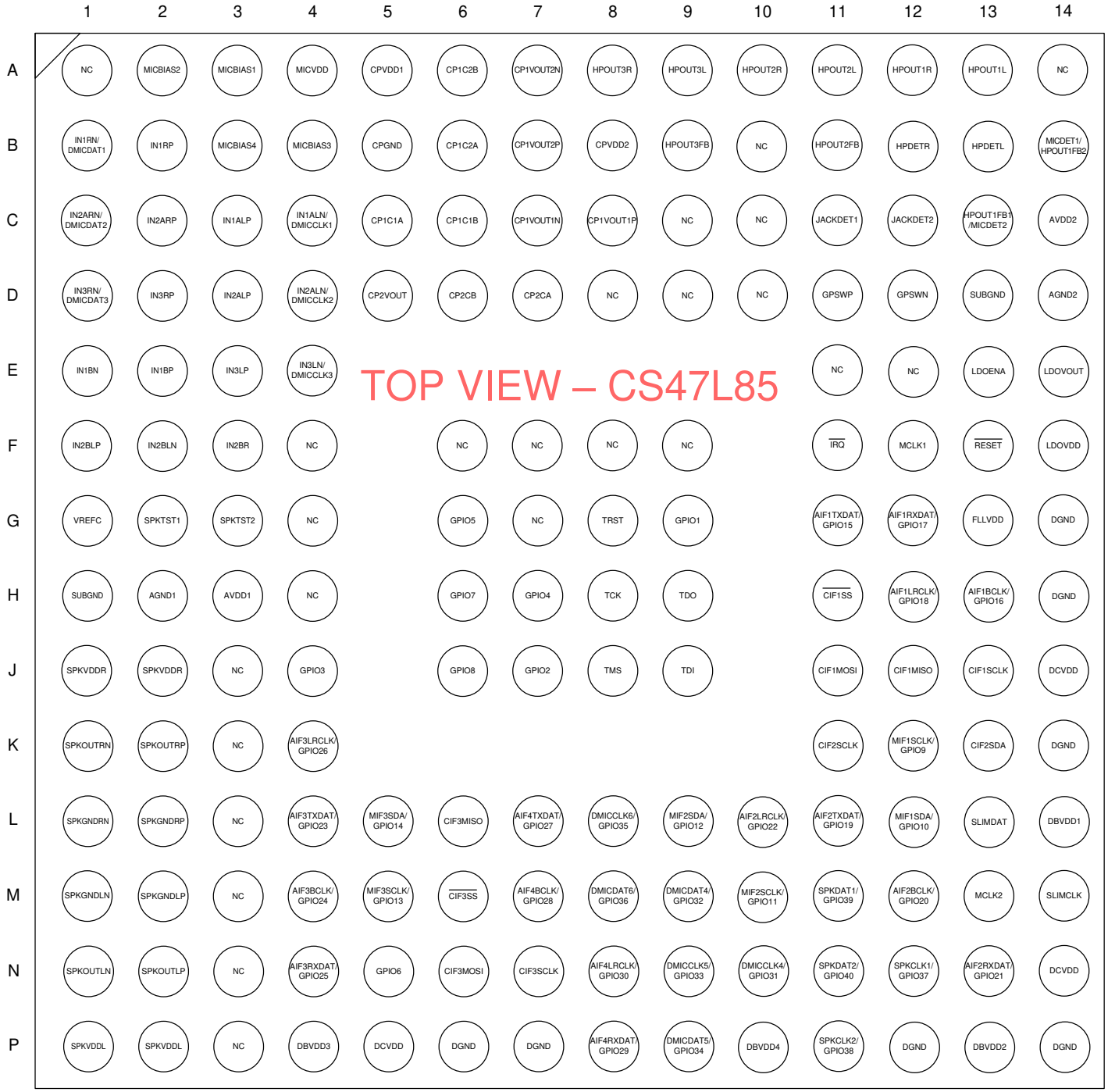
PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
CS47L85-CWZR	-40°C to +85°C	W-CSP (Pb-free, Tape and reel)	MSL1	260°C

Note:
Reel quantity = 4500

PIN DESCRIPTION

A description of each pin on the CS47L85 is provided below.
Note that a table detailing the associated power domain for every input and output pin is provided on the following page.
Note that, where multiple pins share a common name, these pins should be tied together on the PCB.
All Digital Output pins are CMOS outputs, unless otherwise stated.

PIN NO	NAME	TYPE	DESCRIPTION
H2	AGND1	Supply	Analogue ground (Return path for AVDD1)
D14	AGND2	Supply	Analogue ground (Return path for AVDD2)
H13	AIF1BCLK/ GPIO16	Digital Input / Output	Audio interface 1 bit clock / GPIO16. GPIO output is selectable CMOS or Open Drain; BCLK output is CMOS.
H12	AIF1LRCLK/ GPIO18	Digital Input / Output	Audio interface 1 left / right clock / GPIO18. GPIO output is selectable CMOS or Open Drain; LRCLK output is CMOS.
G12	AIF1RXDAT/ GPIO17	Digital Input / Output	Audio interface 1 RX digital audio data / GPIO17. GPIO output is selectable CMOS or Open Drain.
G11	AIF1TXDAT/ GPIO15	Digital Input / Output	Audio interface 1 TX digital audio data / GPIO15. GPIO output is selectable CMOS or Open Drain; TXDAT output is CMOS.
M12	AIF2BCLK/ GPIO20	Digital Input / Output	Audio interface 2 bit clock / GPIO20. GPIO output is selectable CMOS or Open Drain; BCLK output is CMOS.
L10	AIF2LRCLK/ GPIO22	Digital Input / Output	Audio interface 2 left / right clock / GPIO22. GPIO output is selectable CMOS or Open Drain; LRCLK output is CMOS.
N13	AIF2RXDAT/ GPIO21	Digital Input / Output	Audio interface 2 RX digital audio data / GPIO21. GPIO output is selectable CMOS or Open Drain.
L11	AIF2TXDAT/ GPIO19	Digital Input / Output	Audio interface 2 TX digital audio data / GPIO19. GPIO output is selectable CMOS or Open Drain; TXDAT output is CMOS.
M4	AIF3BCLK/ GPIO24	Digital Input / Output	Audio interface 3 bit clock / GPIO24. GPIO output is selectable CMOS or Open Drain; BCLK output is CMOS.
K4	AIF3LRCLK/ GPIO26	Digital Input / Output	Audio interface 3 left / right clock / GPIO26. GPIO output is selectable CMOS or Open Drain; LRCLK output is CMOS.
N4	AIF3RXDAT/GPIO25	Digital Input / Output	Audio interface 3 RX digital audio data / GPIO25. GPIO output is selectable CMOS or Open Drain.
L4	AIF3TXDAT/GPIO23	Digital Input / Output	Audio interface 3 TX digital audio data / GPIO23. GPIO output is selectable CMOS or Open Drain; TXDAT output is CMOS.
M7	AIF4BCLK/ GPIO28	Digital Input / Output	Audio interface 4 bit clock / GPIO28. GPIO output is selectable CMOS or Open Drain; BCLK output is CMOS.
N8	AIF4LRCLK/ GPIO30	Digital Input / Output	Audio interface 4 left / right clock / GPIO30. GPIO output is selectable CMOS or Open Drain; LRCLK output is CMOS.

PIN NO	NAME	TYPE	DESCRIPTION
P8	AIF4RXDAT/ GPIO29	Digital Input / Output	Audio interface 4 RX digital audio data / GPIO29. GPIO output is selectable CMOS or Open Drain.
L7	AIF4TXDAT/ GPIO27	Digital Input / Output	Audio interface 4 TX digital audio data / GPIO27. GPIO output is selectable CMOS or Open Drain; TXDAT output is CMOS.
H3	AVDD1	Supply	Analogue supply
C14	AVDD2	Supply	Analogue supply
J12	CIF1MISO	Digital Output	Control interface 1 (SPI) Master In Slave Out data. The CIFMISO is high impedance when C1F1SS is not asserted.
J11	CIF1MOSI	Digital Input	Control interface 1 (SPI) Master Out Slave In data
J13	CIF1SCLK	Digital Input	Control interface 1 (SPI) clock input
H11	C1F1SS	Digital Input	Control interface 1 (SPI) Slave Select (SS)
K11	CIF2SCLK	Digital Input	Control interface 2 (I2C) clock input
K13	CIF2SDA	Digital Input / Output	Control interface 2 (I2C) data input and output. The SDA output is Open Drain.
L6	CIF3MISO	Digital Output	Control interface 3 (SPI) Master In Slave Out data. The CIFMISO is high impedance when C1F3SS is not asserted.
N6	CIF3MOSI	Digital Input	Control interface 3 (SPI) Master Out Slave In data
N7	CIF3SCLK	Digital Input	Control interface 3 (SPI) clock input
M6	C1F3SS	Digital Input	Control interface 3 (SPI) Slave Select (SS)
C5	CP1C1A	Analogue Output	Charge pump 1 fly-back capacitor 1 pin
C6	CP1C1B	Analogue Output	Charge pump 1 fly-back capacitor 1 pin
B6	CP1C2A	Analogue Output	Charge pump 1 fly-back capacitor 2 pin
A6	CP1C2B	Analogue Output	Charge pump 1 fly-back capacitor 2 pin
C7	CP1VOUT1N	Analogue Output	Charge pump 1 negative output 1 decoupling pin
C8	CP1VOUT1P	Analogue Output	Charge pump 1 positive output 1 decoupling pin
A7	CP1VOUT2N	Analogue Output	Charge pump 1 negative output 2 decoupling pin
B7	CP1VOUT2P	Analogue Output	Charge pump 1 positive output 2 decoupling pin
D7	CP2CA	Analogue Output	Charge pump 2 fly-back capacitor pin
D6	CP2CB	Analogue Output	Charge pump 2 fly-back capacitor pin
D5	CP2VOUT	Analogue Output	Charge pump 2 output decoupling pin / Supply for LDO2
B5	CPGND	Supply	Charge pump ground (Return path for CPVDD1, CPVDD2)
A5	CPVDD1	Supply	Supply for Charge Pumps 1 & 2
B8	CPVDD2	Supply	Secondary supply for Charge Pump 1
L14	DBVDD1	Supply	Digital buffer (I/O) supply (core functions, AIF1, CIF1, CIF2, SLIMbus, MIF1, GPIO1)
P13	DBVDD2	Supply	Digital buffer (I/O) supply (AIF2, PDM, MIF2, MCLK2, GPIO2, JTAG)
P4	DBVDD3	Supply	Digital buffer (I/O) supply (AIF3, AIF4, CIF3, MIF3, GPIO3-8)
P10	DBVDD4	Supply	Digital buffer (I/O) supply (DMIC4, DMIC5, DMIC6)
J14, N14, P5	DCVDD	Supply	Digital core supply
G14, H14, K14, P6, P7, P12, P14	DGND	Supply	Digital ground (Return path for DCVDDn and DBVDDn)
N10	DMICCLK4/ GPIO31	Digital Input / Output	Digital MIC clock output 4 / GPIO31. GPIO output is selectable CMOS or Open Drain; DMICCLK output is CMOS.
M9	DMICDAT4/ GPIO32	Digital Input / Output	Digital MIC data input 4 / GPIO32. GPIO output is selectable CMOS or Open Drain.
N9	DMICCLK5/ GPIO33	Digital Input / Output	Digital MIC clock output 5 / GPIO33. GPIO output is selectable CMOS or Open Drain; DMICCLK output is CMOS.
P9	DMICDAT5/ GPIO34	Digital Input / Output	Digital MIC data input 5 / GPIO34. GPIO output is selectable CMOS or Open Drain.

PIN NO	NAME	TYPE	DESCRIPTION
L8	DMICCLK6/ GPIO35	Digital Input / Output	Digital MIC clock output 6 / GPIO35. GPIO output is selectable CMOS or Open Drain; DMICCLK output is CMOS.
M8	DMICDAT6/ GPIO36	Digital Input / Output	Digital MIC data input 6 / GPIO36. GPIO output is selectable CMOS or Open Drain.
G13	FLLVDD	Supply	Analogue supply (FLL1, FLL2)
G9	GPIO1	Digital Input / Output	General Purpose pin GPIO1. The output configuration is selectable CMOS or Open Drain.
J7	GPIO2	Digital Input / Output	General Purpose pin GPIO2. The output configuration is selectable CMOS or Open Drain.
J4	GPIO3	Digital Input / Output	General Purpose pin GPIO3. The output configuration is selectable CMOS or Open Drain.
H7	GPIO4	Digital Input / Output	General Purpose pin GPIO4. The output configuration is selectable CMOS or Open Drain.
G6	GPIO5	Digital Input / Output	General Purpose pin GPIO5. The output configuration is selectable CMOS or Open Drain.
N5	GPIO6	Digital Input / Output	General Purpose pin GPIO6. The output configuration is selectable CMOS or Open Drain.
H6	GPIO7	Digital Input / Output	General Purpose pin GPIO7. The output configuration is selectable CMOS or Open Drain.
J6	GPIO8	Digital Input / Output	General Purpose pin GPIO8. The output configuration is selectable CMOS or Open Drain.
D11	GPSWP	Analogue Input / Output	General Purpose bi-directional switch contact
D12	GPSWN	Analogue Input / Output	General Purpose bi-directional switch contact
B13	HPDETL	Analogue Input	Headphone left (HPOUT1L) sense input
B12	HPDETR	Analogue Input	Headphone right (HPOUT1R) sense input
C13	HPOUT1FB1/ MICDET2	Analogue Input	HPOUT1L and HPOUT1R ground feedback pin 1/ Microphone & accessory sense input 2
A13	HPOUT1L	Analogue Output	Left headphone 1 output
A12	HPOUT1R	Analogue Output	Right headphone 1 output
B11	HPOUT2FB	Analogue Input	HPOUT2L and HPOUT2R ground loop noise rejection feedback
A11	HPOUT2L	Analogue Output	Left headphone 2 output
A10	HPOUT2R	Analogue Output	Right headphone 2 output
B9	HPOUT3FB	Analogue Input	HPOUT3L and HPOUT3R ground loop noise rejection feedback
A9	HPOUT3L	Analogue Output	Left headphone 3 output
A8	HPOUT3R	Analogue Output	Right headphone 3 output
C4	IN1ALN/ DMICCLK1	Analogue Input / Digital Output	Left channel negative differential Mic/Line input / Digital MIC clock output 1
C3	IN1ALP	Analogue Input	Left channel single-ended Mic/Line input / Left channel positive differential Mic/Line input
E1	IN1BN	Analogue Input	Negative differential Mic/Line input. Also suitable for connection to external accessory interfaces.
E2	IN1BP	Analogue Input	Single-ended Mic/Line input / Positive differential Mic/Line input. Also suitable for connection to external accessory interfaces.
B1	IN1RN/ DMICDAT1	Analogue input / Digital Input	Right channel negative differential Mic/Line input / Digital MIC data input 1
B2	IN1RP	Analogue Input	Right channel single-ended Mic/Line input / Right channel positive differential Mic/Line input
D4	IN2ALN/ DMICCLK2	Analogue Input / Digital Output	Left channel negative differential Mic/Line input / Digital MIC clock output 2
D3	IN2ALP	Analogue Input	Left channel single-ended Mic/Line input / Left channel positive differential Mic/Line input
C1	IN2ARN/ DMICDAT2	Analogue input / Digital Input	Right channel negative differential Mic/Line input / Digital MIC data input 2

PIN NO	NAME	TYPE	DESCRIPTION
C2	IN2ARP	Analogue Input	Right channel single-ended Mic/Line input / Right channel positive differential Mic/Line input
F2	IN2BLN	Analogue Input	Left channel negative differential Mic/Line input. Also suitable for connection to external accessory interfaces.
F1	IN2BLP	Analogue Input	Left channel single-ended Mic/Line input / Left channel positive differential Mic/Line input. Also suitable for connection to external accessory interfaces.
F3	IN2BR	Analogue Input	Right channel single-ended Mic/Line input. Also suitable for connection to external accessory interfaces.
E4	IN3LN/ DMICCLK3	Analogue Input / Digital Output	Left channel negative differential Mic/Line input / Digital MIC clock output 3
E3	IN3LP	Analogue Input	Left channel single-ended Mic/Line input / Left channel positive differential Mic/Line input
D1	IN3RN/ DMICDAT3	Analogue input / Digital Input	Right channel negative differential Mic/Line input / Digital MIC data input 3
D2	IN3RP	Analogue Input	Right channel single-ended Mic/Line input / Right channel positive differential Mic/Line input
F11	IRQ	Digital Output	Interrupt Request (IRQ) output (default is active low). The pin configuration is selectable CMOS or Open Drain.
C11	JACKDET1	Analogue Input	Jack detect input 1
C12	JACKDET2	Analogue Input	Jack detect input 2
E13	LDOENA	Digital Input	Enable pin for LDO1 (generates DCVDD supply). Logic 1 input enables LDO1. If using external DCVDD supply, then LDO1 is not used, and LDOENA must be held at logic 0.
F14	LDOVDD	Supply	Supply for LDO1
E14	LDOVOUT	Analogue Output	LDO1 output. If using external DCVDD, then LDOVOUT must be left floating.
F12	MCLK1	Digital Input	Master clock 1
M13	MCLK2	Digital Input	Master clock 2
A3	MICBIAS1	Analogue Output	Microphone bias 1
A2	MICBIAS2	Analogue Output	Microphone bias 2
B4	MICBIAS3	Analogue Output	Microphone bias 3
B3	MICBIAS4	Analogue Output	Microphone bias 4
B14	MICDET1/ HPOUT1FB2	Analogue Input	Microphone & accessory sense input 1/ HPOUT1L and HPOUT1R ground feedback pin 2
A4	MICVDD	Analogue Output	LDO2 output decoupling pin (generated internally by CS47L85). (Can also be used as reference/supply for external microphones.)
K12	MIF1SCLK/ GPIO9	Digital Input / Output	Master (I2C) Interface 1 clock output / GPIO9. GPIO output is selectable CMOS or Open Drain; SCLK output is Open Drain.
L12	MIF1SDA/ GPIO10	Digital Input / Output	Master (I2C) Interface 1 data input and output / GPIO10. GPIO output is selectable CMOS or Open Drain; SDA output is Open Drain.
M10	MIF2SCLK/ GPIO11	Digital Input / Output	Master (I2C) Interface 2 clock output / GPIO11. GPIO output is selectable CMOS or Open Drain; SCLK output is Open Drain.
L9	MIF2SDA/ GPIO12	Digital Input / Output	Master (I2C) Interface 2 data input and output / GPIO12. GPIO output is selectable CMOS or Open Drain; SDA output is Open Drain.
M5	MIF3SCLK/ GPIO13	Digital Input / Output	Master (I2C) Interface 3 clock output / GPIO13. GPIO output is selectable CMOS or Open Drain; SCLK output is Open Drain.
L5	MIF3SDA/ GPIO14	Digital Input / Output	Master (I2C) Interface 3 data input and output / GPIO14. GPIO output is selectable CMOS or Open Drain; SDA output is Open Drain.
F13	$\overline{\text{RESET}}$	Digital Input	Digital Reset input (active low)
M14	SLIMCLK	Digital Input / Output	SLIM Bus Clock input / output

PIN NO	NAME	TYPE	DESCRIPTION
L13	SLIMDAT	Digital Input / Output	SLIM Bus Data input / output
N12	SPKCLK1/ GPIO37	Digital Input / Output	Digital speaker (PDM) 1 clock output / GPIO37. GPIO output is selectable CMOS or Open Drain; SPKCCLK output is CMOS.
M11	SPKDAT1/ GPIO39	Digital Input / Output	Digital speaker (PDM) 1 data output / GPIO39. GPIO output is selectable CMOS or Open Drain; SPKDAT output is CMOS.
P11	SPKCLK2/ GPIO38	Digital Input / Output	Digital speaker (PDM) 2 clock output / GPIO38. GPIO output is selectable CMOS or Open Drain; SPKCLK output is CMOS.
N11	SPKDAT2/ GPIO40	Digital Input / Output	Digital speaker (PDM) 2 data output / GPIO40. GPIO output is selectable CMOS or Open Drain; SPKDAT output is CMOS.
M1	SPKGNDLN	Supply	Left speaker driver ground (Return path for SPKVDDL). See note.
M2	SPKGNDLP	Supply	Left speaker driver ground (Return path for SPKVDDL). See note.
L1	SPKGNDRN	Supply	Right speaker driver ground (Return path for SPKVDDR). See note.
L2	SPKGNDRP	Supply	Right speaker driver ground (Return path for SPKVDDR). See note.
N1	SPKOUTLN	Analogue Output	Left speaker negative output
N2	SPKOUTLP	Analogue Output	Left speaker positive output
K1	SPKOUTRN	Analogue Output	Right speaker negative output
K2	SPKOUTRP	Analogue Output	Right speaker positive output
G2	SPKTST1	Analogue Output	Test function (recommend no external connection)
G3	SPKTST2	Analogue Output	Test function (recommend no external connection)
P1, P2	SPKVDDL	Supply	Left speaker driver supply
J1, J2	SPKVDDR	Supply	Right speaker driver supply
D13, H1	SUBGND	Supply	Substrate ground
H8	TCK	Digital Input	JTAG clock input. Internal pull-down holds this pin at logic 0 for normal operation.
J9	TDI	Digital Input	JTAG data input. Internal pull-down holds this pin at logic 0 for normal operation.
H9	TDO	Digital Output	JTAG data output
J8	TMS	Digital Input	JTAG mode select input. Internal pull-down holds this pin at logic 0 for normal operation.
G8	TRST	Digital Input	JTAG Test Access Port reset (active low). Internal pull-down holds this pin at logic 0 for normal operation. External connection to DGND is recommended, if the JTAG interface function is not required.
G1	VREFC	Analogue Output	Bandgap reference external capacitor connection

Note:

Separate P/N ground connections are provided for each speaker driver channel; this provides flexible support for current monitoring and output protection circuits. If this option is not used, then the respective ground connections should be tied together on the PCB.

The following table identifies the power domain and ground reference associated with each of the input / output pins.

PIN NO	NAME	POWER DOMAIN	GROUND DOMAIN
H13	AIF1BCLK/GPIO16	DBVDD1	DGND
H12	AIF1LRCLK/GPIO18	DBVDD1	DGND
G12	AIF1RXDAT/GPIO17	DBVDD1	DGND
G11	AIF1TXDAT/GPIO15	DBVDD1	DGND
M12	AIF2BCLK/GPIO20	DBVDD2	DGND
L10	AIF2LRCLK/GPIO22	DBVDD2	DGND
N13	AIF2RXDAT/GPIO21	DBVDD2	DGND
L11	AIF2TXDAT/GPIO19	DBVDD2	DGND
M4	AIF3BCLK/GPIO24	DBVDD3	DGND
K4	AIF3LRCLK/GPIO26	DBVDD3	DGND
N4	AIF3RXDAT/GPIO25	DBVDD3	DGND
L4	AIF3TXDAT/GPIO23	DBVDD3	DGND
M7	AIF4BCLK/GPIO28	DBVDD3	DGND
N8	AIF4LRCLK/GPIO30	DBVDD3	DGND
P8	AIF4RXDAT/GPIO29	DBVDD3	DGND
L7	AIF4TXDAT/GPIO27	DBVDD3	DGND
J12	CIF1MISO	DBVDD1	DGND
J11	CIF1MOSI	DBVDD1	DGND
J13	CIF1SCLK	DBVDD1	DGND
H11	CIF1SS	DBVDD1	DGND
K11	CIF2SCLK	DBVDD1	DGND
K13	CIF2SDA	DBVDD1	DGND
L6	CIF3MISO	DBVDD3	DGND
N6	CIF3MOSI	DBVDD3	DGND
N7	CIF3SCLK	DBVDD3	DGND
M6	CIF3SS	DBVDD3	DGND
N10	DMICCLK4/GPIO31	DBVDD4	DGND
N9	DMICCLK5/GPIO33	DBVDD4	DGND
L8	DMICCLK6/GPIO35	DBVDD4	DGND
M9	DMICDAT4/GPIO32	DBVDD4	DGND
P9	DMICDAT5/GPIO34	DBVDD4	DGND
M8	DMICDAT6/GPIO36	DBVDD4	DGND
G9	GPIO1	DBVDD1	DGND
J7	GPIO2	DBVDD2	DGND
J4	GPIO3	DBVDD3	DGND
H7	GPIO4	DBVDD3	DGND
G6	GPIO5	DBVDD3	DGND
N5	GPIO6	DBVDD3	DGND
H6	GPIO7	DBVDD3	DGND
J6	GPIO8	DBVDD3	DGND
B13	HPDETL	AVDD	AGND
B12	HPDETR	AVDD	AGND
C4	IN1ALN/ DMICCLK1	MICVDD (analogue) / MICVDD, MICBIAS1, MICBIAS2, MICBIAS3 (digital) The DMICCLK1 power domain is selectable using IN1_DMIC_SUP	AGND
C3	IN1ALP	MICVDD	AGND
E1	IN1BN	MICVDD	AGND
E2	IN1BP	MICVDD	AGND
B1	IN1RN/ DMICDAT1	MICVDD (analogue) / MICVDD, MICBIAS1, MICBIAS2, MICBIAS3 (digital) The DMICDAT1 power domain is selectable using IN1_DMIC_SUP	AGND
B2	IN1RP	MICVDD	AGND

PIN NO	NAME	POWER DOMAIN	GROUND DOMAIN
D4	IN2ALN/ DMICCLK2	MICVDD (analogue) / MICVDD, MICBIAS1, MICBIAS2, MICBIAS3 (digital) The DMICCLK2 power domain is selectable using IN2_DMIC_SUP	AGND
D3	IN2ALP	MICVDD	AGND
C1	IN2ARN/ DMICDAT2	MICVDD (analogue) / MICVDD, MICBIAS1, MICBIAS2, MICBIAS3 (digital) The DMICDAT2 power domain is selectable using IN2_DMIC_SUP	AGND
C2	IN2ARP	MICVDD	AGND
F2	IN2BLN	MICVDD	AGND
F1	IN2BLP	MICVDD	AGND
F3	IN2BR	MICVDD	AGND
E4	IN3LN/ DMICCLK3	MICVDD (analogue) / MICVDD, MICBIAS1, MICBIAS2, MICBIAS3 (digital) The DMICCLK3 power domain is selectable using IN3_DMIC_SUP	AGND
E3	IN3LP	MICVDD	AGND
D1	IN3RN/ DMICDAT3	MICVDD (analogue) / MICVDD, MICBIAS1, MICBIAS2, MICBIAS3 (digital) The DMICDAT3 power domain is selectable using IN3_DMIC_SUP	AGND
D2	IN3RP	MICVDD	AGND
F11	IRQ	DBVDD1	DGND
C11	JACKDET1	AVDD	AGND
C12	JACKDET2	AVDD	AGND
E13	LDOENA	DBVDD1	DGND
F12	MCLK1	DBVDD1	DGND
M13	MCLK2	DBVDD2	DGND
K12	MIF1SCLK/GPIO9	DBVDD1	DGND
L12	MIF1SDA/GPIO10	DBVDD1	DGND
M10	MIF2SCLK/GPIO11	DBVDD2	DGND
L9	MIF2SDA/GPIO12	DBVDD2	DGND
M5	MIF3SCLK/GPIO13	DBVDD3	DGND
L5	MIF3SDA/GPIO14	DBVDD3	DGND
F13	RESET	DBVDD1	DGND
M14	SLIMCLK	DBVDD1	DGND
L13	SLIMDAT	DBVDD1	DGND
N12	SPKCLK1/GPIO37	DBVDD2	DGND
P11	SPKCLK2/GPIO38	DBVDD2	DGND
M11	SPKDAT1/GPIO39	DBVDD2	DGND
N11	SPKDAT2/GPIO40	DBVDD2	DGND
H8	TCK	DBVDD2	DGND
J9	TDI	DBVDD2	DGND
H9	TDO	DBVDD2	DGND
J8	TMS	DBVDD2	DGND
G8	TRST	DBVDD2	DGND

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus Logic tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (DCVDD, FLLVDD)	-0.3V	1.6V
Supply voltages (CPVDD1, CPVDD2)	-0.3V	2.5V
Supply voltages (DBVDD1, DBVDD2, DBVDD3, DBVDD4, LDOVDD, AVDD, MICVDD)	-0.3V	5.0V
Supply voltages (SPKVDDL, SPKVDDR)	-0.3V	6.0V
Voltage range digital inputs (DBVDD1 domain)	SUBGND - 0.3V	DBVDD1 + 0.3V
Voltage range digital inputs (DBVDD2 domain)	SUBGND - 0.3V	DBVDD2 + 0.3V
Voltage range digital inputs (DBVDD3 domain)	SUBGND - 0.3V	DBVDD3 + 0.3V
Voltage range digital inputs (DMICDAT1, DMICDAT2, DMICDAT3)	SUBGND - 0.3V	MICVDD + 0.3V
Voltage range digital inputs (DMICDAT4, DMICDAT5, DMICDAT6)	SUBGND - 0.3V	DBVDD4 + 0.3V
Voltage range analogue inputs (IN1Axx, IN2Axx, IN3xx)	SUBGND - 0.3V	MICVDD + 0.3V
Voltage range analogue inputs (IN1Bx, IN2Bxx)	SUBGND - 0.9V	MICVDD + 0.3V
Voltage range analogue inputs (HPOUT1FB1, HPOUT1FB2, HPOUTnFB)	SUBGND - 0.3V	SUBGND + 0.3V
Voltage range analogue inputs (MICDETn)	SUBGND - 0.3V	MICVDD + 0.3V
Voltage range analogue inputs (JACKDET1, JACKDET2, HPDETL, HPDETR)	CP1VOUT2N - 0.3V	AVDD + 0.3V
Voltage range analogue inputs (GPSWP, GPSWN)	SUBGND - 0.3V	MICVDD + 0.3V
Ground (AGND, DGND, CPGND, SPKGNDL, SPKGNDR)	SUBGND - 0.3V	SUBGND + 0.3V
Operating temperature range, T_A	-40ºC	+85ºC
Operating junction temperature, T_J	-40ºC	+125ºC
Storage temperature after soldering	-65ºC	+150ºC

Notes:

1. The DCVDD and FLLVDD pins should be tied together. The associated power domain is referred to as DCVDD.
2. The AVDD1 and AVDD2 pins should be tied together. The associated power domain is referred to as AVDD.
3. The AGND1 and AGND2 pins should be tied together. The associated ground domain is referred to as AGND.
4. The HPOUT1FBn and MICDETn functions share common pins. The Absolute Maximum Rating varies according to the applicable function of each pin.
5. CP1VOUT2N is an internal supply, generated by the CS47L85 Charge Pump (CP1). The CP1VOUT2N voltage may vary between CPGND and -CPVDD.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital Core and FLL supply range See notes 3, 4, 5, 6, 7	DCVDD, FLLVDD	1.14	1.2	1.26	V
Digital supply range (I/O) See note 8	DBVDD1, DBVDD2, DBVDD3, DBVDD4	1.71		3.6	V
LDO supply range See note 3	LDOVDD	1.71	1.8	1.89	V
Charge Pump supply range	CPVDD1	1.71	1.8	1.89	V
	CPVDD2	1.14	1.2	1.26	V
Speaker supply range	SPKVDDL, SPKVDDR	2.4		5.5	V
Analogue supply range See notes 9, 10	AVDD	1.71	1.8	1.89	V
Analogue supply range (FLL) See note 4	FLLVDD	1.14	1.2	1.26	V
Microphone Bias supply See note 11	MICVDD	0.9	2.5	3.78	V
Ground See note 1	DGND, AGND, CPGND, SPKGNDL, SPKGNDR, SUBGND		0		V
Power supply rise time See notes 12 to 17	DCVDD	10		2000	µs
	LDOVDD	10		50000	
	All other supplies	10			
Operating temperature range	T_A	-40		85	°C

Notes:

1. The impedance between DGND, AGND, CPGND and SUBGND should be less than 0.1Ω. The impedance between SPKGNDL, SPKGNDR and SUBGND should be less than 0.2Ω.
2. There are no switch-on power sequencing requirements; the supplies may be enabled in any order.
3. When powering down the device, if DCVDD is powered using the internal LDO (LDO1), then the LDO must be disabled, or else $\overline{\text{RESET}}$ must be asserted (low), before the LDOVDD supply is removed. There are no other switch-off power sequencing requirements.
4. The DCVDD and FLLVDD pins should be tied together. The associated power domain is referred to as DCVDD.
5. An internal LDO (powered by LDOVDD) can be used to provide the DCVDD and FLLVDD supplies.
6. 'Sleep' mode is supported when DCVDD is below the limits noted, provided AVDD and DBVDD1 are present.
7. It is recommended to connect a 4.7Ω resistor in series with the FLLVDD pin connection. Note that the minimum voltage limit applies at the supply end of the 4.7Ω resistor in this case.
8. If the SLIMbus interface is enabled, then the maximum DBVDD1 voltage is 1.98V.
9. The AVDD1 and AVDD2 pins should be tied together. The associated power domain is referred to as AVDD.
10. The AGND1 and AGND2 pins should be tied together. The associated ground domain is referred to as AGND.
11. An internal Charge Pump and LDO (powered by CPVDD1) provide the Microphone Bias supply; the MICVDD pin should not be connected to an external supply.
12. DCVDD and MICVDD minimum rise times do not apply when these domains are powered using the internal LDOs.
13. If DCVDD is supplied externally, and the rise time exceeds 2ms, then $\overline{\text{RESET}}$ must be asserted (low) during the rise, and held asserted until after DCVDD is within the recommended operating limits.
14. LDOVDD maximum rise time does not apply when DCVDD is supplied externally.
15. If DCVDD is powered using the internal LDO (LDO1), and the LDOVDD rise time exceeds 50ms, then $\overline{\text{RESET}}$ must be asserted (low), or LDOENA held low, during the rise. One or both these signals must be held low until after LDOVDD is within the recommended operating limits.
16. The specified minimum power supply rise times assume a minimum decoupling capacitance of 100nF per pin. However, Cirrus Logic strongly advises that the recommended decoupling capacitors are present on the PCB and that appropriate layout guidelines are observed.
17. The specified minimum power supply rise times also assume a maximum PCB inductance of 10nH between decoupling capacitor and pin.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = 1.8V,

With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Signal Level (IN1AL, IN1BL, IN1R, IN2AL, IN2BL, IN2AR, IN2BR, IN3L, IN3R)						
Full-scale input signal level (0dBFS output)	V_{INFS}	Single-ended PGA input, 0dB PGA gain		0.5 -6		V_{RMS} dBV
		Differential PGA input, 0dB PGA gain		1 0		V_{RMS} dBV

Notes:

1. The full-scale input signal level is also the maximum analogue input level, before clipping occurs.
2. The full-scale input signal level changes in proportion with AVDD. For differential input, it is calculated as AVDD / 1.8.
3. A $1.0V_{RMS}$ differential signal equates to $0.5V_{RMS}$/-6dBV per input.
4. A sinusoidal input signal is assumed.

Test Conditions

T_A = +25°C

With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Pin Characteristics (IN1AL, IN1BL, IN1R, IN2AL, IN2BL, IN2AR, IN2BR, IN3L, IN3R)						
Input resistance	R_{IN}	Single-ended PGA input, All PGA gain settings	9	12		kΩ
		Differential PGA input, All PGA gain settings	18	24		
Input capacitance	C_{IN}				5	pF

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Programmable Gain Amplifiers (PGAs)						
Minimum programmable gain				0		dB
Maximum programmable gain				31		dB
Programmable gain step size		Guaranteed monotonic		1		dB

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Microphone Input Signal Level (DMICDAT1, DMICDAT2, DMICDAT3, DMICDAT4, DMICDAT5, DMICDAT6)						
Full-scale input signal level (0dBFS signal to digital core)		0dB gain		-6		dBFS

Notes:

1. The digital microphone input signal level is measured in dBFS, where 0dBFS is a signal level equal to the full-scale range (FSR) of the PDM input. The FSR is defined as the amplitude of a 1kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively - this is the largest 1kHz sine wave that will fit in the digital output range without clipping.

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line / Headphone / Earpiece Output Driver (HPOUTnL, HPOUTnR)						
Load resistance		Normal operation, Single-ended mode	6			Ω
		Normal operation, Differential (BTL) mode	15			
		Device survival with load applied indefinitely	0			
Load capacitance		Single-ended mode			500	pF
		Differential (BTL) mode			200	
Speaker Output Driver (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN)						
Load resistance		Normal operation	4			Ω
		Device survival with load applied indefinitely	0			
Load capacitance					200	pF
Digital Speaker Output (SPKDAT1, SPKDAT2)						
Full-scale output level (0dBFS digital core output)		0dB gain		-6		dBFS

Notes:

1. The digital output signal level is measured in dBFS, where 0dBFS is a signal level equal to the full-scale range (FSR) of the PDM output. The FSR is defined as the amplitude of a 1kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively - this is the largest 1kHz sine wave that will fit in the digital output range without clipping.

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = DBVDD4 = CPVDD1 = AVDD = LDOVDD = 1.8V, CPVDD2 = 1.2V,
DCVDD = FLLVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
TA = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line / Headphone / Earpiece Output Driver (HPOUTnL, HPOUTnR)						
DC offset at Load		Single-ended mode		100	100	µV
		Differential (BTL) mode		200		
Speaker Output Driver (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN)						
DC offset at Load				3		mV
SPKVDD leakage current				1		µA

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = DBVDD4 = CPVDD1 = AVDD = LDOVDD = 1.8V, CPVDD2 = 1.2V,
DCVDD = FLLVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
TA = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Paths (INnL, INnR) to ADC (Differential Input Mode)						
Signal to Noise Ratio (A-weighted)	SNR	48kHz sample rate	93	100		dB
		16kHz sample rate, (wideband voice)		106		
Total Harmonic Distortion	THD	-1dBV input		-89	-81	dB
Total Harmonic Distortion + Noise	THD+N	-1dBV input		-88		dB
Channel separation (Left/Right)		100Hz to 10kHz		100		dB
Input-referred noise floor		A-weighted, PGA gain = +20dB		3.2		μV_{RMS}
Common mode rejection ratio	CMRR	PGA gain = +30dB		80		dB
		PGA gain = 0dB		70		
PSRR (DBVDDn, LDOVDD, CPVDD1, AVDD)	PSRR	100mV (peak-peak) 217Hz		90		dB
		100mV (peak-peak) 10kHz		80		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		100		dB
		100mV (peak-peak) 10kHz		80		
Analogue Input Paths (INnLP, INnRP) to ADC (Single-Ended Input Mode)						
Signal to Noise Ratio (A-weighted)	SNR	48kHz sample rate	91	100		dB
		16kHz sample rate, (wideband voice)		102		
Total Harmonic Distortion	THD	-7dBV input		-85	-78	dB
Total Harmonic Distortion + Noise	THD+N	-7dBV input		-84		dB
Channel separation (Left/Right)		100Hz to 10kHz		100		dB
Input-referred noise floor		A-weighted, PGA gain = +20dB		4		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD1, AVDD)	PSRR	100mV (peak-peak) 217Hz		77		dB
		100mV (peak-peak) 10kHz		50		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		90		dB
		100mV (peak-peak) 10kHz		50		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = DBVDD4 = CPVDD1 = AVDD = LDOVDD = 1.8V, CPVDD2 = 1.2V,
DCVDD = FLLVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
TA = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Line Output (HPOUTnL, HPOUTnR; Load = 10kΩ, 50pF)						
Full-scale output signal level	V_{OUT}	0dBFS input		1 0		Vrms dBV
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1Vrms		121		dB
Dynamic Range	DR	A-weighted, -60dBFS input	105	115		dB
Total Harmonic Distortion	THD	0dBFS input		-92	-84	dB
Total Harmonic Distortion + Noise	THD+N	0dBFS input		-91		dB
Channel separation (Left/Right)		100Hz to 10kHz		100		dB
Output noise floor		A-weighted		0.8		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD1, AVDD)	PSRR	100mV (peak-peak) 217Hz		90		dB
		100mV (peak-peak) 10kHz		72		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		110		
DAC to Headphone Output (HPOUTnL, HPOUTnR; R_L = 32Ω)						
Maximum output power	P_O	0.1% THD+N		32		mW
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1Vrms		121		dB
Dynamic Range	DR	A-weighted, -60dBFS input	105	115		dB
Total Harmonic Distortion	THD	P_O = 20mW		-90		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 20mW		-89		dB
Total Harmonic Distortion	THD	P_O = 2mW		-91	-84	dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 2mW		-90		dB
Channel separation (Left/Right)		100Hz to 10kHz		94		dB
Output noise floor		A-weighted		0.8		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD1, AVDD)	PSRR	100mV (peak-peak) 217Hz		90		dB
		100mV (peak-peak) 10kHz		73		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		110		
DAC to Headphone Output (HPOUTnL, HPOUTnR; R_L = 16Ω)						
Maximum output power	P_O	0.1% THD+N		42		mW
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1Vrms		121		dB
Dynamic Range	DR	A-weighted, -60dBFS input	105	115		dB
Total Harmonic Distortion	THD	P_O = 20mW		-90		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 20mW		-89		dB
Total Harmonic Distortion	THD	P_O = 2mW		-91	-84	dB
Total Harmonic Distortion + Noise	THD+N	P_O = 2mW		-90		dB
Channel separation (Left/Right)		100Hz to 10kHz		92		dB
Output noise floor		A-weighted		0.8		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD1, AVDD)	PSRR	100mV (peak-peak) 217Hz		90		dB
		100mV (peak-peak) 10kHz		73		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		110		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = DBVDD4 = CPVDD1 = AVDD = LDOVDD = 1.8V, CPVDD2 = 1.2V,
DCVDD = FLLVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
TA = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Earpiece Output (HPOUTnL, HPOUTnR, Mono Mode, R_L = 32Ω BTL)						
Maximum output power	P_O	0.1% THD+N		106		mW
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1.41Vrms		127		dB
Dynamic Range	DR	A-weighted, -60dBFS input		119		dB
Total Harmonic Distortion	THD	P_O = 75mW		-92		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 75mW		-91		dB
Total Harmonic Distortion	THD	P_O = 5mW		-92		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 5mW		-91		dB
Output noise floor		A-weighted		0.7		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD1, AVDD)	PSRR	100mV (peak-peak) 217Hz		85		dB
		100mV (peak-peak) 10kHz		73		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		110		
DAC to Earpiece Output (HPOUTnL, HPOUTnR, Mono Mode, R_L = 16Ω BTL)						
Maximum output power	P_O	0.1% THD+N		106		mW
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1.41Vrms		127		dB
Dynamic Range	DR	A-weighted, -60dBFS input		119		dB
Total Harmonic Distortion	THD	P_O = 75mW		-89		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 75mW		-88		dB
Total Harmonic Distortion	THD	P_O = 5mW		-90		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 5mW		-89		dB
Output noise floor		A-weighted		0.7		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD1, AVDD)	PSRR	100mV (peak-peak) 217Hz		85		dB
		100mV (peak-peak) 10kHz		73		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		110		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = DBVDD4 = CPVDD1 = AVDD = LDOVDD = 1.8V, CPVDD2 = 1.2V,
DCVDD = FLLVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
TA = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Speaker Output (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN, Load = 8Ω, 22µH, BTL)						
Maximum output power	P_O	SPKVDD = 5.0V, 1% THD+N		1.4		W
		SPKVDD = 4.2V, 1% THD+N		1.0		
		SPKVDD = 3.6V, 1% THD+N		0.7		
Signal to Noise Ratio	SNR	A-weighted, Output signal = 2.83Vrms		127		dB
Dynamic Range	DR	A-weighted, -60dBFS input	90	101		dB
Total Harmonic Distortion	THD	P_O = 1.0W		-40		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 1.0W		-40		dB
Total Harmonic Distortion	THD	P_O = 0.5W		-70	-59	dB
Total Harmonic Distortion + Noise	THD+N	P_O = 0.5W		-69		dB
Channel separation (Left/Right)		100Hz to 10kHz		80		dB
Output noise floor		A-weighted		0.7		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD1, AVDD)	PSRR	100mV (peak-peak) 217Hz		100		dB
		100mV (peak-peak) 10kHz		80		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		100		dB
		100mV (peak-peak) 10kHz		95		
DAC to Speaker Output (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN, Load = 4Ω, 15µH, BTL)						
Maximum output power	P_O	SPKVDD = 5.0V, 1% THD+N		2.5		W
		SPKVDD = 4.2V, 1% THD+N		1.8		
		SPKVDD = 3.6V, 1% THD+N		1.3		
Signal to Noise Ratio	SNR	A-weighted, Output signal = 2.83Vrms		127		dB
Dynamic Range	DR	A-weighted, -60dBFS input		95		dB
Total Harmonic Distortion	THD	P_O = 1.0W		-40		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 1.0W		-40		dB
Total Harmonic Distortion	THD	P_O = 0.5W		-70		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 0.5W		-69		dB
Channel separation (Left/Right)		100Hz to 10kHz		80		dB
Output noise floor		A-weighted		0.7		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD1, AVDD)	PSRR	100mV (peak-peak) 217Hz		100		dB
		100mV (peak-peak) 10kHz		80		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		100		dB
		100mV (peak-peak) 10kHz		95		

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input / Output (except DMICDAT1/2/3 and DMICCLK1/2/3) **Digital I/O is referenced to DBVDD1, DBVDD2, DBVDD3 or DBVDD4.**						
Input HIGH Level	V_{IH}	V_{DBVDD} = 1.71V to 1.98V	0.75 × V_{DBVDDn}			V
		V_{DBVDDn} = 2.5V ±10%	0.8 × V_{DBVDDn}			
		V_{DBVDDn} = 3.3V ±10%	0.7 × V_{DBVDDn}			
Input LOW Level	V_{IL}	V_{DBVDD} = 1.71V to 1.98V			0.3 × V_{DBVDDn}	V
		V_{DBVDDn} = 2.5V ±10%			0.25 × V_{DBVDDn}	
		V_{DBVDDn} = 3.3V ±10%			0.2 × V_{DBVDDn}	
Note that digital input pins should not be left unconnected or floating.						
Output HIGH Level (I_{OH} = 1mA)	V_{OH}	V_{DBVDD} = 1.71V to 1.98V	0.75 × V_{DBVDDn}			V
		V_{DBVDDn} = 2.5V ±10%	0.65 × V_{DBVDDn}			
		V_{DBVDDn} = 3.3V ±10%	0.7 × V_{DBVDDn}			
Output LOW Level (I_{OL} = 1mA)	V_{OL}	V_{DBVDD} = 1.71V to 1.98V			0.25 × V_{DBVDDn}	V
		V_{DBVDDn} = 2.5V ±10%			0.3 × V_{DBVDDn}	
		V_{DBVDDn} = 3.3V ±10%			0.15 × V_{DBVDDn}	
Input capacitance					5	pF
Input leakage			-10		10	µA
Pull-up / pull-down resistance (where applicable)			35		55	kΩ
Digital Microphone Input / Output (DMICDAT1/2/3 and DMICCLK1/2/3) **DMICDAT1/2/3 and DMICCLK1/2/3 are referenced to a selectable supply, V_{SUP}, according to the INn_DMIC_SUP registers**						
DMICDATn input HIGH Level	V_{IH}		0.65 × V_{SUP}			V
DMICDATn input LOW Level	V_{IL}				0.35 × V_{SUP}	V
DMICCLKn output HIGH Level	V_{OH}	I_{OH} = 1mA	0.8 × V_{SUP}			V
DMICCLKn output LOW Level	V_{OL}	I_{OL} = -1mA			0.2 × V_{SUP}	V
Input capacitance				25		pF
Input leakage			-1		1	µA
General Purpose Input / Output (GPIOn)						
Clock output frequency		GPIO pin configured as OPCLK or FLL output			50	MHz
General Purpose Switch The GPSWP pin should be positive-biased with respect to GPSWN. The GPSWN pin voltage must not exceed GPSWP + 0.3V.						
Switch resistance	$R_{DS(ON)}$	Switch closed, I=1mA		25	40	Ω
Switch resistance	$R_{DS(OFF)}$	Switch open		100		MΩ

Test Conditions

fs ≤ 48kHz

With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Decimation Filters						
Passband		+/- 0.05dB	0		0.454 fs	
		-6dB		0.5 fs		
Passband ripple					+/- 0.05	dB
Stopband			0.546 fs			
Stopband attenuation		f > 0.546 fs	85			dB
Group delay					2	ms
DAC Interpolation Filters						
Passband		+/- 0.05dB	0		0.454 fs	
		-6dB		0.5 fs		
Passband ripple					+/- 0.05	dB
Stopband			0.546 fs			
Stopband attenuation		f > 0.546 fs	85			dB
Group delay					1.5	ms

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = DBVDD4 = CPVDD1 = AVDD = LDOVDD = 1.8V, CPVDD2 = 1.2V
DCVDD = FLLVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Bias (MICBIAS1, MICBIAS2, MICBIAS3, MICBIAS4) Note - No capacitor on MICBIASn Note - In regulator mode, it is required that V_{MICVDD} - $V_{MICBIAS}$ > 200mV						
Minimum Bias Voltage	$V_{MICBIAS}$	Regulator mode (MICBn_BYPASS=0) Load current ≤ 1.0mA		1.5		V
Maximum Bias Voltage				2.8		V
Bias Voltage output step size				0.1		V
Bias Voltage accuracy			-5%		+5%	V
Bias Current		Regulator mode (MICBn_BYPASS=0), V_{MICVDD} - $V_{MICBIAS}$ >200mV			2.4	mA
		Bypass mode (MICBn_BYPASS=1)			5.0	
Output Noise Density		Regulator mode (MICBn_BYPASS=0), MICBn_LVL = 4h, Load current = 1mA, Measured at 1kHz		50		nV/√Hz
Integrated noise voltage		Regulator mode (MICBn_BYPASS=0), MICBn_LVL = 4h, Load current = 1mA, 100Hz to 7kHz, A-weighted		4		µVrms
Power Supply Rejection Ratio (DBVDDn, LDOVDD, CPVDD1, AVDD)	PSRR	100mV (peak-peak) 217Hz		90		dB
		100mV (peak-peak) 10kHz		80		
Load capacitance		Regulator mode (MICBn_BYPASS=0), MICBn_EXT_CAP=0			50	pF
		Regulator mode (MICBn_BYPASS=0), MICBn_EXT_CAP=1	1.8	4.7		µF
Output discharge resistance		MICBn_ENA=0, MICBn_DISCH=1		2		kΩ

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = DBVDD4 = CPVDD1 = AVDD = LDOVDD = 1.8V, CPVDD2 = 1.2V
DCVDD = FLLVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
External Accessory Detect						
Load impedance detection range Detection via HPDETL pin (ACCDET_MODE=001) or HPDETR pin (ACCDET_MODE=010)		HP_IMPEDANCE_ RANGE=00	4		30	Ω
		HP_IMPEDANCE_ RANGE=01	8		100	
		HP_IMPEDANCE_ RANGE=10	100		1000	
		HP_IMPEDANCE_ RANGE=11	1000		10000	
Load impedance detection range Detection via MICDET1 or MICDET2 pin (ACCDET_MODE=100)			400		6000	Ω
Load impedance detection accuracy (result derived from HP_DACVAL, ACCDET_MODE=001 or 010)		HP_IMPEDANCE_ RANGE=01 or 10	-5		+5	%
		HP_IMPEDANCE_ RANGE=00 or 11	-10		+10	
Load impedance detection accuracy (result derived from HP_LVL, ACCDET_MODE= 001, 010 or 100)			-20		+20	%
Load impedance detection range Detection via MICDET1 or MICDET2 pin (ACCDET_MODE=000). 2.2kΩ (2%) MICBIAS resistor. Note these characteristics assume no other component is connected to MICDETn.		for MICD_LVL[0] = 1	0		3	Ω
		for MICD_LVL[1] = 1	17		21	
		for MICD_LVL[2] = 1	36		44	
		for MICD_LVL[3] = 1	62		88	
		for MICD_LVL[4] = 1	115		160	
		for MICD_LVL[5] = 1	207		381	
		for MICD_LVL[8] = 1	475		30000	
Jack Detection input threshold voltage (JACKDETn)	$V_{JACKDET}$	Jack insertion		0.9		V
		Jack removal		1.5		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = DBVDD4 = CPVDD1 = AVDD = LDOVDD = 1.8V, CPVDD2 = 1.2V
DCVDD = FLLVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MICVDD Charge Pump and Regulator (CP2 and LDO2)						
Output voltage	V_{MICVDD}		0.9	2.7	3.3	V
Programmable output voltage step size		LDO2_VSEL=00h to 14h (0.9V to 1.4V)		25		mV
		LDO2_VSEL=14h to 27h (1.4V to 3.3V)		100		
Maximum output current				8		mA
Start-up time		4.7µF on MICVDD		1.5	2.5	ms
Frequency Locked Loop (FLL1, FLL2, FLL3)						
Output frequency		FLL output as SYSCLK or ASYNCCLK source	90		98.3	MHz
		FLL output as DSPCLK source	135		150	
Lock Time		F_{REF} = 32kHz, F_{OUT} = 147.456MHz		10		ms
		F_{REF} = 12MHz, F_{OUT} = 147.456MHz		1		
RESET pin Input						
RESET input pulse width (To trigger a Hardware Reset, the RESET input must be asserted for longer than this duration)			1			µs

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

Device Reset Thresholds						
AVDD Reset Threshold	V_{AVDD}	V_{AVDD} rising			1.66	V
		V_{AVDD} falling	1.06		1.44	
DCVDD Reset Threshold	V_{DCVDD}	V_{DCVDD} rising			1.04	V
		V_{DCVDD} falling	0.49		0.66	
DBVDD1 Reset Threshold	V_{DBVDD1}	V_{DBVDD1} rising			1.66	V
		V_{DBVDD1} falling	1.06		1.44	
Note that the reset thresholds are derived from simulations only, across all operational and process corners. Device performance is not assured outside the voltage ranges defined in the “Recommended Operating Conditions” section. Refer to this section for the CS47L85 power-up sequencing requirements.						

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum full scale output signal and the output with no input signal applied.
2. Total Harmonic Distortion (dB) – THD is the ratio of the RMS sum of the harmonic distortion products in the specified bandwidth (see note below) relative to the RMS amplitude of the fundamental (i.e., test frequency) output.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the ratio of the RMS sum of the harmonic distortion products plus noise in the specified bandwidth (see note below) relative to the RMS amplitude of the fundamental (i.e., test frequency) output.
4. Power Supply Rejection Ratio (dB) - PSRR is the ratio of a specified power supply variation relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.
5. Common Mode Rejection Ratio (dB) – CMRR is the ratio of a specified input signal (applied to both sides of a differential input), relative to the output signal that results from it.
6. Channel Separation (L/R) (dB) – left-to-right and right-to-left channel separation is the difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
7. Multi-Path Crosstalk (dB) – is the difference in level between the output of the active path and the measured signal level in the idle path at the test signal frequency. The active path is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the specified idle path.
8. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.
9. All performance measurements are specified with a 20kHz low pass 'brick-wall' filter and, where noted, an A-weighted filter. Failure to use these filters will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out-of-band noise.

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Junction-to-ambient thermal resistance	Θ_{JA}		30.6		°C/W
Junction-to-board thermal resistance	Θ_{JB}		13.8		°C/W
Junction-to-case thermal resistance	Θ_{JC}		0.44		°C/W
Junction-to-board thermal characterisation parameter	Ψ_{JB}		16.8		°C/W
Junction-to-top thermal characterisation parameter	Ψ_{JT}		0.02		°C/W

Notes:

1. The Thermal Characteristics data is based on simulated test results, with reference to JEDEC JESD51 standards.
2. The thermal resistance (Θ) parameters describe the thermal behaviour in a standardised measurement environment.
3. The thermal characterisation (Ψ) parameters describe the thermal behaviour in the environment of a typical application.

TYPICAL PERFORMANCE

TYPICAL POWER CONSUMPTION

Typical power consumption data is provided below for a number of different operating conditions.

Test Conditions:
DBVDD1 = DBVDD2 = DBVDD3 = DBVDD4 = CPVDD1 = AVDD = LDOVDD = 1.8V,
CPVDD2 = DCVDD = FLLVDD = 1.2V, SPKVDDL = SPKVDDR = 4.2V, MICVDD = 2.5V (powered from LDO2),
T_A = +25ºC, PGA gain = 0dB, fs = 48kHz, 24-bit audio data, I^2S Slave Mode,
SYSCLK = 24.576 MHz (direct MCLK1) unless otherwise

OPERATING MODE	TEST CONDITIONS	SUPPLY CURRENT (1.2V)	SUPPLY CURRENT (1.8V)	SUPPLY CURRENT (4.2V)	TOTAL POWER
Music Playback to Headphone					
AIF1 to DAC to HPOUT (stereo) Load = 32Ω	Quiescent	2.2mA	0.7mA	0.0mA	3.9mW
	1kHz sine wave, P_O=10mW	37.7mA	1.9mA	0.0mA	48.66mW
Music Playback to Earpiece					
AIF1 to DAC to HPOUT (mono) Load = 32Ω, BTL	Quiescent	1.5mA	0.8mA	0.0mA	3.24mW
	1kHz sine wave, P_O=30mW	61.8mA	1.8mA	0.0mA	77.4mW
Music Playback to Speaker					
AIF1 to DAC to SPKOUT (stereo) Load = 8Ω, 22µH, BTL	Quiescent	2.0mA	2.1mA	0.0mA	6.18mW
	1kHz sine wave, P_O=700mW	2.0mA	2.1mA	382mA	1610mW
Stereo Line Record					
Analogue Line to ADC to AIF1 MICVDD=1.8V (CP2/LDO2 bypass)	1kHz sine wave, -1dBFS out	2.1mA	2.4mA	0.0mA	6.84mW
Sleep Mode					
Accessory detect enabled (JD1_ENA=1)		0.00mA	0.01mA	0.000mA	0.018mW

TYPICAL SIGNAL LATENCY

OPERATING MODE	TEST CONDITIONS			LATENCY
	INPUT	OUTPUT	DIGITAL CORE	
AIF to DAC Stereo Path				
Digital input (AIFn) to analogue output (HPOUT).	fs = 192kHz	fs = 192kHz	Synchronous	235µs
	fs = 96kHz	fs = 96kHz	Synchronous	261µs
	fs = 48kHz	fs = 48kHz	Synchronous	335µs
	fs = 44.1kHz	fs = 44.1kHz	Synchronous	361µs
	fs = 16kHz	fs = 16kHz	Synchronous	552µs
	fs = 8kHz	fs = 8kHz	Synchronous	1080µs
	fs = 8kHz	fs = 48kHz	Isochronous	1720µs
	fs = 16kHz	fs = 48kHz	Isochronous	995µs
	fs = 8kHz	fs = 44.1kHz	Asynchronous	1790µs
	fs = 16kHz	fs = 44.1kHz	Asynchronous	1067µs
ADC to AIF Stereo Path				
Analogue input (INn) to digital output (AIFn). Input path High Pass Filter (HPF) enabled.	fs = 192kHz	fs = 192kHz	Synchronous	59µs
	fs = 96kHz	fs = 96kHz	Synchronous	98µs
	fs = 48kHz	fs = 48kHz	Synchronous	220µs
	fs = 44.1kHz	fs = 44.1kHz	Synchronous	235µs
	fs = 16kHz	fs = 16kHz	Synchronous	656µs
	fs = 8kHz	fs = 8kHz	Synchronous	1325µs
	fs = 8kHz	fs = 48kHz	Isochronous	1805µs
	fs = 16kHz	fs = 48kHz	Isochronous	997µs
	fs = 44.1kHz	fs = 8kHz	Asynchronous	1369µs
	fs = 44.1kHz	fs = 16kHz	Asynchronous	883µs

Notes

Signal is routed via the digital core ISRC function in the isochronous test cases only.

Signal is routed via the digital core ASRC function in the asynchronous test cases only.

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK & FREQUENCY LOCKED LOOP (FLL)

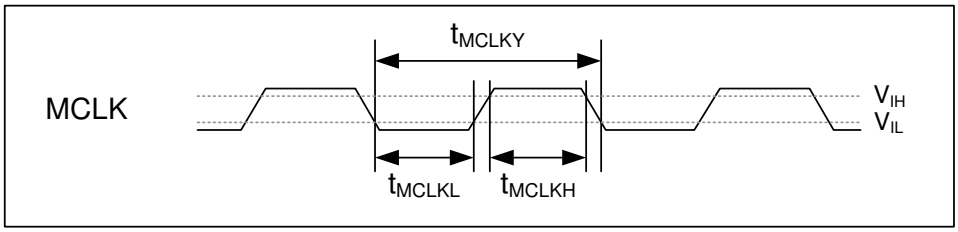


Figure 1 Master Clock Timing

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Master Clock Timing (MCLK1, MCLK2)					
MCLK cycle time	MCLK as input to FLL, FLLn_REFCLK_DIV=00	74			ns
	MCLK as input to FLL, FLLn_REFCLK_DIV=01	37			
	MCLK as input to FLL, FLLn_REFCLK_DIV=10	18			
	MCLK as input to FLL, FLLn_REFCLK_DIV=11	12.5			
	MCLK as direct SYSCLK or ASYNCCLK source	40			
MCLK duty cycle	MCLK as input to FLL	80:20		20:80	%
	MCLK as direct SYSCLK or ASYNCCLK source	60:40		40:60	
Frequency Locked Loops (FLL1, FLL2)					
FLL input frequency	FLLn_REFCLK_DIV=00	0.032		13.5	MHz
	FLLn_REFCLK_DIV=01	0.064		27	
	FLLn_REFCLK_DIV=10	0.128		54	
	FLLn_REFCLK_DIV=11	0.256		80	
FLL synchroniser input frequency	FLLn_SYNCCLK_DIV=00	0.032		13.5	MHz
	FLLn_SYNCCLK_DIV=01	0.064		27	
	FLLn_SYNCCLK_DIV=10	0.128		54	
	FLLn_SYNCCLK_DIV=11	0.256		80	

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal Clocking					
SYSCLK frequency	SYSCLK_FREQ=000, SYSCLK_FRAC=0	-1%	6.144	+1%	MHz
	SYSCLK_FREQ=000, SYSCLK_FRAC=1	-1%	5.6448	+1%	
	SYSCLK_FREQ=001, SYSCLK_FRAC=0	-1%	12.288	+1%	
	SYSCLK_FREQ=001, SYSCLK_FRAC=1	-1%	11.2896	+1%	
	SYSCLK_FREQ=010, SYSCLK_FRAC=0	-1%	24.576	+1%	
	SYSCLK_FREQ=010, SYSCLK_FRAC=1	-1%	22.5792	+1%	
	SYSCLK_FREQ=011, SYSCLK_FRAC=0	-1%	49.152	+1%	
	SYSCLK_FREQ=011, SYSCLK_FRAC=1	-1%	45.1584	+1%	
	SYSCLK_FREQ=100, SYSCLK_FRAC=0	-1%	98.304	+1%	
	SYSCLK_FREQ=100, SYSCLK_FRAC=1	-1%	90.3168	+1%	
ASYNCCLK frequency	ASYNC_CLK_FREQ=000	-1%	6.144	+1%	MHz
		-1%	5.6448	+1%	
	ASYNC_CLK_FREQ=001	-1%	12.288	+1%	
		-1%	11.2896	+1%	
	ASYNC_CLK_FREQ=010	-1%	24.576	+1%	
		-1%	22.5792	+1%	
	ASYNC_CLK_FREQ=011	-1%	49.152	+1%	
		-1%	45.1584	+1%	
	ASYNC_CLK_FREQ=100	-1%	98.304	+1%	
		-1%	90.3168	+1%	
DSPCLK frequency		5		150	MHz

Note:

When MCLK1 or MCLK2 is selected as a source for SYSCLK or ASYNCCLK (either directly or via one of the FLLs), the frequency must be within 1% of the applicable SYSCLK_FREQ or ASYNCCLK_FREQ register setting.

AUDIO INTERFACE TIMING

DIGITAL MICROPHONE (DMIC) INTERFACE TIMING

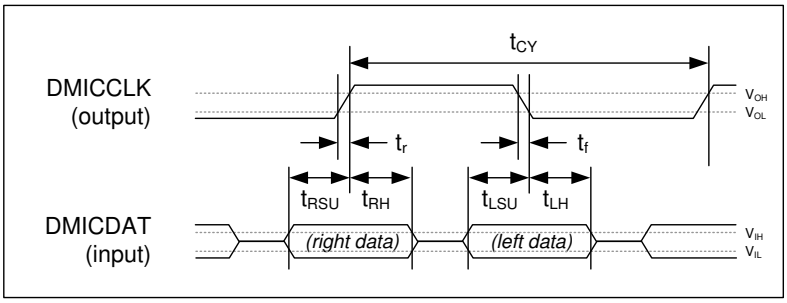


Figure 2 Digital Microphone Interface Timing

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital Microphone Interface Timing					
DMICCLKn cycle time	t_{CY}	160	163	1432	ns
DMICCLKn duty cycle		45		55	%
DMICCLKn rise/fall time (25pF load, 1.8V supply - see note)	t_r, t_f	5		30	ns
DMICDATn (Left) setup time to falling DMICCLK edge	t_{LSU}	15			ns
DMICDATn (Left) hold time from falling DMICCLK edge	t_{LH}	0			ns
DMICDATn (Right) setup time to rising DMICCLK edge	t_{RSU}	15			ns
DMICDATn (Right) hold time from rising DMICCLK edge	t_{RH}	0			ns

Notes:

DMICDATn and DMICCLKn are each referenced to a selectable supply, V_{SUP}.

The applicable supply is selected using the INn_DMIC_SUP registers.

The voltage reference for the IN1, IN2 and IN3 digital microphone interfaces is selectable, using the IN*n*_DMIC_SUP registers - each interface may be referenced to MICVDD, or to the MICBIAS1, MICBIAS2 or MICBIAS3 levels.

The voltage reference for the IN4, IN5 and IN6 digital microphone interfaces is DBVDD4.

DIGITAL SPEAKER (PDM) INTERFACE TIMING

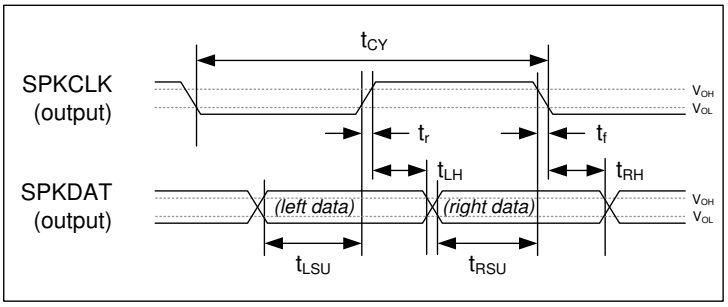


Figure 3 Digital Speaker (PDM) Interface Timing - Mode A

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
PDM Audio Interface Timing					
SPKCLKn cycle time	t_{CY}	160	163	358	ns
SPKCLKn duty cycle		45		55	%
SPKCLKn rise/fall time (25pF load)	t_r, t_f	2		8	ns
SPKDATn set-up time to SPKCLKn rising edge (Left channel)	t_{LSU}	30			ns
SPKDATn hold time from SPKCLKn rising edge (Left channel)	t_{LH}	30			ns
SPKDATn set-up time to SPKCLKn falling edge (Right channel)	t_{RSU}	30			ns
SPKDATn hold time from SPKCLKn falling edge (Right channel)	t_{RH}	30			ns

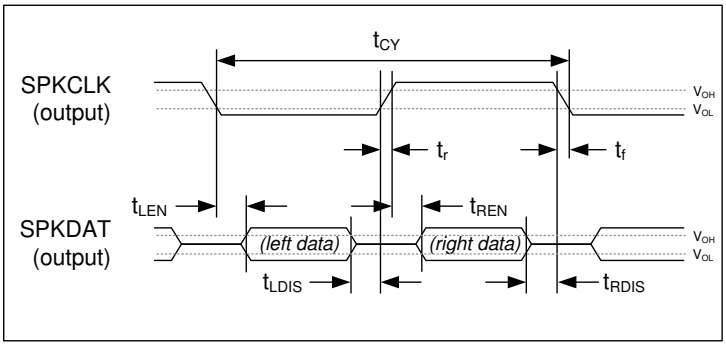


Figure 4 Digital Speaker (PDM) Interface Timing - Mode B

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
PDM Audio Interface Timing					
SPKCLKn cycle time	t_{CY}	160	163	358	ns
SPKCLKn duty cycle		45		55	%
SPKCLKn rise/fall time (25pF load)	t_r, t_f	2		8	ns
SPKDATn enable from SPKCLK rising edge (Right channel)	t_{REN}			15	ns
SPKDATn disable to SPKCLK falling edge (Right channel)	t_{RDIS}			5	ns
SPKDATn enable from SPKCLK falling edge (Left channel)	t_{LEN}			15	ns
SPKDATn disable to SPKCLK rising edge (Left channel)	t_{LDIS}			5	ns

DIGITAL AUDIO INTERFACE - MASTER MODE

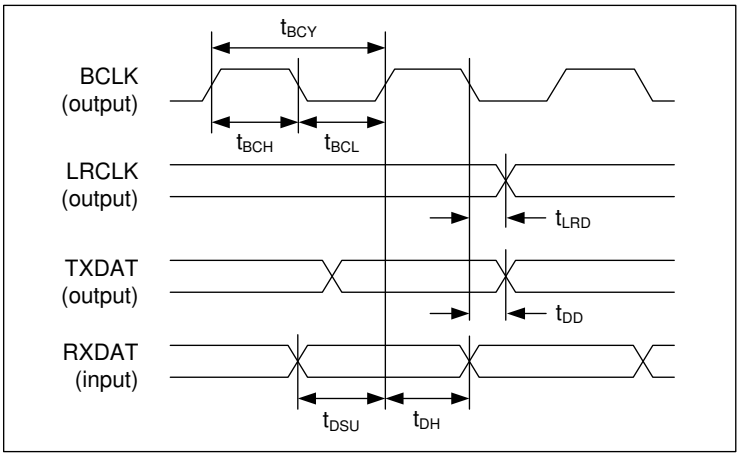


Figure 5 Audio Interface Timing - Master Mode

Note that BCLK and LRCLK outputs can be inverted if required; Figure 5 shows the default, non-inverted polarity.

Test Conditions

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.

C_{LOAD} = 15pF to 25pF (output pins). BCLK slew (10% to 90%) = 3.7ns to 5.6ns.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Master Mode					
AIFnBCLK cycle time	t_{BCY}	40			ns
AIFnBCLK pulse width high	t_{BCH}	18			ns
AIFnBCLK pulse width low	t_{BCL}	18			ns
AIFnLRCLK propagation delay from BCLK falling edge	t_{LRD}	0		8.3	ns
AIFnTXDAT propagation delay from BCLK falling edge	t_{DD}	0		5	ns
AIFnRXDAT setup time to BCLK rising edge	t_{DSU}	11			ns
AIFnRXDAT hold time from BCLK rising edge	t_{DH}	0			ns
Audio Interface Timing - Master Mode, Slave LRCLK					
AIFnLRCLK setup time to BCLK rising edge	t_{LRSU}	14			ns
AIFnLRCLK hold time from BCLK rising edge	t_{LRH}	0			ns

Note:

The descriptions above assume non-inverted polarity of AIFnBCLK.

DIGITAL AUDIO INTERFACE - SLAVE MODE

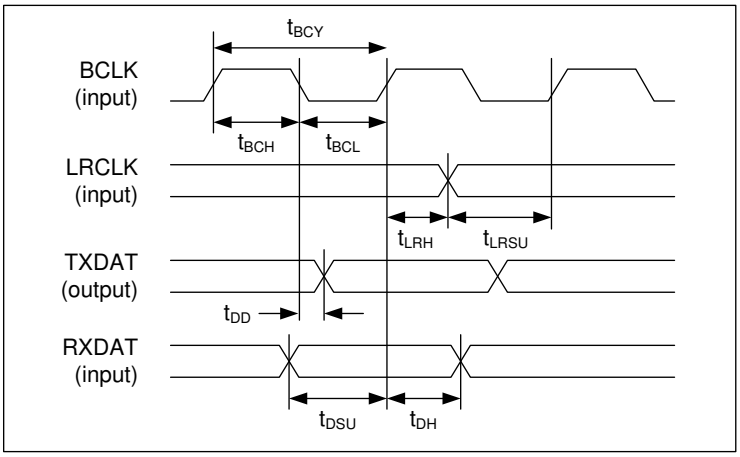


Figure 6 Audio Interface Timing - Slave Mode

Note that BCLK and LRCLK inputs can be inverted if required; Figure 6 shows the default, non-inverted polarity.

Test Conditions

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Slave Mode						
AIFnBCLK cycle time		t_{BCY}	40			ns
AIFnBCLK pulse width high	BCLK as direct SYSCLK or ASYNCCLK source	t_{BCH}	16			ns
	All other conditions		14			
AIFnBCLK pulse width low	BCLK as direct SYSCLK or ASYNCCLK source	t_{BCL}	16			ns
	All other conditions		14			
Audio Interface Timing - Slave Mode C_{LOAD} = 15pF (output pins). BCLK slew (10% to 90%) = 3ns.						
AIFnLRCLK set-up time to BCLK rising edge		t_{LRSU}	7			ns
AIFnLRCLK hold time from BCLK rising edge		t_{LRH}	0			ns
AIFnTXDAT propagation delay from BCLK falling edge		t_{DD}	0		12.2	ns
AIFnRXDAT set-up time to BCLK rising edge		t_{DSU}	2			ns
AIFnRXDAT hold time from BCLK rising edge		t_{DH}	0			ns
Audio Interface Timing - Slave Mode C_{LOAD} = 25pF (output pins). BCLK slew (10% to 90%) = 6ns.						
AIFnLRCLK set-up time to BCLK rising edge		t_{LRSU}	7			ns
AIFnLRCLK hold time from BCLK rising edge		t_{LRH}	0			ns
AIFnTXDAT propagation delay from BCLK falling edge		t_{DD}	0		14.2	ns
AIFnRXDAT set-up time to BCLK rising edge		t_{DSU}	2			ns
AIFnRXDAT hold time from BCLK rising edge		t_{DH}	0			ns
Audio Interface Timing - Slave Mode, Master LRCLK						
AIFnLRCLK propagation delay from BCLK falling edge C_{LOAD} = 15pF (output pins). BCLK slew (10% to 90%) = 3ns.		t_{LRD}			14.8	ns
AIFnLRCLK propagation delay from BCLK falling edge C_{LOAD} = 25pF (output pins). BCLK slew (10% to 90%) = 6ns.					15.9	

Notes:

The descriptions above assume non-inverted polarity of AIFnBCLK.

When AIFnBCLK or AIFnLRCLK is selected as a source for SYSCLK or ASYNCCLK (either directly or via one of the FLLs), the frequency must be within 1% of the applicable SYSCLK_FREQ or ASYNCCLK_FREQ register setting.

DIGITAL AUDIO INTERFACE - TDM MODE

When TDM operation is used on the AIFnTXDAT pins, it is important that two devices do not attempt to drive the AIFnTXDAT pin simultaneously. To support this requirement, the AIFnTXDAT pins can be configured to be tri-stated when not outputting data.

The timing of the AIFnTXDAT tri-stating at the start and end of the data transmission is described in Figure 7 below.

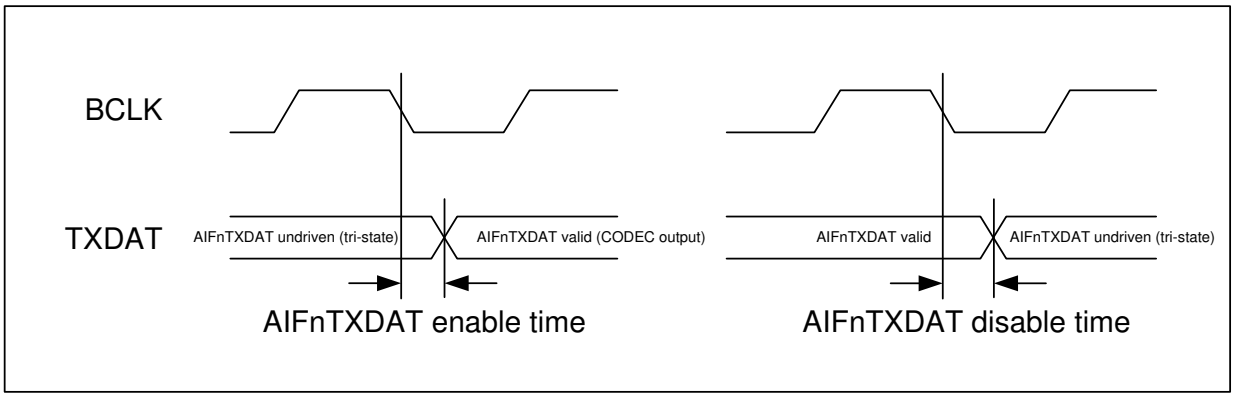


Figure 7 Audio Interface Timing - TDM Mode

Test Conditions

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.

PARAMETER	MIN	TYP	MAX	UNIT
TDM Timing - Master Mode C_{LOAD} (AIFnTXDAT) = 15pF to 25pF. BCLK slew (10% to 90%) = 3.7ns to 5.6ns.				
AIFnTXDAT enable time from BCLK falling edge	0			ns
AIFnTXDAT disable time from BCLK falling edge			6	ns
TDM Timing - Slave Mode C_{LOAD} (AIFnTXDAT) = 15pF). BCLK slew (10% to 90%) = 3ns.				
AIFnTXDAT enable time from BCLK falling edge	2			ns
AIFnTXDAT disable time from BCLK falling edge			12.2	ns
TDM Timing - Slave Mode C_{LOAD} (AIFnTXDAT) = 25pF). BCLK slew (10% to 90%) = 6ns				
AIFnTXDAT enable time from BCLK falling edge	2			ns
AIFnTXDAT disable time from BCLK falling edge			14.2	ns

CONTROL INTERFACE TIMING

2-WIRE (I2C) CONTROL MODE

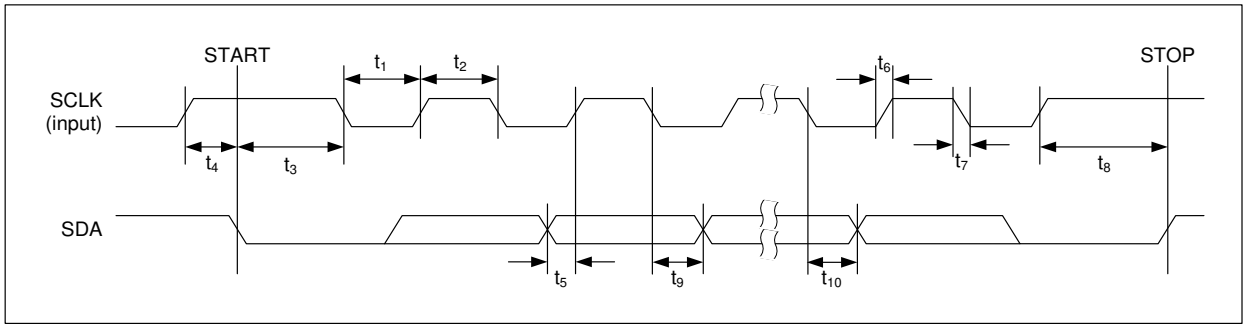


Figure 8 Control Interface Timing - 2-wire (I2C) Control Mode

Test Conditions

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
SCLK Frequency					3400	kHz
SCLK Low Pulse-Width		t_1	160			ns
SCLK High Pulse-Width		t_2	100			ns
Hold Time (Start Condition)		t_3	160			ns
Setup Time (Start Condition)		t_4	160			ns
SDA, SCLK Rise Time (10% to 90%)	SCLK frequency > 1.7MHz	t_6			80	ns
	SCLK frequency > 1MHz				160	
	SCLK frequency ≤ 1MHz				2000	
SDA, SCLK Fall Time (90% to 10%)	SCLK frequency > 1.7MHz	t_7			60	ns
	SCLK frequency > 1MHz				160	
	SCLK frequency ≤ 1MHz				200	
Setup Time (Stop Condition)		t_8	160			ns
SDA Setup Time (data input)		t_5	40			ns
SDA Hold Time (data input)		t_9	0			ns
SDA Valid Time (data/ACK output)	SCLK slew (90% to 10%) = 20ns, C_{LOAD} (SDA) = 15pF	t_{10}			40	ns
	SCLK slew (90% to 10%) = 60ns, C_{LOAD} (SDA) = 100pF				130	
	SCLK slew (90% to 10%) = 160ns, C_{LOAD} (SDA) = 400pF				190	
	SCLK slew (90% to 10%) = 200ns, C_{LOAD} (SDA) = 550pF				220	
Pulse width of spikes that will be suppressed		t_{ps}	0		25	ns

4-WIRE (SPI) CONTROL MODE

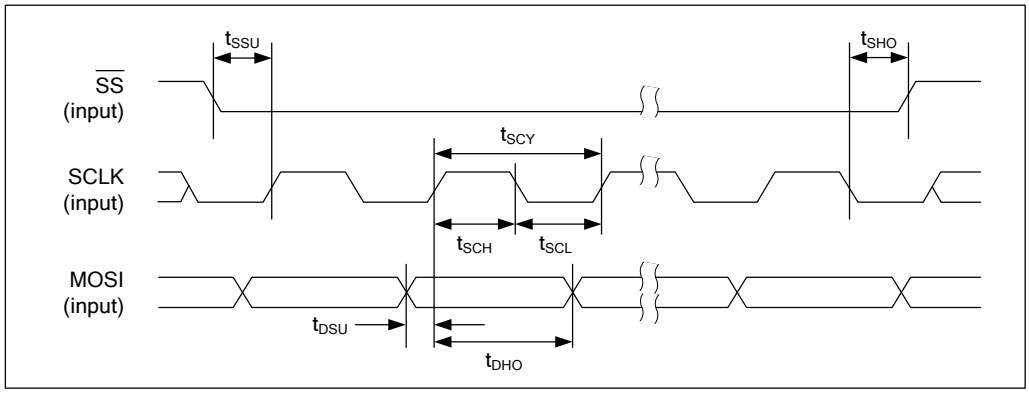


Figure 9 Control Interface Timing - 4-wire (SPI) Control Mode (Write Cycle)

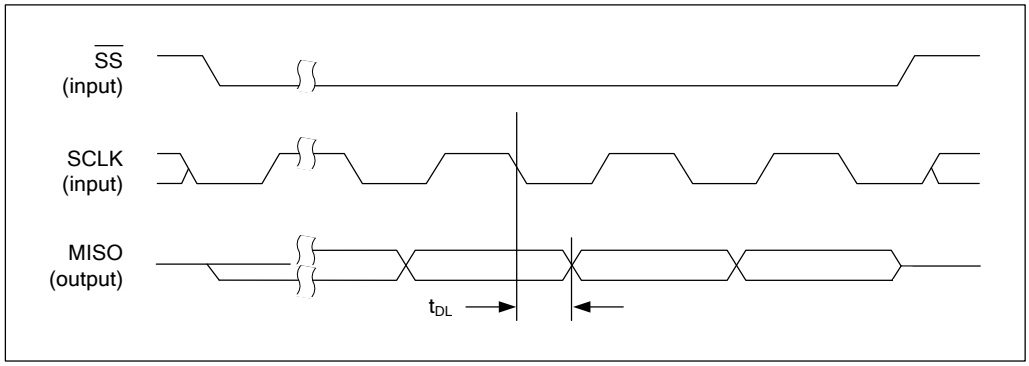


Figure 10 Control Interface Timing - 4-wire (SPI) Control Mode (Read Cycle)

Test Conditions

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
SS falling edge to SCLK rising edge		t_{SSU}	2.6			ns
SCLK falling edge to SS rising edge		t_{SHO}	0			ns
SCLK pulse cycle time	SYSCLK disabled (SYSCLK_ENA=0)	t_{SCY}	50.0			ns
	SYSCLK_ENA=1 and SYSCLK_FREQ = 000		76.8			
	SYSCLK_ENA=1 and SYSCLK_FREQ > 000		38.4			
SCLK pulse width low		t_{SCL}	15.3			ns
SCLK pulse width high		t_{SCH}	15.3			ns
MOSI to SCLK set-up time		t_{DSU}	1.5			ns
MOSI to SCLK hold time		t_{DHO}	1.7			ns
SCLK falling edge to MISO transition	SCLK slew (90% to 10%) = 5ns, C_{LOAD} (MISO) = 25pF	t_{DL}	0		12.6	ns

SLIMBUS INTERFACE TIMING

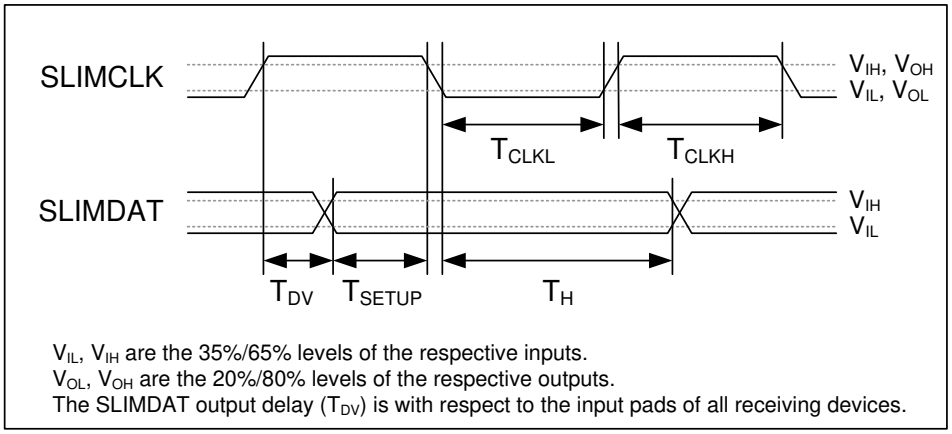


Figure 11 SLIMbus Interface Timing

The signal timing information shown in Figure 11 describe the timing requirements of the SLIMbus interface as a whole, not just the CS47L85 device. Accordingly, the following should be noted:

- T_{DV} is the propagation delay from the rising SLIMCLK edge (at CS47L85 input) to the SLIMDAT output being achieved at the input to all devices across the bus.
- T_{SETUP} is the set-up time for SLIMDAT input (at CS47L85), relative to the falling SLIMCLK edge (at CS47L85).
- T_H is the hold time for SLIMDAT input (at CS47L85) relative to the falling SLIMCLK edge (at CS47L85).

For more details of the interface timing, refer to the MIPI Alliance Specification for Serial Low-power Inter-chip Media Bus (SLIMbus).

Test Conditions

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
SLIMCLK Input						
SLIMCLK cycle time			35			ns
SLIMCLK pulse width high		T_{CLKH}	12			ns
SLIMCLK pulse width low		T_{CLKL}	12			ns
SLIMCLK Output						
SLIMCLK cycle time			40			ns
SLIMCLK pulse width high		T_{CLKH}	12			ns
SLIMCLK pulse width low		T_{CLKL}	12			ns
SLIMCLK slew rate (20% to 80%)	C_{LOAD} = 15pF, SLIMCLK_DRV_STR=0	SR_{CLK}	0.09 x V_{DBVDD1}		0.22 x V_{DBVDD1}	V/ns
	C_{LOAD} = 70pF, SLIMCLK_DRV_STR=0		0.02 x V_{DBVDD1}		0.05 x V_{DBVDD1}	
	C_{LOAD} = 70pF, SLIMCLK_DRV_STR=1		0.04 x V_{DBVDD1}		0.11 x V_{DBVDD1}	
SLIMDAT Input						
SLIMDAT setup time to SLIMCLK falling edge		T_{SETUP}	3.5			ns
SLIMDAT hold time from SLIMCLK falling edge		T_H	2			ns

Test Conditions

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
SLIMDAT Output						
SLIMDAT time for data output valid (wrt SLIMCLK rising edge)	C_{LOAD} = 15pF, SLIMDAT_DRV_STR=0, DBVDD1=1.71V	T_{DV}		4.7	8.1	ns
	C_{LOAD} = 15pF, SLIMDAT_DRV_STR=1, DBVDD1=1.71V			4.3	7.3	
	C_{LOAD} = 30pF, SLIMDAT_DRV_STR=0, DBVDD1=1.71V			6.8	11.8	
	C_{LOAD} = 30pF, SLIMDAT_DRV_STR=1, DBVDD1=1.71V			5.8	10.0	
	C_{LOAD} = 50pF, SLIMDAT_DRV_STR=0, DBVDD1=1.71V			9.6	16.6	
	C_{LOAD} = 50pF, SLIMDAT_DRV_STR=1, DBVDD1=1.71V			7.9	13.7	
	C_{LOAD} = 70pF, SLIMDAT_DRV_STR=0, DBVDD1=1.71V			12.4	21.5	
	C_{LOAD} = 70pF, SLIMDAT_DRV_STR=1, DBVDD1=1.71V			10.0	17.4	
SLIMDAT slew rate (20% to 80%)	C_{LOAD} = 15pF, SLIMDAT_DRV_STR=0	SR_{DATA}			0.64 x V_{DBVDD1}	V/ns
	C_{LOAD} = 30pF, SLIMDAT_DRV_STR=0				0.35 x V_{DBVDD1}	
	C_{LOAD} = 30pF, SLIMDAT_DRV_STR=1				0.46 x V_{DBVDD1}	
	C_{LOAD} = 70pF, SLIMDAT_DRV_STR=0				0.16 x V_{DBVDD1}	
	C_{LOAD} = 70pF, SLIMCLK_DRV_STR=1				0.21 x V_{DBVDD1}	
Other Parameters						
Driver disable time		T_{DD}			6	ns
Bus holder output impedance	0.1 x V_{DBVDD1} < V < 0.9 x V_{DBVDD1}	R_{DATAS}	18		50	kΩ

JTAG INTERFACE TIMING

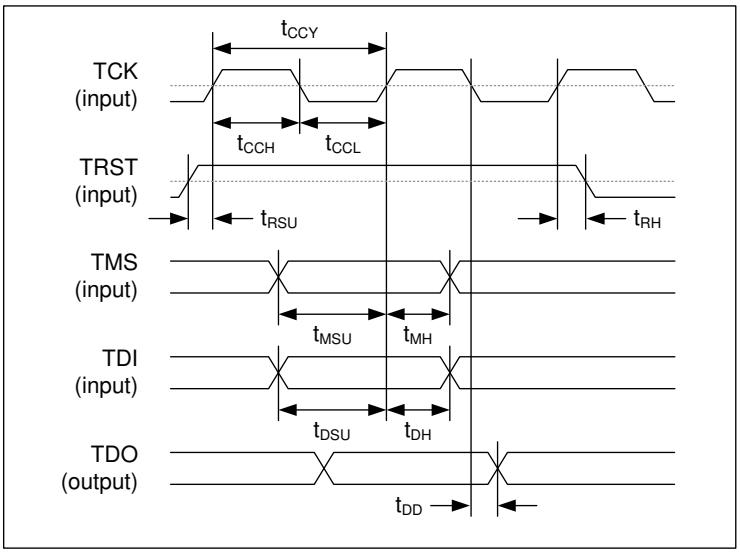


Figure 12 JTAG Interface Timing

Test Conditions

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.
C_{LOAD} = 25pF (output pins). TCK slew (20% to 80%) = 5ns.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
JTAG Interface Timing					
TCK cycle time	T_{CCY}	50			ns
TCK pulse width high	T_{CCH}	20			ns
TCK pulse width low	T_{CCL}	20			ns
TMS setup time to TCK rising edge	T_{MSU}	1			ns
TMS hold time from TCK rising edge	T_{MH}	2			ns
TDI setup time to TCK rising edge	T_{DSU}	1			ns
TDI hold time from TCK rising edge	T_{DH}	2			ns
TDO propagation delay from TCK falling edge	T_{DD}	0		17	ns
TRST setup time to TCK rising edge	T_{RSU}	3			ns
TRST hold time from TCK rising edge	T_{RH}	3			ns
TRST pulse width low		20			ns

DEVICE DESCRIPTION

INTRODUCTION

The CS47L85 is a highly integrated low-power audio hub CODEC for mobile telephony and portable devices. It provides flexible, high-performance audio interfacing for handheld devices in a small and cost-effective package. It provides exceptional levels of performance and signal processing capability, suitable for a wide variety of mobile and handheld devices.

The CS47L85 digital core incorporates the Cirrus Logic Ambient Noise Cancellation (ANC), and provides an extensive capability for programmable signal processing algorithms, including receive (RX) path noise cancellation, transmit (TX) path noise reduction, and Acoustic Echo Cancellation (AEC) algorithms.

The digital core provides signal processing capability for sensor hub functions. The programmable DSP allows many external sensors to be efficiently integrated, enabling increased contextual awareness in a wide variety of advanced user applications.

The CS47L85 digital core supports audio enhancements, such as Dynamic Range Control (DRC), Multi-band Compression (MBC), and Virtual Surround Sound (VSS). Highly flexible digital mixing, including stereo full-duplex asynchronous sample rate conversion, provides use-case flexibility across a broad range of system architectures. A signal generator for controlling haptics vibe actuators is included.

The CS47L85 provides multiple digital audio interfaces, including SLIMbus, in order to provide independent and fully asynchronous connections to different processors (e.g., application processor, baseband processor and wireless transceiver).

A flexible clocking arrangement supports a wide variety of external clock references, including clocking derived from the digital audio interface. Three Frequency Locked Loop (FLL) circuits provide additional flexibility.

Unused circuitry can be disabled under software control, in order to save power; low leakage currents enable extended standby/off time in portable battery-powered applications. The CS47L85 'Always-On' circuitry can be used (in conjunction with the Apps Processor) to 'Wake-Up' the device following a headphone jack detection event.

Versatile GPIO functionality is provided, and support for external accessory / push-button detection inputs. Comprehensive Interrupt (IRQ) logic and status readback are also provided.

HI-FI AUDIO CODEC

The CS47L85 is a high-performance low-power audio CODEC which uses a simple analogue architecture. Six ADCs are incorporated, with multiplexers to support up to nine analogue inputs. Eight DACs are incorporated, providing a dedicated DAC for each analogue output channel.

The analogue outputs comprise three 32mW (121dB SNR) stereo headphone amplifiers with ground-referenced output, and a Class D stereo speaker driver capable of delivering 2.5W per channel into a 4Ω load. Six analogue inputs are provided, each supporting single-ended or differential input modes. In differential mode, the input path SNR is 106dB (16kHz sample rate, i.e., wideband voice mode). The ADC input paths can be bypassed, supporting up to 12 channels of digital microphone input.

The audio CODEC is controlled directly via register access. The simple analogue architecture, combined with the integrated tone generator, enables simple device configuration and testing, minimising debug time and reducing software effort.

The CS47L85 output drivers are designed to support as many different system architectures as possible. Each output has a dedicated DAC which allows mixing, equalisation, filtering, gain and other audio processing to be configured independently for each channel. This allows each signal path to be individually tailored for the load characteristics. All outputs have integrated pop and click suppression features.

The headphone output drivers are ground-referenced, powered from an integrated charge pump, enabling high quality, power efficient headphone playback without any requirement for DC blocking capacitors. Ground loop feedback is incorporated, providing rejection of noise on the ground connections. A mono mode is available on the headphone outputs; this configures the drivers as differential (BTL) outputs, suitable for an earpiece or hearing aid coil.

The Class D speaker drivers deliver excellent power efficiency. High PSRR, low leakage and optimised supply voltage ranges enable powering from switching regulators or directly from the battery. Battery current consumption is minimised across a wide variety of voice communication and multimedia playback use cases.

The CS47L85 is cost-optimised for a wide range of mobile phone applications, and features two channels of Class D power amplification. For applications requiring more than two channels of power amplification (or when using the integrated Class D path to drive a haptics actuator), the PDM output channels can be used to drive up to four external PDM-input speaker drivers. In applications where stereo loudspeakers are physically widely separated, the PDM outputs can ease layout and EMC by avoiding the need to run the Class-D speaker outputs over long distances and interconnects.

DIGITAL AUDIO CORE

The CS47L85 uses a core architecture based on all-digital signal routing, making digital audio effects available on all signal paths, regardless of whether the source data input is analogue or digital. The digital mixing desk allows different audio effects to be applied simultaneously on many independent paths, whilst also supporting a variety of sample rates concurrently. This helps support many new audio use-cases. Soft mute and un-mute control allows smooth transitions between use-cases without interrupting existing audio streams elsewhere.

The CS47L85 digital core provides an extensive capability for programmable signal processing algorithms. The DSP can support functions such as wind noise, side-tone and other programmable filters. A wide range of application-specific filters and audio enhancements can also be implemented, including Dynamic Range Control (DRC), Multi-band Compression (MBC), and Virtual Surround Sound (VSS). These digital effects can be used to improve audibility and stereo imaging while minimising supply current.

The digital core also provides signal processing capability for sensor hub functions of the CS47L85. Sensors and accessories can be connected through 3 master I2C interfaces; the programmable DSP, together with peripheral timer and event logging functions, enables applications to use these inputs to support increased contextual awareness, including advanced motion sensing and navigation functionality.

The Cirrus Logic Ambient Noise Cancellation (ANC) processor within the CS47L85 provides the capability to improve the intelligibility of a voice call by using destructive interference to reduce the acoustic energy of the ambient sound. The Cirrus Logic ANC technology supports receive (RX) path noise cancellation; Transmit (TX) path noise reduction, and multi-mic Acoustic Echo Cancellation (AEC) algorithms are also supported. The CS47L85 is ideal for mobile telephony, providing enhanced voice communication quality for both near-end and far-end users in a wide variety of applications.

Highly flexible digital mixing, including mixing between audio interfaces, is possible. The CS47L85 performs multi-channel full-duplex asynchronous sample rate conversion, providing use-case flexibility across a broad range of system architectures. Automatic sample rate detection is provided, enabling seamless wideband/narrowband voice call handover.

Dynamic Range Controller (DRC) functions are available for optimising audio signal levels. In playback modes, the DRC can be used to maximise loudness, while limiting the signal level to avoid distortion, clipping or battery droop, in particular for high-power output drivers such as speaker amplifiers. In record modes, the DRC assists in applications where the signal level is unpredictable.

The 5-band parametric equaliser (EQ) functions can be used to compensate for the frequency characteristics of the output transducers. EQ functions can be cascaded to provide additional frequency control. Programmable high-pass and low-pass filters are also available for general filtering applications such as removal of wind and other low-frequency noise.

DIGITAL INTERFACES

Four serial digital audio interfaces (AIFs) each support PCM, TDM and I2S data formats for compatibility with most industry-standard chipsets. AIF1 and AIF2 support eight input/output channels; AIF3 and AIF4 support two input/output channels. Bidirectional operation at sample rates up to 192kHz is supported.

12 digital PDM input channels are available (six stereo interfaces); these are typically used for digital microphones, powered from the integrated MICBIAS power supply regulators. Four PDM output channels are also available (two stereo interfaces); these are typically used for external power amplifiers. Embedded mute codes provide a control mechanism for external PDM-input devices.

The CS47L85 features a MIPI-compliant SLIMbus interface, providing eight channels of audio input/output. Mixed audio sample rates are supported on the SLIMbus interface. The SLIMbus interface also supports read/write access to the CS47L85 control registers.

An IEC-60958-3 compatible S/PDIF transmitter is incorporated, enabling stereo S/PDIF output on a GPIO pin. Standard S/PDIF sample rates of 32kHz up to 192kHz are all supported.

Control register access, and high bandwidth data transfer, is supported by two slave SPI interfaces and a slave I2C control interface. The SPI interfaces operate up to 26MHz; the I2C slave interface operates up to 3.4MHz. Full access to the register map is also provided via the SLIMbus port.

The CS47L85 incorporates three master I2C interfaces, offering a flexible capability for additional sensor / accessory input. Typical sensors include accelerometers, gyroscopes and magnetometers for motion sensing and navigation applications. Other example accessories include barometers, or ambient light sensors, for environmental awareness.

OTHER FEATURES

The CS47L85 incorporates two 1kHz tone generators which can be used for ‘beep’ functions through any of the audio signal paths. The phase relationship between the two generators is configurable, providing flexibility in creating differential signals, or for test scenarios.

A white noise generator is provided, which can be routed within the digital core. The noise generator can provide ‘comfort noise’ in cases where silence (digital mute) is not desirable.

Two Pulse Width Modulation (PWM) signal generators are incorporated. The duty cycle of each PWM signal can be modulated by an audio source, or can be set to a fixed value using a control register setting. The PWM signal generators can be output directly on a GPIO pin.

The CS47L85 supports up to 40 GPIO pins, offering a range of input/output functions for interfacing, detection of external hardware, and to provide logic outputs to other devices. The CS47L85 provides 8 dedicated GPIO pins; a further 32 GPIOs are multiplexed with other functions. Comprehensive Interrupt (IRQ) functionality is also provided for monitoring internal and external event conditions.

A signal generator for controlling haptics devices is included, compatible with both Eccentric Rotating Mass (ERM) and Linear Resonant Actuator (LRA) haptic devices. The haptics signal generator is highly configurable, and can execute programmable drive event profiles, including reverse drive control. An external vibe actuator can be driven directly by the Class D speaker output.

The CS47L85 incorporates eight general purpose timers, providing support for the sensor hub capability. Sensor event logging, and other real time application functions, allows many advanced functions to be implemented with a high degree of autonomy from a host processor.

A smart accessory interface is included, supporting most standard 3.5mm accessories. Jack detection, accessory sensing and impedance measurement is provided, for external accessory and push-button detection. Accessory detection can be used as a ‘Wake-Up’ trigger from low-power standby. Microphone activity detection with interrupt is also available.

System clocking can be derived from the MCLK1 or MCLK2 input pins. Alternatively, the SLIMbus interface, or the audio interfaces (configured in Slave mode), can be used to provide a clock reference. Three integrated Frequency Locked Loop (FLL) circuits provide support for a wide range of clocking configurations, including the use of a 32kHz input clock reference.

The CS47L85 can be powered from 1.8V and 1.2V external supplies. A separate supply (4.2V) is typically required for the Class D speaker driver. Integrated Charge Pump and LDO Regulators circuits are used to generate supply rails for internal functions and to support powering or biasing of external microphones.

INPUT SIGNAL PATH

The CS47L85 provides flexible input channels, supporting up to 9 analogue inputs or up to 12 digital inputs. Selectable combinations of analogue (mic or line) and digital inputs are multiplexed into 6 stereo input signal paths. Input paths IN1, IN2 and IN3 support analogue and digital inputs; Input paths IN4, IN5 and IN6 support digital inputs only.

The analogue input paths support single-ended and differential modes, programmable gain control and are digitised using a high performance 24-bit sigma-delta ADC.

The digital input paths interface directly with external digital microphones; a separate microphone interface clock is provided for six separate stereo pairs of digital microphones. Digital delay can be applied to any of the digital input paths; this can be used for phase adjustment of any digital input, including directional control of multiple microphones.

Four microphone bias (MICBIAS) generators are available, which provide a low noise reference for biasing electret condenser microphones (ECMs) or for use as a low noise supply for MEMS microphones and digital microphones.

Digital volume control is available on all inputs (analogue and digital), with programmable ramp control for smooth, glitch-free operation. Any pair of analogue or digital inputs may be selected as input to the Ambient Noise Cancellation (ANC) processing function.

The signal paths and control registers for inputs IN1, IN2 and IN3 are illustrated in Figure 13. The IN4, IN5 and IN6 signal paths supports digital microphone input only.

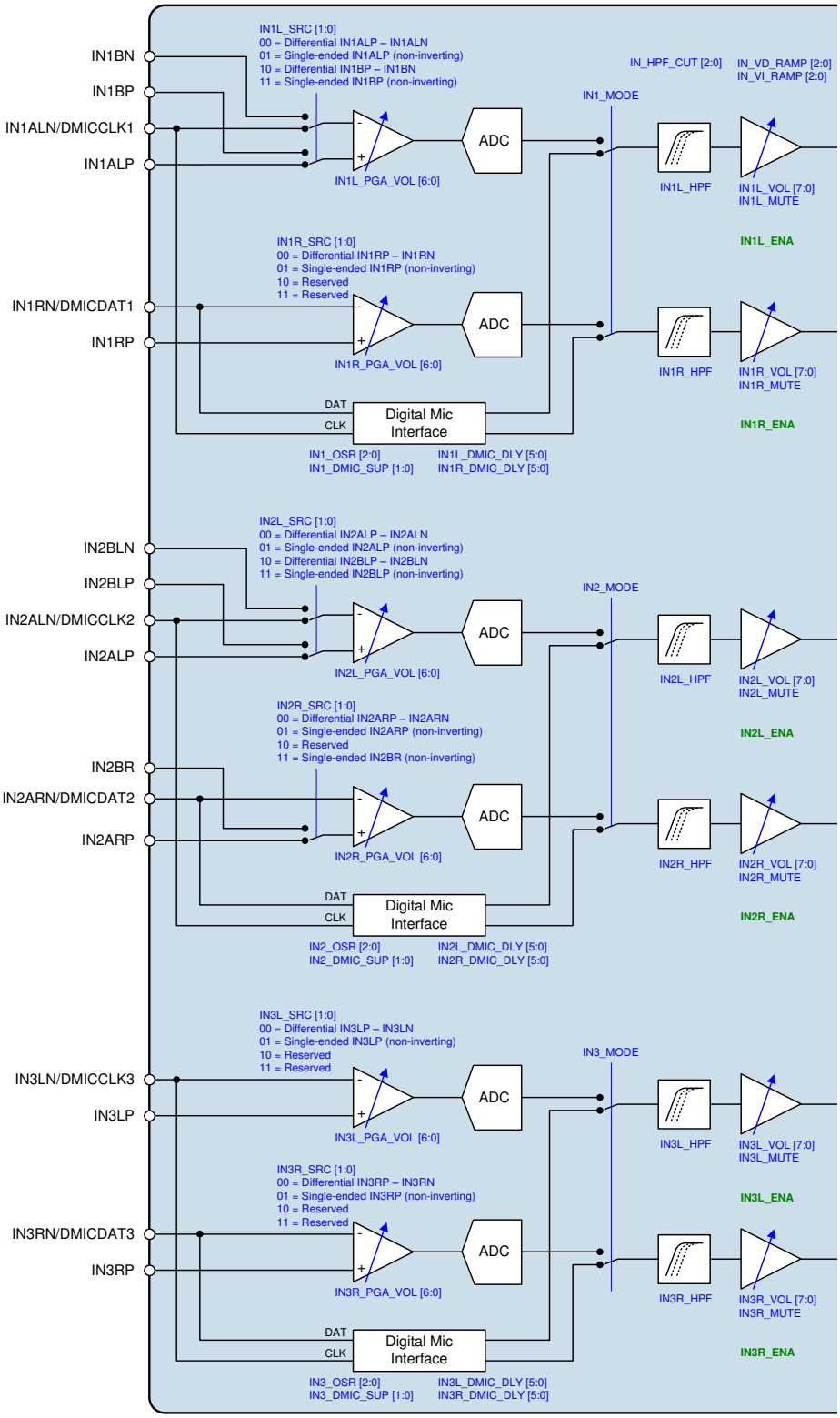


Figure 13 Input Signal Paths

ANALOGUE MICROPHONE INPUT

Up to nine analogue microphones can be connected to the CS47L85, either in single-ended or differential mode. The applicable mode, and input pin selection, is controlled using the IN*nx*_SRC registers, as described later.

The CS47L85 includes external accessory detection circuits, which can detect the presence of a microphone, and the status of a hookswitch or other push-buttons. When using this function, it is recommended to use the IN1B or IN2B analogue microphone input paths, to ensure best immunity to electrical transients arising from the push-buttons.

For single-ended input, the microphone signal is connected to the non-inverting input of the PGAs (IN*n*LP or IN*n*RP). The inverting inputs of the PGAs are connected to an internal reference in this configuration.

For differential input, the non-inverted microphone signal is connected to the non-inverting input of the PGAs (IN*n*LP or IN*n*RP), whilst the inverted (or 'noisy ground') signal is connected to the inverting input pins (IN*n*LN or IN*n*RN).

The gain of the input PGAs is controlled via register settings, as defined in Table 4. Note that the input impedance of the analogue input paths is fixed across all PGA gain settings.

The Electret Condenser Microphone (ECM) analogue input configurations are illustrated in Figure 14 and Figure 15. The integrated MICBIAS generators provide a low noise reference for biasing the ECMs.

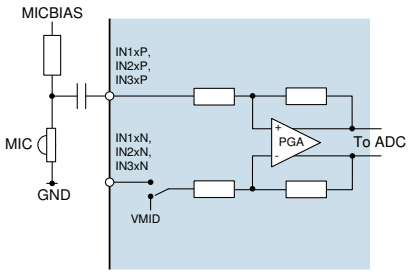


Figure 14 Single-Ended ECM Input

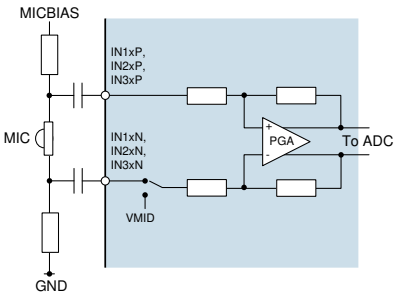


Figure 15 Differential ECM Input

Analogue MEMS microphones can be connected to the CS47L85 in a similar manner to the ECM configurations described above; typical configurations are illustrated in Figure 16 and Figure 17. In this configuration, the integrated MICBIAS generators provide a low-noise power supply for the microphones.

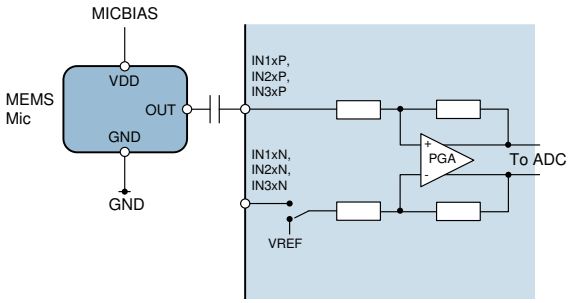


Figure 16 Single-Ended MEMS Input

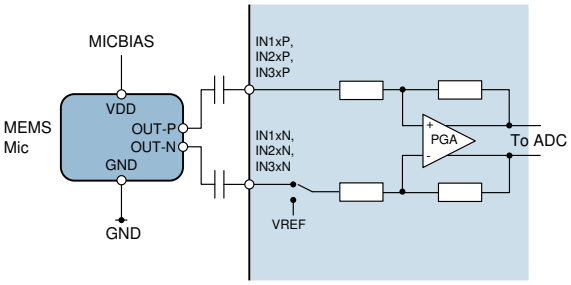


Figure 17 Differential MEMS Input

Note that the MICVDD pin can also be used (instead of MICBIASn) as a reference or power supply for external microphones. The MICBIAS outputs are recommended, as these offer better noise performance and independent enable/disable control.

ANALOGUE LINE INPUT

Line inputs can be connected to the CS47L85 in a similar manner to the microphone inputs described above. Single-ended and differential modes are supported on each of the analogue input paths.

The applicable mode (single-ended or differential) is selected using the IN*nx*_SRC registers, as described later.

The analogue line input configurations are illustrated in Figure 18 and Figure 19. Note that the microphone bias (MICBIAS) is not used for line input connections.

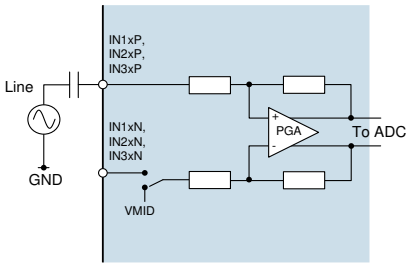


Figure 18 Single-Ended Line Input

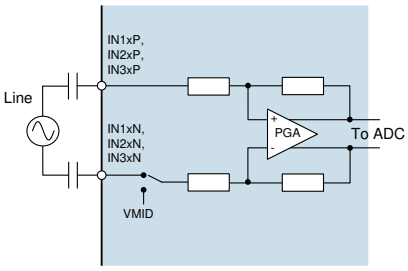


Figure 19 Differential Line Input

DIGITAL MICROPHONE INPUT

Up to 12 digital microphones can be connected to the CS47L85. Digital Microphone (DMIC) operation on Input paths IN1, IN2 and IN3 is selected using the IN*n*_MODE registers, as described later. DMIC operation on Input paths IN4, IN5 and IN6 is implemented on multi-function GPIO pins, which must be configured for the respective DMIC functions when required; see "General Purpose Input / Output" to configure the GPIO pins for DMIC operation.

In digital microphone mode, two channels of audio data are multiplexed on the associated DMICDAT*n* pin. Each stereo digital microphone interface is clocked using the respective DMICCLK*n* pin.

When digital microphone input is enabled, the CS47L85 outputs a clock signal on the applicable DMICCLK*n* pin(s). The DMICCLK*n* frequency is controlled by the respective IN*n*_OSR register, as described in Table 1. See Table 3 for details of the IN*n*_OSR registers.

Note that, if the 384kHz or 768kHz DMICCLKn frequency is selected for one or more of the digital microphone input paths, then the maximum valid Input Path sample rate (all input paths) will be affected as described in Table 1.

Note that the DMICCLK*n* frequencies noted in Table 1 assume that the SYSCLK frequency is a multiple of 6.144MHz (SYSCLK_FRAC=0). If the SYSCLK frequency is a multiple of 5.6448MHz (SYSCLK_FRAC=1), then the DMICCLK*n* frequencies will be scaled accordingly.

CONDITION	DMICCLKn FREQUENCY	VALID SAMPLE RATES	SIGNAL PASSBAND
IN*n*_OSR = 010	384kHz	up to 48kHz	up to 4kHz
IN*n*_OSR = 011	768kHz	up to 96kHz	up to 8kHz
IN*n*_OSR = 100	1.536MHz	up to 192kHz	up to 20kHz
IN*n*_OSR =101	3.072MHz	up to 192kHz	up to 20kHz
IN*n*_OSR =110	6.144MHz	up to 192kHz	up to 96kHz

Table 1 DMICCLK Frequency

The voltage reference for the IN1, IN2 and IN3 digital microphone interfaces is selectable, using the IN*n*_DMIC_SUP registers - each interface may be referenced to MICVDD, or to the MICBIAS1, MICBIAS2 or MICBIAS3 levels. The voltage reference for each digital input path should be set equal to the applicable power supply of the respective microphone(s).

The voltage reference for the IN4, IN5 and IN6 digital microphone interfaces is DBVDD4. The power supply for digital microphones on these input paths (MICBIAS4 is recommended) should be set equal to the DBVDD4 voltage.

A pair of digital microphones is connected as illustrated in Figure 20. The microphones must be configured to ensure that the Left mic transmits a data bit when DMICCLK is high, and the Right mic transmits a data bit when DMICCLK is low. The CS47L85 samples the digital microphone data at the end of each DMICCLK phase. Each microphone must tri-state its data output when the other microphone is transmitting.

Note that the CS47L85 provides integrated pull-down resistors on the DMICDAT*n* pins. This provides a flexible capability for interfacing with other devices.

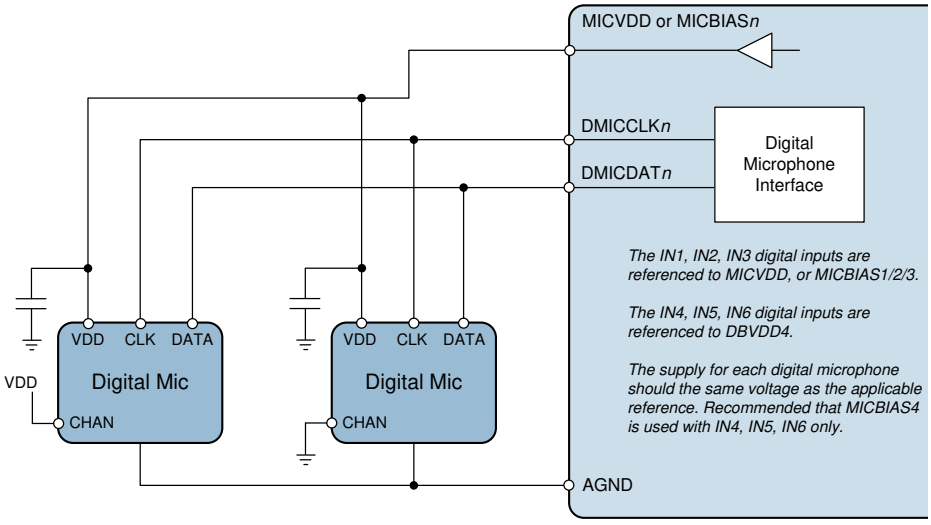


Figure 20 Digital Microphone Input

Two digital microphone channels are interleaved on DMICDAT*n*. The digital microphone interface timing is illustrated in Figure 21. Each microphone must tri-state its data output when the other microphone is transmitting.

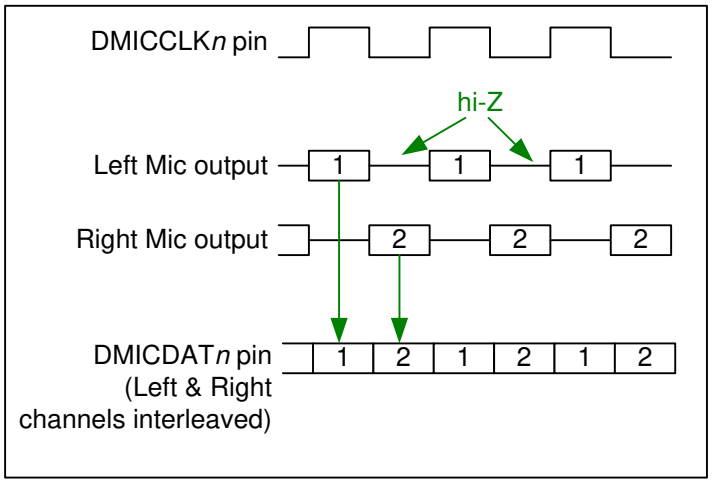


Figure 21 Digital Microphone Interface Timing

When digital microphone input is enabled, the CS47L85 outputs a clock signal on the applicable DMICCLK pin(s). The DMICCLK frequency is selectable, as described in Table 1.

Note that SYSCLK must be present and enabled when using the Digital Microphone inputs; see “Clocking and Sample Rates” for details of SYSCLK and the associated register control fields.

INPUT SIGNAL PATH ENABLE

The input signal paths are enabled using the register bits described in Table 2. The respective bit(s) must be enabled for analogue or digital input on the respective input path(s).

The input signal paths are muted by default. It is recommended that de-selecting the mute should be the final step of the path enable control sequence. Similarly, the mute should be selected as the first step of the path disable control sequence. The input signal path mute functions are controlled using the register bits described in Table 4.

The MICVDD power domain must be enabled when using the analogue input signal path(s). This power domain is provided using an internal Charge Pump (CP2) and LDO Regulator (LDO2). See "Charge Pumps, Regulators and Voltage Reference" for details of these circuits.

The system clock, SYSCLK, must be configured and enabled before any audio path is enabled. The input signal paths should be kept disabled (IN*nx*_ENA=0) if SYSCLK is not enabled. The ASYNCCLK and 32kHz clock may also be required, depending on the path configuration. See "Clocking and Sample Rates" for details of the system clocks (including requirements for reconfiguring SYSCLK while audio paths are enabled).

The CS47L85 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the input signal paths and associated ADCs. If an attempt is made to enable an input signal path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The status bits in Register R769 indicate the status of each of the input signal paths. If an Underclocked Error condition occurs, then these bits provide readback of which input signal path(s) have been successfully enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R768 (0300h) Input_Enables	11	IN6L_ENA	0	Input Path 6 (Left) Enable 0 = Disabled 1 = Enabled
	10	IN6R_ENA	0	Input Path 6 (Right) Enable 0 = Disabled 1 = Enabled
	9	IN5L_ENA	0	Input Path 5 (Left) Enable 0 = Disabled 1 = Enabled
	8	IN5R_ENA	0	Input Path 5 (Right) Enable 0 = Disabled 1 = Enabled
	7	IN4L_ENA	0	Input Path 4 (Left) Enable 0 = Disabled 1 = Enabled
	6	IN4R_ENA	0	Input Path 4 (Right) Enable 0 = Disabled 1 = Enabled
	5	IN3L_ENA	0	Input Path 3 (Left) Enable 0 = Disabled 1 = Enabled
	4	IN3R_ENA	0	Input Path 3 (Right) Enable 0 = Disabled 1 = Enabled
	3	IN2L_ENA	0	Input Path 2 (Left) Enable 0 = Disabled 1 = Enabled
	2	IN2R_ENA	0	Input Path 2 (Right) Enable 0 = Disabled 1 = Enabled
	1	IN1L_ENA	0	Input Path 1 (Left) Enable 0 = Disabled 1 = Enabled
	0	IN1R_ENA	0	Input Path 1 (Right) Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R769 (0301h) Input_Enables_Status	11	IN6L_ENA_STS	0	Input Path 6 (Left) Enable Status 0 = Disabled 1 = Enabled
	10	IN6R_ENA_STS	0	Input Path 6 (Right) Enable Status 0 = Disabled 1 = Enabled
	9	IN5L_ENA_STS	0	Input Path 5 (Left) Enable Status 0 = Disabled 1 = Enabled
	8	IN5R_ENA_STS	0	Input Path 5 (Right) Enable Status 0 = Disabled 1 = Enabled
	7	IN4L_ENA_STS	0	Input Path 4 (Left) Enable Status 0 = Disabled 1 = Enabled
	6	IN4R_ENA_STS	0	Input Path 4 (Right) Enable Status 0 = Disabled 1 = Enabled
	5	IN3L_ENA_STS	0	Input Path 3 (Left) Enable Status 0 = Disabled 1 = Enabled
	4	IN3R_ENA_STS	0	Input Path 3 (Right) Enable Status 0 = Disabled 1 = Enabled
	3	IN2L_ENA_STS	0	Input Path 2 (Left) Enable Status 0 = Disabled 1 = Enabled
	2	IN2R_ENA_STS	0	Input Path 2 (Right) Enable Status 0 = Disabled 1 = Enabled
	1	IN1L_ENA_STS	0	Input Path 1 (Left) Enable Status 0 = Disabled 1 = Enabled
	0	IN1R_ENA_STS	0	Input Path 1 (Right) Enable Status 0 = Disabled 1 = Enabled

Table 2 Input Signal Path Enable

INPUT SIGNAL PATH SAMPLE RATE CONTROL

The input signal paths may be selected as input to the digital mixers or signal processing functions within the CS47L85 digital core. The sample rate for the input signal paths is configured using the IN_RATE register - see Table 22 within the “Digital Core” section.

Note that sample rate conversion is required when routing the input signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

INPUT SIGNAL PATH CONFIGURATION

The CS47L85 supports up to 9 analogue inputs or up to 12 digital inputs. Selectable combinations of analogue (mic or line) and digital inputs are multiplexed into 6 stereo input signal paths.

Input paths IN1, IN2 and IN3 can be configured as single-ended, differential, or digital microphone configuration. The input signal path configuration is selected using the IN*n*_MODE and IN*n*x_SRC registers. Note that input paths IN4, IN5 and IN6 support digital inputs only.

A configurable high pass filter (HPF) is provided on the left and right channels of each input path. The applicable cut-off frequency is selected using the IN_HPF_CUT register. The filter can be enabled on each path independently using the IN*nx*_HPF bits.

The analogue input signal paths (single-ended or differential) each incorporate a PGA to provide gain in the range 0dB to +31dB in 1dB steps. Note that these PGAs do not provide pop suppression functions; it is recommended that the gain should not be adjusted whilst the respective signal path is enabled.

The analogue input PGA gain is controlled using the IN*n*L_PGA_VOL and IN*n*R_PGA_VOL registers. Note that separate volume control is provided for the Left and Right channels of each stereo pair.

When the IN1, IN2 or IN3 input signal path is configured for digital microphone input, the voltage reference for the associated input/output pins is selectable using the IN*n*_DMIC_SUP registers - each interface may be referenced to MICVDD, or to the MICBIAS1, MICBIAS2 or MICBIAS3 levels. The voltage reference for each digital input path should be set equal to the applicable power supply of the respective microphone(s).

The voltage reference for the IN4, IN5 and IN6 digital microphone interfaces is DBVDD4. The power supply for digital microphones on these input paths (MICBIAS4 is recommended) should be set equal to the DBVDD4 voltage.

When the input signal path is configured for digital microphone input, the respective DMICCLKn frequency can be configured using the INn_OSR register bits. Note that, if a digital microphone path is selected as a source for the Rx ANC function (see Table 6), the respective DMICCLKn frequency will be 3.072MHz, regardless of the INn_OSR setting.

A digital delay may be applied to any of the digital microphone input channels. This feature can be used for phase adjustment of any digital input, including directional control of multiple microphones. The delay is controlled using the INnL_DMIC_DLY and INnR_DMIC_DLY registers.

The MICVDD voltage is generated by an internal Charge Pump and LDO Regulator. The MICBIAS1, MICBIAS2 and MICBIAS3 outputs are derived from MICVDD - see “Charge Pumps, Regulators and Voltage Reference”.

The input signal paths are configured using the register bits described in Table 3.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R780 (030Ch) HPF_Control	2:0	IN_HPF_CUT [2:0]	010	Input Path HPF Select Controls the cut-off frequency of the input path HPF circuits. 000 = 2.5Hz 001 = 5Hz 010 = 10Hz 011 = 20Hz 100 = 40Hz All other codes are Reserved
R784 (0310h) IN1L_Control	15	IN1L_HPF	0	Input Path 1 (Left) HPF Enable 0 = Disabled 1 = Enabled
	12:11	IN1_DMIC_SUP [1:0]	00	Input Path 1 DMIC Reference Select (Sets the DMICDAT1 and DMICCLK1 logic levels) 00 = MICVDD 01 = MICBIAS1 10 = MICBIAS2 11 = MICBIAS3
	10	IN1_MODE	00	Input Path 1 Mode 0 = Analogue input 1 = Digital input

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:1	IN1L_PGA_VOL [6:0]	40h	Input Path 1 (Left) PGA Volume (Applicable to analogue inputs only) 00h to 3Fh = Reserved 40h = 0dB 41h = 1dB 42h = 2dB … (1dB steps) 5F = 31dB 60h to 7Fh = Reserved
R785 (0311h) ADC_Digital_Volume_1L	14:13	IN1L_SRC [1:0]	00	Input Path 1 (Left) Source 00 = Differential (IN1ALP - IN1ALN) 01 = Single-ended (IN1ALP) 10 = Differential (IN1BP-IN1BN) 11 = Single-ended (IN1BP)
R786 (0312h) DMIC1L_Control	10:8	IN1_OSR [2:0]	101	Input Path 1 DMIC Oversample Rate When digital microphone input is selected (IN1_MODE=1), this field controls the sample rate as below: 000 = Reserved 001 = Reserved 010 = 384kHz 011 = 768kHz 100 = 1.536MHz 101 = 3.072MHz 110 = 6.144MHz 111 = Reserved When IN1_OSR=010 or 011, then the maximum Input Path sample rate (all input paths) is 48kHz or 96kHz respectively. If Input Path 1 DMIC is selected as a source for the Rx ANC function, the DMICCLK1 frequency will be set to 3.072MHz.
	5:0	IN1L_DMIC_DLY [5:0]	00h	Input Path 1 (Left) Digital Delay (Applicable to digital input only) LSB = 1 sample, Range is 0 to 63. (Sample rate is controlled by IN1_OSR.)
R788 (0314h) IN1R_Control	15	IN1R_HPF	0	Input Path 1 (Right) HPF Enable 0 = Disabled 1 = Enabled
	7:1	IN1R_PGA_VOL [6:0]	40h	Input Path 1 (Right) PGA Volume (Applicable to analogue inputs only) 00h to 3Fh = Reserved 40h = 0dB 41h = 1dB 42h = 2dB … (1dB steps) 5F = 31dB 60h to 7Fh = Reserved
R789 (0315h) ADC_Digital_Volume_1R	14:13	IN1R_SRC [1:0]	00	Input Path 1 (Right) Source 00 = Differential (IN1RP - IN1RN) 01 = Single-ended (IN1RP) 10 = Reserved 11 = Reserved
R790 (0316h) DMIC1R_Control	5:0	IN1R_DMIC_DLY [5:0]	00h	Input Path 1 (Right) Digital Delay (Applicable to digital input only) LSB = 1 sample, Range is 0 to 63. (Sample rate is controlled by IN1_OSR.)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R792 (0318h) IN2L_Control	15	IN2L_HPF	0	Input Path 2 (Left) HPF Enable 0 = Disabled 1 = Enabled
	12:11	IN2_DMIC_SUP [1:0]	00	Input Path 2 DMIC Reference Select (Sets the DMICDAT2 and DMICCLK2 logic levels) 00 = MICVDD 01 = MICBIAS1 10 = MICBIAS2 11 = MICBIAS3
	10	IN2_MODE	00	Input Path 2 Mode 0 = Analogue input 1 = Digital input
	7:1	IN2L_PGA_VOL [6:0]	40h	Input Path 2 (Left) PGA Volume (Applicable to analogue inputs only) 00h to 3Fh = Reserved 40h = 0dB 41h = 1dB 42h = 2dB … (1dB steps) 5F = 31dB 60h to 7Fh = Reserved
R793 (0319h) ADC_Digital_Volume_2L	14:13	IN2L_SRC [1:0]	00	Input Path 2 (Left) Source 00 = Differential (IN2ALP - IN2ALN) 01 = Single-ended (IN2ALP) 10 = Differential (IN2BLP-IN2BLN) 11 = Single-ended (IN2BLP)
R794 (031Ah) DMIC2L_Control	10:8	IN2_OSR [2:0]	101	Input Path 2 DMIC Oversample Rate When digital microphone input is selected (IN2_MODE=1), this field controls the sample rate as below: 000 = Reserved 001 = Reserved 010 = 384kHz 011 = 768kHz 100 = 1.536MHz 101 = 3.072MHz 110 = 6.144MHz 111 = Reserved When IN2_OSR=010 or 011, then the maximum Input Path sample rate (all input paths) is 48kHz or 96kHz respectively. If Input Path 2 DMIC is selected as a source for the Rx ANC function, the DMICCLK2 frequency will be set to 3.072MHz.
	5:0	IN2L_DMIC_DLY [5:0]	00h	Input Path 2 (Left) Digital Delay (Applicable to digital input only) LSB = 1 sample, Range is 0 to 63. (Sample rate is controlled by IN2_OSR.)
R796 (031Ch) IN2R_Con	15	IN2R_HPF	0	Input Path 2 (Right) HPF Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
trol	7:1	IN2R_PGA_VOL [6:0]	40h	Input Path 2 (Right) PGA Volume (Applicable to analogue inputs only) 00h to 3Fh = Reserved 40h = 0dB 41h = 1dB 42h = 2dB … (1dB steps) 5F = 31dB 60h to 7Fh = Reserved
R797 (0319h) ADC_Digital_Volume_2R	14:13	IN2R_SRC [1:0]	00	Input Path 2 (Right) Source 00 = Differential (IN2ARP - IN2ARN) 01 = Single-ended (IN2ARP) 10 = Reserved 11 = Single-ended (IN2BR)
R798 (031Eh) DMIC2R_Control	5:0	IN2R_DMIC_DLY [5:0]	00h	Input Path 2 (Right) Digital Delay (Applicable to digital input only) LSB = 1 sample, Range is 0 to 63. (Sample rate is controlled by IN2_OSR.)
R800 (0320h) IN3L_Control	15	IN3L_HPF	0	Input Path 3 (Left) HPF Enable 0 = Disabled 1 = Enabled
	12:11	IN3_DMIC_SUP [1:0]	00	Input Path 3 DMIC Reference Select (Sets the DMICDAT3 and DMICCLK3 logic levels) 00 = MICVDD 01 = MICBIAS1 10 = MICBIAS2 11 = MICBIAS3
	10	IN3_MODE	00	Input Path 3 Mode 0 = Analogue input 1 = Digital input
	7:1	IN3L_PGA_VOL [6:0]	40h	Input Path 3 (Left) PGA Volume (Applicable to analogue inputs only) 00h to 3Fh = Reserved 40h = 0dB 41h = 1dB 42h = 2dB … (1dB steps) 5F = 31dB 60h to 7Fh = Reserved
R801 (0321h) ADC_Digital_Volume_3L	14:13	IN3L_SRC [1:0]	00	Input Path 3 (Left) Source 00 = Differential (IN3LP - IN3LN) 01 = Single-ended (IN3LP) 10 = Reserved 11 = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R802 (0322h) DMIC3L_ Control	10:8	IN3_OSR [2:0]	101	Input Path 3 DMIC Oversample Rate When digital microphone input is selected (IN3_MODE=1), this field controls the sample rate as below: 000 = Reserved 001 = Reserved 010 = 384kHz 011 = 768kHz 100 = 1.536MHz 101 = 3.072MHz 110 = 6.144MHz 111 = Reserved When IN3_OSR=010 or 011, then the maximum Input Path sample rate (all input paths) is 48kHz or 96kHz respectively. If Input Path 3 DMIC is selected as a source for the Rx ANC function, the DMICCLK3 frequency will be set to 3.072MHz.
	5:0	IN3L_DMIC_DLY [5:0]	00h	Input Path 3 (Left) Digital Delay (Applicable to digital input only) LSB = 1 sample, Range is 0 to 63. (Sample rate is controlled by IN3_OSR.)
R804 (0324h) IN3R_Con trol	15	IN3R_HPF	0	Input Path 3 (Right) HPF Enable 0 = Disabled 1 = Enabled
	7:1	IN3R_PGA_VOL [6:0]	40h	Input Path 3 (Right) PGA Volume (Applicable to analogue inputs only) 00h to 3Fh = Reserved 40h = 0dB 41h = 1dB 42h = 2dB … (1dB steps) 5F = 31dB 60h to 7Fh = Reserved
R805 (0325h) ADC_Digit al_Volume _3R	14:13	IN3R_SRC [1:0]	00	Input Path 3 (Right) Source 00 = Differential (IN3RP - IN3RN) 01 = Single-ended (IN3RP) 10 = Reserved 11 = Reserved
R806 (0326h) DMIC3R_ Control	5:0	IN3R_DMIC_DLY [5:0]	00h	Input Path 3 (Right) Digital Delay (Applicable to digital input only) LSB = 1 sample, Range is 0 to 63. (Sample rate is controlled by IN3_OSR.)
R808 (0328h) IN4L_Cont rol	15	IN4L_HPF	0	Input Path 4 (Left) HPF Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R810 (032Ah) DMIC4L_ Control	10:8	IN4_OSR [2:0]	101	Input Path 4 DMIC Oversample Rate Controls the DMIC4 sample rate as below: 000 = Reserved 001 = Reserved 010 = 384kHz 011 = 768kHz 100 = 1.536MHz 101 = 3.072MHz 110 = 6.144MHz 111 = Reserved When IN4_OSR=010 or 011, then the maximum Input Path sample rate (all input paths) is 48kHz or 96kHz respectively. If Input Path 4 DMIC is selected as a source for the Rx ANC function, the DMICCLK4 frequency will be set to 3.072MHz.
	5:0	IN4L_DMIC_DLY [5:0]	00h	Input Path 4 (Left) Digital Delay (Applicable to digital input only) LSB = 1 sample, Range is 0 to 63. (Sample rate is controlled by IN4_OSR.)
R812 (032Ch) IN4R_Con trol	15	IN4R_HPF	0	Input Path 4 (Right) HPF Enable 0 = Disabled 1 = Enabled
R814 (032Eh) DMIC4R_ Control	5:0	IN4R_DMIC_DLY [5:0]	00h	Input Path 4 (Right) Digital Delay (Applicable to digital input only) LSB = 1 sample, Range is 0 to 63. (Sample rate is controlled by IN4_OSR.)
R816 (0330h) IN5L_Cont rol	15	IN5L_HPF	0	Input Path 5 (Left) HPF Enable 0 = Disabled 1 = Enabled
R818 (0332h) DMIC5L_ Control	10:8	IN5_OSR [2:0]	101	Input Path 5 DMIC Oversample Rate Controls the DMIC5 sample rate as below: 000 = Reserved 001 = Reserved 010 = 384kHz 011 = 768kHz 100 = 1.536MHz 101 = 3.072MHz 110 = 6.144MHz 111 = Reserved When IN5_OSR=010 or 011, then the maximum Input Path sample rate (all input paths) is 48kHz or 96kHz respectively. If Input Path 5 DMIC is selected as a source for the Rx ANC function, the DMICCLK5 frequency will be set to 3.072MHz.
	5:0	IN5L_DMIC_DLY [5:0]	00h	Input Path 5 (Left) Digital Delay (Applicable to digital input only) LSB = 1 sample, Range is 0 to 63. (Sample rate is controlled by IN5_OSR.)
R820 (0334h) IN5R_Con trol	15	IN5R_HPF	0	Input Path 5 (Right) HPF Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R822 (0336h) DMIC5R_ Control	5:0	IN5R_DMIC_DLY [5:0]	00h	Input Path 5 (Right) Digital Delay (Applicable to digital input only) LSB = 1 sample, Range is 0 to 63. (Sample rate is controlled by IN5_OSR.)
R824 (0338h) IN6L_Cont rol	15	IN6L_HPF	0	Input Path 6 (Left) HPF Enable 0 = Disabled 1 = Enabled
R826 (033Ah) DMIC6L_ Control	10:8	IN6_OSR [2:0]	101	Input Path 6 DMIC Oversample Rate Controls the DMIC6 sample rate as below: 000 = Reserved 001 = Reserved 010 = 384kHz 011 = 768kHz 100 = 1.536MHz 101 = 3.072MHz 110 = 6.144MHz 111 = Reserved When IN6_OSR=010 or 011, then the maximum Input Path sample rate (all input paths) is 48kHz or 96kHz respectively. If Input Path 6 DMIC is selected as a source for the Rx ANC function, the DMICCLK6 frequency will be set to 3.072MHz.
	5:0	IN6L_DMIC_DLY [5:0]	00h	Input Path 6 (Left) Digital Delay (Applicable to digital input only) LSB = 1 sample, Range is 0 to 63. (Sample rate is controlled by IN6_OSR.)
R828 (033Ch) IN6R_Con trol	15	IN6R_HPF	0	Input Path 6 (Right) HPF Enable 0 = Disabled 1 = Enabled
R830 (033Eh) DMIC6R_ Control	5:0	IN6R_DMIC_DLY [5:0]	00h	Input Path 6 (Right) Digital Delay (Applicable to digital input only) LSB = 1 sample, Range is 0 to 63. (Sample rate is controlled by IN6_OSR.)

Table 3 Input Signal Path Configuration

INPUT SIGNAL PATH DIGITAL VOLUME CONTROL

A digital volume control is provided on each of the input signal paths, providing -64dB to +31.5dB gain control in 0.5dB steps. An independent mute control is also provided for each input signal path.

Whenever the gain or mute setting is changed, the signal path gain is ramped up or down to the new settings at a programmable rate. For increasing gain (or un-mute), the rate is controlled by the IN_VI_RAMP register. For decreasing gain (or mute), the rate is controlled by the IN_VD_RAMP register. Note that the IN_VI_RAMP and IN_VD_RAMP registers should not be changed while a volume ramp is in progress.

The IN_VU bits control the loading of the input signal path digital volume and mute controls. When IN_VU is set to 0, the digital volume and mute settings will be loaded into the respective control register, but will not actually change the signal path gain. The digital volume and mute settings on all of the input signal paths are updated when a 1 is written to IN_VU. This makes it possible to update the gain of multiple signal paths simultaneously.

Note that, although the digital volume control registers provide 0.5dB steps, the internal circuits provide signal gain adjustment in 0.125dB steps. This allows a very high degree of gain control, and smooth volume ramping under all operating conditions.

The 0dBFS level of the IN1-IN6 digital input paths is not equal to the 0dBFS level of the CS47L85 digital core. The maximum digital input signal level is -6dBFS (see “Electrical Characteristics”). Under 0dBFS gain conditions, a -6dBFS input signal corresponds to a 0dBFS input to the CS47L85 digital core functions.

The digital volume control register fields are described in Table 4 and Table 5.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R777 (0309h) Input_Volume_Ramp	6:4	IN_VD_RAMP [2:0]	010	Input Volume Decreasing Ramp Rate (seconds/6dB) 000 = 0ms 001 = 0.5ms 010 = 1ms 011 = 2ms 100 = 4ms 101 = 8ms 110 = 15ms 111 = 30ms This register should not be changed while a volume ramp is in progress.
	2:0	IN_VI_RAMP [2:0]	010	Input Volume Increasing Ramp Rate (seconds/6dB) 000 = 0ms 001 = 0.5ms 010 = 1ms 011 = 2ms 100 = 4ms 101 = 8ms 110 = 15ms 111 = 30ms This register should not be changed while a volume ramp is in progress.
R785 (0311h) ADC_Digital_Volume_1L	9	IN_VU		Input Signal Paths Volume and Mute Update Writing a 1 to this bit will cause the Input Signal Paths Volume and Mute settings to be updated simultaneously
	8	IN1L_MUTE	1	Input Path 1 (Left) Digital Mute 0 = Un-mute 1 = Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	IN1L_VOL [7:0]	80h	Input Path 1 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 5 for volume range)
R789 (0315h) ADC_Digital_Volume_1R	9	IN_VU		Input Signal Paths Volume and Mute Update Writing a 1 to this bit will cause the Input Signal Paths Volume and Mute settings to be updated simultaneously
	8	IN1R_MUTE	1	Input Path 1 (Right) Digital Mute 0 = Un-mute 1 = Mute
	7:0	IN1R_VOL [7:0]	80h	Input Path 1 (Right) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 5 for volume range)
R793 (0319h) ADC_Digital_Volume_2L	9	IN_VU		Input Signal Paths Volume and Mute Update Writing a 1 to this bit will cause the Input Signal Paths Volume and Mute settings to be updated simultaneously
	8	IN2L_MUTE	1	Input Path 2 (Left) Digital Mute 0 = Un-mute 1 = Mute
	7:0	IN2L_VOL [7:0]	80h	Input Path 2 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 5 for volume range)
R797 (031Dh) ADC_Digital_Volume_2R	9	IN_VU		Input Signal Paths Volume and Mute Update Writing a 1 to this bit will cause the Input Signal Paths Volume and Mute settings to be updated simultaneously
	8	IN2R_MUTE	1	Input Path 2 (Right) Digital Mute 0 = Un-mute 1 = Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	IN2R_VOL [7:0]	80h	Input Path 2 (Right) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 5 for volume range)
R801 (0321h) ADC_Digital_Volume_3L	9	IN_VU		Input Signal Paths Volume and Mute Update Writing a 1 to this bit will cause the Input Signal Paths Volume and Mute settings to be updated simultaneously
	8	IN3L_MUTE	1	Input Path 3 (Left) Digital Mute 0 = Un-mute 1 = Mute
	7:0	IN3L_VOL [7:0]	80h	Input Path 3 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 5 for volume range)
R805 (0325h) ADC_Digital_Volume_3R	9	IN_VU		Input Signal Paths Volume and Mute Update Writing a 1 to this bit will cause the Input Signal Paths Volume and Mute settings to be updated simultaneously
	8	IN3R_MUTE	1	Input Path 3 (Right) Digital Mute 0 = Un-mute 1 = Mute
	7:0	IN3R_VOL [7:0]	80h	Input Path 3 (Right) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 5 for volume range)
R809 (0329h) ADC_Digital_Volume_4L	9	IN_VU		Input Signal Paths Volume and Mute Update Writing a 1 to this bit will cause the Input Signal Paths Volume and Mute settings to be updated simultaneously
	8	IN4L_MUTE	1	Input Path 4 (Left) Digital Mute 0 = Un-mute 1 = Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	IN4L_VOL [7:0]	80h	Input Path 4 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 5 for volume range)
R813 (032Dh) ADC_Digital_Volume_4R	9	IN_VU		Input Signal Paths Volume and Mute Update Writing a 1 to this bit will cause the Input Signal Paths Volume and Mute settings to be updated simultaneously
	8	IN4R_MUTE	1	Input Path 4 (Right) Digital Mute 0 = Un-mute 1 = Mute
	7:0	IN4R_VOL [7:0]	80h	Input Path 4 (Right) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 5 for volume range)
R817 (0331h) ADC_Digital_Volume_5L	9	IN_VU		Input Signal Paths Volume and Mute Update Writing a 1 to this bit will cause the Input Signal Paths Volume and Mute settings to be updated simultaneously
	8	IN5L_MUTE	1	Input Path 5 (Left) Digital Mute 0 = Un-mute 1 = Mute
	7:0	IN5L_VOL [7:0]	80h	Input Path 5 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 5 for volume range)
R821 (0335h) ADC_Digital_Volume_5R	9	IN_VU		Input Signal Paths Volume and Mute Update Writing a 1 to this bit will cause the Input Signal Paths Volume and Mute settings to be updated simultaneously
	8	IN5R_MUTE	1	Input Path 5 (Right) Digital Mute 0 = Un-mute 1 = Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	IN5R_VOL [7:0]	80h	Input Path 5 (Right) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 5 for volume range)
R825 (0339h) ADC_Digital_Volume_6L	9	IN_VU		Input Signal Paths Volume and Mute Update Writing a 1 to this bit will cause the Input Signal Paths Volume and Mute settings to be updated simultaneously
	8	IN6L_MUTE	1	Input Path 6 (Left) Digital Mute 0 = Un-mute 1 = Mute
	7:0	IN6L_VOL [7:0]	80h	Input Path 6 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 5 for volume range)
R829 (033Dh) ADC_Digital_Volume_6R	9	IN_VU		Input Signal Paths Volume and Mute Update Writing a 1 to this bit will cause the Input Signal Paths Volume and Mute settings to be updated simultaneously
	8	IN6R_MUTE	1	Input Path 6 (Right) Digital Mute 0 = Un-mute 1 = Mute
	7:0	IN6R_VOL [7:0]	80h	Input Path 6 (Right) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 5 for volume range)

Table 4 Input Signal Path Digital Volume Control

Input Volume Register	Volume (dB)	Input Volume Register	Volume (dB)	Input Volume Register	Volume (dB)	Input Volume Register	Volume (dB)
00h	-64.0	40h	-32.0	80h	0.0	C0h	Reserved
01h	-63.5	41h	-31.5	81h	0.5	C1h	Reserved
02h	-63.0	42h	-31.0	82h	1.0	C2h	Reserved
03h	-62.5	43h	-30.5	83h	1.5	C3h	Reserved
04h	-62.0	44h	-30.0	84h	2.0	C4h	Reserved
05h	-61.5	45h	-29.5	85h	2.5	C5h	Reserved
06h	-61.0	46h	-29.0	86h	3.0	C6h	Reserved
07h	-60.5	47h	-28.5	87h	3.5	C7h	Reserved
08h	-60.0	48h	-28.0	88h	4.0	C8h	Reserved
09h	-59.5	49h	-27.5	89h	4.5	C9h	Reserved
0Ah	-59.0	4Ah	-27.0	8Ah	5.0	CAh	Reserved
0Bh	-58.5	4Bh	-26.5	8Bh	5.5	CBh	Reserved
0Ch	-58.0	4Ch	-26.0	8Ch	6.0	CCh	Reserved
0Dh	-57.5	4Dh	-25.5	8Dh	6.5	CDh	Reserved
0Eh	-57.0	4Eh	-25.0	8Eh	7.0	CEh	Reserved
0Fh	-56.5	4Fh	-24.5	8Fh	7.5	CFh	Reserved
10h	-56.0	50h	-24.0	90h	8.0	D0h	Reserved
11h	-55.5	51h	-23.5	91h	8.5	D1h	Reserved
12h	-55.0	52h	-23.0	92h	9.0	D2h	Reserved
13h	-54.5	53h	-22.5	93h	9.5	D3h	Reserved
14h	-54.0	54h	-22.0	94h	10.0	D4h	Reserved
15h	-53.5	55h	-21.5	95h	10.5	D5h	Reserved
16h	-53.0	56h	-21.0	96h	11.0	D6h	Reserved
17h	-52.5	57h	-20.5	97h	11.5	D7h	Reserved
18h	-52.0	58h	-20.0	98h	12.0	D8h	Reserved
19h	-51.5	59h	-19.5	99h	12.5	D9h	Reserved
1Ah	-51.0	5Ah	-19.0	9Ah	13.0	DAh	Reserved
1Bh	-50.5	5Bh	-18.5	9Bh	13.5	DBh	Reserved
1Ch	-50.0	5Ch	-18.0	9Ch	14.0	DCh	Reserved
1Dh	-49.5	5Dh	-17.5	9Dh	14.5	DDh	Reserved
1Eh	-49.0	5Eh	-17.0	9Eh	15.0	DEh	Reserved
1Fh	-48.5	5Fh	-16.5	9Fh	15.5	DFh	Reserved
20h	-48.0	60h	-16.0	A0h	16.0	E0h	Reserved
21h	-47.5	61h	-15.5	A1h	16.5	E1h	Reserved
22h	-47.0	62h	-15.0	A2h	17.0	E2h	Reserved
23h	-46.5	63h	-14.5	A3h	17.5	E3h	Reserved
24h	-46.0	64h	-14.0	A4h	18.0	E4h	Reserved
25h	-45.5	65h	-13.5	A5h	18.5	E5h	Reserved
26h	-45.0	66h	-13.0	A6h	19.0	E6h	Reserved
27h	-44.5	67h	-12.5	A7h	19.5	E7h	Reserved
28h	-44.0	68h	-12.0	A8h	20.0	E8h	Reserved
29h	-43.5	69h	-11.5	A9h	20.5	E9h	Reserved
2Ah	-43.0	6Ah	-11.0	AAh	21.0	EAh	Reserved
2Bh	-42.5	6Bh	-10.5	ABh	21.5	EBh	Reserved
2Ch	-42.0	6Ch	-10.0	ACh	22.0	ECh	Reserved
2Dh	-41.5	6Dh	-9.5	ADh	22.5	EDh	Reserved
2Eh	-41.0	6Eh	-9.0	AEh	23.0	EEh	Reserved
2Fh	-40.5	6Fh	-8.5	AFh	23.5	EFh	Reserved
30h	-40.0	70h	-8.0	B0h	24.0	F0h	Reserved
31h	-39.5	71h	-7.5	B1h	24.5	F1h	Reserved
32h	-39.0	72h	-7.0	B2h	25.0	F2h	Reserved
33h	-38.5	73h	-6.5	B3h	25.5	F3h	Reserved
34h	-38.0	74h	-6.0	B4h	26.0	F4h	Reserved
35h	-37.5	75h	-5.5	B5h	26.5	F5h	Reserved
36h	-37.0	76h	-5.0	B6h	27.0	F6h	Reserved
37h	-36.5	77h	-4.5	B7h	27.5	F7h	Reserved
38h	-36.0	78h	-4.0	B8h	28.0	F8h	Reserved
39h	-35.5	79h	-3.5	B9h	28.5	F9h	Reserved
3Ah	-35.0	7Ah	-3.0	BAh	29.0	FAh	Reserved
3Bh	-34.5	7Bh	-2.5	BBh	29.5	FBh	Reserved
3Ch	-34.0	7Ch	-2.0	BCh	30.0	FCh	Reserved
3Dh	-33.5	7Dh	-1.5	BDh	30.5	FDh	Reserved
3Eh	-33.0	7Eh	-1.0	BEh	31.0	FEh	Reserved
00.	-32.5	7Fh	-0.5	BFh	31.5	FFh	Reserved

Table 5 Input Signal Path Digital Volume Range

INPUT SIGNAL PATH ANC CONTROL

The CS47L85 incorporates a stereo Ambient Noise Cancellation (ANC) processor which can provide noise reduction in a variety of different operating conditions.

The Left and Right ANC input sources for the Receive Path ANC function are selected using the IN_RXANCL_SEL and IN_RXANCR_SEL registers, as described in Table 6.

See “Ambient Noise Cancellation” for further details of the ANC function.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3841 (0F01h) ANC_SRC	6:4	IN_RXANCR_SEL [2:0]	000	Right Input source for Rx ANC function 000 = No selection 001 = Input Path 1 010 = Input Path 2 011 = Input Path 3 100 = Input Path 4 101 = Input Path 5 110 = Input Path 6 111 = Reserved
	2:0	IN_RXANCL_SEL [2:0]	000	Left Input source for Rx ANC function 000 = No selection 001 = Input Path 1 010 = Input Path 2 011 = Input Path 3 100 = Input Path 4 101 = Input Path 5 110 = Input Path 6 111 = Reserved

Table 6 Input Signal Paths ANC Control

DIGITAL MICROPHONE PIN CONFIGURATION

Digital Microphone (DMIC) operation on Input paths IN1, IN2 and IN3 is selected using the IN*n*_MODE registers, as described in Table 3. When DMIC is selected, the respective DMICCLKn and DMICDATn pins are configured as digital outputs and inputs respectively.

DMIC operation on Input paths IN4, IN5 and IN6 is implemented on multi-function GPIO pins, which must be configured for the respective DMIC functions when required. The DMIC connections are pin-specific alternative functions on specific GPIO pins. See “General Purpose Input / Output” to configure the GPIO pins for DMIC operation.

The CS47L85 provides integrated pull-down resistors on each of the DMICDATn pins. This provides a flexible capability for interfacing with other devices.

The DMICDAT1, DMICDAT2 and DMICDAT3 pull-down resistors can be configured independently using the register bits described in Table 7. Note that, if the DMICDATn digital microphone input paths are disabled, then the pull-down will be disabled on the respective pin.

In the case of the DMIC4, DMIC5 and DMIC6 interfaces, integrated pull-up and pull-down resistors are provided as part of the GPIO functionality, and can be configured using the register bits described in Table 94.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R840 (0348h) Dig_Mic_Pad_Ctrl	2	DMICDAT3_PD	0	DMICDAT3 Pull-Down Control 0 = Disabled 1 = Enabled
	1	DMICDAT2_PD	0	DMICDAT2 Pull-Down Control 0 = Disabled 1 = Enabled
	0	DMICDAT1_PD	0	DMICDAT1 Pull-Down Control 0 = Disabled 1 = Enabled

Table 7 Digital Microphone Interface Pull-Down Control

DIGITAL CORE

The CS47L85 digital core provides extensive mixing and processing capabilities for multiple signal paths. The configuration is highly flexible, and virtually every conceivable input/output connection can be supported between the available processing blocks.

The digital core provides parametric equalisation (EQ) functions, dynamic range control (DRC), low-pass / high-pass filters (LHPF), and programmable DSP capability. The DSP can support functions such as wind noise, side-tone or other programmable filters, also dynamic range control and compression, or virtual surround sound and other audio enhancements.

The CS47L85 supports multiple signal paths through the digital core. Stereo full-duplex sample rate conversion is provided to allow digital audio to be routed between input (ADC) paths, output (DAC) paths, Digital Audio Interfaces (AIF1, AIF2, AIF3 and AIF4) and SLIMbus paths operating at different sample rates and/or referenced to asynchronous clock domains.

The DSP functions are highly programmable, using application-specific control sequences. It should be noted that the DSP configuration data is lost whenever the DCVDD power domain is removed; the DSP configuration data must be downloaded to the CS47L85 each time the device is powered up.

The procedure for configuring the CS47L85 DSP functions is tailored to each customer's application; please contact your local Cirrus Logic representative for more details.

The digital core incorporates a S/PDIF transmitter, which can provide a stereo S/PDIF output on a GPIO pin. Standard S/PDIF sample rates of 32kHz up to 192kHz can be supported.

The CS47L85 incorporates two 1kHz tone generators which can be used for 'beep' functions through any of the audio signal paths. A white noise generator is incorporated, to provide 'comfort noise' in cases where silence (digital mute) is not desirable.

A haptic signal generator is provided, for use with external haptic devices (e.g., mechanical vibration actuators). Two Pulse Width Modulation (PWM) signal generators are also provided; the PWM waveforms can be modulated by an audio source within the digital core, and can be output on a GPIO pin.

The CS47L85 also incorporates the Cirrus Logic Ambient Noise Cancellation (ANC) functionality; note that this is described in a separate section, see "Ambient Noise Cancellation".

An overview of the digital core mixing and signal processing functions is provided in Figure 22.

The control registers associated with the digital core signal paths are shown in Figure 23 through to Figure 39. The full list of digital mixer control registers (Register R1600 through to R3192) is provided in a separate document - see "Register Map" for further information. Generic register definitions are provided in Table 8.

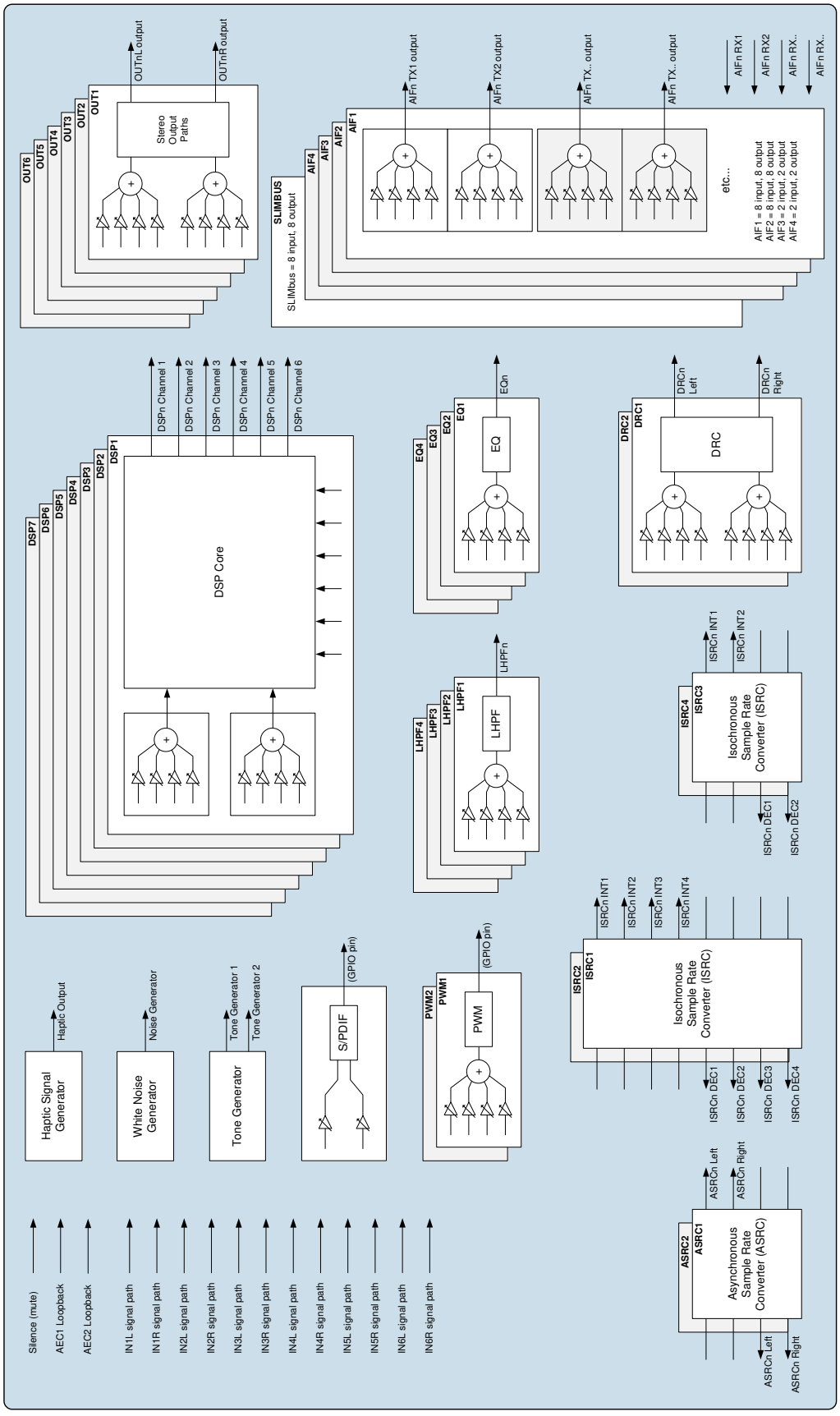


Figure 22 Digital Core

DIGITAL CORE MIXERS

The CS47L85 provides an extensive digital mixing capability. The digital core mixing and signal processing blocks are illustrated in Figure 22.

A 4-input digital mixer is associated with many of these functions, as illustrated. The digital mixer circuit is identical in each instance, providing up to 4 selectable input sources, with independent volume control on each input.

The control registers associated with the digital core signal paths are shown in Figure 23 through to Figure 39. The full list of digital mixer control registers (Register R1600 through to R3192) is provided in a separate document - see “Register Map” for further information.

Further description of the associated control registers is provided below. Generic register definitions are provided in Table 8.

The digital mixer input sources are selected using the associated *_SRC*n* registers; the volume control is implemented via the associated *_VOL*n* registers.

The ASRC, ISRC, and DSP Aux Input functions support selectable input sources, but do not incorporate any digital mixing. The respective input source (*_SRC*n*) registers are identical to those of the digital mixers.

The *_SRC*n* registers select the input source(s) for the respective mixer or signal processing block. Note that the selected input source(s) must be configured for the same sample rate as the block(s) to which they are connected. Sample rate conversion functions are available to support flexible interconnectivity - see “Asynchronous Sample Rate Converter (ASRC)” and “Isochronous Sample Rate Converter (ISRC)”.

The *_SRC*n* registers for all digital core functions should be held at 00h if SYSCLK is not enabled – SYSCLK must be present and enabled before selecting other values for these registers. See “Clocking and Sample Rates” for further details (including requirements for reconfiguring SYSCLK while digital core mixers are enabled).

A status bit associated with each of the configurable input sources provides readback for the respective signal path. If an Underclocked Error condition occurs, then these bits provide readback of which signal path(s) have been successfully enabled.

The generic register definition for the digital mixers is provided in Table 8.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1600 (0640h) to R3192 (0C78h)	15	*_STSn Valid for every digital core function input (digital mixers, DSP Aux inputs, ASRC & ISRC inputs).	0	[Digital Core function] input *n* status 0 = Disabled 1 = Enabled
	7:1	*_VOLn Valid for every digital mixer input.	40h	[Digital Core mixer] input *n* volume -32dB to +16dB in 1dB steps 00h to 20h = -32dB 21h = -31dB 22h = -30dB ... (1dB steps) 40h = 0dB ... (1dB steps) 50h = +16dB 51h to 7Fh = +16dB
	7:0	*_SRCn Valid for every digital core function input (digital mixers, DSP Aux inputs, ASRC & ISRC inputs).	00h	[Digital Core function] input *n* source select 00h = Silence (mute) 04h = Tone generator 1 05h = Tone generator 2 06h = Haptic generator 08h = AEC loopback 1 09h = AEC loopback 2 0Dh = Noise generator 10h = IN1L signal path 11h = IN1R signal path 12h = IN2L signal path 13h = IN2R signal path 14h = IN3L signal path 15h = IN3R signal path 16h = IN4L signal path 17h = IN4R signal path 18h = IN5L signal path 19h = IN5R signal path 1Ah = IN6L signal path 1Bh = IN6R signal path 20h = AIF1 RX1 21h = AIF1 RX2 22h = AIF1 RX3 23h = AIF1 RX4 24h = AIF1 RX5 25h = AIF1 RX6 26h = AIF1 RX7 27h = AIF1 RX8 28h = AIF2 RX1 29h = AIF2 RX2 2Ah = AIF2 RX3 2Bh = AIF2 RX4 2Ch = AIF2 RX5 2Dh = AIF2 RX6 2Eh = AIF2 RX7 2Fh = AIF2 RX8 30h = AIF3 RX1 31h = AIF3 RX2 34h = AIF4 RX1 35h = AIF4 RX2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				38h = SLIMbus RX1 39h = SLIMbus RX2 3Ah = SLIMbus RX3 3Bh = SLIMbus RX4 3Ch = SLIMbus RX5 3Dh = SLIMbus RX6 3Eh = SLIMbus RX7 3Fh = SLIMbus RX8 50h = EQ1 51h = EQ2 52h = EQ3 53h = EQ4 58h = DRC1 Left 59h = DRC1 Right 5Ah = DRC2 Left 5Bh = DRC2 Right 60h = LHPF1 61h = LHPF2 62h = LHPF3 63h = LHPF4 68h = DSP1 channel 1 69h = DSP1 channel 2 6Ah = DSP1 channel 3 6Bh = DSP1 channel 4 6Ch = DSP1 channel 5 6Dh = DSP1 channel 6 70h = DSP2 channel 1 71h = DSP2 channel 2 72h = DSP2 channel 3 73h = DSP2 channel 4 74h = DSP2 channel 5 75h = DSP2 channel 6 78h = DSP3 channel 1 79h = DSP3 channel 2 7Ah = DSP3 channel 3 7Bh = DSP3 channel 4 7Ch = DSP3 channel 5 7Dh = DSP3 channel 6 80h = DSP4 channel 1 81h = DSP4 channel 2 82h = DSP4 channel 3 83h = DSP4 channel 4 84h = DSP4 channel 5 85h = DSP4 channel 6 88h = DSP5 channel 1 89h = DSP5 channel 2 8Ah = DSP5 channel 3 8Bh = DSP5 channel 4 8Ch = DSP5 channel 5 8Dh = DSP5 channel 6 90h = ASRC1 IN1 Left 91h = ASRC1 IN1 Right 92h = ASRC1 IN2 Left 93h = ASRC1 IN2 Right 94h = ASRC2 IN1 Left 95h = ASRC2 IN1 Right 96h = ASRC2 IN2 Left 97h = ASRC2 IN2 Right A0h = ISRC1 INT1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				A1h = ISRC1 INT2 A2h = ISRC1 INT3 A3h = ISRC1 INT4 A4h = ISRC1 DEC1 A5h = ISRC1 DEC2 A6h = ISRC1 DEC3 A7h = ISRC1 DEC4 A8h = ISRC2 INT1 A9h = ISRC2 INT2 AAh = ISRC2 INT3 ABh = ISRC2 INT4 ACh = ISRC2 DEC1 ADh = ISRC2 DEC2 AEh = ISRC2 DEC3 AFh = ISRC2 DEC4 B0h = ISRC3 INT1 B1h = ISRC3 INT2 B4h = ISRC3 DEC1 B5h = ISRC3 DEC2 B8h = ISRC4 INT1 B9h = ISRC4 INT2 BCh = ISRC4 DEC1 BDh = ISRC4 DEC2 C0h = DSP6 channel 1 C1h = DSP6 channel 2 C2h = DSP6 channel 3 C3h = DSP6 channel 4 C4h = DSP6 channel 5 C5h = DSP6 channel 6 C8h = DSP7 channel 1 C9h = DSP7 channel 2 CAh = DSP7 channel 3 CBh = DSP7 channel 4 CCh = DSP7 channel 5 CDh = DSP7 channel 6

Table 8 Digital Core Mixer Control Registers

DIGITAL CORE INPUTS

The digital core comprises multiple input paths as illustrated in Figure 23. Any of these inputs may be selected as a source to the digital mixers or signal processing functions within the CS47L85 digital core.

Note that the outputs from other blocks within the Digital Core may also be selected as input to the digital mixers or signal processing functions within the CS47L85 digital core. Those input sources, which are not shown in Figure 23, are described separately in other sections of the “Digital Core” description.

The bracketed numbers in Figure 23, e.g.,”(10h)” indicate the corresponding *_SRC*n* register setting for selection of that signal as an input to another digital core function.

The sample rate for the input signal paths is configured using the applicable IN_RATE, AIFn_RATE or SLIMRXn_RATE register - see Table 22. Note that sample rate conversion is required when routing the input signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

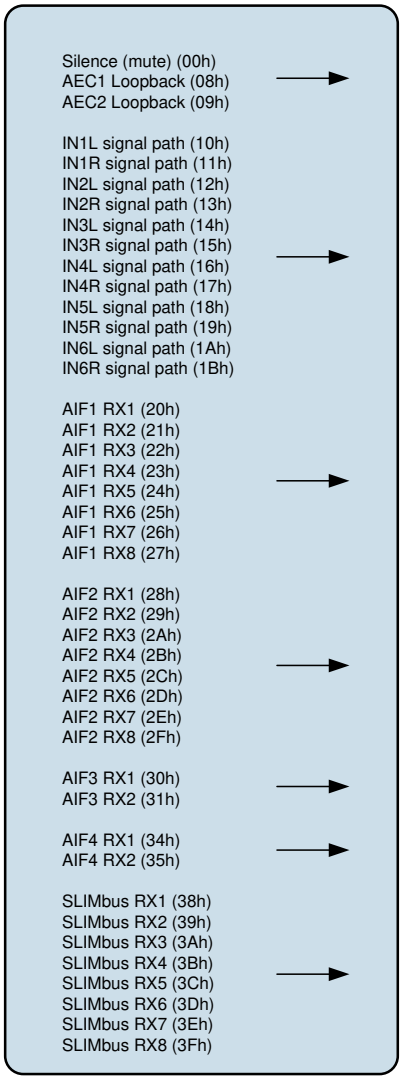


Figure 23 Digital Core Inputs

DIGITAL CORE OUTPUT MIXERS

The digital core comprises multiple output paths. The output paths associated with AIF1, AIF2, AIF3 and AIF4 are illustrated in Figure 24. The output paths associated with OUT1, OUT2, OUT3, OUT4, OUT5 and OUT6 are illustrated in Figure 25. The output paths associated with the SLIMbus interface are illustrated in Figure 26.

A 4-input mixer is associated with each output. The 4 input sources are selectable in each case, and independent volume control is provided for each path.

The AIF1, AIF2, AIF3 and AIF4 output mixer control registers (see Figure 24) are located at register addresses R1792 (700h) through to R1967 (7AEh). The OUT1, OUT2, OUT3, OUT4, OUT5 and OUT6 output mixer control registers (see Figure 25) are located at addresses R1664 (680h) through to R1759 (6DFh). The SLIMbus output mixer control registers (see Figure 26) are located at addresses R1984 (7C0h) through to R2047 (7FFh).

The full list of digital mixer control registers (Register R1600 through to R3192) is provided in a separate document - see "Register Map" for further information. Generic register definitions are provided in Table 8.

The *_SRC*n* registers select the input source(s) for the respective mixers. Note that the selected input source(s) must be configured for the same sample rate as the mixer to which they are connected. Sample rate conversion functions are available to support flexible interconnectivity - see "Asynchronous Sample Rate Converter (ASRC)" and "Isochronous Sample Rate Converter (ISRC)".

The *_SRC*n* registers for all digital core functions should be held at 00h if SYSCLK is not enabled – SYSCLK must be present and enabled before selecting other values for these registers. See "Clocking and Sample Rates" for further details (including requirements for reconfiguring SYSCLK while digital core mixers are enabled).

The sample rate for the output signal paths is configured using the applicable OUT_RATE, AIFn_RATE or SLIMTXn_RATE register - see Table 22. Note that sample rate conversion is required when routing the output signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

The OUT_RATE, AIFn_RATE or SLIMTXn_RATE registers should not be changed if any of the respective *_SRC*n* registers is non-zero. The associated *_SRC*n* registers should be cleared to 00h before writing new values to OUT_RATE, AIFn_RATE or SLIMTXn_RATE. A minimum delay of 125us should be allowed between clearing the *_SRC*n* registers and writing to the associated OUT_RATE, AIFn_RATE or SLIMTXn_RATE registers. See Table 22 for further details.

The CS47L85 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the output mixer paths. If an attempt is made to enable an output mixer path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The status bits in Registers R1600 to R3192 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

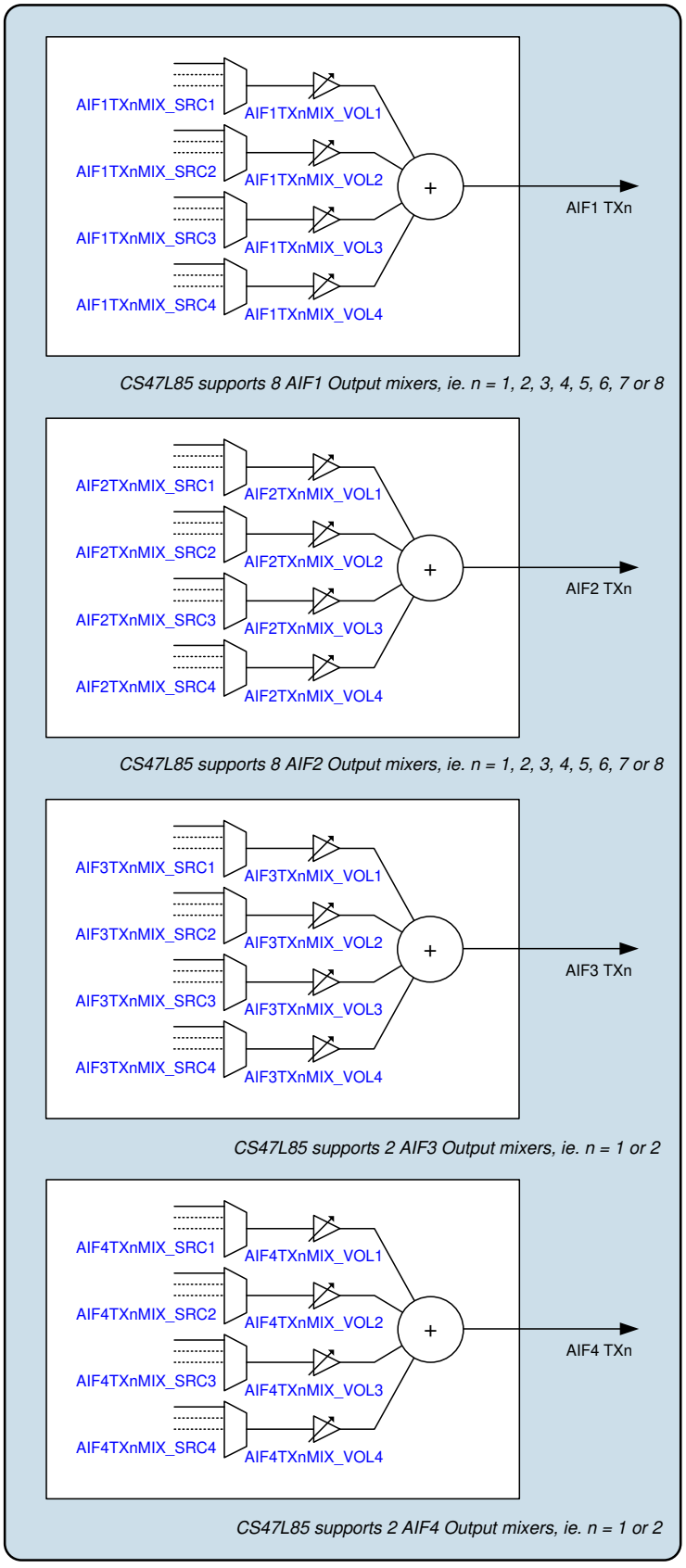


Figure 24 Digital Core AIF Outputs

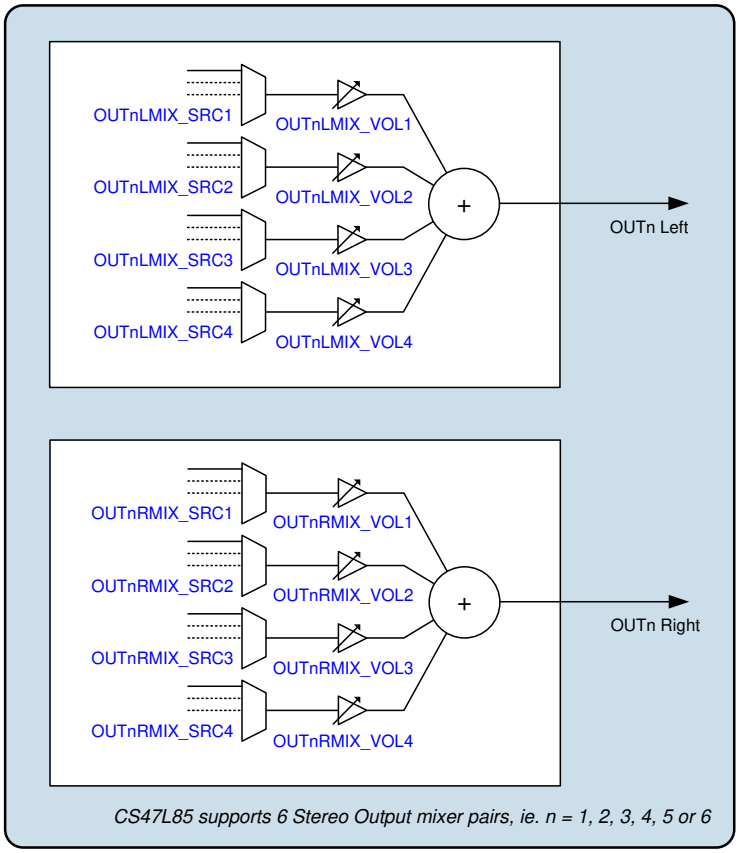


Figure 25 Digital Core OUTn Outputs

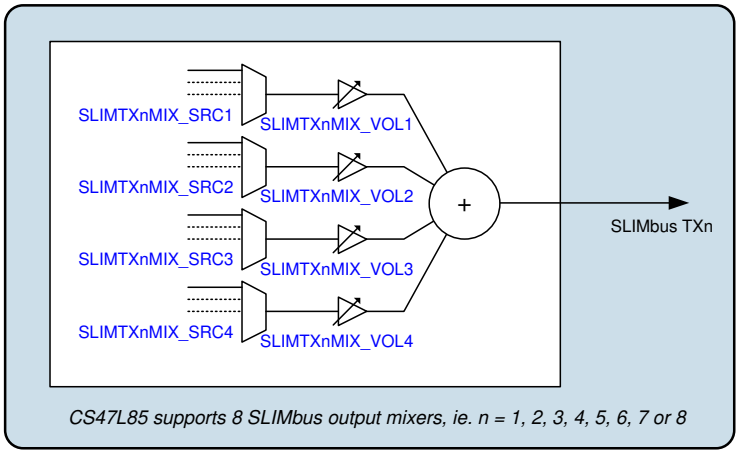


Figure 26 Digital Core SLIMbus Outputs

5-BAND PARAMETRIC EQUALISER (EQ)

The digital core provides four EQ processing blocks as illustrated in Figure 27. A 4-input mixer is associated with each EQ. The 4 input sources are selectable in each case, and independent volume control is provided for each path. Each EQ block supports 1 output.

The EQ provides selective control of 5 frequency bands as described below.

The low frequency band (Band 1) filter can be configured either as a peak filter or a shelving filter. When configured as a shelving filter, is provides adjustable gain below the Band 1 cut-off frequency. As a peak filter, it provides adjustable gain within a defined frequency band that is centred on the Band 1 frequency.

The mid frequency bands (Band 2, Band 3, Band 4) filters are peak filters, which provide adjustable gain around the respective centre frequency.

The high frequency band (Band 5) filter is a shelving filter, which provides adjustable gain above the Band 5 cut-off frequency.

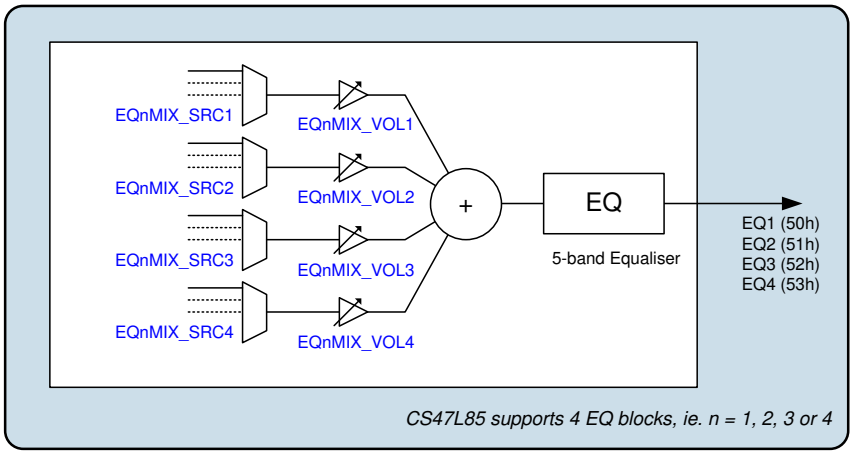


Figure 27 Digital Core EQ Blocks

The EQ1, EQ2, EQ3 and EQ4 mixer control registers (see Figure 27) are located at register addresses R2176 (880h) through to R2207 (89Fh).

The full list of digital mixer control registers (Register R1600 through to R3192) is provided in a separate document - see "Register Map" for further information. Generic register definitions are provided in Table 8.

The *_SRC*n* registers select the input source(s) for the respective EQ processing blocks. Note that the selected input source(s) must be configured for the same sample rate as the EQ to which they are connected. Sample rate conversion functions are available to support flexible interconnectivity - see "Asynchronous Sample Rate Converter (ASRC)" and "Isochronous Sample Rate Converter (ISRC)".

The bracketed numbers in Figure 27, e.g.,"(50h)" indicate the corresponding *_SRC*n* register setting for selection of that signal as an input to another digital core function.

The EQ blocks should be kept disabled (EQ*n*_ENA=0) if SYSCLK is not enabled. The *_SRC*n* registers for all digital core functions should be held at 00h if SYSCLK is not enabled. SYSCLK must be present and enabled before selecting other values for these registers. See "Clocking and Sample Rates" for further details (including requirements for reconfiguring SYSCLK while digital core functions are enabled).

The sample rate for the EQ function is configured using the FX_RATE register - see Table 22. Note that the EQ, DRC and LHPF functions must all be configured for the same sample rate. Sample rate conversion is required when routing the EQ signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

The FX_RATE register should not be changed if any of the associated *_SRC*n* registers is non-zero. The associated *_SRC*n* registers should be cleared to 00h before writing a new value to FX_RATE. A minimum delay of 125us should be allowed between clearing the *_SRC*n* registers and writing to the FX_RATE register. See Table 22 for further details.

The control registers associated with the EQ functions are described in Table 10.

The cut-off or centre frequencies for the 5-band EQ are set using the coefficients held in the registers identified in Table 9. These coefficients are derived using tools provided in Cirrus Logic's WISCE™ evaluation board control software; please contact your local Cirrus Logic representative for more details.

EQ	REGISTER ADDRESSES
EQ1	R3602 (0E10h) to R3620 (0E24h)
EQ2	R3624 (0E28h) to R3642 (0E3Ah)
EQ3	R3646 (0E3Eh) to R3664 (0E53h)
EQ4	R3668 (0E54h) to R3686 (0E66h)

Table 9 EQ Coefficient Registers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3585 (0E01h) FX_Ctrl2	15:4	FX_STS [11:0]	00h	LHPF, DRC, EQ Enable Status Indicates the status of each of the respective signal processing functions. [11] = EQ4 [10] = EQ3 [9] = EQ2 [8] = EQ1 [7] = DRC2 (Right) [6] = DRC2 (Left) [5] = DRC1 (Right) [4] = DRC1 (Left) [3] = LHPF4 [2] = LHPF3 [1] = LHPF2 [0] = LHPF1 Each bit is coded as: 0 = Disabled 1 = Enabled
R3600 (0E10h) EQ1_1	15:11	EQ1_B1_GAIN [4:0]	01100	EQ1 Band 1 Gain -12dB to +12dB in 1dB steps (see Table 11 for gain range)
	10:6	EQ1_B2_GAIN [4:0]	01100	EQ1 Band 2 Gain -12dB to +12dB in 1dB steps (see Table 11 for gain range)
	5:1	EQ1_B3_GAIN [4:0]	01100	EQ1 Band 3 Gain -12dB to +12dB in 1dB steps (see Table 11 for gain range)
	0	EQ1_ENA	0	EQ1 Enable 0 = Disabled 1 = Enabled
R3601 (0E11h) EQ1_2	15:11	EQ1_B4_GAIN [4:0]	01100	EQ1 Band 4 Gain -12dB to +12dB in 1dB steps (see Table 11 for gain range)
	10:6	EQ1_B5_GAIN [4:0]	01100	EQ1 Band 5 Gain -12dB to +12dB in 1dB steps (see Table 11 for gain range)
	0	EQ1_B1_MODE	0	EQ1 Band 1 Mode 0 = Shelving filter 1 = Peak filter
R3602 (0E12h) to R3620 (E24h)	15:0	EQ1_B1_* EQ1_B2_* EQ1_B3_* EQ1_B4_* EQ1_B5_*		EQ1 Frequency Coefficients Refer to WISCE evaluation board control software for the derivation of these field values.
R3622 (0E26h) EQ2_1	15:11	EQ2_B1_GAIN [4:0]	01100	EQ2 Band 1 Gain -12dB to +12dB in 1dB steps (see Table 11 for gain range)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	10:6	EQ2_B2_GAIN [4:0]	01100	EQ2 Band 2 Gain -12dB to +12dB in 1dB steps (see Table 11 for gain range)
	5:1	EQ2_B3_GAIN [4:0]	01100	EQ2 Band 3 Gain -12dB to +12dB in 1dB steps (see Table 11 for gain range)
	0	EQ2_ENA	0	EQ2 Enable 0 = Disabled 1 = Enabled
R3623 (0E27h) EQ2_2	15:11	EQ2_B4_GAIN [4:0]	01100	EQ2 Band 4 Gain -12dB to +12dB in 1dB steps (see Table 11 for gain range)
	10:6	EQ2_B5_GAIN [4:0]	01100	EQ2 Band 5 Gain -12dB to +12dB in 1dB steps (see Table 11 for gain range)
	0	EQ2_B1_MODE	0	EQ2 Band 1 Mode 0 = Shelving filter 1 = Peak filter
R3624 (0E28h) to R3642 (E3Ah)	15:0	EQ2_B1_* EQ2_B2_* EQ2_B3_* EQ2_B4_* EQ2_B5_*		EQ2 Frequency Coefficients Refer to WISCE evaluation board control software for the deriviation of these field values.
R3644 (0E3Ch) EQ3_1	15:11	EQ3_B1_GAIN [4:0]	01100	EQ3 Band 1 Gain -12dB to +12dB in 1dB steps (see Table 11 for gain range)
	10:6	EQ3_B2_GAIN [4:0]	01100	EQ3 Band 2 Gain -12dB to +12dB in 1dB steps (see Table 11 for gain range)
	5:1	EQ3_B3_GAIN [4:0]	01100	EQ3 Band 3 Gain -12dB to +12dB in 1dB steps (see Table 11 for gain range)
	0	EQ3_ENA	0	EQ3 Enable 0 = Disabled 1 = Enabled
R3645 (0E3Dh) EQ3_2	15:11	EQ3_B4_GAIN [4:0]	01100	EQ3 Band 4 Gain -12dB to +12dB in 1dB steps (see Table 11 for gain range)
	10:6	EQ3_B5_GAIN [4:0]	01100	EQ3 Band 5 Gain -12dB to +12dB in 1dB steps (see Table 11 for gain range)
	0	EQ3_B1_MODE	0	EQ3 Band 1 Mode 0 = Shelving filter 1 = Peak filter
R3646 (0E3Eh) to R3664 (E50h)	15:0	EQ3_B1_* EQ3_B2_* EQ3_B3_* EQ3_B4_* EQ3_B5_*		EQ3 Frequency Coefficients Refer to WISCE evaluation board control software for the derivation of these field values.
R3666 (0E52h) EQ4_1	15:11	EQ4_B1_GAIN [4:0]	01100	EQ4 Band 1 Gain -12dB to +12dB in 1dB steps (see Table 11 for gain range)
	10:6	EQ4_B2_GAIN [4:0]	01100	EQ4 Band 2 Gain -12dB to +12dB in 1dB steps (see Table 11 for gain range)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	5:1	EQ4_B3_GAIN [4:0]	01100	EQ4 Band 3 Gain -12dB to +12dB in 1dB steps (see Table 11 for gain range)
	0	EQ4_ENA	0	EQ4 Enable 0 = Disabled 1 = Enabled
R3667 (0E53h) EQ4_2	15:11	EQ4_B4_GAIN [4:0]	01100	EQ4 Band 4 Gain -12dB to +12dB in 1dB steps (see Table 11 for gain range)
	10:6	EQ4_B5_GAIN [4:0]	01100	EQ4 Band 5 Gain -12dB to +12dB in 1dB steps (see Table 11 for gain range)
	0	EQ4_B1_MODE	0	EQ4 Band 1 Mode 0 = Shelving filter 1 = Peak filter
R3668 (0E54h) to R3686 (E66h)	15:0	EQ4_B1_* EQ4_B2_* EQ4_B3_* EQ4_B4_* EQ4_B5_*		EQ4 Frequency Coefficients Refer to WISCE evaluation board control software for the derivation of these field values.

Table 10 EQ Enable and Gain Control

EQ GAIN SETTING	GAIN (dB)	EQ GAIN SETTING	GAIN (dB)
00000	-12	01101	+1
00001	-11	01110	+2
00010	-10	01111	+3
00011	-9	10000	+4
00100	-8	10001	+5
00101	-7	10010	+6
00110	-6	10011	+7
00111	-5	10100	+8
01000	-4	10101	+9
01001	-3	10110	+10
01010	-2	10111	+11
01011	-1	11000	+12
01100	0	11001 to 11111	Reserved

Table 11 EQ Gain Control Range

The CS47L85 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the commanded EQ and digital mixing functions. If an attempt is made to enable an EQ signal path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The FX_STS field in Register R3585 indicates the status of each of the EQ, DRC and LHPF signal paths. If an Underclocked Error condition occurs, then this register provides readback of which EQ, DRC or LHPF signal path(s) have been successfully enabled.

The status bits in Registers R1600 to R3192 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

DYNAMIC RANGE CONTROL (DRC)

The digital core provides two stereo Dynamic Range Control (DRC) processing blocks as illustrated in Figure 28. A 4-input mixer is associated with each DRC input channel. The 4 input sources are selectable in each case, and independent volume control is provided for each path. The stereo DRC blocks support 2 outputs each.

The function of the DRC is to adjust the signal gain in conditions where the input amplitude is unknown or varies over a wide range, e.g. when recording from microphones built into a handheld system, or to restrict the dynamic range of an output signal path.

The DRC can apply Compression and Automatic Level Control to the signal path. It incorporates 'anti-clip' and 'quick release' features for handling transients in order to improve intelligibility in the presence of loud impulsive noises.

The DRC also incorporates a Noise Gate function, which provides additional attenuation of very low-level input signals. This means that the signal path is quiet when no signal is present, giving an improvement in background noise level under these conditions.

A Signal Detect function is provided within the DRC; this can be used to detect the presence of an audio signal, and used to trigger other events. The Signal Detect function can be used as an Interrupt event, or used to trigger the Control Write Sequencer (note - DRC1 only).

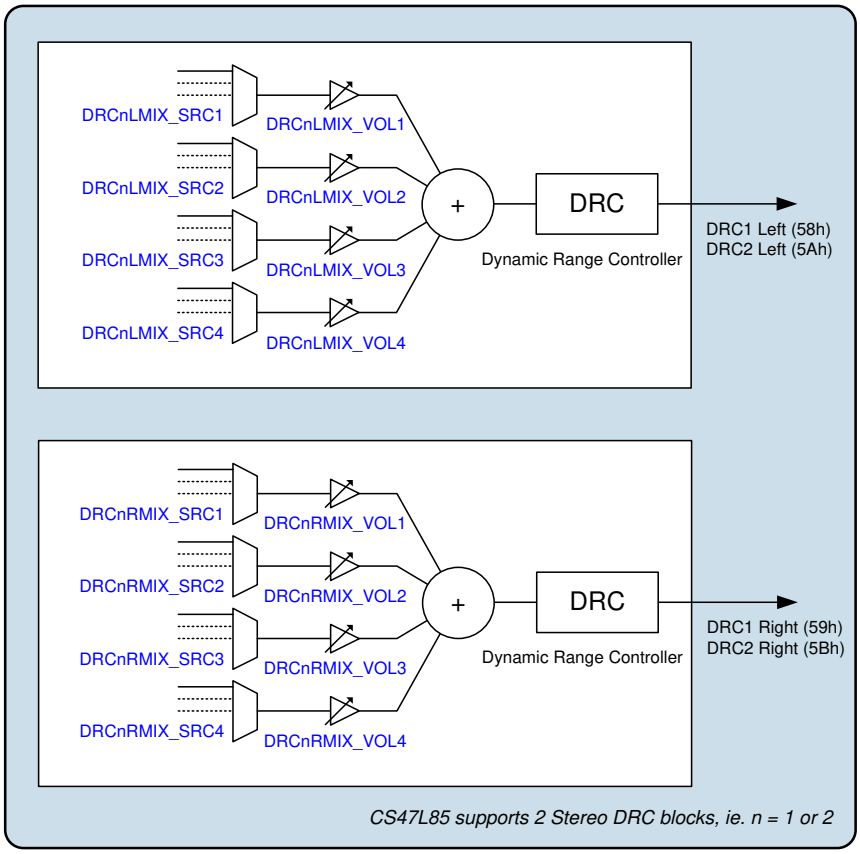


Figure 28 Dynamic Range Control (DRC) Block

The DRC1 and DRC2 mixer control registers (see Figure 28) are located at register addresses R2240 (8C0h) through to R2271 (08DFh).

The full list of digital mixer control registers (Register R1600 through to R3192) is provided in a separate document - see "Register Map" for further information. Generic register definitions are provided in Table 8.

The *_SRC*n* registers select the input source(s) for the respective DRC processing blocks. Note that the selected input source(s) must be configured for the same sample rate as the DRC to which they are connected. Sample rate conversion functions are available to support flexible interconnectivity - see "Asynchronous Sample Rate Converter (ASRC)" and "Isochronous Sample Rate Converter (ISRC)".

The bracketed numbers in Figure 28, e.g.,"(58h)" indicate the corresponding *_SRC*n* register setting for selection of that signal as an input to another digital core function.

The DRC blocks should be kept disabled (DRC*nx*_ENA=0) if SYSCLK is not enabled. The *_SRC*n* registers for all digital

core functions should be held at 00h if SYSCLK is not enabled. SYSCLK must be present and enabled before selecting other values for these registers. See “Clocking and Sample Rates” for further details (including requirements for reconfiguring SYSCLK while digital core functions are enabled).

The sample rate for the DRC function is configured using the FX_RATE register - see Table 22. Note that the EQ, DRC and LHPF functions must all be configured for the same sample rate. Sample rate conversion is required when routing the DRC signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

The FX_RATE register should not be changed if any of the associated *_SRC*n* registers is non-zero. The associated *_SRC*n* registers should be cleared to 00h before writing a new value to FX_RATE. A minimum delay of 125us should be allowed between clearing the *_SRC*n* registers and writing to the FX_RATE register. See Table 22 for further details.

The DRC functions are enabled using the control registers described in Table 12.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3712 (0E80h) DRC1_ctrl1	1	DRC1L_ENA	0	DRC1 (Left) Enable 0 = Disabled 1 = Enabled
	0	DRC1R_ENA	0	DRC1 (Right) Enable 0 = Disabled 1 = Enabled
R3720 (0E88h) DRC2_ctrl1	1	DRC2L_ENA	0	DRC2 (Left) Enable 0 = Disabled 1 = Enabled
	0	DRC2R_ENA	0	DRC2 (Right) Enable 0 = Disabled 1 = Enabled

Table 12 DRC Enable

The following description of the DRC is applicable to each of the DRCs. The associated register control fields are described in Table 14 and Table 15 for DRC1 and DRC2 respectively.

DRC COMPRESSION / EXPANSION / LIMITING

The DRC supports two different compression regions, separated by a “Knee” at a specific input amplitude. In the region above the knee, the compression slope DRCn_HI_COMP applies; in the region below the knee, the compression slope DRCn_LO_COMP applies. (Note that ‘n’ identifies the applicable DRC 1 or 2.)

The DRC also supports a noise gate region, where low-level input signals are heavily attenuated. This function can be enabled or disabled according to the application requirements. The DRC response in this region is defined by the expansion slope DRCn_NG_EXP.

For additional attenuation of signals in the noise gate region, an additional “knee” can be defined (shown as “Knee2” in Figure 29). When this knee is enabled, this introduces an infinitely steep drop-off in the DRC response pattern between the DRCn_LO_COMP and DRCn_NG_EXP regions.

The overall DRC compression characteristic in “steady state” (i.e. where the input amplitude is near-constant) is illustrated in Figure 29.

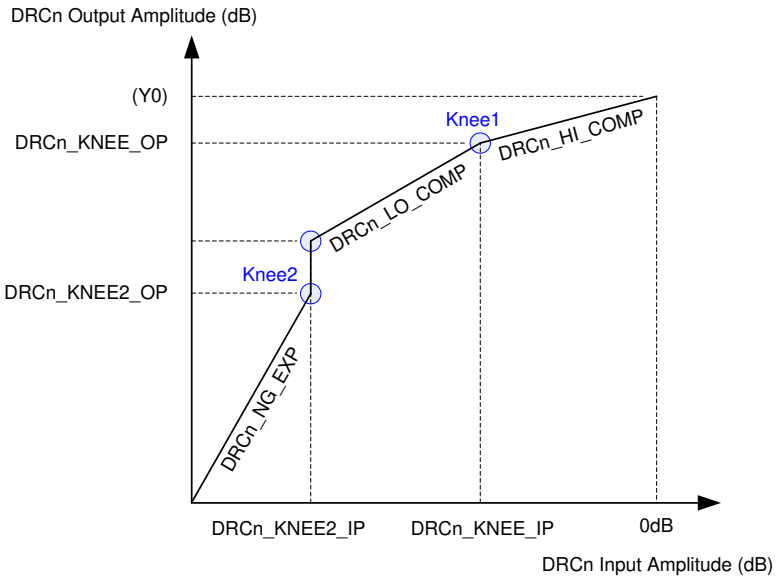


Figure 29 DRC Response Characteristic

The slope of the DRC response is determined by register fields DRCn_HI_COMP and DRCn_LO_COMP. A slope of 1 indicates constant gain in this region. A slope less than 1 represents compression (i.e. a change in input amplitude produces only a smaller change in output amplitude). A slope of 0 indicates that the target output amplitude is the same across a range of input amplitudes; this is infinite compression.

When the noise gate is enabled, the DRC response in this region is determined by the DRCn_NG_EXP register. A slope of 1 indicates constant gain in this region. A slope greater than 1 represents expansion (i.e., a change in input amplitude produces a larger change in output amplitude).

When the DRCn_KNEE2_OP knee is enabled ("Knee2" in Figure 29), this introduces the vertical line in the response pattern illustrated, resulting in infinitely steep attenuation at this point in the response.

The DRC parameters are listed in Table 13.

REF	PARAMETER	DESCRIPTION
1	DRCn_KNEE_IP	Input level at Knee1 (dB)
2	DRCn_KNEE_OP	Output level at Knee2 (dB)
3	DRCn_HI_COMP	Compression ratio above Knee1
4	DRCn_LO_COMP	Compression ratio below Knee1
5	DRCn_KNEE2_IP	Input level at Knee2 (dB)
6	DRCn_NG_EXP	Expansion ratio below Knee2
7	DRCn_KNEE2_OP	Output level at Knee2 (dB)

Table 13 DRC Response Parameters

The noise gate is enabled when the DRCn_NG_ENA register is set. When the noise gate is not enabled, parameters 5, 6, 7 above are ignored, and the DRCn_LO_COMP slope applies to all input signal levels below Knee1.

The DRCn_KNEE2_OP knee is enabled when the DRCn_KNEE2_OP_ENA register is set. When this bit is not set, then parameter 7 above is ignored, and the Knee2 position always coincides with the low end of the DRCn_LO_COMP region.

The "Knee1" point in Figure 29 is determined by register fields DRCn_KNEE_IP and DRCn_KNEE_OP.

Parameter Y0, the output level for a 0dB input, is not specified directly, but can be calculated from the other parameters, using the equation:

Y0 = DRCn_KNEE_OP - (DRCn_KNEE_IP x DRCn_HI_COMP)

GAIN LIMITS

The minimum and maximum gain applied by the DRC is set by register fields DRCn_MINGAIN, DRCn_MAXGAIN and DRCn_NG_MINGAIN. These limits can be used to alter the DRC response from that illustrated in Figure 29. If the range between maximum and minimum gain is reduced, then the extent of the dynamic range control is reduced.

The minimum gain in the Compression regions of the DRC response is set by DRCn_MINGAIN. The mimimum gain in the Noise Gate region is set by DRCn_NG_MINGAIN. The minimum gain limit prevents excessive attenuation of the signal path.

The maximum gain limit set by DRCn_MAXGAIN prevents quiet signals (or silence) from being excessively amplified.

DYNAMIC CHARACTERISTICS

The dynamic behaviour determines how quickly the DRC responds to changing signal levels. Note that the DRC responds to the average (RMS) signal amplitude over a period of time.

The DRCn_ATK determines how quickly the DRC gain decreases when the signal amplitude is high. The DRCn_DCY determines how quickly the DRC gain increases when the signal amplitude is low.

These register fields are described in Table 14. Note that the register defaults are suitable for general purpose microphone use.

ANTI-CLIP CONTROL

The DRC includes an Anti-Clip feature to avoid signal clipping when the input amplitude rises very quickly. This feature uses a feed-forward technique for early detection of a rising signal level. Signal clipping is avoided by dynamically increasing the gain attack rate when required. The Anti-Clip feature is enabled using the DRCn_ANTICLIP bit.

Note that the feed-forward processing increases the latency in the input signal path.

Note that the Anti-Clip feature operates entirely in the digital domain. It cannot be used to prevent signal clipping in the analogue domain nor in the source signal. Analogue clipping can only be prevented by reducing the analogue signal gain or by adjusting the source signal.

QUICK RELEASE CONTROL

The DRC includes a Quick-Release feature to handle short transient peaks that are not related to the intended source signal. For example, in handheld microphone recording, transient signal peaks sometimes occur due to user handling, key presses or accidental tapping against the microphone. The Quick Release feature ensures that these transients do not cause the intended signal to be masked by the longer time constant of DRCn_DCY.

The Quick-Release feature is enabled by setting the DRCn_QR bit. When this bit is enabled, the DRC measures the crest factor (peak to RMS ratio) of the input signal. A high crest factor is indicative of a transient peak that may not be related to the intended source signal. If the crest factor exceeds the level set by DRCn_QR_THR, then the normal decay rate (DRCn_DCY) is ignored and a faster decay rate (DRCn_QR_DCY) is used instead.

SIGNAL ACTIVITY DETECT

The DRC incorporates a configurable signal detect function, allowing the signal level at the DRC input to be monitored and to be used to trigger other events. This can be used to detect the presence of a microphone signal on an ADC or digital mic channel, or can be used to detect an audio signal received over the digital audio interface.

The DRC Signal Detect function is enabled by setting DRCn_SIG_DET register bit. (Note that the respective DRCn must also be enabled.) The detection threshold is either a Peak level (Crest Factor) or an RMS level, depending on the DRCn_SIG_DET_MODE register bit. When Peak level is selected, the threshold is determined by DRCn_SIG_DET_PK, which defines the applicable Crest Factor (Peak to RMS ratio) threshold. If RMS level is selected, then the threshold is set using DRCn_SIG_DET_RMS.

The DRC Signal Detect function is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see “Interrupts”.

The Control Write Sequencer can be triggered by the DRC1 Signal Detect function. This is enabled using the DRC1_WSEQ_SIG_DET_ENA register bit. See “Control Write Sequencer” for further details.

Note that signal detection is supported on DRC1 and DRC2, but the triggering of the Control Write Sequencer is available on DRC1 only.

DRC REGISTER CONTROLS

The DRC control registers are described in Table 14 and Table 15 for DRC1 and DRC2 respectively.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3585 (0E01h) FX_Ctrl2	15:4	FX_STS [11:0]	00h	LHPF, DRC, EQ Enable Status Indicates the status of each of the respective signal processing functions. [11] = EQ4 [10] = EQ3 [9] = EQ2 [8] = EQ1 [7] = DRC2 (Right) [6] = DRC2 (Left) [5] = DRC1 (Right) [4] = DRC1 (Left) [3] = LHPF4 [2] = LHPF3 [1] = LHPF2 [0] = LHPF1 Each bit is coded as: 0 = Disabled 1 = Enabled
R3712 (0E80h) DRC1_ctrl1	15:11	DRC1_SIG_DET_RMS [4:0]	00h	DRC1 Signal Detect RMS Threshold. This is the RMS signal level for signal detect to be indicated when DRC1_SIG_DET_MODE=1. 00h = -30dB 01h = -31.5dB …. (1.5dB steps) 1Eh = -75dB 1Fh = -76.5dB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	10:9	DRC1_SIG_DET_PK [1:0]	00	DRC1 Signal Detect Peak Threshold. This is the Peak/RMS ratio, or Crest Factor, level for signal detect to be indicated when DRC1_SIG_DET_MODE=0. 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB
	8	DRC1_NG_ENA	0	DRC1 Noise Gate Enable 0 = Disabled 1 = Enabled
	7	DRC1_SIG_DET_MODE	0	DRC1 Signal Detect Mode 0 = Peak threshold mode 1 = RMS threshold mode
	6	DRC1_SIG_DET	0	DRC1 Signal Detect Enable 0 = Disabled 1 = Enabled
	5	DRC1_KNEE2_OP_ENA	0	DRC1 KNEE2_OP Enable 0 = Disabled 1 = Enabled
	4	DRC1_QR	1	DRC1 Quick-release Enable 0 = Disabled 1 = Enabled
	3	DRC1_ANTICLIP	1	DRC1 Anti-clip Enable 0 = Disabled 1 = Enabled
	2	DRC1_WSEQ_SIG_DET_ENA	0	DRC1 Signal Detect Write Sequencer Select 0 = Disabled 1 = Enabled
R3713 (0E81h) DRC1_ctrl2	12:9	DRC1_ATK [3:0]	0100	DRC1 Gain attack rate (seconds/6dB) 0000 = Reserved 0001 = 181us 0010 = 363us 0011 = 726us 0100 = 1.45ms 0101 = 2.9ms 0110 = 5.8ms 0111 = 11.6ms 1000 = 23.2ms 1001 = 46.4ms 1010 = 92.8ms 1011 = 185.6ms 1100 to 1111 = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	8:5	DRC1_DCY [3:0]	1001	DRC1 Gain decay rate (seconds/6dB) 0000 = 1.45ms 0001 = 2.9ms 0010 = 5.8ms 0011 = 11.6ms 0100 = 23.25ms 0101 = 46.5ms 0110 = 93ms 0111 = 186ms 1000 = 372ms 1001 = 743ms 1010 = 1.49s 1011 = 2.97s 1100 to1111 = Reserved
	4:2	DRC1_MINGAIN [2:0]	100	DRC1 Minimum gain to attenuate audio signals 000 = 0dB 001 = -12dB 010 = -18dB 011 = -24dB 100 = -36dB 101 = Reserved 11X = Reserved
	1:0	DRC1_MAXGAIN [1:0]	11	DRC1 Maximum gain to boost audio signals (dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 36dB
R3714 (0E82h) DRC1_ctrl3	15:12	DRC1_NG_MING AIN [3:0]	0000	DRC1 Minimum gain to attenuate audio signals when the noise gate is active. 0000 = -36dB 0001 = -30dB 0010 = -24dB 0011 = -18dB 0100 = -12dB 0101 = -6dB 0110 = 0dB 0111 = 6dB 1000 = 12dB 1001 = 18dB 1010 = 24dB 1011 = 30dB 1100 = 36dB 1101 to 1111 = Reserved
	11:10	DRC1_NG_EXP [1:0]	00	DRC1 Noise Gate slope 00 = 1 (no expansion) 01 = 2 10 = 4 11 = 8
	9:8	DRC1_QR_THR [1:0]	00	DRC1 Quick-release threshold (crest factor in dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:6	DRC1_QR_DCY [1:0]	00	DRC1 Quick-release decay rate (seconds/6dB) 00 = 0.725ms 01 = 1.45ms 10 = 5.8ms 11 = Reserved
	5:3	DRC1_HI_COMP [2:0]	011	DRC1 Compressor slope (upper region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 0 110 = Reserved 111 = Reserved
	2:0	DRC1_LO_COMP [2:0]	000	DRC1 Compressor slope (lower region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 0 101 = Reserved 11X = Reserved
R3715 (0E83h) DRC1_ctrl4	10:5	DRC1_KNEE_IP [5:0]	000000	DRC1 Input signal level at the Compressor 'Knee'. 000000 = 0dB 000001 = -0.75dB 000010 = -1.5dB … (-0.75dB steps) 111100 = -45dB 111101 = Reserved 11111X = Reserved
	4:0	DRC1_KNEE_OP [4:0]	00000	DRC1 Output signal at the Compressor 'Knee'. 00000 = 0dB 00001 = -0.75dB 00010 = -1.5dB … (-0.75dB steps) 11110 = -22.5dB 11111 = Reserved
R3716 (0E84h) DRC1_ctrl5	9:5	DRC1_KNEE2_IP [4:0]	00000	DRC1 Input signal level at the Noise Gate threshold 'Knee2'. 00000 = -36dB 00001 = -37.5dB 00010 = -39dB … (-1.5dB steps) 11110 = -81dB 11111 = -82.5dB Only applicable when DRC1_NG_ENA = 1.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	4:0	DRC1_KNEE2_ OP [4:0]	00000	DRC1 Output signal at the Noise Gate threshold 'Knee2'. 00000 = -30dB 00001 = -31.5dB 00010 = -33dB … (-1.5dB steps) 11110 = -75dB 11111 = -76.5dB Only applicable when DRC1_KNEE2_OP_ENA = 1.

Table 14 DRC1 Control Registers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3585 (0E01h) FX_Ctrl2	15:4	FX_STS [11:0]	00h	LHPF, DRC, EQ Enable Status Indicates the status of each of the respective signal processing functions. [11] = EQ4 [10] = EQ3 [9] = EQ2 [8] = EQ1 [7] = DRC2 (Right) [6] = DRC2 (Left) [5] = DRC1 (Right) [4] = DRC1 (Left) [3] = LHPF4 [2] = LHPF3 [1] = LHPF2 [0] = LHPF1 Each bit is coded as: 0 = Disabled 1 = Enabled
R3720 (0E88h) DRC2_ctrl1	15:11	DRC2_SIG_DET _RMS [4:0]	00h	DRC2 Signal Detect RMS Threshold. This is the RMS signal level for signal detect to be indicated when DRC2_SIG_DET_MODE=1. 00h = -30dB 01h = -31.5dB …. (1.5dB steps) 1Eh = -75dB 1Fh = -76.5dB
	10:9	DRC2_SIG_DET _PK [1:0]	00	DRC2 Signal Detect Peak Threshold. This is the Peak/RMS ratio, or Crest Factor, level for signal detect to be indicated when DRC2_SIG_DET_MODE=0. 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB
	8	DRC2_NG_ENA	0	DRC2 Noise Gate Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7	DRC2_SIG_DET_MODE	0	DRC2 Signal Detect Mode 0 = Peak threshold mode 1 = RMS threshold mode
	6	DRC2_SIG_DET	0	DRC2 Signal Detect Enable 0 = Disabled 1 = Enabled
	5	DRC2_KNEE2_OP_ENA	0	DRC2 KNEE2_OP Enable 0 = Disabled 1 = Enabled
	4	DRC2_QR	1	DRC2 Quick-release Enable 0 = Disabled 1 = Enabled
	3	DRC2_ANTICLIP	1	DRC2 Anti-clip Enable 0 = Disabled 1 = Enabled
R3721 (0E89h) DRC2_ctrl2	12:9	DRC2_ATK [3:0]	0100	DRC2 Gain attack rate (seconds/6dB) 0000 = Reserved 0001 = 181us 0010 = 363us 0011 = 726us 0100 = 1.45ms 0101 = 2.9ms 0110 = 5.8ms 0111 = 11.6ms 1000 = 23.2ms 1001 = 46.4ms 1010 = 92.8ms 1011 = 185.6ms 1100 to 1111 = Reserved
	8:5	DRC2_DCY [3:0]	1001	DRC2 Gain decay rate (seconds/6dB) 0000 = 1.45ms 0001 = 2.9ms 0010 = 5.8ms 0011 = 11.6ms 0100 = 23.25ms 0101 = 46.5ms 0110 = 93ms 0111 = 186ms 1000 = 372ms 1001 = 743ms 1010 = 1.49s 1011 = 2.97s 1100 to1111 = Reserved
	4:2	DRC2_MINGAIN [2:0]	100	DRC2 Minimum gain to attenuate audio signals 000 = 0dB 001 = -12dB (default) 010 = -18dB 011 = -24dB 100 = -36dB 101 = Reserved 11X = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1:0	DRC2_MAXGAIN [1:0]	11	DRC2 Maximum gain to boost audio signals (dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 36dB
R3722 (0E8Ah) DRC2_ctrl3	15:12	DRC2_NG_MING AIN [3:0]	0000	DRC2 Minimum gain to attenuate audio signals when the noise gate is active. 0000 = -36dB 0001 = -30dB 0010 = -24dB 0011 = -18dB 0100 = -12dB 0101 = -6dB 0110 = 0dB 0111 = 6dB 1000 = 12dB 1001 = 18dB 1010 = 24dB 1011 = 30dB 1100 = 36dB 1101 to 1111 = Reserved
	11:10	DRC2_NG_EXP [1:0]	00	DRC2 Noise Gate slope 00 = 1 (no expansion) 01 = 2 10 = 4 11 = 8
	9:8	DRC2_QR_THR [1:0]	00	DRC2 Quick-release threshold (crest factor in dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB
	7:6	DRC2_QR_DCY [1:0]	00	DRC2 Quick-release decay rate (seconds/6dB) 00 = 0.725ms 01 = 1.45ms 10 = 5.8ms 11 = Reserved
	5:3	DRC2_HI_COMP [2:0]	011	DRC2 Compressor slope (upper region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 0 110 = Reserved 111 = Reserved
	2:0	DRC2_LO_COMP [2:0]	000	DRC2 Compressor slope (lower region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 0 101 = Reserved 11X = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3723 (0E8Bh) DRC2_ctrl4	10:5	DRC2_KNEE_IP [5:0]	000000	DRC2 Input signal level at the Compressor 'Knee'. 000000 = 0dB 000001 = -0.75dB 000010 = -1.5dB … (-0.75dB steps) 111100 = -45dB 111101 = Reserved 11111X = Reserved
	4:0	DRC2_KNEE_OP [4:0]	00000	DRC2 Output signal at the Compressor 'Knee'. 00000 = 0dB 00001 = -0.75dB 00010 = -1.5dB … (-0.75dB steps) 11110 = -22.5dB 11111 = Reserved
R3724 (0E8Ch) DRC2_ctrl5	9:5	DRC2_KNEE2_IP [4:0]	00000	DRC2 Input signal level at the Noise Gate threshold 'Knee2'. 00000 = -36dB 00001 = -37.5dB 00010 = -39dB … (-1.5dB steps) 11110 = -81dB 11111 = -82.5dB Only applicable when DRC2_NG_ENA = 1.
	4:0	DRC2_KNEE2_OP [4:0]	00000	DRC2 Output signal at the Noise Gate threshold 'Knee2'. 00000 = -30dB 00001 = -31.5dB 00010 = -33dB … (-1.5dB steps) 11110 = -75dB 11111 = -76.5dB Only applicable when DRC2_KNEE2_OP_ENA = 1.

Table 15 DRC2 Control Registers

The CS47L85 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the commanded DRC and digital mixing functions. If an attempt is made to enable a DRC signal path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The FX_STS field in Register R3585 indicates the status of each of the EQ, DRC and LHPF signal paths. If an Underclocked Error condition occurs, then this register provides readback of which EQ, DRC or LHPF signal path(s) have been successfully enabled.

The status bits in Registers R1600 to R3192 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

LOW PASS / HIGH PASS DIGITAL FILTER (LHPF)

The digital core provides four Low Pass Filter (LPF) / High Pass Filter (HPF) processing blocks as illustrated in Figure 30. A 4-input mixer is associated with each filter. The 4 input sources are selectable in each case, and independent volume control is provided for each path. Each Low/High Pass Filter (LHPF) block supports 1 output.

The Low Pass Filter / High Pass Filter can be used to remove unwanted 'out of band' noise from a signal path. Each filter can be configured either as a Low Pass filter or High Pass filter.

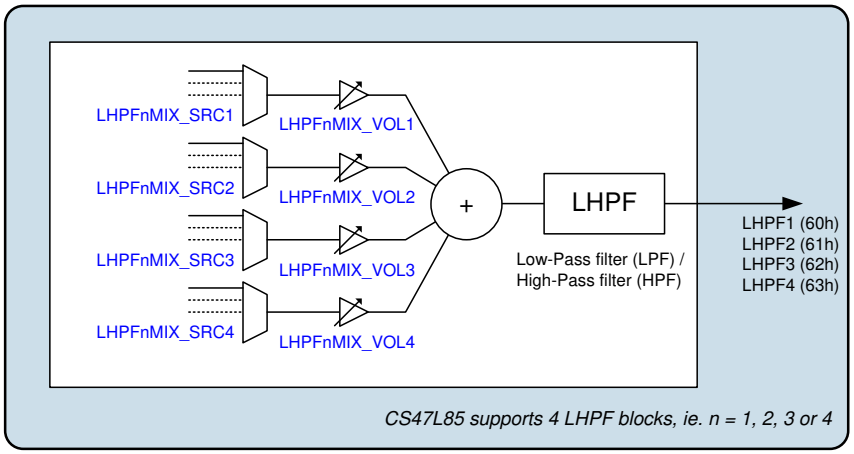


Figure 30 Digital Core LPF/HPF Blocks

The LHPF1, LHPF2, LHPF3 and LHPF4 mixer control registers (see Figure 30) are located at register addresses R2304 (900h) through to R2335 (91Fh).

The full list of digital mixer control registers (Register R1600 through to R3192) is provided in a separate document - see "Register Map" for further information. Generic register definitions are provided in Table 8.

The *_SRC*n* registers select the input source(s) for the respective LHPF processing blocks. Note that the selected input source(s) must be configured for the same sample rate as the LHPF to which they are connected. Sample rate conversion functions are available to support flexible interconnectivity - see "Asynchronous Sample Rate Converter (ASRC)" and "Isochronous Sample Rate Converter (ISRC)".

The bracketed numbers in Figure 30, e.g.,"(60h)" indicate the corresponding *_SRC*n* register setting for selection of that signal as an input to another digital core function.

The LHPF blocks should be kept disabled (LHPF*n*_ENA=0) if SYSCLK is not enabled. The *_SRC*n* registers for all digital core functions should be held at 00h if SYSCLK is not enabled. SYSCLK must be present and enabled before selecting other values for these registers. See "Clocking and Sample Rates" for further details (including requirements for reconfiguring SYSCLK while digital core functions are enabled).

The sample rate for the LHPF function is configured using the FX_RATE register - see Table 22. Note that the EQ, DRC and LHPF functions must all be configured for the same sample rate. Sample rate conversion is required when routing the LHPF signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

The FX_RATE register should not be changed if any of the associated *_SRC*n* registers is non-zero. The associated *_SRC*n* registers should be cleared to 00h before writing a new value to FX_RATE. A minimum delay of 125us should be allowed between clearing the *_SRC*n* registers and writing to the FX_RATE register. See Table 22 for further details.

The control registers associated with the LHPF functions are described in Table 16.

The cut-off frequencies for the LHPF blocks are set using the coefficients held in registers R3777, R3781, R3785 and R3789 for LHPF1, LHPF2, LHPF3 and LHPF4 respectively. These coefficients are derived using tools provided in Cirrus Logic's WISCE evaluation board control software; please contact your local Cirrus Logic representative for more details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3585 (0E01h) FX_Ctrl2	15:4	FX_STS [11:0]	00h	LHPF, DRC, EQ Enable Status Indicates the status of each of the respective signal processing functions. [11] = EQ4 [10] = EQ3 [9] = EQ2 [8] = EQ1 [7] = DRC2 (Right) [6] = DRC2 (Left) [5] = DRC1 (Right) [4] = DRC1 (Left) [3] = LHPF4 [2] = LHPF3 [1] = LHPF2 [0] = LHPF1 Each bit is coded as: 0 = Disabled 1 = Enabled
R3776 (0EC0h) HPLPF1_1	1	LHPF1_MODE	0	Low/High Pass Filter 1 Mode 0 = Low-Pass 1 = High-Pass
	0	LHPF1_ENA	0	Low/High Pass Filter 1 Enable 0 = Disabled 1 = Enabled
R3777 (0EC1h) HPLPF1_2	15:0	LHPF1_COEFF [15:0]	0000h	Low/High Pass Filter 1 Frequency Coefficient Refer to WISCE evaluation board control software for the derivation of this field value.
R3780 (0EC4h) HPLPF2_1	1	LHPF2_MODE	0	Low/High Pass Filter 2 Mode 0 = Low-Pass 1 = High-Pass
	0	LHPF2_ENA	0	Low/High Pass Filter 2 Enable 0 = Disabled 1 = Enabled
R3781 (0EC5h) HPLPF2_2	15:0	LHPF2_COEFF [15:0]	0000h	Low/High Pass Filter 2 Frequency Coefficient Refer to WISCE evaluation board control software for the derivation of this field value.
R3784 (0EC8h) HPLPF3_1	1	LHPF3_MODE	0	Low/High Pass Filter 3 Mode 0 = Low-Pass 1 = High-Pass
	0	LHPF3_ENA	0	Low/High Pass Filter 3 Enable 0 = Disabled 1 = Enabled
R3785 (0EC9h) HPLPF3_2	15:0	LHPF3_COEFF [15:0]	0000h	Low/High Pass Filter 3 Frequency Coefficient Refer to WISCE evaluation board control software for the derivation of this field value.
R3788 (0ECCh) HPLPF4_1	1	LHPF4_MODE	0	Low/High Pass Filter 4 Mode 0 = Low-Pass 1 = High-Pass
	0	LHPF4_ENA	0	Low/High Pass Filter 4 Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3789 (0ECDh) HPLPF4_2	15:0	LHPF4_COEFF [15:0]	0000h	Low/High Pass Filter 4 Frequency Coefficient Refer to WISCE evaluation board control software for the derivation of this field value.

Table 16 Low Pass Filter / High Pass Filter Control

The CS47L85 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the commanded LHPF and digital mixing functions. If an attempt is made to enable an LHPF signal path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The FX_STS field in Register R3585 indicates the status of each of the EQ, DRC and LHPF signal paths. If an Underclocked Error condition occurs, then this register provides readback of which EQ, DRC or LHPF signal path(s) have been successfully enabled.

The status bits in Registers R1600 to R3192 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

DIGITAL CORE DSP

The digital core provides seven programmable DSP processing blocks as illustrated in Figure 31. Each block supports 8 inputs (Left, Right, Aux1, Aux2, … Aux6). A 4-input mixer is associated with the Left and Right inputs, providing further expansion of the number of input paths. Each of the input sources is selectable, and independent volume control is provided for Left and Right input mixer channels. Each DSP block supports 6 outputs.

The functionality of the DSP processing blocks is not fixed, and a wide range of audio enhancements algorithms may be performed. The procedure for configuring the CS47L85 DSP functions is tailored to each customer's application; please contact your local Cirrus Logic representative for more details.

For details of the DSP Firmware requirements relating to clocking, register access, and code execution, refer to the "DSP Firmware Control" section.

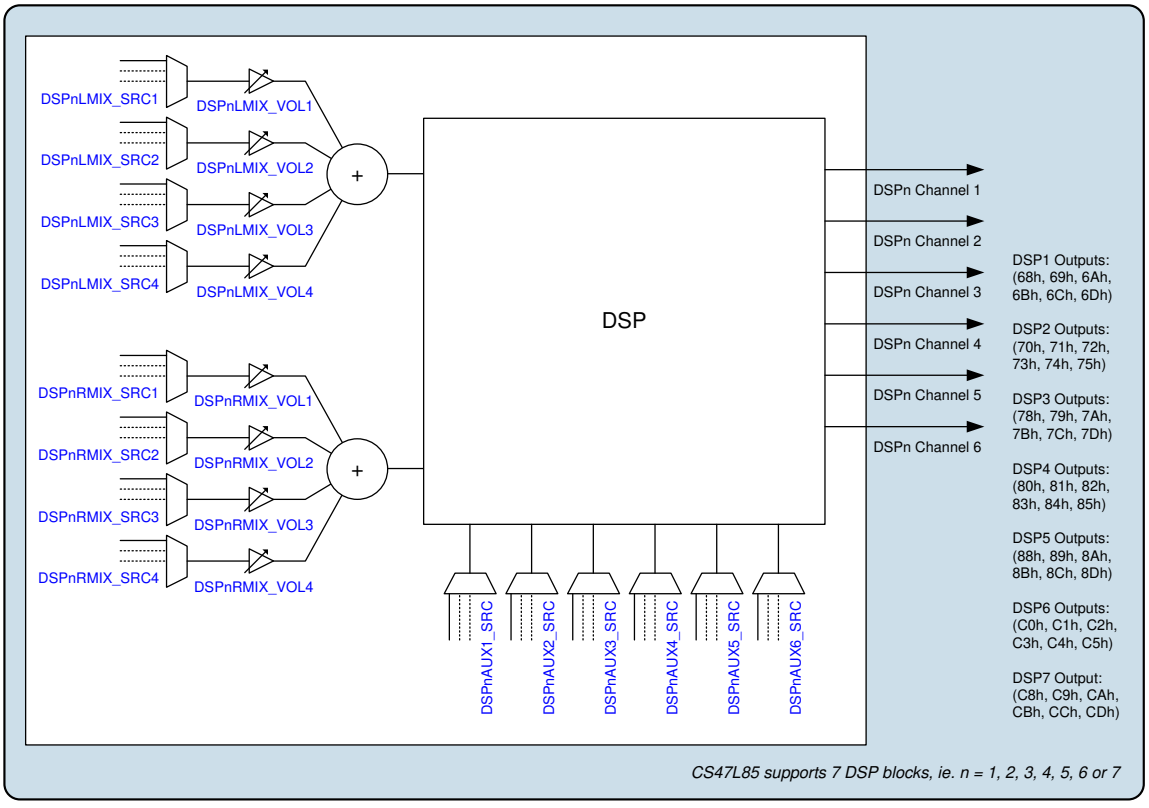


Figure 31 Digital Core DSP Blocks

The DSPn mixer / input control registers (see Figure 31) are located at register addresses R2368 (940h) through to R2676 (A74h).

The full list of digital mixer control registers (Register R1600 through to R3192) is provided in a separate document - see "Register Map" for further information. Generic register definitions are provided in Table 8.

The *_SRC*n* registers select the input source(s) for the respective DSP processing blocks. Note that the selected input source(s) must be configured for the same sample rate as the DSP to which they are connected. Sample rate conversion functions are available to support flexible interconnectivity - see "Asynchronous Sample Rate Converter (ASRC)" and "Isochronous Sample Rate Converter (ISRC)".

The bracketed numbers in Figure 31, e.g.,"(68h)" indicate the corresponding *_SRC*n* register setting for selection of that signal as an input to another digital core function.

The *_SRC*n* registers for all digital core functions should be held at 00h if SYSCLK is not enabled – SYSCLK must be present and enabled before selecting other values for these registers. See "Clocking and Sample Rates" for further details (including requirements for reconfiguring SYSCLK while digital core mixers are enabled).

The sample rate for each of the DSP functions is configured using the respective DSPn_RATE registers - see Table 22. Sample rate conversion is required when routing the DSPn signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

The DSPn_RATE registers should not be changed if any of the respective *_SRC*n* registers is non-zero. The associated *_SRC*n* registers should be cleared to 00h before writing new values to DSPn_RATE. A minimum delay of 125us should be allowed between clearing the *_SRC*n* registers and writing to the associated DSPn_RATE registers. See Table 22 for further details.

The CS47L85 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the commanded DSP mixing functions. If an attempt is made to enable a DSP mixer path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The status bits in Registers R1600 to R3192 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

SPDIF OUTPUT GENERATOR

The CS47L85 incorporates an IEC-60958-3 compatible S/PDIF output generator, as illustrated in Figure 32; this provides a stereo S/PDIF output on a GPIO pin. The S/PDIF transmitter allows full control over the S/PDIF validity bits and channel status information.

The input sources to the S/PDIF transmitter are selectable for each channel, and independent volume control is provided for each path. The *TX1 and *TX2 registers control channels 'A' and 'B' (respectively) of the S/PDIF output.

The S/PDIF signal can be output directly on a GPIO pin. See "General Purpose Input / Output" to configure a GPIO pin for this function.

Note that the S/PDIF signal cannot be selected as input to the digital mixers or signal processing functions within the CS47L85 digital core.

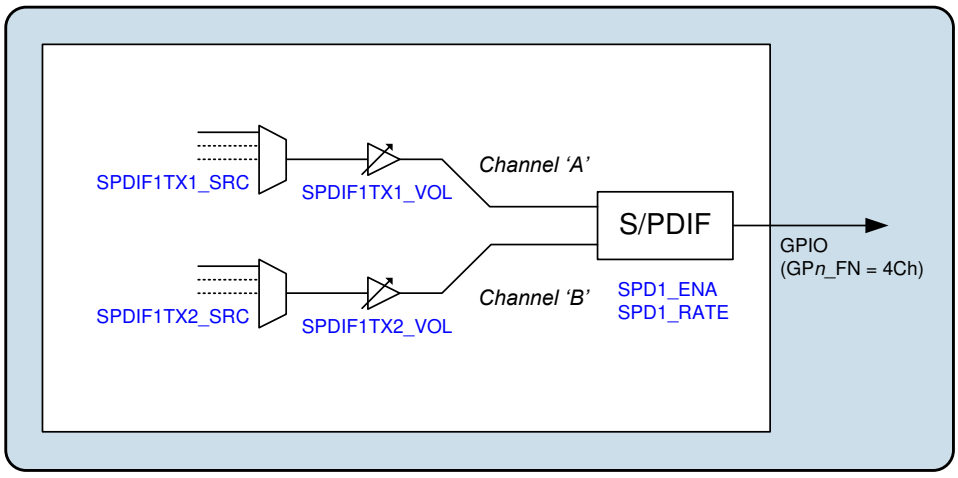


Figure 32 Digital Core S/PDIF Output Generator

The S/PDIF input control registers (see Figure 32) are located at register addresses R2048 (800h) through to R2057 (809h).

The full list of digital mixer control registers (Register R1600 through to R3192) is provided in a separate document - see "Register Map" for further information. Generic register definitions are provided in Table 8.

The *_SRC*n* registers select the input source(s) for the two S/PDIF channels. Note that the selected input source(s) must be synchronised to the SYSCLK clocking domain, and configured for the same sample rate as the S/PDIF generator. Sample rate conversion functions are available to support flexible interconnectivity - see "Asynchronous Sample Rate Converter (ASRC)" and "Isochronous Sample Rate Converter (ISRC)".

The S/PDIF output generator should be kept disabled (SPD1_ENA=0) if SYSCLK is not enabled. The *_SRC*n* registers for all digital core functions should be held at 00h if SYSCLK is not enabled. SYSCLK must be present and enabled before selecting other values for these registers. See "Clocking and Sample Rates" for further details (including requirements for reconfiguring SYSCLK while digital core functions are enabled).

The sample rate of the S/PDIF generator is configured using the SPD1_RATE register - see Table 22. The S/PDIF transmitter supports sample rates in the range 32kHz up to 192kHz. Note that sample rate conversion is required when linking the S/PDIF generator to any signal chain that is asynchronous and/or configured for a different sample rate.

The SPD1_RATE register should not be changed if any of the associated *_SRC*n* registers is non-zero. The associated *_SRC*n* registers should be cleared to 00h before writing new values to SPD1_RATE. A minimum delay of 125us should be allowed between clearing the *_SRC*n* registers and writing to the SPD1_RATE register. See Table 22 for further details.

The S/PDIF generator is enabled using the SPD1_ENA register bit, as described in Table 17.

The S/PDIF output contains audio data derived from the selected sources. Audio samples up to 24-bit width can be accommodated. The Validity bits and the Channel Status bits in the S/PDIF data are configured using the corresponding fields in registers R1474 (5C2h) to R1477 (5C5h).

Refer to S/PDIF specification (IEC 60958-3) for full details of the S/PDIF protocol and configuration parameters.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1474 (05C2h) SPD1_TX_ Control	13	SPD1_VAL2	0	S/PDIF validity (Subframe B)
	12	SPD1_VAL1	0	S/PDIF validity (Subframe A)
	0	SPD1_ENA	0	S/PDIF Generator Enable 0 = Disabled 1 = Enabled
R1475 (05C3h) SPD1_TX_ Channel_St atus_1	15:8	SPD1_CATCODE [7:0]	00h	S/PDIF Category code
	7:6	SPD1_CHSTMODE [1:0]	00	S/PDIF Channel Status mode
	5:3	SPD1_PREEMPH [2:0]	000	S/PDIF Pre-emphasis mode
	2	SPD1_NOCOPY	0	S/PDIF Copyright status
	1	SPD1_NOAUDIO	0	S/PDIF Audio / Non-audio indication
	0	SPD1_PRO	0	S/PDIF Consumer / Professional Mode
R1476 (05C4h) SPD1_TX_ Channel_St atus_2	15:12	SPD1_FREQ [3:0]	0000	S/PDIF Indicated sample frequency
	11:8	SPD1_CHNUM2 [3:0]	1011	S/PDIF Channel number (Subframe B)
	7:4	SPD1_CHNUM1 [3:0]	0000	S/PDIF Channel number (Subframe A)
	3:0	SPD1_SRCNUM [3:0]	0001	S/PDIF Source number
R1477 (05C5h) SPD1_TX_ Channel_St atus_3	11:8	SPD1_ORGSAMP [3:0]	0000	S/PDIF Original sample frequency
	7:5	SPD1_TXWL [2:0]	000	S/PDIF Audio sample word length
	4	SPD1_MAXWL	0	S/PDIF Maximum audio sample word length
	3:2	SPD1_SC31_30 [1:0]	00	S/PDIF Channel Status [31:30]
	1:0	SPD1_CLKACU [1:0]	00	Transmitted clock accuracy

Table 17 S/PDIF Output Generator Control

The CS47L85 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the digital mixer paths. If an attempt is made to enable the SPDIF generator, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The status bits in Registers R1600 to R3192 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

TONE GENERATOR

The CS47L85 incorporates two 1kHz tone generators which can be used for 'beep' functions through any of the audio signal paths. The phase relationship between the two generators is configurable, providing flexibility in creating differential signals, or for test scenarios.

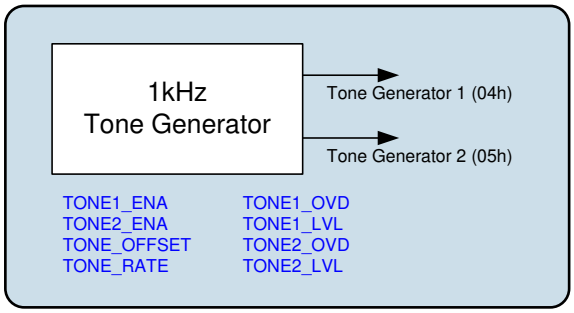


Figure 33 Digital Core Tone Generator

The tone generators can be selected as input to any of the digital mixers or signal processing functions within the CS47L85 digital core. The bracketed numbers in Figure 33, e.g.,"(04h)" indicate the corresponding *_SRC*n* register setting for selection of that signal as an input to another digital core function.

SYSCLK must be present and enabled before setting the TONE*n*_ENA bits. The tone generators should be kept disabled (TONE*n*_ENA=0) if SYSCLK is not enabled. See "Clocking and Sample Rates" for further details (including requirements for reconfiguring SYSCLK while digital core functions are enabled).

The sample rate for the tone generators is configured using the TONE_RATE register - see Table 22. Note that sample rate conversion is required when routing the tone generator output(s) to any signal chain that is asynchronous and/or configured for a different sample rate.

The tone generators are enabled using the TONE1_ENA and TONE2_ENA register bits as described in Table 18. The phase relationship is configured using TONE_OFFSET.

The tone generators can also provide a configurable DC signal level, for use as a test signal. The DC output is selected using the TONEn_OVD register bits, and the DC signal amplitude is configured using the TONEn_LVL registers, as described in Table 18.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (0020h) Tone_Generator_1	9:8	TONE_OFFSET [1:0]	00	Tone Generator Phase Offset Sets the phase of Tone Generator 2 relative to Tone Generator 1 00 = 0 degrees (in phase) 01 = 90 degrees ahead 10 = 180 degrees ahead 11 = 270 degrees ahead
	5	TONE2_OVD	0	Tone Generator 2 Override 0 = Disabled (1kHz tone output) 1 = Enabled (DC signal output) The DC signal level, when selected, is configured using TONE2_LVL[23:0]
	4	TONE1_OVD	0	Tone Generator 1 Override 0 = Disabled (1kHz tone output) 1 = Enabled (DC signal output) The DC signal level, when selected, is configured using TONE1_LVL[23:0]
	1	TONE2_ENA	0	Tone Generator 2 Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	TONE1_ENA	0	Tone Generator 1 Enable 0 = Disabled 1 = Enabled
R33 (0021h) Tone_Generator_2	15:0	TONE1_LVL [23:8]	1000h	Tone Generator 1 DC output level TONE1_LVL [23:8] is coded as 2's complement. Bits [23:20] contain the integer portion; bits [19:0] contain the fractional portion. The digital core 0dBFS level corresponds to 1000_00h (+1) or F000_00h (-1).
R34 (0022h) Tone_Generator_3	7:0	TONE1_LVL [7:0]	00h	Tone Generator 1 DC output level TONE1_LVL [23:8] is coded as 2's complement. Bits [23:20] contain the integer portion; bits [19:0] contain the fractional portion. The digital core 0dBFS level corresponds to 1000_00h (+1) or F000_00h (-1).
R35 (0023h) Tone_Generator_4	15:0	TONE2_LVL [23:8]	1000h	Tone Generator 2 DC output level TONE2_LVL [23:8] is coded as 2's complement. Bits [23:20] contain the integer portion; bits [19:0] contain the fractional portion. The digital core 0dBFS level corresponds to 1000_00h (+1) or F000_00h (-1).
R36 (0024h) Tone_Generator_5	7:0	TONE2_LVL [7:0]	00h	Tone Generator 2 DC output level TONE2_LVL [23:8] is coded as 2's complement. Bits [23:20] contain the integer portion; bits [19:0] contain the fractional portion. The digital core 0dBFS level corresponds to 1000_00h (+1) or F000_00h (-1).

Table 18 Tone Generator Control

NOISE GENERATOR

The CS47L85 incorporates a white noise generator, which can be routed within the digital core. The main purpose of the noise generator is to provide 'comfort noise' in cases where silence (digital mute) is not desirable.

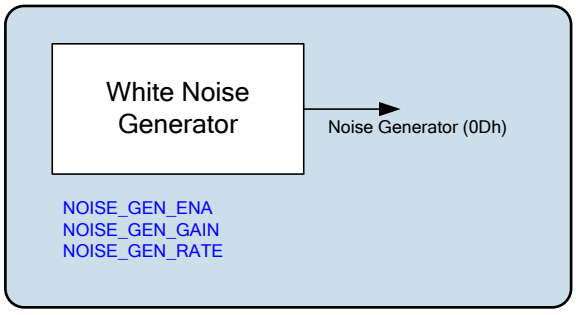


Figure 34 Digital Core Noise Generator

The noise generator can be selected as input to any of the digital mixers or signal processing functions within the CS47L85 digital core. The bracketed number (0Dh) in Figure 34 indicates the corresponding *_SRC*n* register setting for selection of the noise generator as an input to another digital core function.

SYSCLK must be present and enabled before setting the NOISE_GEN_ENA bit. The noise generator should be kept disabled (NOISE_GEN_ENA=0) if SYSCLK is not enabled. See "Clocking and Sample Rates" for further details (including requirements for reconfiguring SYSCLK while digital core functions are enabled).

The sample rate for the noise generator is configured using the NOISE_GEN_RATE register - see Table 22. Note that sample rate conversion is required when routing the noise generator output to any signal chain that is asynchronous

and/or configured for a different sample rate.

The noise generator is enabled using the NOISE_GEN_ENA register bit as described in Table 19. The signal level is configured using NOISE_GEN_GAIN.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R160 (00A0h) Comfort_Noise_Generator	5	NOISE_GEN_ENA	0	Noise Generator Enable 0 = Disabled 1 = Enabled
	4:0	NOISE_GEN_GAIN [4:0]	00h	Noise Generator Signal Level 00h = -114dBFS 01h = -108dBFS 02h = -102dBFS …(6dB steps) 11h = -6dBFS 12h = 0dBFS All other codes are Reserved

Table 19 Noise Generator Control

HAPTIC SIGNAL GENERATOR

The CS47L85 incorporates a signal generator for use with haptic devices (e.g., mechanical vibration actuators). The haptic signal generator is compatible with both Eccentric Rotating Mass (ERM) and Linear Resonant Actuator (LRA) haptic devices.

The haptic signal generator is highly configurable, and includes the capability to execute a programmable event profile comprising three distinct operating phases.

The resonant frequency of the haptic signal output (for LRA devices) is selectable, providing support for many different actuator components.

The haptic signal generator is a digital signal generator which is incorporated within the digital core of the CS47L85. The haptic signal may be routed, via one of the digital core output mixers, to a Class D speaker output for connection to the external haptic device, as illustrated in Figure 35. (Note that the digital PDM output paths may also be used for haptic signal output.)

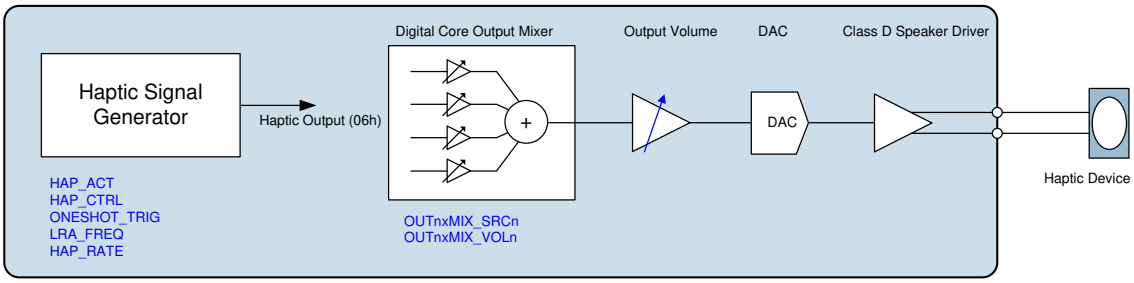


Figure 35 Digital Core Haptic Signal Generator

The bracketed number (06h) in Figure 35 indicates the corresponding *_SRC*n* register setting for selection of the haptic signal generator as an input to another digital core function.

The haptic signal generator is selected as input to one of the digital core output mixers by setting the *_SRC*n* register of the applicable output mixer to (06h).

SYSCLK must be present and enabled before setting HAP_CTRL>00. The haptic signal generator should be kept disabled (HAP_CTRL=00) if SYSCLK is not enabled. See “Clocking and Sample Rates” for further details (including requirements for reconfiguring SYSCLK while digital core functions are enabled).

The sample rate for the haptic signal generator is configured using the HAP_RATE register - see Table 22. Note that sample rate conversion is required when routing the haptic signal generator output to any signal chain that is asynchronous and/or configured for a different sample rate.

The haptic signal generator is configured for an ERM or LRA actuator using the HAP_ACT register bit. The required resonant frequency is configured using the LRA_FREQ field. (Note that the resonant frequency is only applicable to LRA actuators.)

The signal generator can be enabled in Continuous mode or configured for One-Shot mode using the HAP_CTRL register, as described in Table 20. In One-Shot mode, the output is triggered by writing to the ONESHOT_TRIG bit.

In One-Shot mode, the signal generator profile comprises the distinct phases (1, 2, 3). The duration and intensity of each output phase is programmable.

In Continuous mode, the signal intensity is controlled using the PHASE2_INTENSITY field only.

In the case of an ERM actuator (HAP_ACT = 0), the haptic output is a DC signal level, which may be positive or negative, as selected by the *_INTENSITY registers.

For an LRA actuator (HAP_ACT = 1), the haptic output is an AC signal; selecting a negative signal level corresponds to a 180 degree phase inversion. In some applications, phase inversion may be desirable during the final phase, to halt the physical motion of the haptic device.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R144 (0090h) Haptics_Control_1	4	ONESHOT_TRIG	0	Haptic One-Shot Trigger Writing '1' starts the one-shot profile (i.e., Phase 1, Phase 2, Phase 3)
	3:2	HAP_CTRL [1:0]	00	Haptic Signal Generator Control 00 = Disabled 01 = Continuous 10 = One-Shot 11 = Reserved
	1	HAP_ACT	0	Haptic Actuator Select 0 = Eccentric Rotating Mass (ERM) 1 = Linear Resonant Actuator (LRA)
R145 (0091h) Haptics_Control_2	14:0	LRA_FREQ [14:0]	7FFFh	Haptic Resonant Frequency Selects the haptic signal frequency (LRA actuator only, HAP_ACT = 1) Haptic Frequency (Hz) = System Clock / (2 x (LRA_FREQ+1)) where System Clock = 6.144MHz or 5.6448MHz, derived by division from SYSCLK or ASYNCCLK. If HAP_RATE<1000, then SYSCLK is the clock source, and the applicable System Clock frequency is determined by SYSCLK. If HAP_RATE>=1000, then ASYNCCLK is the clock source, and the applicable System Clock frequency is determined by ASYNCCLK. Valid for Haptic Frequency in the range 100Hz to 250Hz For 6.144MHz System Clock: 77FFh = 100Hz 4491h = 175Hz 2FFFh = 250Hz For 5.6448MHz System Clock: 6E3Fh = 100Hz 3EFFh = 175Hz 2C18h = 250Hz

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R146 (0092h) Haptics_phase_1_intensity	7:0	PHASE1_INTENSITY [7:0]	00h	Haptic Output Level (Phase 1) Selects the signal intensity of Phase 1 in one-shot mode. Coded as 2's complement. Range is +/- Full Scale (FS). For ERM actuator, this selects the DC signal level for the haptic output. For LRA actuator, this selects the AC peak amplitude; Negative values correspond to a 180 degree phase shift.
R147 (0093h) Haptics_Control_phase_1_duration	8:0	PHASE1_DURATION [8:0]	000h	Haptic Output Duration (Phase 1) Selects the duration of Phase 1 in one-shot mode. 000h = 0ms 001h = 0.625ms 002h = 1.25ms … (0.625ms steps) 1FFh = 319.375ms
R148 (0094h) Haptics_phase_2_intensity	7:0	PHASE2_INTENSITY [7:0]	00h	Haptic Output Level (Phase 2) Selects the signal intensity in Continuous mode or Phase 2 of one-shot mode. Coded as 2's complement. Range is +/- Full Scale (FS). For ERM actuator, this selects the DC signal level for the haptic output. For LRA actuator, this selects the AC peak amplitude; Negative values correspond to a 180 degree phase shift.
R149 (0095h) Haptics_phase_2_duration	10:0	PHASE2_DURATION [10:0]	000h	Haptic Output Duration (Phase 2) Selects the duration of Phase 2 in one-shot mode. 000h = 0ms 001h = 0.625ms 002h = 1.25ms … (0.625ms steps) 7FFh = 1279.375ms
R150 (0096h) Haptics_phase_3_intensity	7:0	PHASE3_INTENSITY [7:0]	00h	Haptic Output Level (Phase 3) Selects the signal intensity of Phase 3 in one-shot mode. Coded as 2's complement. Range is +/- Full Scale (FS). For ERM actuator, this selects the DC signal level for the haptic output. For LRA actuator, this selects the AC peak amplitude; Negative values correspond to a 180 degree phase shift.
R151 (0097h) Haptics_phase_3_duration	8:0	PHASE3_DURATION [8:0]	000h	Haptic Output Duration (Phase 3) Selects the duration of Phase 3 in one-shot mode. 000h = 0ms 001h = 0.625ms 002h = 1.25ms … (0.625ms steps) 1FFh = 319.375ms
R152 (0098h) Haptics_Status	0	ONESHOT_STS	0	Haptic One-Shot status 0 = One-Shot event not in progress 1 = One-Shot event in progress

Table 20 Haptic Signal Generator Control

PWM GENERATOR

The CS47L85 incorporates two Pulse Width Modulation (PWM) signal generators as illustrated in Figure 36. The duty cycle of each PWM signal can be modulated by an audio source, or can be set to a fixed value using a control register setting.

A 4-input mixer is associated with each PWM generator. The 4 input sources are selectable in each case, and independent volume control is provided for each path.

The PWM signal generators can be output directly on a GPIO pin. See “General Purpose Input / Output” to configure a GPIO pin for this function.

Note that the PWM signal generators cannot be selected as input to the digital mixers or signal processing functions within the CS47L85 digital core.

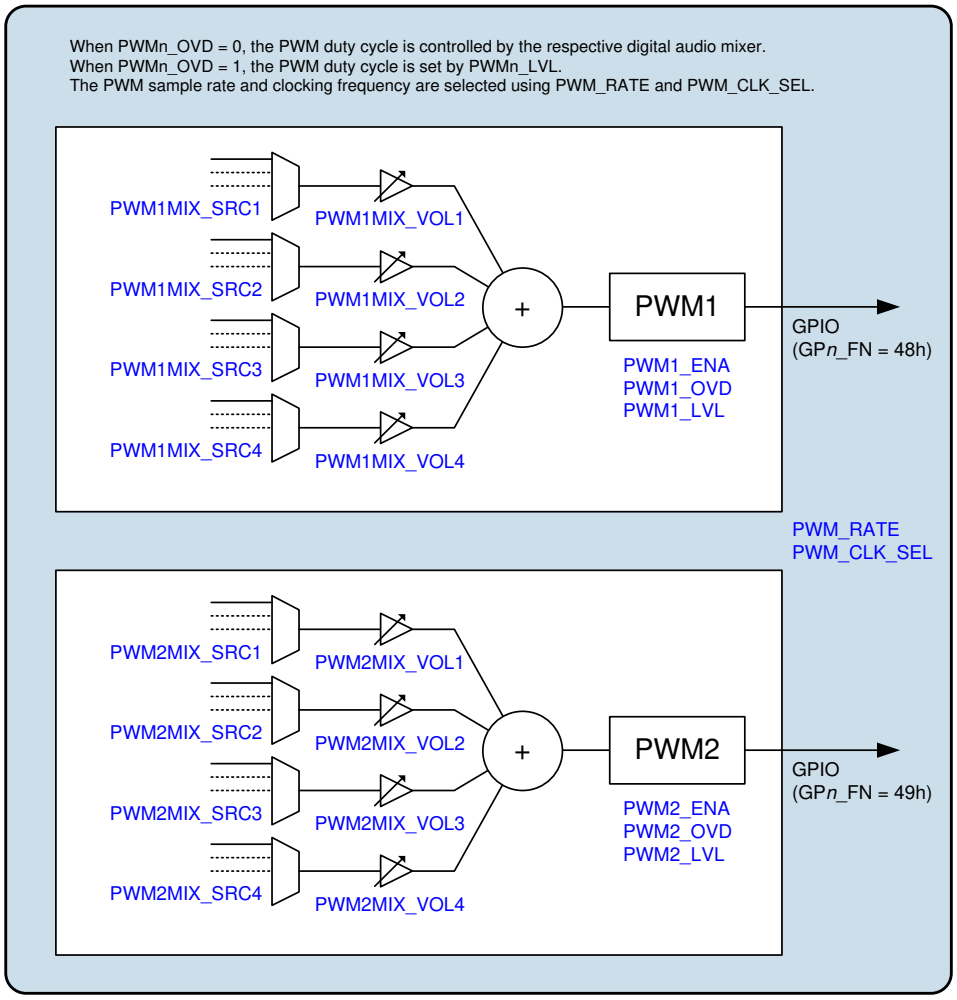


Figure 36 Digital Core Pulse Width Modulation (PWM) Generator

The PWM1 and PWM2 mixer control registers (see Figure 36) are located at register addresses R1600 (640h) through to R1615 (64Fh).

The full list of digital mixer control registers (Register R1600 through to R3192) is provided in a separate document - see “Register Map” for further information. Generic register definitions are provided in Table 8.

The *_SRC*n* registers select the input source(s) for the respective mixers. Note that the selected input source(s) must be configured for the same sample rate as the mixer to which they are connected. Sample rate conversion functions are available to support flexible interconnectivity - see “Asynchronous Sample Rate Converter (ASRC)” and “Isochronous Sample Rate Converter (ISRC)”.

The PWM generators should be kept disabled (PWM*n*_ENA=0) if SYSCLK is not enabled. The *_SRC*n* registers for all digital core functions should be held at 00h if SYSCLK is not enabled. SYSCLK must be present and enabled before

selecting other values for these registers. See “Clocking and Sample Rates” for further details (including requirements for reconfiguring SYSCLK while digital core functions are enabled).

The PWM sample rate (cycle time) is configured using the PWM_RATE register - see Table 22. Note that sample rate conversion is required when linking the PWM generators to any signal chain that is asynchronous and/or configured for a different sample rate.

The PWM_RATE register should not be changed if any of the associated *_SRC*n* registers is non-zero. The associated *_SRC*n* registers should be cleared to 00h before writing a new value to PWM_RATE. A minimum delay of 125us should be allowed between clearing the *_SRC*n* registers and writing to the PWM_RATE register. See Table 22 for further details.

The PWM generators are enabled using PWM1_ENA and PWM2_ENA respectively, as described in Table 21.

Under default conditions (PWM*n*_OVD = 0), the duty cycle of the PWM generators is controlled by an audio signal path; a 4-input mixer is associated with each PWM generator, as illustrated in Figure 36.

When the PWM*n*_OVD bit is set, the duty cycle of the respective PWM generator is set to a fixed ratio; in this case, the duty cycle ratio is configurable using the PWM*n*_LVL registers.

The PWM generator clock frequency is selected using PWM_CLK_SEL. For best performance, this register should be set to the highest available setting. Note that the PWM generator clock must not be set to a higher frequency than SYSCLK (if PWM_RATE<1000) or ASYNCCLK (if PWM_RATE≥1000).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R48 (0030h) PWM_Drive _1	10:8	PWM_CLK_SEL [2:0]	000	PWM Clock Select 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) All other codes are Reserved The frequencies in brackets apply for 44.1kHz-related sample rates only. PWM_CLK_SEL controls the resolution of the PWM generator; higher settings correspond to higher resolution. The PWM Clock must be less than or equal to SYSCLK (if PWM_RATE<1000) or less than or equal to ASYNCCLK (if PWM_RATE>=1000).
	5	PWM2_OVD	0	PWM2 Generator Override 0 = Disabled (PWM duty cycle is controlled by audio source) 1 = Enabled (PWM duty cycle is controlled by PWM2_LVL).
	4	PWM1_OVD	0	PWM1 Generator Override 0 = Disabled (PWM1 duty cycle is controlled by audio source) 1 = Enabled (PWM1 duty cycle is controlled by PWM1_LVL).
	1	PWM2_ENA	0	PWM2 Generator Enable 0 = Disabled 1 = Enabled
	0	PWM1_ENA	0	PWM1 Generator Enable 0 = Disabled 1 = Enabled
R49 (0031h) PWM_Drive _2	9:0	PWM1_LVL [9:0]	100h	PWM1 Override Level Sets the PWM1 duty cycle when PWM1_OVD=1. Coded as 2’s complement. 000h = 50% duty cycle 200h = 0% duty cycle

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R50 (0032h) PWM_Drive _3	9:0	PWM2_LVL [9:0]	100h	PWM2 Override Level Sets the PWM2 duty cycle when PWM2_OVD=1. Coded as 2's complement. 000h = 50% duty cycle 200h = 0% duty cycle

Table 21 Pulse Width Modulation (PWM) Generator Control

The CS47L85 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the digital mixer paths. If an attempt is made to enable a PWM signal mixer path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The status bits in Registers R1600 to R3192 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

SAMPLE RATE CONTROL

The CS47L85 supports multiple signal paths through the digital core. Stereo full-duplex sample rate conversion is provided to allow digital audio to be routed between interfaces operating at different sample rates and/or referenced to asynchronous clock domains.

Two independent clock domains are supported for the audio signal paths, referenced to SYSCLK and ASYNCCLK respectively, as described in "Clocking and Sample Rates". Every digital signal path must be synchronised either to SYSCLK or to ASYNCCLK.

Up to five different sample rates may be in use at any time on the CS47L85. Three of these sample rates must be synchronised to SYSCLK; the remaining two, where required, must be synchronised to ASYNCCLK.

Sample rate conversion is required when routing any audio path between digital functions that are asynchronous and/or configured for different sample rates.

There are two Asynchronous Sample Rate Converters (ASRCs). Each ASRC supports 2-way stereo conversion paths between the SYSCLK and ASYNCCLK domains. The ASRCs are described later, and is illustrated in Figure 38.

There are four Isochronous Sample Rate Converters (ISRCs). ISRC1 and ISRC2 support 2-way, 4-channel conversion paths between sample rates on the SYSCLK domain, or between sample rates on the ASYNCCLK domain. ISRC3 and ISRC4 provide similar functionality for up to 2 channels each. The ISRCs are described later, and are illustrated in Figure 39.

The sample rate of different blocks within the CS47L85 digital core are controlled as illustrated in Figure 37 - the *_RATE registers select the applicable sample rate for each respective group of digital functions.

The *_RATE registers should not be changed if any of the *_SRC*n* registers associated with the respective functions is non-zero. The associated *_SRC*n* registers should be cleared to 00h before writing new values to the *_RATE registers. A minimum delay of 125us should be allowed between clearing the *_SRC*n* registers and writing to the associated *_RATE registers. See Table 22 for further details.

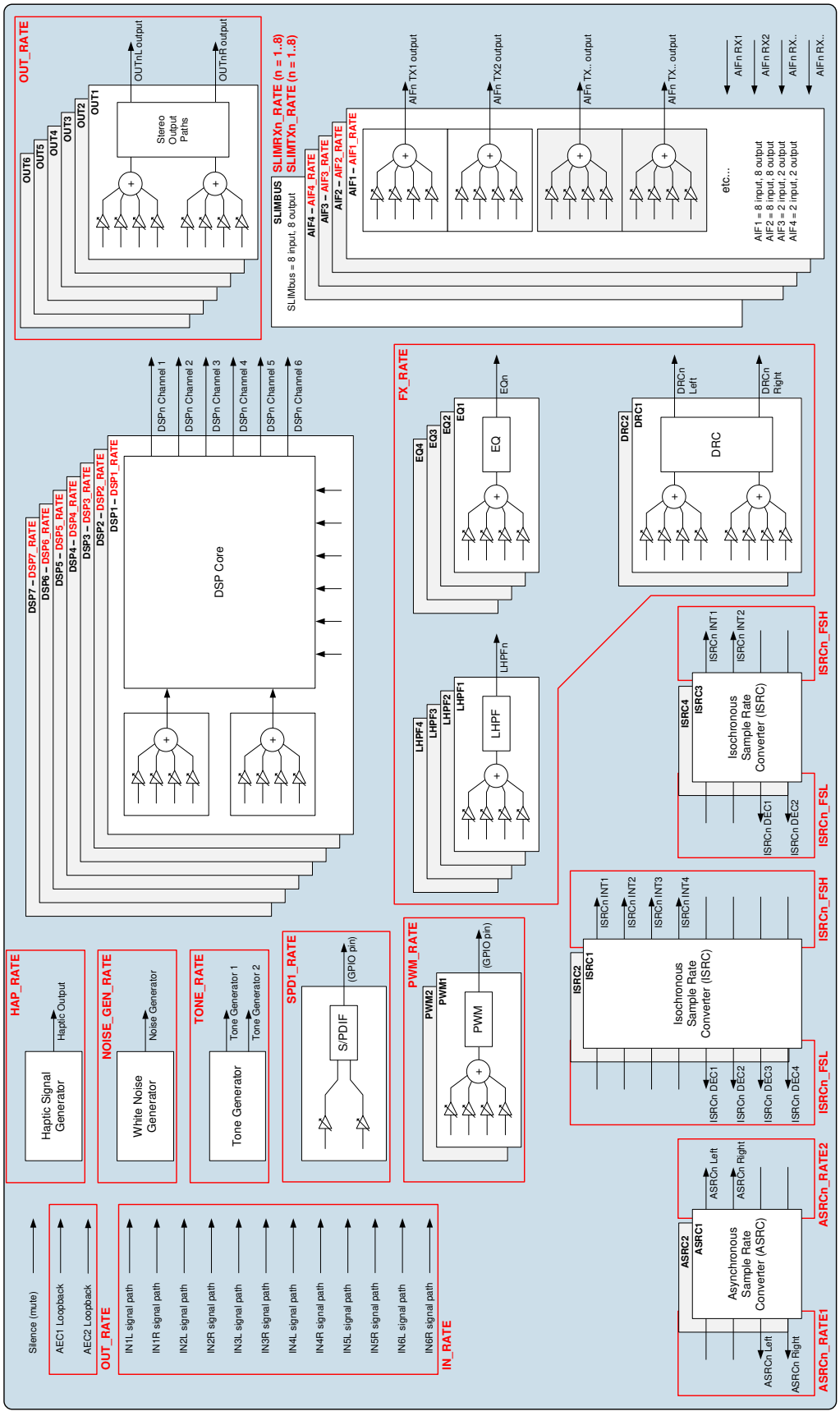


Figure 37 Digital Core Sample Rate Control

The input signal paths may be selected as input to the digital mixers or signal processing functions. The sample rate for the input signal paths is configured using the IN_RATE register.

The output signal paths are derived from the respective output mixers. The sample rate for the output signal paths is configured using the OUT_RATE register. The sample rate of the AEC Loopback path is also set by the OUT_RATE register.

The AIFn RX inputs may be selected as input to the digital mixers or signal processing functions. The AIFn TX outputs are derived from the respective output mixers. The sample rates for digital audio interfaces (AIF1, AIF2, AIF3 and AIF4) are configured using the AIFn_RATE registers (where 'n' identifies the applicable AIF 1, 2, 3 or 4) respectively.

The SLIMbus interface supports up to 8 input channels and 8 output channels. The sample rate of each channel can be configured independently, using the SLIMTXn_RATE and SLIMRXn_RATE registers.

Note that the SLIMbus interface provides simultaneous support for SYSCLK-referenced and ASYNCCLK-referenced sample rates on different channels. For example, 48kHz and 44.1kHz SLIMbus audio paths can be simultaneously supported.

The EQ, LHPF and DRC functions can be enabled in any signal path within the digital core. The sample rate for these functions is configured using the FX_RATE register. Note that the EQ, DRC and LHPF functions must all be configured for the same sample rate.

The DSPn functions can be enabled in any signal path within the digital core. The applicable sample rates are configured using the DSPn_RATE registers (where 'n' identifies the applicable DSP 1 through to 7) respectively.

The S/PDIF transmitter can be enabled on a GPIO pin. Stereo inputs to this function can be configured from any of the digital core inputs, mixers, or signal processing functions. The sample rate of the S/PDIF transmitter is configured using the SPD1_RATE register.

The tone generators and noise generator can be selected as input to any of the digital mixers or signal processing functions. The sample rates for these sources are configured using the TONE_RATE and NOISE_GEN_RATE registers respectively.

The haptic signal generator can be used to control an external vibe actuator, which can be driven directly by the Class D speaker output. The sample rate for the haptic signal generator is configured using the HAP_RATE register.

The PWM signal generators can be modulated by an audio source, derived from the associated signal mixers. The sample rate (cycle time) for the PWM signal generators is configured using the PWM_RATE register.

The sample rate control registers are described in Table 22. Refer to the register descriptions for details of the valid selections in each case. Note that the input (ADC) and output (DAC) signal paths must always be associated with the SYSCLK clocking domain; different sample rates may be selected concurrently, but both these rates must be synchronised to SYSCLK.

The control registers associated with the ASRC and ISRCs are described in Table 23 and Table 24 respectively within the following sections.

Note that 32-bit register addressing is used from R12888 (3000h) upwards; 16-bit format is used otherwise. The registers noted in Table 22 contain a mixture of 16-bit and 32-bit register addresses.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (0020h) Tone_Generator_1	14:11	TONE_RATE [3:0]	0000	Tone Generator Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz.
R48 (0030h) PWM_Drive_1	14:11	PWM_RATE [3:0]	0000	PWM Frequency (sample rate) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All PWMnMIX_SRCm registers should be set to 00h before changing PWM_RATE.
R144 0090h) Haptics_Control_1	14:11	HAP_RATE [3:0]	0000	Haptic Signal Generator Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz.
R160 (00A0h) Comfort_Noise_Generator	14:11	NOISE_GEN_RATE [3:0]	0000	Noise Generator Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz.
R776 (0308h) Input_Rate	14:11	IN_RATE [3:0]	0000	Input Signal Paths Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. If 384kHz/768kHz DMIC rate is selected on any of the input paths (INn_OSR=01X), then the Input Paths sample rate is valid up to 48kHz/96kHz respectively.
R1032 (0408h) Output_Rate_1	14:11	OUT_RATE [3:0]	0000	Output Signal Paths Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All OUTnxMIX_SRCm registers should be set to 00h before changing OUT_RATE.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1283 (0503h) AIF1_Rate _Ctrl	14:11	AIF1_RATE [3:0]	0000	AIF1 Audio Interface Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All AIF1TXMIX_SRCn registers should be set to 00h before changing AIF1_RATE.
R1347 (0543h) AIF2_Rate _Ctrl	14:11	AIF2_RATE [3:0]	0000	AIF2 Audio Interface Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All AIF2TXMIX_SRCn registers should be set to 00h before changing AIF2_RATE.
R1411 (0583h) AIF3_Rate _Ctrl	14:11	AIF3_RATE [3:0]	0000	AIF3 Audio Interface Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All AIF3TXMIX_SRCn registers should be set to 00h before changing AIF3_RATE.
R1443 (05A3h) AIF4_Rate _Ctrl	14:11	AIF4_RATE [3:0]	0000	AIF4 Audio Interface Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All AIF4TXMIX_SRCn registers should be set to 00h before changing AIF4_RATE.
R1474 (05C2h) SPD1_TX _Control	7:4	SPD1_RATE [3:0]	0000	S/PDIF Transmitter Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 All other codes are Reserved. The selected sample rate is valid in the range 32kHz to 192kHz. All SPDIF1TXn_SRC registers should be set to 00h before changing SPD1_RATE.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1509 (05E5h) SLIMbus_ Rates_1	14:11	SLIMRX2_RATE [3:0]	0000	SLIMbus RX Channel 2 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz.
	6:3	SLIMRX1_RATE [3:0]	0000	SLIMbus RX Channel 1 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz.
R1510 (05E6h) SLIMbus_ Rates_2	14:11	SLIMRX4_RATE [3:0]	0000	SLIMbus RX Channel 4 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz.
	6:3	SLIMRX3_RATE [3:0]	0000	SLIMbus RX Channel 3 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz.
R1511 (05E7h) SLIMbus_ Rates_3	14:11	SLIMRX6_RATE [3:0]	0000	SLIMbus RX Channel 6 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz.
	6:3	SLIMRX5_RATE [3:0]	0000	SLIMbus RX Channel 5 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1512 (05E8h) SLIMbus_ Rates_4	14:11	SLIMRX8_RATE [3:0]	0000	SLIMbus RX Channel 8 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz.
	6:3	SLIMRX7_RATE [3:0]	0000	SLIMbus RX Channel 7 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz.
R1513 (05E9h) SLIMbus_ Rates_5	14:11	SLIMTX2_RATE [3:0]	0000	SLIMbus TX Channel 2 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All SLIMTX2MIX_SRCn registers should be set to 00h before changing SLIMTX2_RATE.
	6:3	SLIMTX1_RATE [3:0]	0000	SLIMbus TX Channel 1 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All SLIMTX1MIX_SRCn registers should be set to 00h before changing SLIMTX1_RATE.
R1514 (05EAh) SLIMbus_ Rates_6	14:11	SLIMTX4_RATE [3:0]	0000	SLIMbus TX Channel 4 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All SLIMTX4MIX_SRCn registers should be set to 00h before changing SLIMTX4_RATE.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6:3	SLIMTX3_RATE [3:0]	0000	SLIMbus TX Channel 3 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All SLIMTX3MIX_SRCn registers should be set to 00h before changing SLIMTX3_RATE.
R1515 (05EBh) SLIMbus_ Rates_7	14:11	SLIMTX6_RATE [3:0]	0000	SLIMbus TX Channel 6 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All SLIMTX6MIX_SRCn registers should be set to 00h before changing SLIMTX6_RATE.
	6:3	SLIMTX5_RATE [3:0]	0000	SLIMbus TX Channel 5 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All SLIMTX5MIX_SRCn registers should be set to 00h before changing SLIMTX5_RATE.
R1516 (05ECh) SLIMbus_ Rates_8	14:11	SLIMTX8_RATE [3:0]	0000	SLIMbus TX Channel 8 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All SLIMTX8MIX_SRCn registers should be set to 00h before changing SLIMTX8_RATE.
	6:3	SLIMTX7_RATE [3:0]	0000	SLIMbus TX Channel 7 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All SLIMTX7MIX_SRCn registers should be set to 00h before changing SLIMTX7_RATE.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3584 (0E00h) FX_Ctrl1	14:11	FX_RATE [3:0]	0000	FX Sample Rate (EQ, LHPF, DRC) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All EQnMIX_SRCm, DRCnxMIX_SRCm, and LHPFnMIX_SRCm registers should be set to 00h before changing FX_RATE.
R1048064 (FFE00h) DSP1_Config_1	14:11	DSP1_RATE [3:0]	0000	DSP1 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All DSP1xMIX_SRCn registers should be set to 00h before changing DSP1_RATE.
R1572352 (17FE00h) DSP2_Config_1	14:11	DSP2_RATE [3:0]	0000	DSP2 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All DSP2xMIX_SRCn registers should be set to 00h before changing DSP2_RATE.
R2096640 (1FFE00h) DSP3_Config_1	14:11	DSP3_RATE [3:0]	0000	DSP3 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All DSP3xMIX_SRCn registers should be set to 00h before changing DSP3_RATE.
R2620928 (27FE00h) DSP4_Config_1	14:11	DSP4_RATE [3:0]	0000	DSP4 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All DSP4xMIX_SRCn registers should be set to 00h before changing DSP4_RATE.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3145216 (2FFE00h) DSP5_Config_1	14:11	DSP5_RATE [3:0]	0000	DSP5 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All DSP5xMIX_SRCn registers should be set to 00h before changing DSP5_RATE.
R3669504 (37FE00h) DSP6_Config_1	14:11	DSP6_RATE [3:0]	0000	DSP6 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All DSP6xMIX_SRCn registers should be set to 00h before changing DSP6_RATE.
R4193792 (3FFE00h) DSP7_Config_1	14:11	DSP7_RATE [3:0]	0000	DSP7 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All DSP7xMIX_SRCn registers should be set to 00h before changing DSP7_RATE.

Table 22 Digital Core Sample Rate Control

ASYNCHRONOUS SAMPLE RATE CONVERTER (ASRC)

The CS47L85 supports multiple signal paths through the digital core. Two independent clock domains are supported for the audio signal paths, referenced to SYSCLK and ASYNCCLK respectively, as described in “Clocking and Sample Rates”. Every digital signal path must be synchronised either to SYSCLK or to ASYNCCLK.

There are two Asynchronous Sample Rate Converters (ASRCs). Each ASRC provides two stereo signal paths between the SYSCLK and ASYNCCLK domains, as illustrated in Figure 38.

The sample rate on the SYSCLK domain is selected using the ASRCn_RATE1 registers - the rate can be set equal to SAMPLE_RATE_1, SAMPLE_RATE_2 or SAMPLE_RATE_3.

The sample rate on the ASYNCCLK domain is selected using the ASRCn_RATE2 registers - the rate can be set equal to ASYNC_SAMPLE_RATE_1 or ASYNC_SAMPLE_RATE_2.

See “Clocking and Sample Rates” for details of the sample rate control registers.

The ASRCn_RATE1 and ASRCn_RATE2 registers should not be changed if any of the respective *_SRC*n* registers is non-zero. The associated *_SRC*n* registers should be cleared to 00h before writing new values to ASRCn_RATE1 or ASRCn_RATE2. A minimum delay of 125us should be allowed between clearing the *_SRC*n* registers and writing to the associated ASRCn_RATE1 or ASRCn_RATE2 registers. See Table 23 for further details.

Each ASRC supports sample rates in the range 8kHz to 192kHz. For each ASRC, the ratio of the applicable SAMPLE_RATE_n and ASYNC_SAMPLE_RATE_n registers must not exceed 6.

The ASRC*n* IN1 (Left and Right) paths convert from the SYSCLK domain to the ASYNCCLK domain. These paths are enabled using the ASRC*n*_IN1L_ENA and ASRC*n*_IN1R_ENA register bits respectively.

The ASRC*n* IN2 (Left and Right) paths convert from the ASYNCCLK domain to the SYSCLK domain. These paths are enabled using the ASRC*n*_IN2L_ENA and ASRC*n*_IN2R_ENA register bits respectively.

Synchronisation (lock) between different clock domains is not instantaneous when the clocking or sample rate configurations are updated. The lock status of each ASRC path is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see “Interrupts”.

The ASRC Lock status of each ASRC path can be output directly on a GPIO pin as an external indication of ASRC Lock. See “General Purpose Input / Output” to configure a GPIO pin for this function.

The CS47L85 performs automatic checks to confirm that the SYSCLK or ASYNCCLK frequency is high enough to support the commanded ASRC and digital mixing functions. If an attempt is made to enable an ASRC signal path, and there are insufficient SYSCLK or ASYNCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The status bits in Register R3809 indicate the status of each of the ASRC signal paths. If an Underclocked Error condition occurs, then these bits provide readback of which ASRC signal path(s) have been successfully enabled.

The status bits in Registers R1600 to R3192 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

The Asynchronous Sample Rate Converter (ASRC) signal paths and control registers are illustrated in Figure 38.

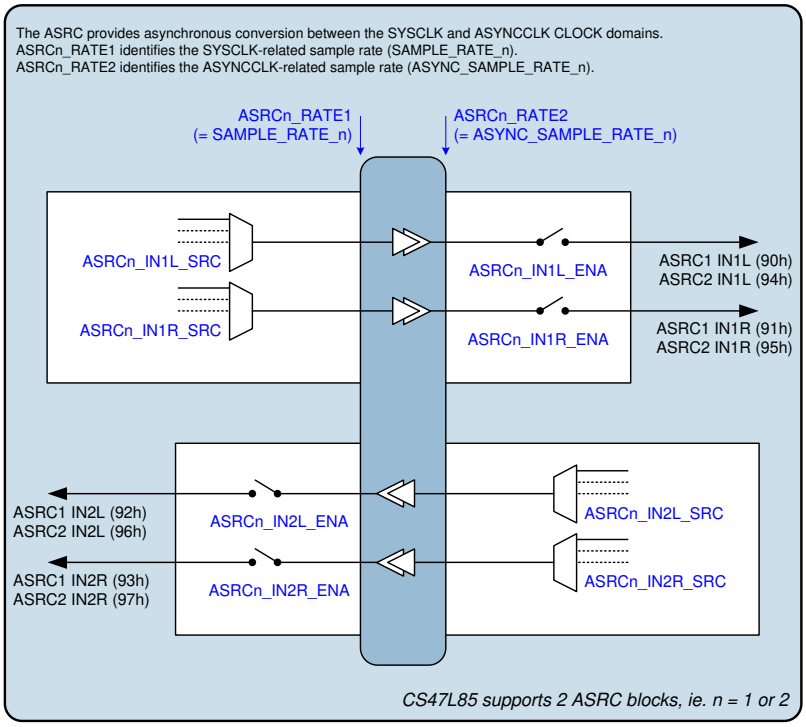


Figure 38 Asynchronous Sample Rate Converters (ASRCs)

The ASRC1 and ASRC2 input control registers (see Figure 38) are located at register addresses R2688 (A80h) through to R2744 (AB8h).

The full list of digital mixer control registers (Register R1600 through to R3192) is provided in a separate document - see "Register Map" for further information. Generic register definitions are provided in Table 8.

The *_SRC*n* registers select the input source(s) for the respective ASRC processing blocks. Note that the selected input source(s) must be configured for the same sample rate as the ASRC to which they are connected.

The bracketed numbers in Figure 38, e.g.,"(90h)" indicate the corresponding *_SRC*n* register setting for selection of that signal as an input to another digital core function.

The ASRC paths should be kept disabled (ASRC*n*_IN*mx*_ENA=0) if SYSCLK is not enabled. The *_SRC*n* registers for all digital core functions should be held at 00h if SYSCLK is not enabled – SYSCLK must be present and enabled before selecting other values for these registers. See "Clocking and Sample Rates" for further details (including requirements for reconfiguring SYSCLK while digital core functions are enabled).

The register bits associated with the ASRCs are described in Table 23.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3792 (0ED0h) ASRC2_ENABLE	3	ASRC2_IN2L_ENA	0	ASRC2 IN2 (Left) Enable (Left ASRC2 channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
	2	ASRC2_IN2R_ENA	0	ASRC2 IN2 (Right) Enable (Right ASRC2 channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
	1	ASRC2_IN1L_ENA	0	ASRC2 IN1 (Left) Enable (Left ASRC2 channel from SYSCLK domain to ASYNCCLK domain) 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	ASRC2_IN1R_ENA	0	ASRC2 IN1 (Right) Enable (Right ASRC2 channel from SYSCLK domain to ASYNCCLK domain) 0 = Disabled 1 = Enabled
R3793 (0ED1h) ASRC2_STATUS	3	ASRC2_IN2L_ENA_STS	0	ASRC2 IN2 (Left) Enable Status (Left ASRC2 channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
	2	ASRC2_IN2R_ENA_STS	0	ASRC2 IN2 (Right) Enable Status (Right ASRC2 channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
	1	ASRC2_IN1L_ENA_STS	0	ASRC2 IN1 (Left) Enable Status (Left ASRC2 channel from SYSCLK domain to ASYNCCLK domain) 0 = Disabled 1 = Enabled
	0	ASRC2_IN1R_ENA_STS	0	ASRC2 IN1 (Right) Enable Status (Right ASRC2 channel from SYSCLK domain to ASYNCCLK domain) 0 = Disabled 1 = Enabled
R3794 (0ED2h) ASRC2_RATE1	14:11	ASRC2_RATE1 [3:0]	0000	ASRC2 Sample Rate select for SYSCLK domain 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All ASRC2_IN1x_SRC registers should be set to 00h before changing ASRC2_RATE1.
R3795 (0ED3h) ASRC2_RATE2	14:11	ASRC2_RATE2 [3:0]	1000	ASRC2 Sample Rate select for ASYNCCLK domain 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All ASRC2_IN2x_SRC registers should be set to 00h before changing ASRC2_RATE2.
R3808 (0EE0h) ASRC1_ENABLE	3	ASRC1_IN2L_ENA	0	ASRC1 IN2 (Left) Enable (Left ASRC1 channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
	2	ASRC1_IN2R_ENA	0	ASRC1 IN2 (Right) Enable (Right ASRC1 channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1	ASRC1_IN1L_ENA	0	ASRC1 IN1 (Left) Enable (Left ASRC1 channel from SYSCLK domain to ASYNCCLK domain) 0 = Disabled 1 = Enabled
	0	ASRC1_IN1R_ENA	0	ASRC1 IN1 (Right) Enable (Right ASRC1 channel from SYSCLK domain to ASYNCCLK domain) 0 = Disabled 1 = Enabled
R3809 (0EE1h) ASRC1_STATUS	3	ASRC1_IN2L_ENA_STS	0	ASRC1 IN2 (Left) Enable Status (Left ASRC1 channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
	2	ASRC1_IN2R_ENA_STS	0	ASRC1 IN2 (Right) Enable Status (Right ASRC1 channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
	1	ASRC1_IN1L_ENA_STS	0	ASRC1 IN1 (Left) Enable Status (Left ASRC1 channel from SYSCLK domain to ASYNCCLK domain) 0 = Disabled 1 = Enabled
	0	ASRC1_IN1R_ENA_STS	0	ASRC1 IN1 (Right) Enable Status (Right ASRC1 channel from SYSCLK domain to ASYNCCLK domain) 0 = Disabled 1 = Enabled
R3810 (0EE2h) ASRC1_RATE1	14:11	ASRC1_RATE1 [3:0]	0000	ASRC1 Sample Rate select for SYSCLK domain 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All ASRC1_IN1x_SRC registers should be set to 00h before changing ASRC1_RATE1.
R3811 (0EE3h) ASRC1_RATE2	14:11	ASRC1_RATE2 [3:0]	1000	ASRC1 Sample Rate select for ASYNCCLK domain 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All ASRC1_IN2x_SRC registers should be set to 00h before changing ASRC1_RATE2.

Table 23 Digital Core ASRC Control

ISOCHRONOUS SAMPLE RATE CONVERTER (ISRC)

The CS47L85 supports multiple signal paths through the digital core. The Isochronous Sample Rate Converters (ISRCs) provide sample rate conversion between synchronised sample rates on the SYSCLK clock domain, or between synchronised sample rates on the ASYNCCLK clock domain.

There are four Isochronous Sample Rate Converters (ISRCs). ISRC1 and ISRC2 provide four signal paths between two different sample rates; ISRC3 and ISRC4 provide two signal paths between two different sample rates, as illustrated in Figure 39.

The sample rates associated with each ISRC can be set independently. Note that the two sample rates associated with any single ISRC must both be referenced to the same clock domain (SYSCLK or ASYNCCLK).

When an ISRC is used on the SYSCLK domain, then the associated sample rates may be selected from SAMPLE_RATE_1, SAMPLE_RATE_2 or SAMPLE_RATE_3.

When an ISRC is used on the ASYNCCLK domain, then the associated sample rates are ASYNC_SAMPLE_RATE_1 and ASYNC_SAMPLE_RATE_2.

See “Clocking and Sample Rates” for details of the sample rate control registers.

Each ISRC supports sample rates in the range 8kHz to 192kHz. The higher of the sample rates associated with each ISRC must be an integer multiple of the lower sample rate; all possible integer ratios are supported (i.e., up to 24).

Each ISRC converts between a sample rate selected by ISRCn_FSL and a sample rate selected by ISRCn_FSH, (where ‘n’ identifies the applicable ISRC 1, 2, 3 or 4). Note that, in each case, the higher of the two sample rates must be selected by ISRCn_FSH.

The ISRCn_FSL and ISRCn_FSH registers should not be changed if any of the respective *_SRC*n* registers is non-zero. The associated *_SRC*n* registers should be cleared to 00h before writing new values to ISRCn_FSL or ISRCn_FSH. A minimum delay of 125us should be allowed between clearing the *_SRC*n* registers and writing to the associated ISRCn_FSL or ISRCn_FSH registers. See Table 24 for further details.

The ISRC*n* ‘interpolation’ paths (increasing sample rate) are enabled using the ISRC*n*_INT*m*_ENA register bits, (where ‘*m*’ identifies the applicable channel).

The ISRC*n* ‘decimation’ paths (decreasing sample rate) are enabled using the ISRC*n*_DEC*m*_ENA register bits.

The CS47L85 performs automatic checks to confirm that the SYSCLK or ASYNCCLK frequency is high enough to support the commanded ISRC and digital mixing functions. If an attempt is made to enable an ISRC signal path, and there are insufficient SYSCLK or ASYNCCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The status bits in Registers R1600 to R3192 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

The Isochronous Sample Rate Converter (ISRC) signal paths and control registers are illustrated in Figure 39.

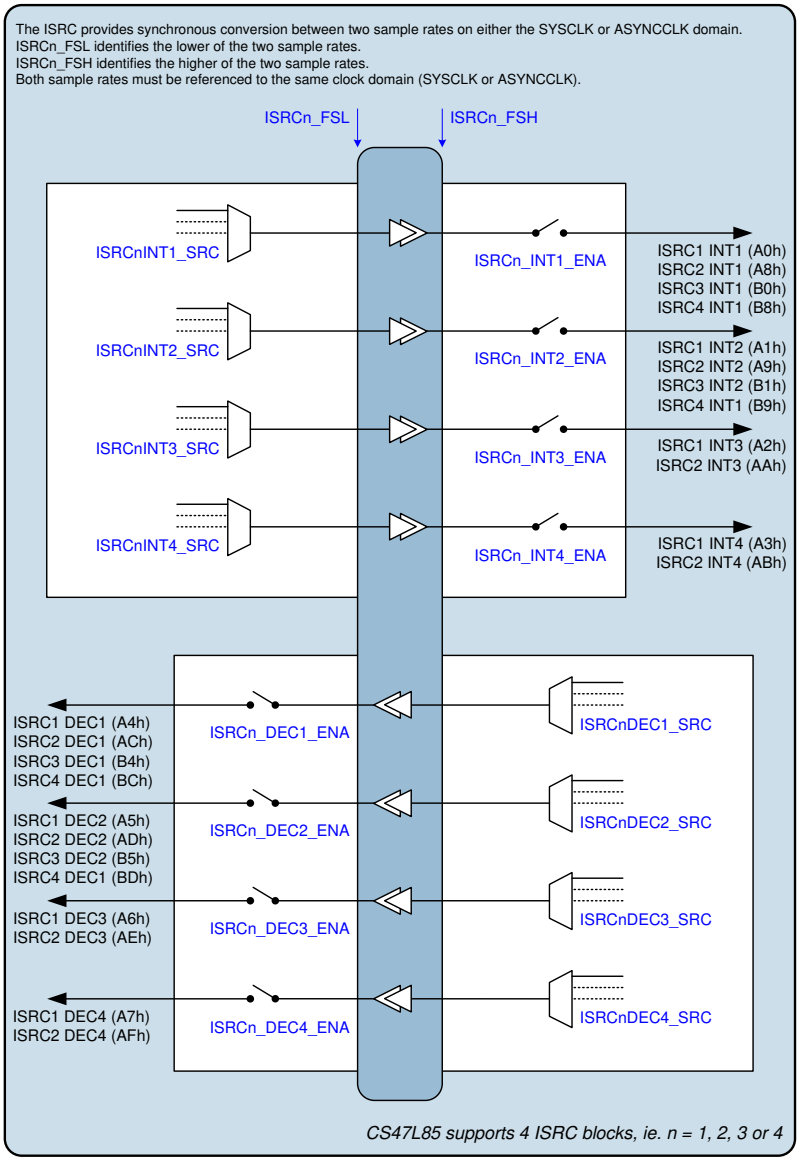


Figure 39 Isochronous Sample Rate Converters (ISRCs)

The ISRC input control registers (see Figure 39) are located at register addresses R2816 (B00h) through to R3015 (0BC7h).

The full list of digital mixer control registers (Register R1600 through to R3192) is provided in a separate document - see "Register Map" for further information. Generic register definitions are provided in Table 8.

The *_SRC registers select the input source(s) for the respective ISRC processing blocks. Note that the selected input source(s) must be configured for the same sample rate as the ISRC to which they are connected.

The bracketed numbers in Figure 39, e.g.,"(A4h)" indicate the corresponding *_SRC register setting for selection of that signal as an input to another digital core function.

The ISRC paths should be kept disabled (ISRC*n*_INT*m*_ENA=0, ISRC*n*_DEC*m*_ENA=0) if SYSCLK is not enabled. The *_SRC*n* registers for all digital core functions should be held at 00h if SYSCLK is not enabled. SYSCLK must be present and enabled before selecting other values for these registers. See "Clocking and Sample Rates" for further details (including requirements for reconfiguring SYSCLK while digital core functions are enabled).

The register bits associated with the ISRCs are described in Table 24.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3824 (0EF0h) ISRC1_CTRL_1	14:11	ISRC1_FSH [3:0]	0000	ISRC1 High Sample Rate (Sets the higher of the ISRC1 sample rates) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. The ISRC1_FSH and ISRC1_FSL fields must both select sample rates referenced to the same clock domain (SYSCLK or ASYNCCLK). All ISRC1_DECn_SRC registers should be set to 00h before changing ISRC1_FSH.
R3825 (0EF1h) ISRC1_CTRL_2	14:11	ISRC1_FSL [3:0]	0000	ISRC1 Low Sample Rate (Sets the lower of the ISRC1 sample rates) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. The ISRC1_FSH and ISRC1_FSL fields must both select sample rates referenced to the same clock domain (SYSCLK or ASYNCCLK). All ISRC1_INTn_SRC registers should be set to 00h before changing ISRC1_FSL.
R3826 (0EF2h) ISRC1_CTRL_3	15	ISRC1_INT1_ENA	0	ISRC1 INT1 Enable (Interpolation Channel 1 path from ISRC1_FSL rate to ISRC1_FSH rate) 0 = Disabled 1 = Enabled
	14	ISRC1_INT2_ENA	0	ISRC1 INT2 Enable (Interpolation Channel 2 path from ISRC1_FSL rate to ISRC1_FSH rate) 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	13	ISRC1_INT3_ENA	0	ISRC1 INT3 Enable (Interpolation Channel 3 path from ISRC1_FSL rate to ISRC1_FSH rate) 0 = Disabled 1 = Enabled
	12	ISRC1_INT4_ENA	0	ISRC1 INT4 Enable (Interpolation Channel 4 path from ISRC1_FSL rate to ISRC1_FSH rate) 0 = Disabled 1 = Enabled
	9	ISRC1_DEC1_ENA	0	ISRC1 DEC1 Enable (Decimation Channel 1 path from ISRC1_FSH rate to ISRC1_FSL rate) 0 = Disabled 1 = Enabled
	8	ISRC1_DEC2_ENA	0	ISRC1 DEC2 Enable (Decimation Channel 2 path from ISRC1_FSH rate to ISRC1_FSL rate) 0 = Disabled 1 = Enabled
	7	ISRC1_DEC3_ENA	0	ISRC1 DEC3 Enable (Decimation Channel 3 path from ISRC1_FSH rate to ISRC1_FSL rate) 0 = Disabled 1 = Enabled
	6	ISRC1_DEC4_ENA	0	ISRC1 DEC4 Enable (Decimation Channel 4 path from ISRC1_FSH rate to ISRC1_FSL rate) 0 = Disabled 1 = Enabled
R3827 (0EF3h) ISRC2_CTRL_1	14:11	ISRC2_FSH [3:0]	0000	ISRC2 High Sample Rate (Sets the higher of the ISRC2 sample rates) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. The ISRC2_FSH and ISRC2_FSL fields must both select sample rates referenced to the same clock domain (SYSCLK or ASYNCCLK). All ISRC2_DECn_SRC registers should be set to 00h before changing ISRC2_FSH.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3828 (0EF4h) ISRC2_CTRL_2	14:11	ISRC2_FSL [3:0]	0000	ISRC2 Low Sample Rate (Sets the lower of the ISRC2 sample rates) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. The ISRC2_FSH and ISRC2_FSL fields must both select sample rates referenced to the same clock domain (SYSCLK or ASYNCCLK). All ISRC2_INTn_SRC registers should be set to 00h before changing ISRC2_FSL.
R3829 (0EF5h) ISRC2_CTRL_3	15	ISRC2_INT1_ENA	0	ISRC2 INT1 Enable (Interpolation Channel 1 path from ISRC2_FSL rate to ISRC2_FSH rate) 0 = Disabled 1 = Enabled
	14	ISRC2_INT2_ENA	0	ISRC2 INT2 Enable (Interpolation Channel 2 path from ISRC2_FSL rate to ISRC2_FSH rate) 0 = Disabled 1 = Enabled
	13	ISRC2_INT3_ENA	0	ISRC2 INT3 Enable (Interpolation Channel 3 path from ISRC2_FSL rate to ISRC2_FSH rate) 0 = Disabled 1 = Enabled
	12	ISRC2_INT4_ENA	0	ISRC2 INT4 Enable (Interpolation Channel 4 path from ISRC2_FSL rate to ISRC2_FSH rate) 0 = Disabled 1 = Enabled
	9	ISRC2_DEC1_ENA	0	ISRC2 DEC1 Enable (Decimation Channel 1 path from ISRC2_FSH rate to ISRC2_FSL rate) 0 = Disabled 1 = Enabled
	8	ISRC2_DEC2_ENA	0	ISRC2 DEC2 Enable (Decimation Channel 2 path from ISRC2_FSH rate to ISRC2_FSL rate) 0 = Disabled 1 = Enabled
	7	ISRC2_DEC3_ENA	0	ISRC2 DEC3 Enable (Decimation Channel 3 path from ISRC2_FSH rate to ISRC2_FSL rate) 0 = Disabled 1 = Enabled
	6	ISRC2_DEC4_ENA	0	ISRC2 DEC4 Enable (Decimation Channel 4 path from ISRC2_FSH rate to ISRC2_FSL rate) 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3830 (0EF6h) ISRC3_CTRL_1	14:11	ISRC3_FSH [3:0]	0000	ISRC3 High Sample Rate (Sets the higher of the ISRC3 sample rates) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. The ISRC3_FSH and ISRC3_FSL fields must both select sample rates referenced to the same clock domain (SYSCLK or ASYNCCLK). All ISRC3_DECn_SRC registers should be set to 00h before changing ISRC3_FSH.
R3831 (0EF7h) ISRC3_CTRL_2	14:11	ISRC3_FSL [3:0]	0000	ISRC3 Low Sample Rate (Sets the lower of the ISRC3 sample rates) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. The ISRC3_FSH and ISRC3_FSL fields must both select sample rates referenced to the same clock domain (SYSCLK or ASYNCCLK). All ISRC3_INTn_SRC registers should be set to 00h before changing ISRC3_FSL.
R3832 (0EF8h) ISRC3_CTRL_3	15	ISRC3_INT1_ENA	0	ISRC3 INT1 Enable (Interpolation Channel 1 path from ISRC3_FSL rate to ISRC3_FSH rate) 0 = Disabled 1 = Enabled
	14	ISRC3_INT2_ENA	0	ISRC3 INT2 Enable (Interpolation Channel 2 path from ISRC3_FSL rate to ISRC3_FSH rate) 0 = Disabled 1 = Enabled
	9	ISRC3_DEC1_ENA	0	ISRC3 DEC1 Enable (Decimation Channel 1 path from ISRC3_FSH rate to ISRC3_FSL rate) 0 = Disabled 1 = Enabled
	8	ISRC3_DEC2_ENA	0	ISRC3 DEC2 Enable (Decimation Channel 2 path from ISRC3_FSH rate to ISRC3_FSL rate) 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3833 (0EF9h) ISRC4_CTRL_1	14:11	ISRC4_FSH [3:0]	0000	ISRC4 High Sample Rate (Sets the higher of the ISRC4 sample rates) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. The ISRC4_FSH and ISRC4_FSL fields must both select sample rates referenced to the same clock domain (SYSCLK or ASYNCCLK). All ISRC4_DECn_SRC registers should be set to 00h before changing ISRC4_FSH.
R3834 (0EFAh) ISRC4_CTRL_2	14:11	ISRC4_FSL [3:0]	0000	ISRC4 Low Sample Rate (Sets the lower of the ISRC4 sample rates) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. The ISRC4_FSH and ISRC4_FSL fields must both select sample rates referenced to the same clock domain (SYSCLK or ASYNCCLK). All ISRC4_INTn_SRC registers should be set to 00h before changing ISRC4_FSL.
R3835 (0EFBh) ISRC4_CTRL_3	15	ISRC4_INT1_ENA	0	ISRC4 INT1 Enable (Interpolation Channel 1 path from ISRC4_FSL rate to ISRC4_FSH rate) 0 = Disabled 1 = Enabled
	14	ISRC4_INT2_ENA	0	ISRC4 INT2 Enable (Interpolation Channel 2 path from ISRC4_FSL rate to ISRC4_FSH rate) 0 = Disabled 1 = Enabled
	9	ISRC4_DEC1_ENA	0	ISRC4 DEC1 Enable (Decimation Channel 1 path from ISRC4_FSH rate to ISRC4_FSL rate) 0 = Disabled 1 = Enabled
	8	ISRC4_DEC2_ENA	0	ISRC4 DEC2 Enable (Decimation Channel 2 path from ISRC4_FSH rate to ISRC4_FSL rate) 0 = Disabled 1 = Enabled

Table 24 Digital Core ISRC Control

DSP FIRMWARE CONTROL

The CS47L85 digital core incorporates seven DSP processing blocks, capable of running a wide range of audio enhancement functions. Different firmware configurations can be loaded onto each DSP, enabling the CS47L85 to be highly customised for specific application requirements. Full read/write access to the device register map is supported from each DSP core, including access to the firmware registers of the other DSPs. Synchronisation of different DSPs is supported, and shared data memory space is provided for the DSP2 and DSP3 blocks; these features enable enhanced processing capabilities for the associated DSPs.

Examples of the DSP functions include Virtual Surround Sound (VSS), Multiband Compressor (MBC), and the Cirrus Logic SoundClear® suite of audio processing algorithms. Note that it is possible to implement more than one type of audio enhancement function on a single DSP; the precise combination(s) of functions will vary from one firmware configuration to another.

The DSP blocks each employ the same internal architecture, and provide an equivalent processing capability. Note that the DSPs differ in terms of the firmware memory sizes associated with each. DSPs 1 to 5 can be clocked at up to 150MHz, corresponding to 150 MIPS each. DSP6 and DSP7 are designed for low power operation, clocked at up to 75MHz each. The DSP6 core is optimised for always-on (voice trigger) software functions.

DSP firmware can be configured using Cirrus Logic-supplied software packages. A software programming guide can also be provided to assist users in developing their own software algorithms - please contact your local Cirrus Logic representative for further information.

In order to use the DSP blocks, the required firmware configuration must first be loaded onto the device by writing the appropriate files to the CS47L85 register map. The firmware configuration will comprise Program, Coefficient and Data content. In some cases, the Coefficient content must be derived using tools provided in Cirrus Logic's WISCE evaluation board control software.

Details of how to load the firmware configuration onto the CS47L85 are described below. Note that the WISCE evaluation board control software provides support for easy loading of Program, Coefficient and Data content onto the CS47L85. Please contact your local Cirrus Logic representative for more details of the WISCE evaluation board control software.

After loading the DSP firmware, the DSP functions must be enabled using the associated register control fields.

The audio signal paths connecting to/from the DSP processing blocks are configured as described in the "Digital Core" section. Note that the DSP firmware must be loaded and enabled before audio signal paths can be enabled.

DSP FIRMWARE MEMORY AND REGISTER MAPPING

The DSP firmware memory is programmed by writing to the registers referenced in Table 25. Note that clocking is not required for access to the firmware registers by the host processor.

The CS47L85 Program, Coefficient and Data register memory space is described in Table 25. The full register map listing is provided in a separate document - see "Register Map" for further information. The shared DSP2/DSP3 memory space is implemented at two different register address locations; reading or writing at either address will access the same memory data.

If multiple DSPs write to a shared memory address at the same time, then the address at which the collision occurred will be reported in the DSP3_DUALMEM_COLLISION_ADDR register. Note that this field is coded in 24-bit DSP data word units, and is defined relative to the base address of the applicable shared memory area.

The DSP memory controller provides an input to the Interrupt control circuit. An interrupt event is triggered if a memory collision occurs. (Note that the DSP software should be written to ensure this never happens; the interrupt is intended for development purposes only.) See "Interrupts" for more details of the Interrupt event handling.

The Program firmware parameters are formatted as 40-bit words. For this reason, 3 x 32-bit register addresses are required for every 2 x 40-bit words.

	DESCRIPTION	REGISTER ADDRESS		DSP MEMORY SIZE
DSP1	Program memory	08_0000h to 08_5FFEh	(12288 registers)	8k x 40-bit words
	X Data memory	0A_0000h to 0A_7FFEh	(16384 registers)	16k x 24-bit words
	Y Data memory	0C_0000h to 0C_1FFEh	(4096 registers)	4k x 24-bit words
	Coefficient memory	0E_0000h to 0E_1FFEh	(4096 registers)	4k x 24-bit words
DSP2	Program memory	10_0000h to 10_EFFEh	(30720 registers)	20k x 40-bit words
	X Data memory	12_0000h to 12_BFFEh	(24576 registers)	24k x 24-bit words
	X Data memory (Shared DSP2/DSP3)	13_6000h to 13_7FFEh	(4096 registers)	4k x 24-bit words
	Y Data memory	14_0000h to 14_BFFEh	(24576 registers)	24k x 24-bit words
	Coefficient memory	16_0000h to 16_1FFEh	(4096 registers)	4k x 24-bit words
DSP3	Program memory	18_0000h to 18_EFFEh	(30720 registers)	20k x 40-bit words
	X Data memory	1A_0000h to 1B_1FFEh	(36864 registers)	36k x 24-bit words
	X Data memory (Shared DSP2/DSP3)	1B_6000h to 1B_7FFEh	(4096 registers)	4k x 24-bit words
	Y Data memory	1C_0000h to 1C_BFFEh	(24576 registers)	24k x 24-bit words
	Coefficient memory	1E_0000h to 1E_1FFEh	(4096 registers)	4k x 24-bit words
DSP4	Program memory	20_0000h to 20_8FFEh	(18432 registers)	12k x 40-bit words
	X Data memory	22_0000h to 23_1FFEh	(36864 registers)	36k x 24-bit words
	Y Data memory	24_0000h to 24_BFFEh	(24576 registers)	24k x 24-bit words
	Coefficient memory	26_0000h to 26_1FFEh	(4096 registers)	4k x 24-bit words
DSP5	Program memory	28_0000h to 28_8FFEh	(18432 registers)	12k x 40-bit words
	X Data memory	2A_0000h to 2A_9FFEh	(20480 registers)	20k x 24-bit words
	Y Data memory	2C_0000h to 2C_3FFEh	(8192 registers)	8k x 24-bit words
	Coefficient memory	2E_0000h to 2E_1FFEh	(4096 registers)	4k x 24-bit words
DSP6	Program memory	30_0000h to 30_5FFEh	(12288 registers)	8k x 40-bit words
	X Data memory	32_0000h to 33_3FFEh	(40960 registers)	40k x 24-bit words
	Y Data memory	34_0000h to 34_BFFEh	(24576 registers)	24k x 24-bit words
	Coefficient memory	36_0000h to 36_1FFEh	(4096 registers)	4k x 24-bit words
DSP7	Program memory	38_0000h to 38_8FFEh	(18432 registers)	12k x 40-bit words
	X Data memory	3A_0000h to 3A_7FFEh	(16384 registers)	16k x 24-bit words
	Y Data memory	3C_0000h to 3C_1FFEh	(4096 registers)	4k x 24-bit words
	Coefficient memory	3E_0000h to 3E_1FFEh	(4096 registers)	4k x 24-bit words

Table 25 DSP Program, Coefficient and Data Registers

The X-Memory on each DSP supports read/write access to all register fields throughout the device - including the CODEC control registers, and the firmware memory of all of the integrated DSP cores. Access to the register address space is supported using a number of register 'windows' within the X-Memory on each DSP.

The register window space is additional to the X Data memory sizes described in Table 25. Note that the X-memory addresses of these register windows are the same for all DSP cores - regardless of the different X-memory sizes.

Addresses 0xC000 to 0xDFFF in X-Memory map directly to addresses 0x0000 to 0x1FFF in the device register space. This fixed register window contains primarily the CODEC control registers; it also includes the 'Virtual DSP' control registers (described later in this section). Each X-Memory address within this window maps onto one 16-bit register in the CODEC memory space.

Four moveable register windows are also provided, starting at X-Memory addresses 0xF000, 0xF400, 0xF800, and 0xFC00 respectively. Each window represents 1024 addresses in the X-Memory space. The start address, within the corresponding device register space, for each window is configured using the DSPn_EXT_[A/B/C/D]_PAGE registers (where 'A' defines the first window, 'B' defines the second window, etc.).

Two different mapping modes are supported, selected using the DSPn_EXT_[A/B/C/D]_PSIZE16 control bits for the respective window. In 16-bit mode, each address within the window maps onto one 16-bit register in the device memory space; the window equates to 1024 x 16-bit registers. In 32-bit mode, each address within the window maps onto two 16-bit registers in the device memory space; the window equates to 1024 x 32-bit registers.

Note that the X-Memory is only 24-bits wide; as a result, the upper 8 bits of the odd-numbered register addresses are not mapped, and cannot be accessed, in 32-bit mode.

The DSPn_EXT_[A/B/C/D]_PAGE registers are defined with an LSB = 512. Accordingly, the base address of each window

must be aligned with 512-word boundaries. Note that the base addresses are entirely independent of each other; for example, overlapping windows are permissible if required, and there is no requirement for the A/B/C/D windows to be at incremental locations.

The register map window functions are illustrated in Figure 40. Further information on the definition and usage of the DSP firmware memories is provided in the software programming guide - please contact your local Cirrus Logic representative if required.

Note that SYSCLK must be present and enabled, if the DSP firmware requires read or write access to control registers below address 0x40000. See “Clocking and Sample Rates” for further details of the CS47L85 system clocks.

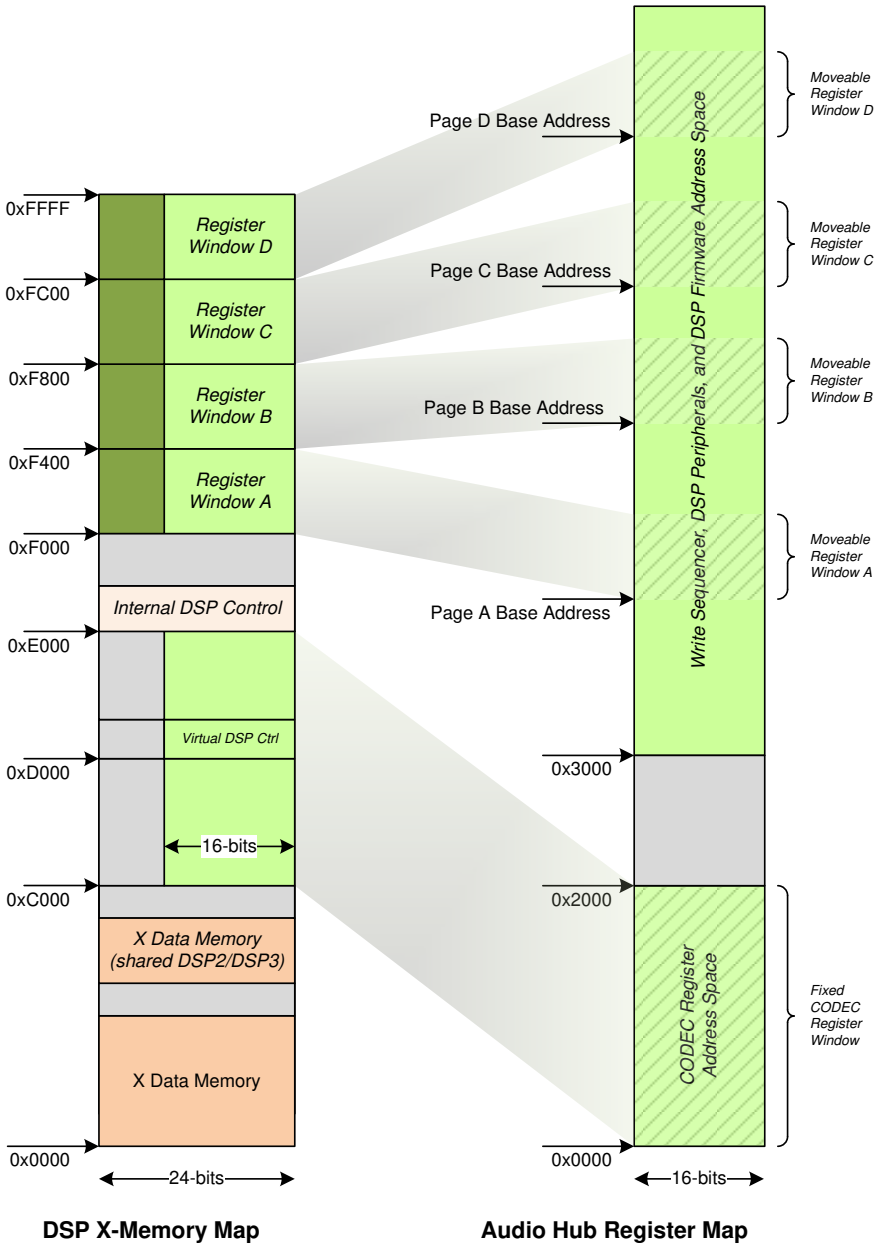


Figure 40 X Data Memory Map

Note that the full CS47L85 register space is illustrated here as 16-bit width. (SPI/I2C/SLIMbus register access uses 32-bit data width at 0x3000 and above.) However, the window ‘Base Address’ registers are referenced to 16-bit width, and 16-bit register mapping is shown. Hence, the device register map is shown here entirely as 16-bit width for ease of explanation.

The control registers associated with the register map window functions are described in Table 26.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
DSP1 Base Address = R1048064 (0FFE00h) DSP2 Base Address = R1572352 (17FE00h) DSP3 Base Address = R2096640 (1FFE00h) DSP4 Base Address = R2620928 (27FE00h) DSP5 Base Address = R3145216 (2FFE00h) DSP6 Base Address = R3669504 (37FE00h) DSP7 Base Address = R4193792 (3FFE00h)				
base address + 54h DSPn_Ext_window_A	31	DSPn_EXT_A_PSIZE16	0	Register Window A page width select 0 = 32-bit 1 = 16-bit Note that, in 32-bit mode, only the lower 24 bits can be accessed.
	15:0	DSPn_EXT_A_PAGE [15:0]	0000h	Sets the Base Address of Register Window A in X-Memory. Coded as LSB = 512 (200h)
base address + 56h DSPn_Ext_window_B	31	DSPn_EXT_B_PSIZE16	0	Register Window B page width select 0 = 32-bit 1 = 16-bit Note that, in 32-bit mode, only the lower 24 bits can be accessed.
	15:0	DSPn_EXT_B_PAGE [15:0]	0000h	Sets the Base Address of Register Window B in X-Memory. Coded as LSB = 512 (200h)
base address + 58h DSPn_Ext_window_C	31	DSPn_EXT_C_PSIZE16	0	Register Window C page width select 0 = 32-bit 1 = 16-bit Note that, in 32-bit mode, only the lower 24 bits can be accessed.
	15:0	DSPn_EXT_C_PAGE [15:0]	0000h	Sets the Base Address of Register Window C in X-Memory. Coded as LSB = 512 (200h)
base address + 5Ah DSPn_Ext_window_D	31	DSPn_EXT_D_PSIZE16	0	Register Window D page width select 0 = 32-bit 1 = 16-bit Note that, in 32-bit mode, only the lower 24 bits can be accessed.
	15:0	DSPn_EXT_D_PAGE [15:0]	0000h	Sets the Base Address of Register Window D in X-Memory. Coded as LSB = 512 (200h)

Table 26 X Data Memory Window Control

DSP FIRMWARE CONTROL

The DSP memory (Program, Coefficient, X-Data, and Y-Data) is enabled using the DSPn_MEM_ENA register bit for the respective DSP. This memory must be enabled (DSPn_MEM_ENA=1) for read/write access, code execution, and DMA functions. The DSP memory is disabled, and the contents lost, whenever the respective DSPn_MEM_ENA bit is set to 0.

The DSP6_MEM_ENA bit has no function; the DSP6 memory is enabled at all times during normal operation.

The DSPn_MEM_ENA bits are not affected by Software Reset; these bits will remain in their previous state under Software Reset conditions. Accordingly, the DSP memory contents will be maintained through Software Reset, provided DCVDD is held above its reset threshold.

On DSP1 to DSP5, and on DSP7, the DSP firmware memory is cleared under Hardware Reset conditions. For DSP6 only, the contents of the DSP memory are retained during Hardware Reset, provided DCVDD is held above its reset threshold.

The DSP firmware memory is always cleared under Power-On Reset (POR), and ‘Sleep’ mode conditions. See the “Applications Information” section for a summary of the CS47L85 reset behaviour.

Clocking is required for each of the DSP processing blocks, when executing software or when supporting DMA functions. (Note that clocking is not required for access to the firmware registers by the host processor.)

Clocking within each DSP is enabled and disabled automatically, as required by the respective DSP Core and DMA channel status.

The clock source for each DSP is derived from DSPCLK. See “Clocking and Sample Rates” for details of how to configure DSPCLK.

The clock frequency for each DSP is selected using the DSPn_CLK_SEL register (where ‘n’ identifies the applicable DSP block, 1 to 7). The DSP clock frequency must be less than or equal to the DSPCLK frequency. For DSP6 and DSP7, the maximum DSP clock frequency is 75MHz.

Note that the DSPn_CLK_SEL fields select a range of frequencies for each valid decode value. The clock frequency for each DSP will be derived as DSPCLK divided by 1, 2, 4, 8, or 16. The required division ratios, within the selected DSP clock frequency ranges, are configured automatically for each DSP core.

The DSPn_CLK_SEL_STS fields provide readback of the clock frequency range for the respective DSP cores. These can be used to confirm the clock frequency, in cases where code execution has a minimum clock frequency requirement. The DSPn_CLK_SEL_STS field is only valid when the respective core is running code; typical usage of this field would be for the DSP core itself to readback the clock status, and to take action as applicable (in particular, if the available clock does not meet the application requirements).

Note that the DSPn_CLK_SEL_STS fields indicate a range of frequencies for each decode value. The exact clock frequency for each DSP cannot be provided directly by the CS47L85, but can be derived using knowledge of the DSPCLK frequency, if available.

After the DSP firmware has been loaded, and the clocks configured, the DSP blocks are enabled using the DSPn_CORE_ENA register bits. When the DSP is configured and enabled, the firmware execution can be started by writing ‘1’ to the respective DSPn_START bit.

Alternative methods to trigger the firmware execution can also be configured using the DSPn_START_IN_SEL register fields. Note that this provides the capability to synchronously trigger multiple DSP blocks.

Using the DSPn_START_IN_SEL registers, the DSP firmware execution can be linked to the respective DMA function, the IRQ2 status, ‘DSPn Start’ signals from another DSP, or to the FIFO status in one of the Event Loggers:

- DMA function - firmware execution commences when all enabled DSP input (WDMA) channel buffers have been filled, and all enabled DSP output (RDMA) channel buffers have been emptied
- DSPn Start signals - firmware execution commences when the respective Start signal is triggered in the selected DSP core (1 to 4 only)
- IRQ2 - firmware execution commences when one or more of the unmasked IRQ2 events has occurred
- Event Logger status - firmware execution commences when the FIFO ‘Not Empty’ status is asserted within the respective Event Logger

The DSPn_CORE_ENA bit must be set to ‘1’ to enable firmware execution on the respective DSP block. Note that the usage of the DSPn_START bit may vary depending on the particular firmware that is being executed: in some applications (e.g., when an alternative trigger is selected using DSPn_START_IN_SEL), writing to the DSPn_START bit will not be required.

The DSPCLK system clock must be configured and enabled before any DSP processing core is enabled. The DSP blocks should be kept disabled (DSPn_CORE_ENA=0) if DSPCLK is not enabled. See “Clocking and Sample Rates” for details of the system clocks (including requirements for reconfiguring DSPCLK while DSP cores are enabled).

The audio signal paths connecting to/from the DSP processing blocks are configured as described in the “Digital Core” section. Note that the DSP firmware must be loaded and enabled before audio signal paths can be enabled.

The DSP memory and clocking control registers are described in Table 27.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
DSP1 Base Address = R1048064 (0FFE00h) DSP2 Base Address = R1572352 (17FE00h) DSP3 Base Address = R2096640 (1FFE00h) DSP4 Base Address = R2620928 (27FE00h) DSP5 Base Address = R3145216 (2FFE00h) DSP6 Base Address = R3669504 (37FE00h) DSP7 Base Address = R4193792 (3FFE00h)				
base address DSPn_Config_1	18:16	DSPn_CLK_SEL [2:0]	000	DSPn Clock Frequency Select 000=5.5MHz to 9.375MHz 001=9.375MHz to 18.75MHz 010=18.75MHz to 37.5MHz 011=37.5MHz to 75MHz 100=75MHz to 150MHz All other codes are Reserved **[DSP6, DSP7]** – valid codes are 000 to 011 only. Note that, because DSPCLK could be any frequency (within the valid ranges), it is not possible to quote exact frequencies in this register definition. The DSPn Clock must be less than or equal to the DSPCLK frequency. The exact frequency will be derived as DSPCLK divided by 1, 2, 4, 8, or 16.
	4	DSPn_MEM_ENA	0	DSPn Memory Control 0 = Disabled 1 = Enabled The DSPn memory contents are lost when DSPn_MEM_ENA=0. Note that this bit is not affected by Software Reset; it will remain in its previous condition. **[DSP6 only]** – This bit has no function; DSP6 memory is enabled at all times.
	1	DSPn_CORE_ENA	0	DSPn Enable Controls the DSPn firmware execution 0 = Disabled 1 = Enabled
	0	DSPn_START		DSPn Start Write '1' to Start DSPn firmware execution
base address +06h DSPn_Status_2	31:16	DSPn_DUALMEM_COLLISION_ADDR [15:0]	0000h	DSPn Dual Memory Collision Address In the event of a DSPn memory access collision, this field will report the address at which the collision occurred. The address is defined relative to the base address of the shared data memory. The LSB represents one 24-bit DSP memory word.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:1	DSPn_CLK_SEL_STS [2:0]	000	DSPn Clock Frequency (Read only, Only valid when the respective DSP Core is enabled) 000=5.5MHz to 9.375MHz 001=9.375MHz to 18.75MHz 010=18.75MHz to 37.5MHz 011=37.5MHz to 75MHz 100=75MHz to 150MHz All other codes are Reserved Note that, because DSPCLK could be any frequency (within the valid ranges), it is not possible to quote exact frequencies in this register definition. The exact frequency will be derived as DSPCLK divided by 1, 2, 4, 8, or 16.
	0	DSPn_CLK_AVAIL	0	DSPn Clock Availability (Read only) 0 = No Clock 1 = Clock Available Note – this bit exists for legacy software support only; it is not recommended for future designs, as the readback may be unreliable on the latest device architectures.
base address +38h DSPn_External_Start	4:0	DSPn_START_IN_SEL [4:0]	00h	DSPn Firmware Execution control Selects the trigger for DSPn firmware execution. 00h = DMA 01h = DSP1 Start 1 02h = DSP1 Start 1 03h = DSP2 Start 1 04h = DSP2 Start 2 05h = DSP3 Start 1 06h = DSP3 Start 2 07h = DSP4 Start 1 08h = DSP4 Start 2 0Bh = IRQ2 10h = Event Logger 1 11h = Event Logger 2 12h = Event Logger 3 13h = Event Logger 4 14h = Event Logger 5 15h = Event Logger 6 16h = Event Logger 7 17h = Event Logger 8 All other codes are Reserved. Note that the DSPn_START bit will also start the DSPn firmware execution, regardless of this register setting.

Table 27 DSP Memory and Clocking Control

DSP DIRECT MEMORY ACCESS (DMA) CONTROL

Each DSP provides a multi-channel DMA function; this is configured using the registers described in Table 28.

There are 8 WDMA (DSP input) and 6 RDMA (DSP output) channels for each DSP; these are enabled using the DSPn_WDMA_CHANNEL_ENABLE and DSPn_RDMA_CHANNEL_ENABLE fields. The status of each WDMA channel is indicated in DSPn_WDMA_ACTIVE_CHANNELS.

The DMA can access the X data memory or Y data memory associated with the respective DSP. The applicable memory is selected using bit [15] of the respective *_START_ADDRESS register.

The start address of each DMA channel is configured as described in Table 28. Note that the required address is defined relative to the base address of the selected (X data or Y data) memory.

The buffer length of the DMA channels is configured using the DSPn_DMA_BUFFER_LENGTH field. The selected buffer length applies to all enabled DMA channels.

Note that the start address registers, and buffer length registers, are defined in 24-bit DSP data word units. This means that the LSB of these fields represents one 24-bit DSP memory word. (Note that this differs from the CS47L85 register map layout, as described in Table 25).

The parameters of a DMA channel (i.e., Start Address or Offset Address) must not be changed whilst the respective DMA is enabled. All of the DMA channels must be disabled before changing the DMA buffer length.

Each DMA channel uses a twin buffer mechanism to support uninterrupted data flow through the DSP. The buffers are called 'ping' and 'pong' respectively, and are of configurable size, as noted above. Data is transferred to/from each of the buffers in turn.

When the 'ping' input data buffer is full, the DSPn_PING_FULL bit will be asserted (set to '1'), and a 'DSP Start' signal will be generated. The 'Start' signal from the DMA is typically used to start Firmware execution, as noted in Table 27. Meanwhile, further DSP input data will be filling up the 'pong' buffer.

When the 'pong' input buffer is full, the DSPn_PONG_FULL bit will be asserted, and another 'DSP Start' signal will be generated. The DSP Firmware must take care to read the input data from the applicable buffer, in accordance with the DSPn_PING_FULL and DSPn_PONG_FULL status bits.

Twin buffers are also used on the DSP output (RDMA) channels. The output 'ping' buffers are emptied at the same time as the input 'ping' buffers are filled; the output 'pong' buffers are emptied at the same time as the input 'pong' buffers are filled.

The DSP cores support 24-bit signal processing. Under default conditions, the DSP audio data is in 2's complement Q3.20 format (ie. 0xF00000 corresponds to the -1.0 level, and 0x100000 corresponds to the +1.0 level; a sine wave with peak values of +/-1.0 corresponds to the 0 dBFS level). If DSP*n*_DMA_WORD_SEL is set, audio data is transferred to and from DSP*n* in Q0.23 format. The applicable format should be set according to the requirements of the specific DSP firmware.

Note that the DSP cores are optimised for Q3.20 audio data processing; Q0.23 data can be supported, but the firmware implementation may incur a reduction in power efficiency due to the higher MIPS required for arithmetic operations in non-native data word format.

The DSPCLK system clock must be configured and enabled before any DMA channel is enabled. The DMA channels should be kept disabled (DSPn_[WDMA/RDMA]_CHANNEL_ENABLE=00h) if DSPCLK is not enabled. See "Clocking and Sample Rates" for details of the system clocks (including requirements for reconfiguring DSPCLK while DMA channels are enabled).

Further details of the DMA are provided in the software programming guide - please contact your local Cirrus Logic representative if required.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
DSP1 Base Address = R1048064 (0FFE00h) DSP2 Base Address = R1572352 (17FE00h) DSP3 Base Address = R2096640 (1FFE00h) DSP4 Base Address = R2620928 (27FE00h) DSP5 Base Address = R3145216 (2FFE00h) DSP6 Base Address = R3669504 (37FE00h) DSP7 Base Address = R4193792 (3FFE00h)				
base address +04h DSPn_Status_1	31	DSPn_PING_FULL	0	DSPn WDMA Ping Buffer Status 0 = Not Full 1 = Full
	30	DSPn_PONG_FULL	0	DSPn WDMA Pong Buffer Status 0 = Not Full 1 = Full

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	23:16	DSPn_WDMA_ACTIVE_CHANNELS [7:0]	00h	DSPn WDMA Channel Status There are 8 WDMA channels; each bit of this field indicates the status of the respective WDMA channel. Each bit is coded as: 0 = Inactive 1 = Active
base address +10h DSPn_WDMA_Buffer_1	31:16	DSPn_START_ADDRESS_WDMA_BUFFER_1 [15:0]	0000h	DSPn WDMA Channel 1 Start Address Bit [15] = Memory select 0 = X Data memory 1 = Y Data memory Bits [14:0] = Address select The address is defined relative to the base address of the applicable data memory. The LSB represents one 24-bit DSP memory word. Note that the start address is also controlled by the respective DSPn_WDMA_CHANNEL_OFFSET bit.
	15:0	DSPn_START_ADDRESS_WDMA_BUFFER_0 [15:0]	0000h	DSPn WDMA Channel 0 Start Address *Register description is as above.*
base address +12h DSPn_WDMA_Buffer_2	31:16	DSPn_START_ADDRESS_WDMA_BUFFER_3 [15:0]	0000h	DSPn WDMA Channel 3 Start Address *Register description is as above.*
	15:0	DSPn_START_ADDRESS_WDMA_BUFFER_2 [15:0]	0000h	DSPn WDMA Channel 2 Start Address *Register description is as above.*
base address +14h DSPn_WDMA_Buffer_3	31:16	DSPn_START_ADDRESS_WDMA_BUFFER_5 [15:0]	0000h	DSPn WDMA Channel 5 Start Address *Register description is as above.*
	15:0	DSPn_START_ADDRESS_WDMA_BUFFER_4 [15:0]	0000h	DSPn WDMA Channel 4 Start Address *Register description is as above.*
base address +16h DSPn_WDMA_Buffer_4	31:16	DSPn_START_ADDRESS_WDMA_BUFFER_7 [15:0]	0000h	DSPn WDMA Channel 7 Start Address *Register description is as above.*
	15:0	DSPn_START_ADDRESS_WDMA_BUFFER_6 [15:0]	0000h	DSPn WDMA Channel 6 Start Address *Register description is as above.*
base address +20h DSPn_RDMA_Buffer_1	31:16	DSPn_START_ADDRESS_RDMA_BUFFER_1 [15:0]	0000h	DSPn RDMA Channel 1 Start Address Bit [15] = Memory select 0 = X Data memory 1 = Y Data memory Bits [14:0] = Address select The address is defined relative to the base address of the applicable data memory. The LSB represents one 24-bit DSP memory word. Note that the start address is also controlled by the respective DSPn_RDMA_CHANNEL_OFFSET bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	15:0	DSPn_START_ADDRESS_RDMA_BUFFER_0 [15:0]	0000h	DSPn RDMA Channel 0 Start Address *Register description is as above.*
base address +22h DSPn_RDMA_Buffer_2	31:16	DSPn_START_ADDRESS_RDMA_BUFFER_3 [15:0]	0000h	DSPn RDMA Channel 3 Start Address *Register description is as above.*
	15:0	DSPn_START_ADDRESS_RDMA_BUFFER_2 [15:0]	0000h	DSPn RDMA Channel 2 Start Address *Register description is as above.*
base address +24h DSPn_RDMA_Buffer_3	31:16	DSPn_START_ADDRESS_RDMA_BUFFER_5 [15:0]	0000h	DSPn RDMA Channel 5 Start Address *Register description is as above.*
	15:0	DSPn_START_ADDRESS_RDMA_BUFFER_4 [15:0]	0000h	DSPn RDMA Channel 4 Start Address *Register description is as above.*
base address +30h DSPn_DMA_Config_1	23:16	DSPn_WDMA_CHANNEL_ENABLE [7:0]	00h	DSPn WDMA Channel Enable There are 8 WDMA channels; each bit of this field enables the respective WDMA channel. Each bit is coded as: 0 = Disabled 1 = Enabled
	13:0	DSPn_DMA_BUFFER_LENGTH [13:0]	0000h	DSPn DMA Buffer Length Selects the amount of data transferred in each DMA channel. The LSB represents one 24-bit DSP memory word.
base address +32h DSPn_DMA_Config_2	7:0	DSPn_WDMA_CHANNEL_OFFSET [7:0]	00h	DSPn WDMA Channel Offset There are 8 WDMA channels; each bit of this field offsets the Start Address of the respective WDMA channel. Each bit is coded as: 0 = No offset 1 = Offset by 8000h
base address +34h DSPn_DMA_Config_3	21:16	DSPn_RDMA_CHANNEL_OFFSET [5:0]	00h	DSPn RDMA Channel Offset There are 6 RDMA channels; each bit of this field offsets the Start Address of the respective RDMA channel. Each bit is coded as: 0 = No offset 1 = Offset by 8000h
	5:0	DSPn_RDMA_CHANNEL_ENABLE [5:0]	00h	DSPn RDMA Channel Enable There are 6 RDMA channels; each bit of this field enables the respective RDMA channel. Each bit is coded as: 0 = Disabled 1 = Enabled
base address +36h DSPn_DMA_Config_4	0	DSPn_DMA_WORD_SEL	0	DSPn Data Word Format 0 = Q3.20 format (4 integer bits, 20 fractional bits) 1 = Q0.23 format (1 integer bit, 23 fractional bits) The data word format should be set according to the requirements of the applicable DSP firmware.

Table 28 DSP Direct Memory Access (DMA) Control

DSP INTERRUPTS

The DSP cores provide inputs to the Interrupt circuit, and can be used to trigger an Interrupt event when the associated conditions occur. For each DSP, the following Interrupts are provided:

- DMA Interrupt - asserted when all enabled DSP input (WDMA) channel buffers have been filled, and all enabled DSP output (RDMA) channel buffers have been emptied
- DSP Start 1, DSP Start 2 Interrupts - asserted when the respective Start signal is triggered
- DSP Busy Interrupt - asserted when the DSP is busy (i.e., when firmware execution or DMA processes are started)

The CS47L85 also provides 16 control bits that allow the DSP cores to generate programmable Interrupt events. When a '1' is written to these bits (see Table 29), the respective DSP Interrupt (DSP_IRQn_EINTx) will be triggered. The associated Interrupt bits are latched once set; they can be polled at any time, or used to control the IRQ signal.

See "Interrupts" for further details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5632 (1600h) ADSP2_IRQ0	1	DSP_IRQ2	0	DSP IRQ2 Write '1' to trigger the DSP_IRQ2_EINTn interrupt.
	0	DSP_IRQ1	0	DSP IRQ1 Write '1' to trigger the DSP_IRQ1_EINTn interrupt.
R5633 (1601h) ADSP2_IRQ1	1	DSP_IRQ4	0	DSP IRQ4 Write '1' to trigger the DSP_IRQ4_EINTn interrupt.
	0	DSP_IRQ3	0	DSP IRQ3 Write '1' to trigger the DSP_IRQ3_EINTn interrupt.
R5634 (1602h) ADSP2_IRQ2	1	DSP_IRQ6	0	DSP IRQ6 Write '1' to trigger the DSP_IRQ6_EINTn interrupt.
	0	DSP_IRQ5	0	DSP IRQ5 Write '1' to trigger the DSP_IRQ5_EINTn interrupt.
R5635 (1603h) ADSP2_IRQ3	1	DSP_IRQ8	0	DSP IRQ8 Write '1' to trigger the DSP_IRQ8_EINTn interrupt.
	0	DSP_IRQ7	0	DSP IRQ7 Write '1' to trigger the DSP_IRQ7_EINTn interrupt.
R5636 (1604h) ADSP2_IRQ4	1	DSP_IRQ10	0	DSP IRQ10 Write '1' to trigger the DSP_IRQ10_EINTn interrupt.
	0	DSP_IRQ9	0	DSP IRQ9 Write '1' to trigger the DSP_IRQ9_EINTn interrupt.
R5637 (1605h) ADSP2_IRQ5	1	DSP_IRQ12	0	DSP IRQ12 Write '1' to trigger the DSP_IRQ12_EINTn interrupt.
	0	DSP_IRQ11	0	DSP IRQ11 Write '1' to trigger the DSP_IRQ11_EINTn interrupt.
R5638 (1606h) ADSP2_IRQ6	1	DSP_IRQ14	0	DSP IRQ14 Write '1' to trigger the DSP_IRQ14_EINTn interrupt.
	0	DSP_IRQ13	0	DSP IRQ13 Write '1' to trigger the DSP_IRQ13_EINTn interrupt.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5639 (1607h) ADSP2_IRQ7	1	DSP_IRQ16	0	DSP IRQ16 Write '1' to trigger the DSP_IRQ16_EINTn interrupt.
	0	DSP_IRQ15	0	DSP IRQ15 Write '1' to trigger the DSP_IRQ15_EINTn interrupt.

Table 29 DSP Interrupts

DSP DEBUG SUPPORT

General purpose 'scratch' registers are provided for each DSP. These have no assigned function, and can be used to assist in algorithm development.

The JTAG interface provides test and debug access to the CS47L85, as described in the "JTAG Interface" section. The JTAG interface clock can be enabled independently for each DSP core, using the DSPn_DBG_CLK_ENA register bits.

When using the JTAG interface to access any DSP core, the respective DSPn_DBG_CLK_ENA and DSPn_CORE_ENA bits must also be set.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
DSP1 Base Address = R1048064 (0FFE00h) DSP2 Base Address = R1572352 (17FE00h) DSP3 Base Address = R2096640 (1FFE00h) DSP4 Base Address = R2620928 (27FE00h) DSP5 Base Address = R3145216 (2FFE00h) DSP6 Base Address = R3669504 (37FE00h) DSP7 Base Address = R4193792 (3FFE00h)				
base address DSPn_Config_1	3	DSPn_DBG_CLK_ENA	0	DSPn Debug Clock Enable 0 = Disabled 1 = Enabled
base address +40h DSPn_Scratch_1	31:16	DSPn_SCRATCH_1 [15:0]	0000h	DSPn Scratch Register 1
	15:0	DSPn_SCRATCH_0 [15:0]	0000h	DSPn Scratch Register 0
base address +42h DSPn_Scratch_2	31:16	DSPn_SCRATCH_3 [15:0]	0000h	DSPn Scratch Register 3
	15:0	DSPn_SCRATCH_2 [15:0]	0000h	DSPn Scratch Register 2

Table 30 DSP Debug Support

VIRTUAL DSP REGISTERS

The DSP control registers, described throughout this section, are implemented for each DSP core. Each control register has a unique location within the CS47L85 register map.

An additional set of DSP control registers is also defined, which can be used in firmware to access any of the DSPs; these are known as 'Virtual DSP' or 'DSP 0' registers, and are defined at address R4096 (1000h) in the device register map. The full register map listing is provided in a separate document - see "Register Map" for further information.

Note that read/write access to the Virtual DSP registers is only possible via firmware running on the integrated DSP cores. When DSP firmware accesses the virtual registers, then the registers will automatically be mapped onto the control registers corresponding to whichever DSP core is making the read/write access. For example, if DSP1 accesses these registers, then the registers will read/write the DSP1 control registers. If DSP2 accesses the virtual registers, they will be mapped onto the DSP2 control registers.

The Virtual DSP registers are designed to allow software to be transferable to any of the DSPs without modification to the software code.

The Virtual DSP registers are defined at register addresses R4096 (1000h) to R4192 (1060h) in the device register map. Note that these registers cannot be accessed directly at the addresses shown; they can only be accessed through DSP firmware code, using the register window function illustrated in Figure 40. The virtual DSP registers are located at address 0xD000 in the X Data memory map.

DSP PERIPHERAL CONTROL

The CS47L85 incorporates a suite of DSP peripheral functions, which can be integrated together to support the sensor hub capability. Three Master I2C Interfaces are provided, for external sensor connectivity. Configurable Event Log functions provide multi-channel monitoring of internal and external signals. The General Purpose Timers provide time-stamp data for the Event Logs, and support watchdog and other miscellaneous time-based functions. Maskable GPIO provides an efficient mechanism for multiple DSPs to access the respective input and output signals.

The DSP peripherals are designed to provide a comprehensive sensor hub capability, operating with a high degree of autonomy from the host processor.

MASTER INTERFACES

The CS47L85 incorporates three I2C Master Interfaces, offering a flexible capability for additional sensor / accessory input. The Master Interfaces (MIF1, MIF2, MIF3) can support single-master I2C operation up to 1MHz. The Master Interfaces support 7-bit and 10-bit Slave addressing modes.

The Master Interfaces are ideally suited for connection to external sensors such as accelerometers, gyroscopes and magnetometers for motion sensing and navigation applications. Other example accessories include barometers, or ambient light sensors, for environmental awareness. Flow control bits for the TX and RX data buffers enable easy integration with external devices, and with internal DSP functions.

Clocking for the Master Interfaces is derived from DSPCLK, which must be enabled and present when using any of these interfaces. Standard I2C bus rates can be supported for typical DSPCLK frequencies using the register settings described in Table 31.

ADDRESS	CONDITION	VALUE
MIF*n* Base Address	—	0x0000_0006
MIF*n* Base Address + 0x040	—	0x0000_0000
MIF*n* Base Address + 0x042	10kHz I2C mode	0x01CC_01CC
	100kHz I2C mode	0x002E_002E
	400kHz I2C mode	0x000C_000C
	1MHz I2C mode	0x0005_0005
Notes: 1. The 'Base Address' register for each Master Interface (MIF*n*) is noted in Table 32. 2. It is assumed that the DSPCLK frequency is one of the nominal (typical) frequencies specified in Table 105.		

Table 31 Master Interface Clock Configuration

The Transmit (Master Write) and Receive (Master Read) actions are each supported by 16-byte data buffers, allowing I2C transfers of up to 2,097,152 data bytes (2MB). The number of data bytes transmitted (or received) in each I2C operation is selected using the MIFn_TX_LENGTH (or MIFn_RX_LENGTH) field respectively.

Data to be transmitted is managed using the TX data buffers; the application software must load data into the buffer registers (MIFn_TX_BYTEx), and then write '1' to the MIFn_TX_DONE bit to commit that data for transmission. The MIFn_TX_REQUEST bit indicates when the buffer registers are ready for loading new data. Internal buffering of the TX data enables uninterrupted I2C Writes. If new data is not ready for transmission, SCLK will halt until the buffer registers have been filled.

Data received on the interface is managed using the RX data buffers; the MIFn_RX_REQUEST bit indicates when the buffer registers contain new data. The application software must read the buffer registers (MIFn_RX_BYTEn), and then write '1' to the MIFn_RX_DONE bit to confirm the data has been read. Internal buffering of the RX data enables uninterrupted I2C Reads. If the buffers are not ready to receive new data, SCLK will halt until the buffer registers have been read.

The Master Interface divides each I2C transaction into one or more data Blocks. The Block Length is configurable using the MIFn_TX_BLOCK_LENGTH and MIFn_RX_BLOCK_LENGTH register fields. The Block Length is equal to the number of bytes transmitted/received for each TX_DONE/RX_DONE action. The maximum Block Length is 16 bytes, corresponding to the size of the TX and RX data buffers.

Note that the order in which the data bytes in the TX/RX buffers are transferred depends upon the selected MIFn_WORD_SIZE setting. Correct setting of the word size ensures that each data word is transmitted/received as Most-Significant-Byte first.

The Master Interface is configured for Read (RX) or Write (TX) operation using the MIF*n*_READ_WRITE_SEL bit. Each I2C transfer is started by writing 1 to the MIF*n*_START bit. In the case of a Master Write, data must be committed to the TX data buffers using the TX_DONE bit, to enable the transfer to proceed - note that the first block of transmit data can be

committed to the TX buffers before or after writing to the START bit for the respective transfer.

The DSPCLK system clock must be configured and enabled before a Master Interface transaction is scheduled. The Master Interfaces should be kept idle if DSPCLK is not enabled. See “Clocking and Sample Rates” for details of the system clocks (including requirements for reconfiguring DSPCLK while DSP peripherals are enabled).

The MIFn_BUSY_STS bit indicates when the Master Interface is executing an I2C transaction. This bit is set high during each I2C transaction, and set low on completion. An Interrupt event is also triggered on completion of the I2C transfer, if the corresponding MIFn_DONE_EINTx is unmasked as an input to the IRQ circuit.

Additional status bits are provided to indicate Watchdog Timeout, or a NACK error signal received. See Table 32 for further details of these bits.

Note that the ‘MIF DONE’ indication described above will be asserted each time an I2C transfer completes, including when an error condition has occurred. It is recommended that the Master Interface status bits be checked after each I2C transaction, in order that corrective action can be taken when necessary.

The external connections associated with each I2C Master Interface (MIF) are implemented on multi-function GPIO pins, which must be configured for the respective MIF functions when required. The MIFnSCLK and MIFnSDA connections are pin-specific alternative functions available on specific GPIO pins. See “General Purpose Input / Output” to configure the GPIO pins for the MIF operation.

The Master Interface provides inputs to the Interrupt control circuit. An interrupt event is triggered on completion of each TX/RX Block, and on completion of the I2C transaction - see “Interrupts”.

Typical Master I2C transfers are illustrated in Figure 41 through to Figure 43.

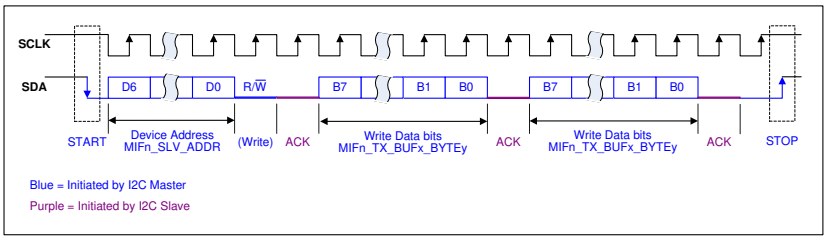


Figure 41 Master I2C Write

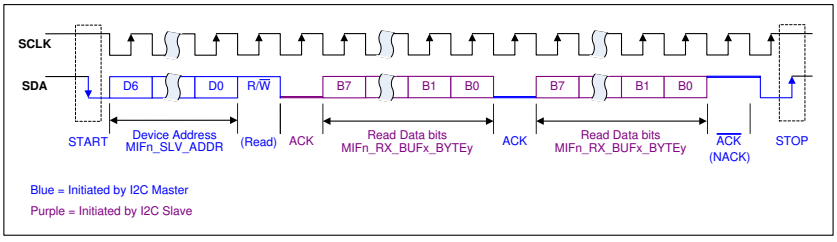


Figure 42 Master I2C Read

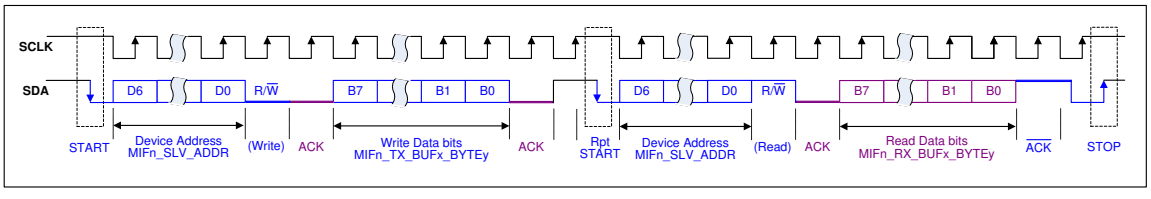


Figure 43 Master I2C Write & Read

The MIF control registers are described in Table 32.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
MIF1 Base Address = R262144 (40000h) MIF2 Base Address = R263168 (40400h) MIF3 Base Address = R264192 (40800h)				
base address +002h MIFn_I2C_CONFIG_2	10:1	MIFn_SLV_ADDR [9:0]	000h	Address of Slave on which transactions are executed. For 7-bit mode, lower 7 bits of field are used.
	0	MIFn_ADDR_MODE	0	Selects the addressing mode of I2C Master 0= 7-bit mode 1= 10-bit mode
base address +004h MIFn_I2C_CONFIG_3	3	MIFn_NACK_RESPONSE	0	Selects the action taken if NACK is received from Slave. 0 = Stop Condition sent. 1 = Stop Condition not sent; next transaction will commence with a Repeated Start. Note that, if the Stop Condition is not sent, the Master retains control of the bus until a subsequent action is scheduled. The next transaction will commence with a Repeated Start in this case.
	2	MIFn_SCL_MON_ENA	1	Enables bus monitoring functions on SCLK 0 = Disabled 1 = Enabled This feature enables support for clock stretching by Slave devices, and enables Bus Synchronisation as part of multi-master operation.
	1	MIFn_RPT_START	0	Selects the action taken on completion of a bus transaction. 0 = Stop Condition sent. 1 = Stop Condition not sent; next transaction will commence with a Repeated Start. Note that, if the Stop Condition is not sent, the Master retains control of the bus until a subsequent action is scheduled. The next transaction will commence with a Repeated Start in this case.
	0	MIFn_START_BYTE_ENA	0	Selects whether a Start Byte is transmitted before an I2C transaction. 0 = Disabled 1 = Enabled The Start Byte is a dummy transaction that provides support for bus devices that use low-frequency polling to detect I2C activity. The Start Byte, when enabled, is transmitted before the Slave Address byte(s). It is not acknowledged on the bus by any device.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
base address +008h MIFn_I2C_CONFIG_5	0	MIFn_WDT_ENA	0	Watchdog Timer (WDT) control 0 = Disabled 1 = Enabled When bus monitoring functions are enabled (MIFn_SCL_MON_ENA=1), the Watchdog Timer is used to detect the SCLK line being pulled low for a prolonged duration.
base address +080h MIFn_I2C_STATUS_1	2	MIFn_WDT_TIMEOUT_STS	0	Watchdog Timer (WDT) Error Status This bit, when set, indicates that the WDT expired during the I2C transaction. This bit is latched when set; it is cleared by writing '1'. This bit is automatically cleared on next I2C transaction.
	0	MIFn_NACK_STS	0	NACK Error Status This bit, when set, indicates that a NACK Error signal was received during the I2C transaction. This bit is latched when set; it is cleared by writing '1'. This bit is automatically cleared on next I2C transaction.
base address +100h MIFn_CONFIG_1	0	MIFn_START	0	Starts the I2C transaction Write '1' to start.
base address +104h MIFn_CONFIG_3	17:16	MIFn_WORD_SIZE [1:0]	00	Selects the data word format. I2C transactions are made up of 1-Byte data words; the sequence order of these words differs according to the applicable word format. Correct setting of the MIFn_WORD_SIZE field ensures that each data word is transmitted/received as Most-Significant-Byte first. 00 = 8-bit (1, 2, 3, 4, 5, 6, 7, 8, etc) 01 = 16-bit (2, 1, 4, 3, 6, 5, 8, 7, etc) 10 = 32-bit (4, 3, 2, 1, 8, 7, 6, 5, etc) The numbers in brackets describe the order in which the applicable MIFn_[TX|RX]_BYTEx fields are transmitted/received over the I2C interface.
	0	MIFn_READ_WRITE_SEL	0	Selects the I2C Command type 0 = Master Write 1 = Master Read
base address +106h MIFn_CONFIG_4	20:0	MIFn_TX_LENGTH [20:0]	00_0000h	Selects the total number of data bytes in an I2C Write operation. 00_0000h = 1 byte 00_0001h = 2 bytes 00_0002h = 3 bytes … 1F_FFFFh = 2,097,152 bytes

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
base address +110h MIFn_CONFIG_5	20:0	MIFn_RX_LENGTH [20:0]	00_0000h	Selects the total number of data bytes in an I2C Read operation. 00_0000h = 1 byte 00_0001h = 2 bytes 00_0002h = 3 bytes … 1F_FFFFh = 2,097,152 bytes
base address +112h MIFn_CONFIG_6	7:0	MIFn_TX_BLOCK_LENGTH [7:0]	10h	Selects the interval at which the MIFn_BLOCK Interrupt is triggered during I2C Write operations. 00h = 1 byte 01h = 1 byte 02h = 2 bytes … 10h = 16 bytes All other codes are Reserved
base address +114h MIFn_CONFIG_7	7:0	MIFn_RX_BLOCK_LENGTH [7:0]	10h	Selects the interval at which the MIFn_BLOCK Interrupt is triggered during I2C Read operations. 00h = 1 byte 01h = 1 byte 02h = 2 bytes … 10h = 16 bytes All other codes are Reserved
base address +116h MIFn_CONFIG_8	4	MIFn_RX_DONE	0	RX Buffer access control bit Write '1' to indicate that data in the RX Buffer has been read. In normal operation, a '1' is written after reading the RX buffer. This causes the MIFn_RX_REQUEST bit to be reset to '0'. (Note that, if further data is available to read, then the MIFn_RX_REQUEST bit will remain set in this case.)
	0	MIFn_TX_DONE	0	TX Buffer access control bit Write '1' to indicate the TX Buffer has been filled with data for transmission. In normal operation, a '1' is written after writing the TX buffer. This causes the MIFn_TX_REQUEST bit to be reset to '0'.
base address +180h MIFn_STATUS_1	8	MIFn_BUSY_STS	0	MIF Busy Status. This bit, when set, indicates that the Master Interface is executing an I2C transaction.
	8	MIFn_RX_REQUEST	0	RX Buffer flow control bit 0 = No data available to read 1 = Buffer data is available to read
	1	MIFn_TX_REQUEST	0	TX Buffer flow control bit 0 = TX buffer not available to write 1 = TX buffer is available to write
base address +182h MIFn_STATUS_2	20:0	MIFn_BYTE_COUNT [20:0]	00_0000h	Number of data bytes transferred in current transaction. Note that this field is cleared on completion of the I2C transaction.
base address +200h MIFn_TX_1	31:24	MIFn_TX_BYTE4 [7:0]	00h	TX Byte 4
	23:16	MIFn_TX_BYTE3 [7:0]	00h	TX Byte 3
	15:8	MIFn_TX_BYTE2 [7:0]	00h	TX Byte 2
	7:0	MIFn_TX_BYTE1 [7:0]	00h	TX Byte 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
base address +202h MIFn_TX_2	31:24	MIFn_TX_BYTE8 [7:0]	00h	TX Byte 8
	23:16	MIFn_TX_BYTE7 [7:0]	00h	TX Byte 7
	15:8	MIFn_TX_BYTE6 [7:0]	00h	TX Byte 6
	7:0	MIFn_TX_BYTE5 [7:0]	00h	TX Byte 5
base address +204h MIFn_TX_3	31:24	MIFn_TX_BYTE12 [7:0]	00h	TX Byte 12
	23:16	MIFn_TX_BYTE11 [7:0]	00h	TX Byte 11
	15:8	MIFn_TX_BYTE10 [7:0]	00h	TX Byte 10
	7:0	MIFn_TX_BYTE9 [7:0]	00h	TX Byte 9
base address +206h MIFn_TX_4	31:24	MIFn_TX_BYTE16 [7:0]	00h	TX Byte 16
	23:16	MIFn_TX_BYTE15 [7:0]	00h	TX Byte 15
	15:8	MIFn_TX_BYTE14 [7:0]	00h	TX Byte 14
	7:0	MIFn_TX_BYTE13 [7:0]	00h	TX Byte 13
base address +300h MIFn_RX_1	31:24	MIFn_RX_BYTE4 [7:0]	00h	RX Byte 4
	23:16	MIFn_RX_BYTE3 [7:0]	00h	RX Byte 3
	15:8	MIFn_RX_BYTE2 [7:0]	00h	RX Byte 2
	7:0	MIFn_RX_BYTE1 [7:0]	00h	RX Byte 1
base address +302h MIFn_RX_2	31:24	MIFn_RX_BYTE8 [7:0]	00h	RX Byte 8
	23:16	MIFn_RX_BYTE7 [7:0]	00h	RX Byte 7
	15:8	MIFn_RX_BYTE6 [7:0]	00h	RX Byte 6
	7:0	MIFn_RX_BYTE5 [7:0]	00h	RX Byte 5
base address +304h MIFn_RX_3	31:24	MIFn_RX_BYTE12 [7:0]	00h	RX Byte 12
	23:16	MIFn_RX_BYTE11 [7:0]	00h	RX Byte 11
	15:8	MIFn_RX_BYTE10 [7:0]	00h	RX Byte 10
	7:0	MIFn_RX_BYTE9 [7:0]	00h	RX Byte 9
base address +306h MIFn_RX_4	31:24	MIFn_RX_BYTE16 [7:0]	00h	RX Byte 16
	23:16	MIFn_RX_BYTE15 [7:0]	00h	RX Byte 15
	15:8	MIFn_RX_BYTE14 [7:0]	00h	RX Byte 14
	7:0	MIFn_RX_BYTE13 [7:0]	00h	RX Byte 13

Table 32 Master Interface (MIFn) Control

EVENT LOGGERS

The CS47L85 provides 8 Event Log functions, supporting multi-channel, edge-sensitive monitoring and recording of internal or external signals. An “event” is recorded when a logic transition (edge) is detected on a selected signal source. The Event Loggers allow status information to be captured from a large number of sources, to be prioritised and acted upon as required.

The logged events are held in a FIFO buffer, which is managed by the application software. A 32-bit timestamp, derived from one of the General Purpose Timers, is associated and recorded with each FIFO index, to provide a comprehensive record of the detected events.

Each Event Logger must be associated with one of the General Purpose Timers. The selected Timer is the source of timestamp data for any logged events. If DSPCLK is disabled, then the Timer also provides the clock source for the Event Logger. (If DSPCLK is enabled, then DSPCLK is used as the clock source instead.)

A maximum of one event per cycle of the clock source (see above) can be logged. If more than one event occurs within the cycle time, then the highest priority (lowest channel number) event will be logged at the rising edge of the clock. In this case, any lower priority events will be queued, and will be logged as soon as no higher priority events are pending. It is possible for recurring events on a high priority channel to be logged, while low priority ones remain queued. Note that recurring instances of events that are ‘queued’ would not be logged.

The Event Logger can use a slow clock (e.g., 32kHz), but higher clock frequencies may also be commonly used, depending on the application and use case. The clock frequency determines the maximum possible event logging rate, as described above.

The Event Logger is enabled using the EVENTLOGn_ENA register bit (where ‘n’ identifies the respective Event Logger, 1 to 8).

The Event Logger can be reset by writing ‘1’ to the EVENTLOGn_RST bit. Executing this function will clear all the Event Logger status flags, and will clear the contents of the FIFO buffer.

The associated Timer (and timestamp source) is selected using EVENTLOGn_TIME_SEL. Note that the Event Logger must be disabled (EVENTLOGn_ENA = 0) when selecting the Timer source.

The Event Logger allows up to 16 input channels to be configured for detection and logging. The EVENTLOGn_CHx_SEL register selects the applicable input source for each channel (where ‘x’ identifies the channel number, 1 to 16). The polarity selection and de-bounce options are configured using the EVENTLOGn_CHx_POL and EVENTLOGn_CHx_DB bits respectively.

The input channels can be enabled or disabled freely, using EVENTLOGn_CHx_ENA, without having to disable the Event Logger entirely. An input channel must be disabled whenever the associated _SEL, _POL, or _DB fields are written. It is possible to re-configure input channels while the Event Logger is enabled, provided the channel(s) being re-configured are disabled when doing so.

The available input sources include GPIO inputs, External Accessory status (Jack, Mic, Sensors), and signals generated by the integrated DSP Cores. A list of the valid input sources for the Event Loggers is provided in Table 34.

Note that, to log both rising and falling events from any source, two separate input channels must be configured - one for each polarity.

If an Input channel is configured for Rising Edge detection (EVENTLOGn_CHx_POL=0), and the corresponding input signal is ‘Logic 1’ at the time when the Event Logger is enabled, then an event will be logged in respect of this initial state. Similarly, if an Input channel is configured for Falling Edge detection, and is Logic ‘0’ when the Event Logger is enabled, then a corresponding event will be logged. If Rising and Falling edges are both configured for detection, then an event will always be logged in respect of the initial condition.

Each event (signal transition) which meets the criteria of an enabled channel will be written to the 16-stage FIFO buffer. The buffer is filled cyclically, but does not overwrite unread data when full. An error condition occurs if the buffer fills up completely.

Note the “FIFO” behaviour is not enforced or fully implemented in the device hardware, but assumes that a compatible software implementation is in place. New events are written to the buffer in a cyclic manner, but the data can be read out in any order, if desired. The designed FIFO behaviour requires the software to update the Read Pointer (RPTR) in the intended manner for smooth operation.

The entire contents of the 16-stage FIFO buffer can be accessed directly in the register map. Each FIFO index (y = 0 to 15) comprises the EVENTLOGn_FIFOy_ID (identifying the source signal of the associated log event), the EVENTLOGn_FIFOy_POL (the polarity of the respective event transition), and the EVENTLOGn_FIFOy_TIME field (containing the 32-bit timestamp, from the associated Timer).

The FIFO buffer is managed using the EVENTLOGn_FIFO_WPTR and EVENTLOGn_FIFO_RPTR registers. The Write Pointer (WPTR) field identifies the index location (0 to 15) in which the next event will be logged. The Read Pointer (RPTR) field identifies the index location of the first set of unread data, if any exists. Both of these fields are initialised to 0 when the Event Logger is reset.

If RPTR <> WPTR, then the buffer contains new data. The number of new events is equal to the difference between the two pointer values (WPTR - RPTR, allowing for wrap-around beyond index 15). For example, if WPTR = 12 and RPTR = 8, this means that there are 4 unread data sets in the buffer, at index locations 8, 9, 10, and 11.

After reading the new data from the buffer, the RPTR value should be incremented by the corresponding amount (e.g., increment by 4, in the example described above). Note that the RPTR value can either be incremented once for each read, or can be incremented in larger steps after a 'batch' read.

If RPTR = WPTR, then the buffer is either empty (0 events) or full (16 events). In this case, the status bits described below will confirm the current status of the buffer.

The EVENTLOGn_NOT_EMPTY bit indicates whether the FIFO buffer is empty. When this bit is set, it indicates one or more new sets of data in the FIFO.

The EVENTLOGn_WMARK_STS bit indicates when the number of FIFO index locations available for new events reaches a configurable threshold, known as the watermark level. The watermark level is held in the EVENTLOGn_WMARK register.

The EVENTLOGn_FULL bit indicates when the FIFO buffer is full. When this bit is set, it indicates that there are 16 sets of new event data in the FIFO. Note that this does not mean that a buffer overflow condition has occurred; but further events will not be logged or indicated until the buffer has been cleared.

Following a 'Buffer Full' condition, the FIFO operation will resume as soon as the RPTR field has been updated to a new value. Note that writing the same value to RPTR will not re-start the FIFO operation, even if the entire buffer contents have been read. After all of the required data has been read from the buffer, the RPTR value should be set equal to the WPTR value; note that an intermediate (different) value must always be written to the RPTR field in order to clear the 'Buffer Full' status and re-start the FIFO operation.

The Control Write Sequencer is automatically triggered whenever the NOT_EMPTY status of the Event Log buffer is asserted. A different control sequence may be configured for each of the Event Loggers. See "Control Write Sequencer" for further details.

The Event Log status flags are inputs to the Interrupt control circuit and can be used to trigger an Interrupt event when the respective FIFO condition (Full, Not Empty, or Watermark level) occurs - see "Interrupts".

The Event Log status can be output directly on a GPIO pin as an external indication of the Event Logger. See "General Purpose Input / Output" to configure a GPIO pin for this function.

The Event Log NOT_EMPTY status can also be selected as a 'Start' trigger for DSP firmware execution. See "DSP Firmware Control" for further details.

The Event Logger control registers are described in Table 33.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
Event Log 1 Base Address = R294912 (48000h) Event Log 2 Base Address = R295424 (48200h) Event Log 3 Base Address = R295936 (48400h) Event Log 4 Base Address = R296448 (48600h) Event Log 5 Base Address = R296960 (48800h) Event Log 6 Base Address = R297472 (48A00h) Event Log 7 Base Address = R297984 (48C00h) Event Log 8 Base Address = R298496 (48E00h)				
base address EVENTLOGn_CONTROL	1	EVENTLOGn_RST	0	Event Log Reset Write '1' to Reset the status outputs and clear the FIFO buffer.
	0	EVENTLOGn_ENA	0	Event Log Enable 0 = Disabled 1 = Enabled
base address +04h EVENTLOGn_TIMER_SEL	1:0	EVENTLOGn_TIMER_SEL [1:0]	00	Event Log Timer Source Select 00 = Timer 1 01 = Timer 2 10 = Timer 3 11 = Timer 4 Note that the Event Log must be disabled when updating this register
base address +0Ch EVENTLOGn_FIFO_CONTROL1	3:0	EVENTLOGn_FIFO_WMARK [3:0]	1h	Event Log FIFO Watermark The Watermark status output is asserted when the number of FIFO locations available for new events is less than or equal to the FIFO Watermark. Valid from 0 to 15.
base address +0Eh EVENTLOGn_FIFO_POINTER1	18	EVENTLOGn_FULL	0	Event Log FIFO Full Status This bit, when set, indicates that the FIFO buffer is full. It is cleared when a new value is written to the FIFO Read Pointer, or when the Event Log is Reset.
	17	EVENTLOGn_WMARK_STS	0	Event Log FIFO Watermark Status This bit, when set, indicates that the FIFO space available for new events to be logged is less than or equal to the Watermark threshold.
	16	EVENTLOGn_NOT_EMPTY	0	Event Log FIFO Not Empty Status This bit, when set, indicates one or more new sets of logged event data in the FIFO.
	11:8	EVENTLOGn_FIFO_WPTR [3:0]	0h	Event Log FIFO Write Pointer Indicates the FIFO index location in which the next event will be logged. This is a read-only field.
	3:0	EVENTLOGn_FIFO_RPTR [3:0]	0h	Event Log FIFO Read Pointer Indicates the FIFO index location of the first set of unread data, if any exists. For the intended FIFO behaviour, this field must be incremented after the respective data has been read.
base address +20h EVENTLOGn_CH_ENABLE	15	EVENTLOGn_CH16_ENA	0	Event Log Channel 16 Enable 0 = Disabled 1 = Enabled
	14	EVENTLOGn_CH15_ENA	0	Event Log Channel 15 Enable *Register description is as above.*

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	13	EVENTLOGn_CH14_ENA	0	Event Log Channel 14 Enable *Register description is as above.*
	12	EVENTLOGn_CH13_ENA	0	Event Log Channel 13 Enable *Register description is as above.*
	11	EVENTLOGn_CH12_ENA	0	Event Log Channel 12 Enable *Register description is as above.*
	10	EVENTLOGn_CH11_ENA	0	Event Log Channel 11 Enable *Register description is as above.*
	9	EVENTLOGn_CH10_ENA	0	Event Log Channel 10 Enable *Register description is as above.*
	8	EVENTLOGn_CH9_ENA	0	Event Log Channel 9 Enable *Register description is as above.*
	7	EVENTLOGn_CH8_ENA	0	Event Log Channel 8 Enable *Register description is as above.*
	6	EVENTLOGn_CH7_ENA	0	Event Log Channel 7 Enable *Register description is as above.*
	5	EVENTLOGn_CH6_ENA	0	Event Log Channel 6 Enable *Register description is as above.*
	4	EVENTLOGn_CH5_ENA	0	Event Log Channel 5 Enable *Register description is as above.*
	3	EVENTLOGn_CH4_ENA	0	Event Log Channel 4 Enable *Register description is as above.*
	2	EVENTLOGn_CH3_ENA	0	Event Log Channel 3 Enable *Register description is as above.*
	1	EVENTLOGn_CH2_ENA	0	Event Log Channel 2 Enable *Register description is as above.*
	0	EVENTLOGn_CH1_ENA	0	Event Log Channel 1 Enable *Register description is as above.*
base address +40h EVENTLOGn_CH1_DEFINE	15	EVENTLOGn_CH1_DB	0	Event Log Channel 1 de-bounce 0 = Disabled 1 = Enabled Note that channel must be disabled when updating this register
	14	EVENTLOGn_CH1_POL	0	Event Log Channel 1 polarity 0 = Rising edge triggered 1 = Falling edge triggered Note that channel must be disabled when updating this register
	8:0	EVENTLOGn_CH1_SEL [8:0]	000h	Event Log Channel 1 source. See Table 34 for valid selections. Note that channel must be disabled when updating this register
base address +42h EVENTLOGn_CH2_DEFINE	15	EVENTLOGn_CH2_DB	0	Event Log Channel 2 de-bounce *Register description is as above.*
	14	EVENTLOGn_CH2_POL	0	Event Log Channel 2 polarity *Register description is as above.*
	8:0	EVENTLOGn_CH2_SEL [8:0]	000h	Event Log Channel 2 source *Register description is as above.*
base address +44h EVENTLOGn_CH3_DEFINE	15	EVENTLOGn_CH3_DB	0	Event Log Channel 3 de-bounce *Register description is as above.*
	14	EVENTLOGn_CH3_POL	0	Event Log Channel 3 polarity *Register description is as above.*
	8:0	EVENTLOGn_CH3_SEL [8:0]	000h	Event Log Channel 3 source *Register description is as above.*
base address +46h EVENTLOGn_CH4_DE	15	EVENTLOGn_CH4_DB	0	Event Log Channel 4 de-bounce *Register description is as above.*

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
FINE	14	EVENTLOGn_CH4_POL	0	Event Log Channel 4 polarity *Register description is as above.*
	8:0	EVENTLOGn_CH4_SEL [8:0]	000h	Event Log Channel 4 source *Register description is as above.*
base address +48h EVENTLOGn_CH5_DEFINE	15	EVENTLOGn_CH5_DB	0	Event Log Channel 5 de-bounce *Register description is as above.*
	14	EVENTLOGn_CH5_POL	0	Event Log Channel 5 polarity *Register description is as above.*
	8:0	EVENTLOGn_CH5_SEL [8:0]	000h	Event Log Channel 5 source *Register description is as above.*
base address +4Ah EVENTLOGn_CH6_DEFINE	15	EVENTLOGn_CH6_DB	0	Event Log Channel 6 de-bounce *Register description is as above.*
	14	EVENTLOGn_CH6_POL	0	Event Log Channel 6 polarity *Register description is as above.*
	8:0	EVENTLOGn_CH6_SEL [8:0]	000h	Event Log Channel 6 source *Register description is as above.*
base address +4Ch EVENTLOGn_CH7_DEFINE	15	EVENTLOGn_CH7_DB	0	Event Log Channel 7 de-bounce *Register description is as above.*
	14	EVENTLOGn_CH7_POL	0	Event Log Channel 7 polarity *Register description is as above.*
	8:0	EVENTLOGn_CH7_SEL [8:0]	000h	Event Log Channel 7 source *Register description is as above.*
base address +4Eh EVENTLOGn_CH8_DEFINE	15	EVENTLOGn_CH8_DB	0	Event Log Channel 8 de-bounce *Register description is as above.*
	14	EVENTLOGn_CH8_POL	0	Event Log Channel 8 polarity *Register description is as above.*
	8:0	EVENTLOGn_CH8_SEL [8:0]	000h	Event Log Channel 8 source *Register description is as above.*
base address +50h EVENTLOGn_CH9_DEFINE	15	EVENTLOGn_CH9_DB	0	Event Log Channel 9 de-bounce *Register description is as above.*
	14	EVENTLOGn_CH9_POL	0	Event Log Channel 9 polarity *Register description is as above.*
	8:0	EVENTLOGn_CH9_SEL [8:0]	000h	Event Log Channel 9 source *Register description is as above.*
base address +52h EVENTLOGn_CH10_DEFINE	15	EVENTLOGn_CH10_DB	0	Event Log Channel 10 de-bounce *Register description is as above.*
	14	EVENTLOGn_CH10_POL	0	Event Log Channel 10 polarity *Register description is as above.*
	8:0	EVENTLOGn_CH10_SEL [8:0]	000h	Event Log Channel 10 source *Register description is as above.*
base address +54h EVENTLOGn_CH11_DEFINE	15	EVENTLOGn_CH11_DB	0	Event Log Channel 11 de-bounce *Register description is as above.*
	14	EVENTLOGn_CH11_POL	0	Event Log Channel 11 polarity *Register description is as above.*
	8:0	EVENTLOGn_CH11_SEL [8:0]	000h	Event Log Channel 11 source *Register description is as above.*
base address +56h EVENTLOGn_CH12_DEFINE	15	EVENTLOGn_CH12_DB	0	Event Log Channel 12 de-bounce *Register description is as above.*
	14	EVENTLOGn_CH12_POL	0	Event Log Channel 12 polarity *Register description is as above.*
	8:0	EVENTLOGn_CH12_SEL [8:0]	000h	Event Log Channel 12 source *Register description is as above.*
base address +58h EVENTLOGn_CH13_DEFINE	15	EVENTLOGn_CH13_DB	0	Event Log Channel 13 de-bounce *Register description is as above.*
	14	EVENTLOGn_CH13_POL	0	Event Log Channel 13 polarity *Register description is as above.*

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	8:0	EVENTLOGn_CH13_SEL [8:0]	000h	Event Log Channel 13 source *Register description is as above.*
base address +5Ah EVENTLOGn_CH14_DEFINE	15	EVENTLOGn_CH14_DB	0	Event Log Channel 14 de-bounce *Register description is as above.*
	14	EVENTLOGn_CH14_POL	0	Event Log Channel 14 polarity *Register description is as above.*
	8:0	EVENTLOGn_CH14_SEL [8:0]	000h	Event Log Channel 14 source *Register description is as above.*
base address +5Ch EVENTLOGn_CH15_DEFINE	15	EVENTLOGn_CH15x_DB	0	Event Log Channel 15 de-bounce *Register description is as above.*
	14	EVENTLOGn_CH15_POL	0	Event Log Channel 15 polarity *Register description is as above.*
	8:0	EVENTLOGn_CH15_SEL [8:0]	000h	Event Log Channel 15 source *Register description is as above.*
base address +5Eh EVENTLOGn_CH16_DEFINE	15	EVENTLOGn_CH16_DB	0	Event Log Channel 16 de-bounce *Register description is as above.*
	14	EVENTLOGn_CH16_POL	0	Event Log Channel 16 polarity *Register description is as above.*
	8:0	EVENTLOGn_CH16_SEL [8:0]	000h	Event Log Channel 16 source *Register description is as above.*
base address +80h EVENTLOGn_FIFO0_READ	12	EVENTLOGn_FIFO0_POL	0	Event Log FIFO Index 0 polarity 0 = Rising edge 1 = Falling edge
	8:0	EVENTLOGn_FIFO0_ID [8:0]	000h	Event Log FIFO Index 0 source See Table 34 for valid selections
base address +82h EVENTLOGn_FIFO0_TIME	31:0	EVENTLOGn_FIFO0_TIME [31:0]	0000 0000h	Event Log FIFO Index 0 Time
base address +84h EVENTLOGn_FIFO1_READ	12	EVENTLOGn_FIFO1_POL	0	Event Log FIFO Index 1 polarity *Register description is as above.*
	8:0	EVENTLOGn_FIFO1_ID [8:0]	000h	Event Log FIFO Index 1 source *Register description is as above.*
base address +86h EVENTLOGn_FIFO1_TIME	31:0	EVENTLOGn_FIFO1_TIME [31:0]	0000 0000h	Event Log FIFO Index 1 Time
base address +88h EVENTLOGn_FIFO2_READ	12	EVENTLOGn_FIFO2_POL	0	Event Log FIFO Index 2 polarity *Register description is as above.*
	8:0	EVENTLOGn_FIFO2_ID [8:0]	000h	Event Log FIFO Index 2 source *Register description is as above.*
base address +8Ah EVENTLOGn_FIFO2_TIME	31:0	EVENTLOGn_FIFO2_TIME [31:0]	0000 0000h	Event Log FIFO Index 2 Time
base address +8Ch EVENTLOGn_FIFO3_READ	12	EVENTLOGn_FIFO3_POL	0	Event Log FIFO Index 3 polarity *Register description is as above.*
	8:0	EVENTLOGn_FIFO3_ID [8:0]	000h	Event Log FIFO Index 3 source *Register description is as above.*
base address +8Eh EVENTLOGn_FIFO3_TIME	31:0	EVENTLOGn_FIFO3_TIME [31:0]	0000 0000h	Event Log FIFO Index 3 Time
base address +90h EVENTLOGn_FIFO4_READ	12	EVENTLOGn_FIFO4_POL	0	Event Log FIFO Index 4 polarity *Register description is as above.*
	8:0	EVENTLOGn_FIFO4_ID [8:0]	000h	Event Log FIFO Index 4 source *Register description is as above.*
base address +92h EVENTLOGn_FIFO4_TIME	31:0	EVENTLOGn_FIFO4_TIME [31:0]	0000 0000h	Event Log FIFO Index 4 Time

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
base address +94h EVENTLOGn_FIFO5_READ	12	EVENTLOGn_FIFO5_POL	0	Event Log FIFO Index 5 polarity *Register description is as above.*
	8:0	EVENTLOGn_FIFO5_ID [8:0]	000h	Event Log FIFO Index 5 source *Register description is as above.*
base address +96h EVENTLOGn_FIFO5_TIME	31:0	EVENTLOGn_FIFO5_TIME [31:0]	0000 0000h	Event Log FIFO Index 5 Time
base address +98h EVENTLOGn_FIFO6_READ	12	EVENTLOGn_FIFO6_POL	0	Event Log FIFO Index 6 polarity *Register description is as above.*
	8:0	EVENTLOGn_FIFO6_ID [8:0]	000h	Event Log FIFO Index 6 source *Register description is as above.*
base address +9Ah EVENTLOGn_FIFO6_TIME	31:0	EVENTLOGn_FIFO6_TIME [31:0]	0000 0000h	Event Log FIFO Index 6 Time
base address +9Ch EVENTLOGn_FIFO7_READ	12	EVENTLOGn_FIFO7_POL	0	Event Log FIFO Index 7 polarity *Register description is as above.*
	8:0	EVENTLOGn_FIFO7_ID [8:0]	000h	Event Log FIFO Index 7 source *Register description is as above.*
base address +9Eh EVENTLOGn_FIFO7_TIME	31:0	EVENTLOGn_FIFO7_TIME [31:0]	0000 0000h	Event Log FIFO Index 7 Time
base address +A0h EVENTLOGn_FIFO8_READ	12	EVENTLOGn_FIFO8_POL	0	Event Log FIFO Index 8 polarity *Register description is as above.*
	8:0	EVENTLOGn_FIFO8_ID [8:0]	000h	Event Log FIFO Index 8 source *Register description is as above.*
base address +A2h EVENTLOGn_FIFO8_TIME	31:0	EVENTLOGn_FIFO8_TIME [31:0]	0000 0000h	Event Log FIFO Index 8 Time
base address +A4h EVENTLOGn_FIFO9_READ	12	EVENTLOGn_FIFO9_POL	0	Event Log FIFO Index 9 polarity *Register description is as above.*
	8:0	EVENTLOGn_FIFO9_ID [8:0]	000h	Event Log FIFO Index 9 source *Register description is as above.*
base address +A6h EVENTLOGn_FIFO9_TIME	31:0	EVENTLOGn_FIFO9_TIME [31:0]	0000 0000h	Event Log FIFO Index 9 Time
base address +A8h EVENTLOGn_FIFO10_READ	12	EVENTLOGn_FIFO10_POL	0	Event Log FIFO Index 10 polarity *Register description is as above.*
	8:0	EVENTLOGn_FIFO10_ID [8:0]	000h	Event Log FIFO Index 10 source *Register description is as above.*
base address +AAh EVENTLOGn_FIFO10_TIME	31:0	EVENTLOGn_FIFO10_TIME [31:0]	0000 0000h	Event Log FIFO Index 10 Time
base address +ACh EVENTLOGn_FIFO11_READ	12	EVENTLOGn_FIFO11_POL	0	Event Log FIFO Index 11 polarity *Register description is as above.*
	8:0	EVENTLOGn_FIFO11_ID [8:0]	000h	Event Log FIFO Index 11 source *Register description is as above.*
base address +AEh EVENTLOGn_FIFO11_TIME	31:0	EVENTLOGn_FIFO11_TIME [31:0]	0000 0000h	Event Log FIFO Index 11 Time
base address +B0h EVENTLOGn_FIFO12_READ	12	EVENTLOGn_FIFO12_POL	0	Event Log FIFO Index 12 polarity *Register description is as above.*
	8:0	EVENTLOGn_FIFO12_ID [8:0]	000h	Event Log FIFO Index 12 source *Register description is as above.*
base address +B2h EVENTLOGn_FIFO12_TIME	31:0	EVENTLOGn_FIFO12_TIME [31:0]	0000 0000h	Event Log FIFO Index 12 Time
base address +B4h EVENTLOGn_FIFO13_	12	EVENTLOGn_FIFO13_POL	0	Event Log FIFO Index 13 polarity *Register description is as above.*

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
READ	8:0	EVENTLOGn_FIFO13_ID [8:0]	000h	Event Log FIFO Index 13 source *Register description is as above.*
base address +B6h EVENTLOGn_FIFO13_TIME	31:0	EVENTLOGn_FIFO13_TIME [31:0]	0000 0000h	Event Log FIFO Index 13 Time
base address +B8h EVENTLOGn_FIFO14_READ	12	EVENTLOGn_FIFO14_POL	0	Event Log FIFO Index 14 polarity *Register description is as above.*
	8:0	EVENTLOGn_FIFO14_ID [8:0]	000h	Event Log FIFO Index 14 source *Register description is as above.*
base address +BAh EVENTLOGn_FIFO14_TIME	31:0	EVENTLOGn_FIFO14_TIME [31:0]	0000 0000h	Event Log FIFO Index 14 Time
base address +BCh EVENTLOGn_FIFO15_READ	12	EVENTLOGn_FIFO15_POL	0	Event Log FIFO Index 15 polarity *Register description is as above.*
	8:0	EVENTLOGn_FIFO15_ID [8:0]	000h	Event Log FIFO Index 15 source *Register description is as above.*
base address +BEh EVENTLOGn_FIFO15_TIME	31:0	EVENTLOGn_FIFO15_TIME [31:0]	0000 0000h	Event Log FIFO Index 15 Time

Table 33 Event Logger (EVENTLOGn) Control

A list of the valid input sources for the Event Loggers is provided in Table 34.

The “EDGE” type noted is coded as “S” (single edge) or “D” (dual edge). Note that a single-edge input source will only provide valid input to the Event Logger in the default (Rising Edge Triggered) polarity.

It is advised to take care when enabling IRQ1 or IRQ2 as an input source for the Event Loggers; a recursive loop, where the IRQ signal is also an output from the same Event Logger, must be avoided.

ID	DESCRIPTION	EDGE	ID	DESCRIPTION	EDGE	ID	DESCRIPTION	EDGE
3	irq1	D	259	gpio4	D	354	event3_full	S
4	irq2	D	260	gpio5	D	355	event4_full	S
9	sysclk_fail	S	261	gpio6	D	356	event5_full	S
24	fll1_lock	D	262	gpio7	D	357	event6_full	S
25	fll2_lock	D	263	gpio8	D	358	event7_full	S
26	fll3_lock	D	264	gpio9	D	359	event8_full	S
32	frame_start_g1r1	S	265	gpio10	D	368	event1_wmark	S
33	frame_start_g1r2	S	266	gpio11	D	369	event2_wmark	S
34	frame_start_g1r3	S	267	gpio12	D	370	event3_wmark	S
40	frame_start_g2r1_sys	S	268	gpio13	D	371	event4_wmark	S
41	frame_start_g2r2_sys	S	269	gpio14	D	372	event5_wmark	S
80	hpdet	S	270	gpio15	D	373	event6_wmark	S
88	micdet	S	271	gpio16	D	374	event7_wmark	S
96	jd1_rise	S	272	gpio17	D	375	event8_wmark	S
97	jd1_fall	S	273	gpio18	D	384	dsp1_dma	S
98	jd2_rise	S	274	gpio19	D	385	dsp2_dma	S
99	jd2_fall	S	275	gpio20	D	386	dsp3_dma	S
100	micd_clamp_rise	S	276	gpio21	D	387	dsp4_dma	S
101	micd_clamp_fall	S	277	gpio22	D	388	dsp5_dma	S
128	drc1_sig_det	D	278	gpio23	D	389	dsp6_dma	S
129	drc2_sig_det	D	279	gpio24	D	390	dsp7_dma	S

ID	DESCRIPTION	EDGE	ID	DESCRIPTION	EDGE	ID	DESCRIPTION	EDGE
136	asrc1_in1_lock	D	280	gpio25	D	416	dsp1_start1	S
137	asrc1_in2_lock	D	281	gpio26	D	417	dsp2_start1	S
138	asrc2_in1_lock	D	282	gpio27	D	418	dsp3_start1	S
139	asrc2_in2_lock	D	283	gpio28	D	419	dsp4_start1	S
160	dsp_irq1	S	284	gpio29	D	420	dsp5_start1	S
161	dsp_irq2	S	285	gpio30	D	421	dsp6_start1	S
162	dsp_irq3	S	286	gpio31	D	422	dsp7_start1	S
163	dsp_irq4	S	287	gpio32	D	432	dsp1_start2	S
164	dsp_irq5	S	288	gpio33	D	433	dsp2_start2	S
165	dsp_irq6	S	289	gpio34	D	434	dsp3_start2	S
166	dsp_irq7	S	290	gpio35	D	435	dsp4_start2	S
167	dsp_irq8	S	291	gpio36	D	436	dsp5_start2	S
168	dsp_irq9	S	292	gpio37	D	437	dsp6_start2	S
169	dsp_irq10	S	293	gpio38	D	438	dsp7_start2	S
170	dsp_irq11	S	294	gpio39	D	448	dsp1_start	S
171	dsp_irq12	S	295	gpio40	D	449	dsp2_start	S
172	dsp_irq13	S	320	Timer1	S	450	dsp3_start	S
173	dsp_irq14	S	321	Timer2	S	451	dsp4_start	S
174	dsp_irq15	S	322	Timer3	S	452	dsp5_start	S
175	dsp_irq16	S	323	Timer4	S	453	dsp6_start	S
176	hp1l_sc	S	324	Timer5	S	454	dsp7_start	S
177	hp1r_sc	S	325	Timer6	S	464	dsp1_busy	D
178	hp2l_sc	S	326	Timer7	S	465	dsp2_busy	D
179	hp2r_sc	S	327	Timer8	S	466	dsp3_busy	D
180	hp3l_sc	S	336	event1_not_empty	S	467	dsp4_busy	D
181	hp3r_sc	S	337	event2_not_empty	S	468	dsp5_busy	D
182	spkoutl_short	D	338	event3_not_empty	S	469	dsp6_busy	D
183	spkoutr_short	D	339	event4_not_empty	S	470	dsp7_busy	D
224	spk_shutdown	D	340	event5_not_empty	S	480	mif1_done	S
225	spk_overheat	S	341	event6_not_empty	S	481	mif2_done	S
226	spk_overheat_warn	S	342	event7_not_empty	S	482	mif3_done	S
256	gpio1	D	343	event8_not_empty	S	496	mif1_block	S
257	gpio2	D	352	event1_full	S	497	mif2_block	S
258	gpio3	D	353	event2_full	S	498	mif3_block	S

Table 34 Event Logger Input Sources

GENERAL PURPOSE TIMERS

The CS47L85 incorporates 8 general purpose timers, which support a wide variety of possible uses. In particular, these timers provide essential support for the sensor hub capability. The timers allow time stamp information to be associated with external sensor activity, and other system events, enabling real time data to be more easily integrated into user applications. The timers allow many advanced functions to be implemented with a high degree of autonomy from a host processor.

The timers can use either internal system clocks, or external clock signals, as a reference. The selected reference is scaled down, using configurable dividers, to the required clock count frequency.

The reference clock for each Timer is selected using TIMERn_REFCLK_SRC, (where 'n' identifies the applicable Timer, 1 through to 8).

If SYSCLK, ASYNCCLK, or DSPCLK is selected, then a lower clock frequency, derived from the applicable system clock, can be selected using the TIMERn_REFCLK_FREQ_SEL register. The applicable division ratio is determined automatically, assuming the respective clock source has been correctly configured as described in the "Clocking and Sample Rates" section.

If any source other than DSPCLK is selected, then the clock can be further divided using the TIMERn_REFCLK_DIV register. Division ratios in the range 1 to 128 can be selected.

Note that, if DSPCLK is enabled, then the CS47L85 will synchronise the selected reference clock to DSPCLK. As a result of this, if a non-DSPCLK is selected as source, the following additional constraints must be observed: the reference clock frequency (after TIMERn_REFCLK_FREQ_SEL and after TIMERn_REFCLK_DIV) must be less than DSPCLK / 3, and must be less than 12MHz; it must also be close to 50% duty cycle. The TIMERn_REFCLK_DIV register can be used to ensure that these criteria are met.

One final division, controlled by TIMERn_PRESCALE, determines the Timer count frequency. This register is valid for all clock reference sources; division ratios in the range 1 to 128 can be selected. The output from this division corresponds to the frequency at which the TIMERn_COUNT registers are incremented (or decremented).

The maximum count value of the Timer is determined by the TIMERn_MAX_COUNT field. This is the final count value (when counting up), or the initial count value (when counting down). The current value of the Timer counter can be read from the TIMERn_CUR_COUNT field.

The Timer is started by writing '1' to the TIMERn_START bit. Note that, if the Timer is already running, it will re-start from its initial value. The Timer is stopped by writing '1' to the TIMERn_STOP bit. The count direction (up or down) is selected using the TIMERn_DIR bit.

The TIMERn_CONTINUOUS bit selects whether the Timer automatically re-starts after the 'end of count' condition has been reached. The TIMERn_RUNNING_STS indicates whether the Timer is running, or if it has stopped.

Note that the Timers should be stopped before making any changes to the respective configuration registers. The Timer configuration should only be changed when TIMERn_RUNNING_STS=0.

The reference clock for each Timer should be configured and enabled before starting the Timer, and whenever the Timer is running. If the reference clock is interrupted while the Timer is running, the Timer operation pauses, and resumes again when the clock restarts. See "Clocking and Sample Rates" for details of the system clocks (including requirements for reconfiguring SYSCLK or DSPCLK while DSP peripherals are enabled).

The Timer status is an input to the Interrupt control circuit and can be used to trigger an Interrupt event after the final count value is reached - see "Interrupts". Note that the Interrupt does not occur immediately when the final count value is reached; the Interrupt is triggered at the point when the next update to the Timer count value would be due.

The Timer status can be output directly on a GPIO pin as an external indication of the Timer activity. See "General Purpose Input / Output" to configure a GPIO pin for this function.

The Timers can be used as a Watchdog function to trigger a shutdown of the Class D speaker drivers. See "Thermal Shutdown and Short Circuit Protection" to configure this function.

The Timer block is illustrated in Figure 44.

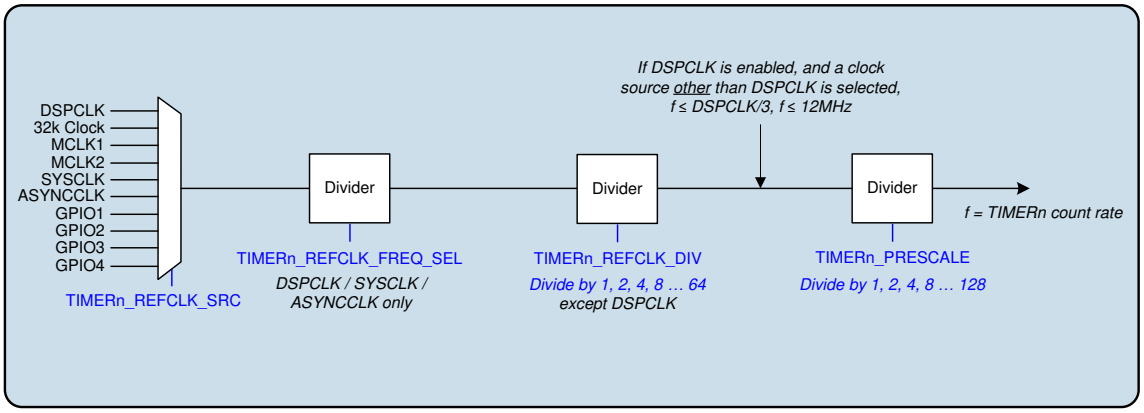


Figure 44 General Purpose Timer

The Timer control registers are described in Table 35.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
Timer 1 Base Address = R311296 (4C000h) Timer 2 Base Address = R311424 (4C080h) Timer 3 Base Address = R311552 (4C100h) Timer 4 Base Address = R311680 (4C180h) Timer 5 Base Address = R311808 (4C200h) Timer 6 Base Address = R311936 (4C280h) Timer 7 Base Address = R312064 (4C300h) Timer 8 Base Address = R312192 (4C380h)				
base address Timer*n*_Control	21	TIMERn_CONTINUOUS	0	Timer Continuous Mode select 0 = Single mode 1 = Continuous mode Timer must be stopped (TIMERn_RUNNING_STS=0) when updating this register
	20	TIMERn_DIR	0	Timer Count Direction 0 = Down 1 = Up Timer must be stopped (TIMERn_RUNNING_STS=0) when updating this register
	18:16	TIMERn_PRESCALE [2:0]	000	Timer Count Rate Prescale 000 = Divide by 1 001 = Divide by 2 010 = Divide by 4 011 = Divide by 8 100 = Divide by 16 101 = Divide by 32 110 = Divide by 64 111 = Divide by 128 Timer must be stopped (TIMERn_RUNNING_STS=0) when updating this register

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	14:12	TIMERn_REFCLK_DIV [2:0]	000	Timer Reference Clock Divide (Not valid for DSPCLK source). 000 = Divide by 1 001 = Divide by 2 010 = Divide by 4 011 = Divide by 8 100 = Divide by 16 101 = Divide by 32 110 = Divide by 64 111 = Divide by 128 If DSPCLK is enabled, and DSPCLK is not selected as source, then the output frequency from this divider must be set less than or equal to DSPCLK/3, and less than or equal to 12MHz. If DSPCLK is disabled, then the output of this divider will be used as clock reference for any associated Event Logger. In this case, the divider output corresponds to the frequency of Event Logging opportunities on the respective module(s). Timer must be stopped (TIMERn_RUNNING_STS=0) when updating this register
	10:8	TIMERn_REFCLK_FREQ_SEL [2:0]	000	Timer Reference Frequency Select Only valid when SYSCLK, ASYNCCLK, or DSPCLK is the source. The selected frequency must be less than or equal to the frequency of the respective source. SYSCLK or ASYNCCLK source: 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) All other codes are Reserved DSPCLK source: 000 = 5.5MHz to 9.375MHz 001 = 9.375MHz to 18.75MHz 010 = 18.75MHz to 37.5MHz 011 = 37.5MHz to 75MHz All other codes are Reserved Note that, because DSPCLK could be any frequency (within the valid ranges), it is not possible to quote exact frequencies in this register definition. The exact frequency will be derived as DSPCLK divided by 1, 2, 4, 8, or 16. Timer must be stopped (TIMERn_RUNNING_STS=0) when updating this register.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:0	TIMERn_REFCLK_SRC [3:0]	0000	Timer Reference Source Select 0000 = DSPCLK 0001 = 32kHz clock 0100 = MCLK1 0101 = MCLK2 1000 = SYSCLK 1001 = ASYNCCLK 1100 = GPIO1 1101 = GPIO2 1110 = GPIO3 1111 = GPIO4 All other codes are Reserved Timer must be stopped (TIMERn_RUNNING_STS=0) when updating this register
base address +02h Timer*n*_Count_Preset	31:0	TIMERn_MAX_COUNT [31:0]	0000 0000h	Timer Maximum Count Final count value (when counting up) Starting count value (when counting down) Timer must be stopped (TIMERn_RUNNING_STS=0) when updating this register
base address +06h Timer*n*_Start_and_Stop	4	TIMERn_STOP	0	Timer Stop Control Write '1' to stop.
	0	TIMERn_START	0	Timer Start Control Write '1' to start. If the Timer is already running, then it will re-start from its initial value.
base address +08h Timer*n*_Status	0	TIMERn_RUNNING_STS	0	Timer Running Status 0 = Timer stopped 1 = Timer running
base address +0Ah Timer*n*_Count_Readback	31:0	TIMERn_CUR_COUNT [31:0]	0000h	Timer Current Count value

Table 35 General Purpose Timer (TIMERn) Control

DSP GPIO

The CS47L85 supports up to 40 GPIO pins, which can be assigned to application-specific functions. There are 8 dedicated GPIO pins, and a further 32 GPIOs that are implemented as alternate functions to a pin-specific capability.

The GPIOs can be used to provide status outputs and control signals to external hardware; the supported functions include Interrupt (IRQ) output, FLL Clock output, Accessory Detection status, and S/PDIF or PWM-coded audio channels. See “General Purpose Input / Output” for further details.

The GPIOs can support miscellaneous logic input and output, interfacing directly with the integrated DSPs, or with the Host Application software. A basic level of I/O functionality is described in the “General Purpose Input / Output” section, under the configuration where GPn_FN = 001h. (The GPn_FN register selects the functionality for the respective pin, GPIOn.)

The DSP GPIO function provides an advanced I/O capability, supporting the requirements of the CS47L85 as a multi-purpose sensor hub. The DSP GPIO pins are accessed using maskable sets of I/O control registers; this allows the selected combinations of GPIOs to be controlled with ease, regardless of how the allocation of GPIO pins has been implemented in hardware. In a typical use case, one GPIO mask is defined for each DSP, or for each functional process; this provides a highly efficient mechanism for each DSP to independently access the respective input and output signals.

The DSP GPIO function is selected by setting GPn_FN = 002h for the respective GPIO pin (where ‘n’ identifies the applicable GPIOn pin).

Each DSP GPIO is controlled using register bits that determine the direction (input/output) and the logic state (0/1) of the pin. These register bits are replicated in 8 control ‘sets’; each of the control sets has the capability to determine the logic level of any DSP GPIO.

Mask bits are provided within each control set, to determine which of the control sets has control of each DSP GPIO. To avoid logic contention, a DSP GPIO output must be controlled (unmasked) in a maximum of one control set at any time.

Note that write access to the direction control bits (DSPGPn_SETx_DIR) and level control bits (DSPGPn_SETx_LVL) is only valid when the channel (DSPGPn) is unmasked in the respective control set. Register writes to these fields will be implemented for the unmasked DSP GPIOs, and will be ignored in respect of the masked DSP GPIOs. Note that the level control bits (DSPGPn_SETx_LVL) are provide output level control only; they cannot be used for input readback.

The logic level of the unmasked DSP GPIO outputs in any control set are typically configured using a single register write. (GPIOs 1 to 32 are set in a single operation; a separate register write is required for GPIOs 33 to 40.) Writing to these registers will determine the logic level of the unmasked DSP GPIOs in that set only; all other outputs are unaffected.

Status bits are provided, for readback of DSP GPIO inputs. There is only one set of status bits, indicating the logic level of every input or output pin that is configured as a DSP GPIO. (Note that, for any pin configured as a GPIO input, with GPn_FN = 001h, the applicable DSPGPn_STS bit will also provide valid readback of the pin status.)

The status bits will also indicate the logic level of the DSP GPIO outputs. The respective pins are driven as outputs if configured as a DSP GPIO output, and unmasked in one of the control sets. Note that a DSP GPIO will continue to be driven as an output, even if the mask bit is subsequently asserted in that set. The pin will only cease to be driven if it is configured as a DSP GPIO input, and is unmasked in one of the control sets, or else if the pin is configured as an input, under a different GPn_FN register selection.

The DSP GPIO functions are implemented alongside the ‘standard’ GPIO capability, providing an alternative method of maskable I/O control for all of the GPIO pins. The DSP GPIO control bits in the register map are implemented in a manner that supports efficient read/write access for multiple GPIOs at once.

The DSP GPIO logic is illustrated in Figure 45, also showing the control registers that are common to the ‘standard’ GPIO.

The DSP GPIO function is selected by setting GPn_FN = 002h for the respective GPIO pin. Integrated pull-up and pull-down resistors are provided on each of the GPIO pins, which are also valid for DSP GPIO function. A ‘bus keeper’ function is supported on the GPIO pins; this is enabled using the respective pull-up and pull-down control bits. The bus keeper function holds the logic level unchanged whenever the pin is undriven (e.g., if the signal is tri-stated). See Table 94 for details of the GPIO pull-up and pull-down control bits.

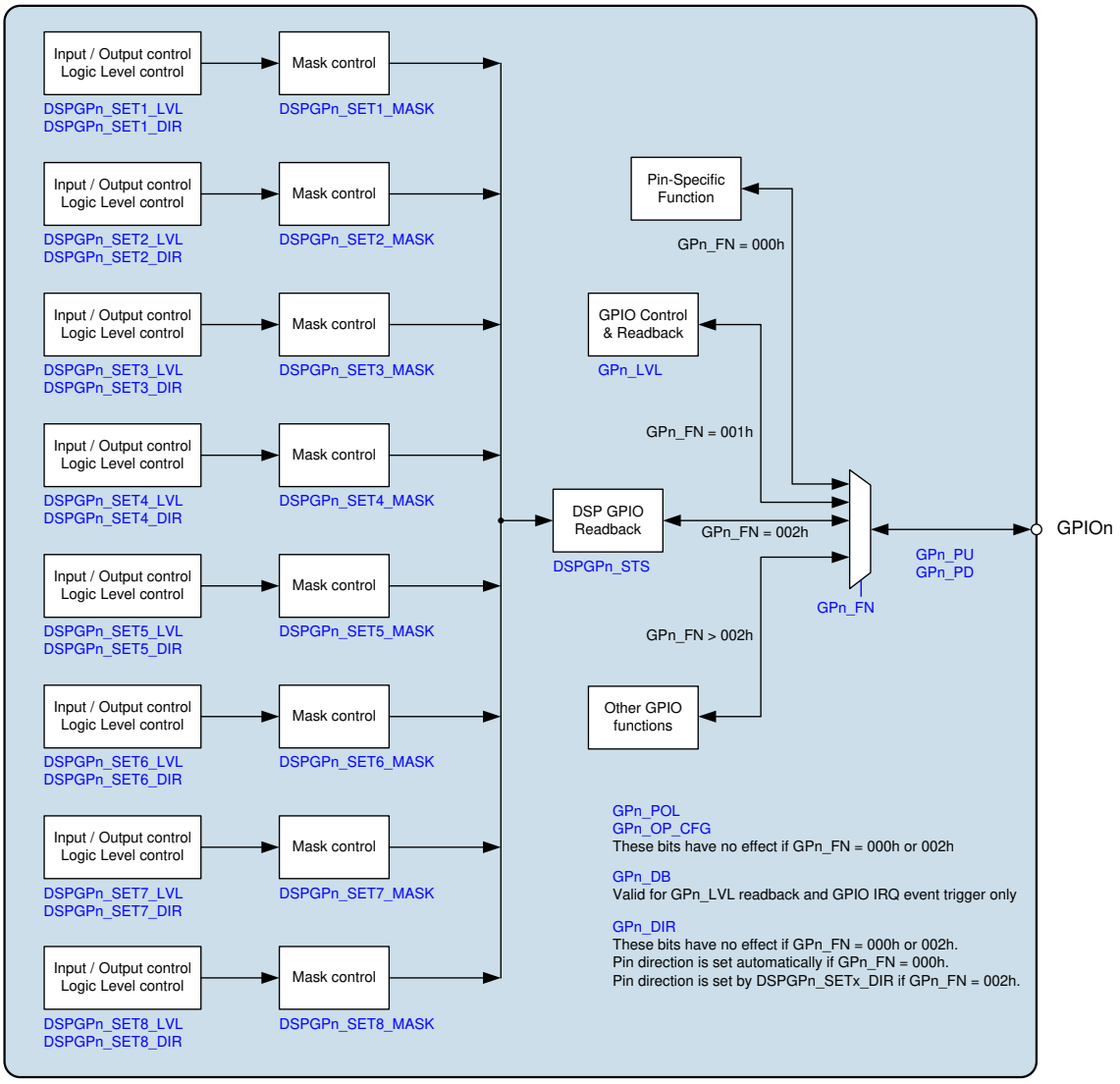


Figure 45 DSP GPIO Control

The control registers associated with the DSP GPIO are described in Table 36.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R315392 (4D000h) DSPGP_Status_1	31	DSPGP32_STS	0	DSPGP32 Status Valid for DSPGP input and output
	30	DSPGP31_STS	0	DSPGP31 Status
	29	DSPGP30_STS	0	DSPGP30 Status
	28	DSPGP29_STS	0	DSPGP29 Status
	27	DSPGP28_STS	0	DSPGP28 Status
	26	DSPGP27_STS	0	DSPGP27 Status
	25	DSPGP26_STS	0	DSPGP26 Status
	24	DSPGP25_STS	0	DSPGP25 Status
	23	DSPGP24_STS	0	DSPGP24 Status
	22	DSPGP23_STS	0	DSPGP23 Status
	21	DSPGP22_STS	0	DSPGP22 Status
	20	DSPGP21_STS	0	DSPGP21 Status
	19	DSPGP20_STS	0	DSPGP20 Status
	18	DSPGP19_STS	0	DSPGP19 Status
	17	DSPGP18_STS	0	DSPGP18 Status
	16	DSPGP17_STS	0	DSPGP17 Status
	15	DSPGP16_STS	0	DSPGP16 Status
	14	DSPGP15_STS	0	DSPGP15 Status
	13	DSPGP14_STS	0	DSPGP14 Status
	12	DSPGP13_STS	0	DSPGP13 Status
	11	DSPGP12_STS	0	DSPGP12 Status
	10	DSPGP11_STS	0	DSPGP11 Status
	9	DSPGP10_STS	0	DSPGP10 Status
	8	DSPGP9_STS	0	DSPGP9 Status
	7	DSPGP8_STS	0	DSPGP8 Status
	6	DSPGP7_STS	0	DSPGP7 Status
	5	DSPGP6_STS	0	DSPGP6 Status
	4	DSPGP5_STS	0	DSPGP5 Status
	3	DSPGP4_STS	0	DSPGP4 Status
	2	DSPGP3_STS	0	DSPGP3 Status
	1	DSPGP2_STS	0	DSPGP2 Status
	0	DSPGP1_STS	0	DSPGP1 Status
R315394 (4D002h) DSPGP_Status_2	7	DSPGP40_STS	0	DSPGP40 Status
	6	DSPGP39_STS	0	DSPGP39 Status
	5	DSPGP38_STS	0	DSPGP38 Status
	4	DSPGP37_STS	0	DSPGP37 Status
	3	DSPGP36_STS	0	DSPGP36 Status
	2	DSPGP35_STS	0	DSPGP35 Status
	1	DSPGP34_STS	0	DSPGP34 Status
	0	DSPGP33_STS	0	DSPGP33 Status
R315424 (4D020h) DSPGP_SET1_Mask_1 R315456 (4D040h) DSPGP_SET2_Mask_1	31	DSPGP32_SETn_MASK	1	DSP SETn GPIO32 Mask Control 0 = Unmasked 1 = Masked A GPIO pin should be unmasked in a maximum of one SET at any time.
	30	DSPGP31_SETn_MASK	1	DSP SETn GPIO31 Mask Control
R315488 (4D060h) DSPGP_SET3_Mask_1	29	DSPGP30_SETn_MASK	1	DSP SETn GPIO30 Mask Control
	28	DSPGP29_SETn_MASK	1	DSP SETn GPIO29 Mask Control
	27	DSPGP28_SETn_MASK	1	DSP SETn GPIO28 Mask Control
R315520 (4D080h) DSPGP_SET4_Mask_1	26	DSPGP27_SETn_MASK	1	DSP SETn GPIO27 Mask Control
	25	DSPGP26_SETn_MASK	1	DSP SETn GPIO26 Mask Control
R315552 (4D0A0h) DSPGP_SET5_Mask_1	24	DSPGP25_SETn_MASK	1	DSP SETn GPIO25 Mask Control
	23	DSPGP24_SETn_MASK	1	DSP SETn GPIO24 Mask Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R315584 (4D0C0h) DSPGP_SET6_Mask_1 R315616 (4D0E0h) DSPGP_SET7_Mask_1 R315648 (4D100h) DSPGP_SET8_Mask_1	22	DSPGP23_SETn_MASK	1	DSP SETn GPIO23 Mask Control
	21	DSPGP22_SETn_MASK	1	DSP SETn GPIO22 Mask Control
	20	DSPGP21_SETn_MASK	1	DSP SETn GPIO21 Mask Control
	19	DSPGP20_SETn_MASK	1	DSP SETn GPIO20 Mask Control
	18	DSPGP19_SETn_MASK	1	DSP SETn GPIO19 Mask Control
	17	DSPGP18_SETn_MASK	1	DSP SETn GPIO18 Mask Control
	16	DSPGP17_SETn_MASK	1	DSP SETn GPIO17 Mask Control
	15	DSPGP16_SETn_MASK	1	DSP SETn GPIO16 Mask Control
	14	DSPGP15_SETn_MASK	1	DSP SETn GPIO15 Mask Control
	13	DSPGP14_SETn_MASK	1	DSP SETn GPIO14 Mask Control
	12	DSPGP13_SETn_MASK	1	DSP SETn GPIO13 Mask Control
	11	DSPGP12_SETn_MASK	1	DSP SETn GPIO12 Mask Control
	10	DSPGP11_SETn_MASK	1	DSP SETn GPIO11 Mask Control
	9	DSPGP10_SETn_MASK	1	DSP SETn GPIO10 Mask Control
	8	DSPGP9_SETn_MASK	1	DSP SETn GPIO9 Mask Control
	7	DSPGP8_SETn_MASK	1	DSP SETn GPIO8 Mask Control
	6	DSPGP7_SETn_MASK	1	DSP SETn GPIO7 Mask Control
	5	DSPGP6_SETn_MASK	1	DSP SETn GPIO6 Mask Control
	4	DSPGP5_SETn_MASK	1	DSP SETn GPIO5 Mask Control
	3	DSPGP4_SETn_MASK	1	DSP SETn GPIO4 Mask Control
	2	DSPGP3_SETn_MASK	1	DSP SETn GPIO3 Mask Control
	1	DSPGP2_SETn_MASK	1	DSP SETn GPIO2 Mask Control
	0	DSPGP1_SETn_MASK	1	DSP SETn GPIO1 Mask Control
R315426 (4D022h) DSPGP_SET1_Mask_2 R315458 (4D042h) DSPGP_SET2_Mask_2 R315490 (4D062h) DSPGP_SET3_Mask_2 R315522 (4D082h) DSPGP_SET4_Mask_2 R315554 (4D0A2h) DSPGP_SET5_Mask_2 R315586 (4D0C2h) DSPGP_SET6_Mask_2 R315618 (4D0E2h) DSPGP_SET7_Mask_2 R315650 (4D102h) DSPGP_SET8_Mask_2	7	DSPGP40_SETn_MASK	1	DSP SETn GPIO40 Mask Control
	6	DSPGP39_SETn_MASK	1	DSP SETn GPIO39 Mask Control
	5	DSPGP38_SETn_MASK	1	DSP SETn GPIO38 Mask Control
	4	DSPGP37_SETn_MASK	1	DSP SETn GPIO37 Mask Control
	3	DSPGP36_SETn_MASK	1	DSP SETn GPIO36 Mask Control
	2	DSPGP35_SETn_MASK	1	DSP SETn GPIO35 Mask Control
	1	DSPGP34_SETn_MASK	1	DSP SETn GPIO34 Mask Control
	0	DSPGP33_SETn_MASK	1	DSP SETn GPIO33 Mask Control
R315432 (4D028h) DSPGP_SET1_Direction_1 R315464 (4D048h) DSPGP_SET2_Direction_1 R315496 (4D068h) DSPGP_SET3_Direction_1 R315528 (4D088h)	31	DSPGP32_SETn_DIR	1	DSP SETn GPIO32 Direction Control 0 = Output 1 = Input
	30	DSPGP31_SETn_DIR	1	DSP SETn GPIO31 Direction Control
	29	DSPGP30_SETn_DIR	1	DSP SETn GPIO30 Direction Control
	28	DSPGP29_SETn_DIR	1	DSP SETn GPIO29 Direction Control
	27	DSPGP28_SETn_DIR	1	DSP SETn GPIO28 Direction Control
	26	DSPGP27_SETn_DIR	1	DSP SETn GPIO27 Direction Control
	25	DSPGP26_SETn_DIR	1	DSP SETn GPIO26 Direction Control
	24	DSPGP25_SETn_DIR	1	DSP SETn GPIO25 Direction Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
DSPGP_SET4_Direction_1 R315560 (4D0A8h) DSPGP_SET5_Direction_1 R315592 (4D0C8h) DSPGP_SET6_Direction_1 R315624 (4D0E8h) DSPGP_SET7_Direction_1 R315656 (4D108h) DSPGP_SET8_Direction_1	23	DSPGP24_SETn_DIR	1	DSP SETn GPIO24 Direction Control
	22	DSPGP23_SETn_DIR	1	DSP SETn GPIO23 Direction Control
	21	DSPGP22_SETn_DIR	1	DSP SETn GPIO22 Direction Control
	20	DSPGP21_SETn_DIR	1	DSP SETn GPIO21 Direction Control
	19	DSPGP20_SETn_DIR	1	DSP SETn GPIO20 Direction Control
	18	DSPGP19_SETn_DIR	1	DSP SETn GPIO19 Direction Control
	17	DSPGP18_SETn_DIR	1	DSP SETn GPIO18 Direction Control
	16	DSPGP17_SETn_DIR	1	DSP SETn GPIO17 Direction Control
	15	DSPGP16_SETn_DIR	1	DSP SETn GPIO16 Direction Control
	14	DSPGP15_SETn_DIR	1	DSP SETn GPIO15 Direction Control
	13	DSPGP14_SETn_DIR	1	DSP SETn GPIO14 Direction Control
	12	DSPGP13_SETn_DIR	1	DSP SETn GPIO13 Direction Control
	11	DSPGP12_SETn_DIR	1	DSP SETn GPIO12 Direction Control
	10	DSPGP11_SETn_DIR	1	DSP SETn GPIO11 Direction Control
	9	DSPGP10_SETn_DIR	1	DSP SETn GPIO10 Direction Control
	8	DSPGP9_SETn_DIR	1	DSP SETn GPIO9 Direction Control
	7	DSPGP8_SETn_DIR	1	DSP SETn GPIO8 Direction Control
	6	DSPGP7_SETn_DIR	1	DSP SETn GPIO7 Direction Control
	5	DSPGP6_SETn_DIR	1	DSP SETn GPIO6 Direction Control
	4	DSPGP5_SETn_DIR	1	DSP SETn GPIO5 Direction Control
	3	DSPGP4_SETn_DIR	1	DSP SETn GPIO4 Direction Control
	2	DSPGP3_SETn_DIR	1	DSP SETn GPIO3 Direction Control
	1	DSPGP2_SETn_DIR	1	DSP SETn GPIO2 Direction Control
	0	DSPGP1_SETn_DIR	1	DSP SETn GPIO1 Direction Control
R315434 (4D02Ah) DSPGP_SET1_Direction_2 R315466 (4D04Ah) DSPGP_SET2_Direction_2 R315498 (4D06Ah) DSPGP_SET3_Direction_2 R315530 (4D08Ah) DSPGP_SET4_Direction_2 R315562 (4D0AAh) DSPGP_SET5_Direction_2 R315594 (4D0CAh) DSPGP_SET6_Direction_2 R315626 (4D0EAh) DSPGP_SET7_Direction_2 R315658 (4D10Ah) DSPGP_SET8_Direction_2	7	DSPGP40_SETn_DIR	1	DSP SETn GPIO40 Direction Control
	6	DSPGP39_SETn_DIR	1	DSP SETn GPIO39 Direction Control
	5	DSPGP38_SETn_DIR	1	DSP SETn GPIO38 Direction Control
	4	DSPGP37_SETn_DIR	1	DSP SETn GPIO37 Direction Control
	3	DSPGP36_SETn_DIR	1	DSP SETn GPIO36 Direction Control
	2	DSPGP35_SETn_DIR	1	DSP SETn GPIO35 Direction Control
	1	DSPGP34_SETn_DIR	1	DSP SETn GPIO34 Direction Control
	0	DSPGP33_SETn_DIR	1	DSP SETn GPIO33 Direction Control
R315440 (4D030h) DSPGP_SET1_Level_ R315472 (4D050h) DSPGP_SET2_Level_1 R315504 (4D070h) DSPGP_SET3_Level_1	31	DSPGP32_SETn_LVL	0	DSP SETn GPIO32 Output Level 0 = Logic 0 1 = Logic 1
	30	DSPGP31_SETn_LVL	0	DSP SETn GPIO31 Output Level
	29	DSPGP30_SETn_LVL	0	DSP SETn GPIO30 Output Level
	28	DSPGP29_SETn_LVL	0	DSP SETn GPIO29 Output Level
	27	DSPGP28_SETn_LVL	0	DSP SETn GPIO28 Output Level
	26	DSPGP27_SETn_LVL	0	DSP SETn GPIO27 Output Level
	25	DSPGP26_SETn_LVL	0	DSP SETn GPIO26 Output Level

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R315536 (4D090h) DSPGP_SET4_Level_1 R315568 (4D0B0h) DSPGP_SET5_Level_1 R315600 (4D0D0h) DSPGP_SET6_Level_1 R315632 (4D0F0h) DSPGP_SET7_Level_1 R315664 (4D110h) DSPGP_SET8_Level_1	24	DSPGP25_SETn_LVL	0	DSP SETn GPIO25 Output Level
	23	DSPGP24_SETn_LVL	0	DSP SETn GPIO24 Output Level
	22	DSPGP23_SETn_LVL	0	DSP SETn GPIO23 Output Level
	21	DSPGP22_SETn_LVL	0	DSP SETn GPIO22 Output Level
	20	DSPGP21_SETn_LVL	0	DSP SETn GPIO21 Output Level
	19	DSPGP20_SETn_LVL	0	DSP SETn GPIO20 Output Level
	18	DSPGP19_SETn_LVL	0	DSP SETn GPIO19 Output Level
	17	DSPGP18_SETn_LVL	0	DSP SETn GPIO18 Output Level
	16	DSPGP17_SETn_LVL	0	DSP SETn GPIO17 Output Level
	15	DSPGP16_SETn_LVL	0	DSP SETn GPIO16 Output Level
	14	DSPGP15_SETn_LVL	0	DSP SETn GPIO15 Output Level
	13	DSPGP14_SETn_LVL	0	DSP SETn GPIO14 Output Level
	12	DSPGP13_SETn_LVL	0	DSP SETn GPIO13 Output Level
	11	DSPGP12_SETn_LVL	0	DSP SETn GPIO12 Output Level
	10	DSPGP11_SETn_LVL	0	DSP SETn GPIO11 Output Level
	9	DSPGP10_SETn_LVL	0	DSP SETn GPIO10 Output Level
	8	DSPGP9_SETn_LVL	0	DSP SETn GPIO9 Output Level
	7	DSPGP8_SETn_LVL	0	DSP SETn GPIO8 Output Level
	6	DSPGP7_SETn_LVL	0	DSP SETn GPIO7 Output Level
	5	DSPGP6_SETn_LVL	0	DSP SETn GPIO6 Output Level
	4	DSPGP5_SETn_LVL	0	DSP SETn GPIO5 Output Level
	3	DSPGP4_SETn_LVL	0	DSP SETn GPIO4 Output Level
	2	DSPGP3_SETn_LVL	0	DSP SETn GPIO3 Output Level
	1	DSPGP2_SETn_LVL	0	DSP SETn GPIO2 Output Level
	0	DSPGP1_SETn_LVL	0	DSP SETn GPIO1 Output Level
R315442 (4D032h) DSPGP_SET1_Level_2 R315474 (4D052h) DSPGP_SET2_Level_2 R315506 (4D072h) DSPGP_SET3_Level_2 R315538 (4D092h) DSPGP_SET4_Level_2 R315570 (4D0B2h) DSPGP_SET5_Level_2 R315602 (4D0D2h) DSPGP_SET6_Level_2 R315634 (4D0F2h) DSPGP_SET7_Level_2 R315666 (4D112h) DSPGP_SET8_Level_2	7	DSPGP40_SETn_LVL	0	DSP SETn GPIO40 Output Level
	6	DSPGP39_SETn_LVL	0	DSP SETn GPIO39 Output Level
	5	DSPGP38_SETn_LVL	0	DSP SETn GPIO38 Output Level
	4	DSPGP37_SETn_LVL	0	DSP SETn GPIO37 Output Level
	3	DSPGP36_SETn_LVL	0	DSP SETn GPIO36 Output Level
	2	DSPGP35_SETn_LVL	0	DSP SETn GPIO35 Output Level
	1	DSPGP34_SETn_LVL	0	DSP SETn GPIO34 Output Level
	0	DSPGP33_SETn_LVL	0	DSP SETn GPIO33 Output Level

Table 36 DSP GPIO Control

AMBIENT NOISE CANCELLATION

The Cirrus Logic Ambient Noise Cancellation (ANC) processor within the CS47L85 provides the capability to improve the intelligibility of a voice call by using destructive interference to reduce the acoustic energy of the ambient sound. The stereo ANC capability supports a wide variety of headset/handset applications.

The ANC processor is configured using parameters that are determined during product development and downloaded to the CS47L85. The configuration settings are specific to the acoustic properties of the target application. The primary acoustic elements in an application are typically the microphones and the speaker, but other components such as the plastics and the PCBs also have significant importance to the acoustic coefficient data.

Note that the ANC configuration parameters are application-specific, and must be recalculated following any change in the design of the acoustic elements of that application. Any mismatch between the acoustic coefficient data and the target application will give inferior ANC performance.

The signal path configuration settings are adjusted during product calibration to compensate for component tolerances. Also, calibration allows DC offsets in the earpiece output path to be measured and compensated, thus reducing power consumption and minimising any pops and clicks in the output signal path.

The ANC processor employs stereo digital circuits to process the ambient noise (microphone) signals; the noise input paths (analogue or digital) are selected as described in Table 6. The selected sources are filtered and processed in accordance with the acoustic parameters programmed into the CS47L85. The resulting noise cancellation signals can be mixed with the output signal paths using the register bits described in Table 73.

Noise cancellation is applied selectively to different audio frequency bands; a low frequency limiter ensures that the ANC algorithms deliver noise reduction in the most sensitive frequency bands, without introducing distortion in other frequency bands.

The ANC processor is adaptive to different ambient noise levels in order to provide the most natural sound at the headphone audio output. The stereo ANC signal processing supports a very high level of noise cancellation capability for a wide variety of headset/handset applications. It also incorporates a noise gating function, which ensures that the noise cancellation performance is optimised across a wide range of input signal conditions.

Note that the ANC configuration data is lost whenever the DCVDD power domain is removed; the ANC configuration data must be downloaded to the CS47L85 each time the device is powered up.

The procedure for configuring the CS47L85 ANC functions is tailored to each customer's application; please contact your local Cirrus Logic representative for more details.

DIGITAL AUDIO INTERFACE

The CS47L85 provides four audio interfaces, AIF1, AIF2, AIF3 and AIF4. Each of these is independently configurable on the respective transmit (TX) and receive (RX) paths. AIF1 and AIF2 support up to 8 channels of input and output signal paths; AIF3 and AIF4 support up to 2 channels of input and output signal paths.

The data source(s) for the audio interface transmit (TX) paths can be selected from any of the CS47L85 input signal paths, or from the digital core processing functions. The audio interface receive (RX) paths can be selected as inputs to any of the digital core processing functions or digital core outputs. See “Digital Core” for details of the digital core routing options.

The digital audio interfaces provide flexible connectivity for multiple processors and other audio devices. Typical connections include Applications Processor, Baseband Processor and Wireless Transceiver. Note that the SLIMbus interface also provides digital audio input/output paths, providing options for additional interfaces. A typical configuration is illustrated in Figure 46.

The audio interfaces AIF1 and AIF2 are referenced to DBVDD1 and DBVDD2 respectively; interfaces AIF3 and AIF4 are referenced to DBVDD3. This enables the CS47L85 to connect easily between application sub-systems on different voltage domains.

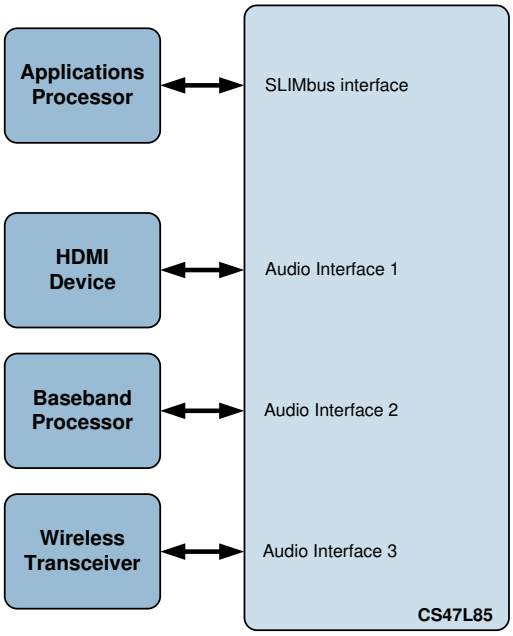


Figure 46 Typical AIF Connections

In the general case, the digital audio interface uses four pins:

- TXDAT: Data output
- RXDAT: Data input
- BCLK: Bit clock, for synchronisation
- LRCLK: Left/Right data alignment clock

In master interface mode, the clock signals BCLK and LRCLK are outputs from the CS47L85. In slave mode, these signals are inputs, as illustrated below.

Four different audio data formats are supported by the digital audio interface:

- DSP mode A
- DSP mode B
- I2S
- Left Justified

The Left Justified and DSP-B modes are valid in Master mode only (i.e., BCLK and LRCLK are outputs from the CS47L85). These modes cannot be supported in Slave mode.

All four of these modes are MSB first. Data words are encoded in 2's complement format. Each of the audio interface modes is described in the following sections. Refer to the "Signal Timing Requirements" section for timing information.

Two variants of DSP mode are supported - 'Mode A' and 'Mode B'. Mono PCM operation can be supported using the DSP modes.

MASTER AND SLAVE MODE OPERATION

The CS47L85 digital audio interfaces can operate as a master or slave as shown in Figure 47 and Figure 48. The associated control bits are described in "Digital Audio Interface Control".

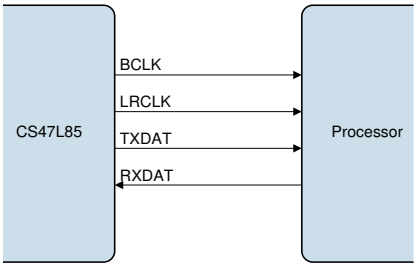


Figure 47 Master Mode

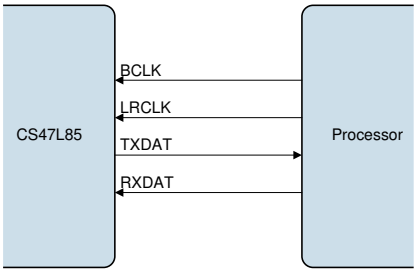


Figure 48 Slave Mode

AUDIO DATA FORMATS

The CS47L85 digital audio interfaces can be configured to operate in I^2S, Left-Justified, DSP-A or DSP-B interface modes. Note that Left-Justified and DSP-B modes are valid in Master mode only (i.e., BCLK and LRCLK are outputs from the CS47L85).

The digital audio interfaces also provide flexibility to support multiple 'slots' of audio data within each LRCLK frame. This flexibility allows multiple audio channels to be supported within a single LRCLK frame.

The data formats described in this section are generic descriptions, assuming only one stereo pair of audio samples per LRCLK frame. In these cases, the AIF is configured to transmit (or receive) in the first available position in each frame (i.e., the Slot 0 position).

The options for multi-channel operation are described in the following section ("AIF Timeslot Configuration").

The audio data modes supported by the CS47L85 are described below. Note that the polarity of the BCLK and LRCLK signals can be inverted if required; the following descriptions all assume the default, non-inverted polarity of these signals.

In DSP mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK following a rising edge of LRCLK. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In master mode, the LRCLK output will resemble the frame pulse shown in Figure 49 and Figure 50. In slave mode, it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs at least one BCLK period before the rising edge of the next frame pulse.

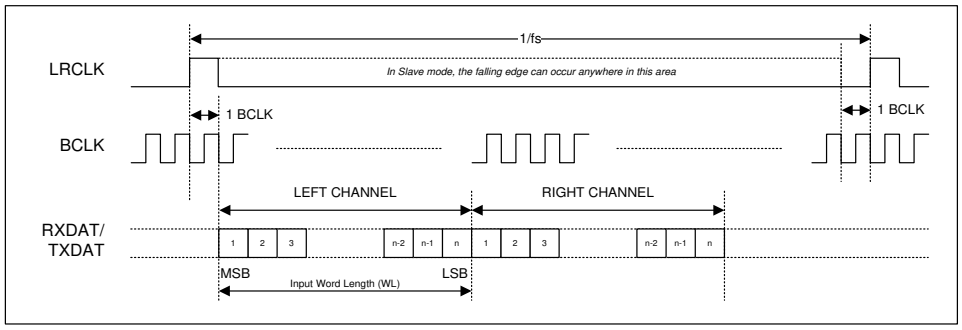


Figure 49 DSP Mode A Data Format

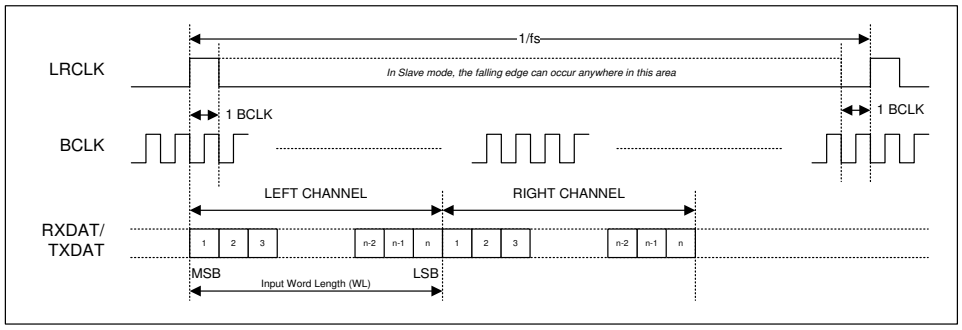


Figure 50 DSP Mode B Data Format

PCM operation is supported in DSP interface mode. CS47L85 data that is output on the Left Channel will be read as mono PCM data by the receiving equipment. Mono PCM data received by the CS47L85 will be treated as Left Channel data. This data may be routed to the Left/Right playback paths using the control fields described in the “Digital Core” section.

In I^2S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

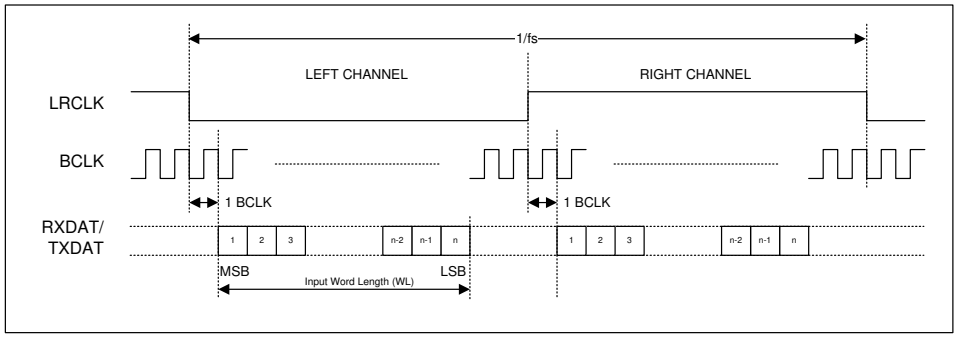


Figure 51 I2S Data Format (assuming n-bit word length)

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.

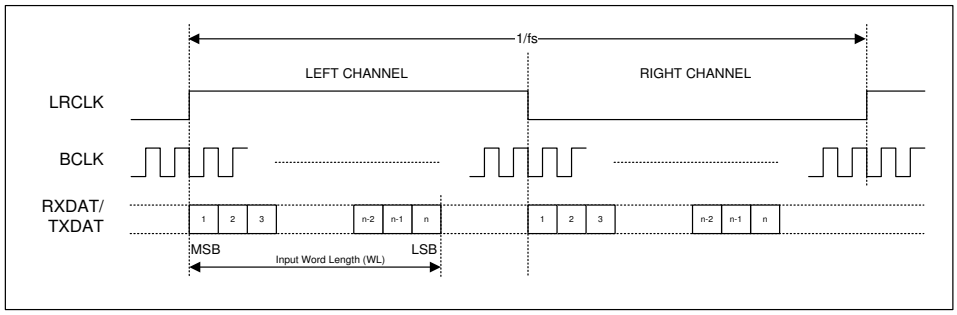


Figure 52 Left Justified Data Format (assuming n-bit word length)

AIF TIMESLOT CONFIGURATION

Digital audio interfaces AIF1 and AIF2 support multi-channel operation, with up to 8 channels of input and output in each case. A high degree of flexibility is provided to define the position of the audio samples within each LRCLK frame; the audio channel samples may be arranged in any order within the frame.

AIF3 and AIF4 also provide flexible configuration options, but these interfaces support only 1 stereo input and 1 stereo output path.

Note that, on each interface, all input and output channels must operate at the same sample rate (fs).

Each of the audio channels can be enabled or disabled independently on the transmit (TX) and receive (RX) signal paths. For each enabled channel, the audio samples are assigned to one timeslot within the LRCLK frame.

In DSP modes, the timeslots are ordered consecutively from the start of the LRCLK frame. In I2S and Left-Justified modes, the even-numbered timeslots are arranged in the first half of the LRCLK frame, and the odd-numbered timeslots are arranged in the second half of the frame.

The timeslots are assigned independently for the transmit (TX) and receive (RX) signal paths. There is no requirement to assign every available timeslot to an audio sample; some slots may be unused, if desired. Care is required, however, to ensure that no timeslot is allocated to more than one audio channel.

The number of BCLK cycles within a slot is configurable; this is the Slot Length. The number of valid data bits within a slot is also configurable; this is the Word Length. The number of BCLK cycles per LRCLK frame must be configured; it must be ensured that there are enough BCLK cycles within each LRCLK frame to transmit or receive all of the enabled audio channels.

Examples of the AIF Timeslot Configurations are illustrated in Figure 53 to Figure 56. One example is shown for each of the four possible data formats.

Figure 53 shows an example of DSP Mode A format. Four enabled audio channels are shown, allocated to timeslots 0 through to 3.

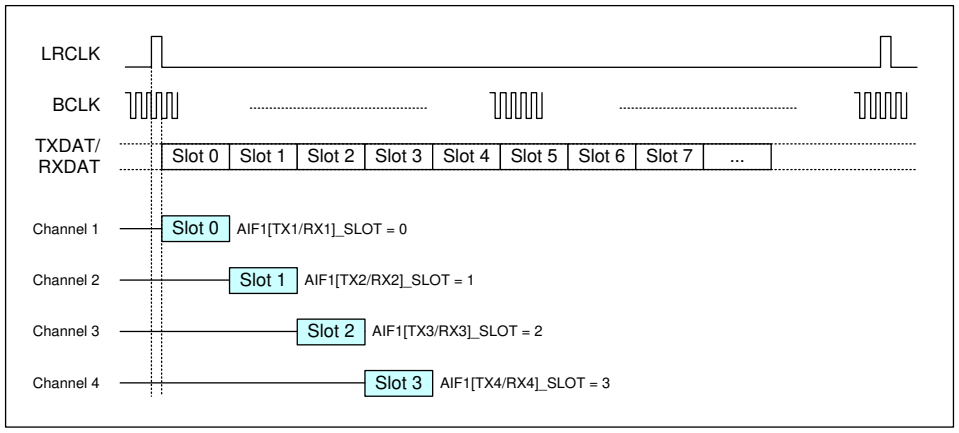


Figure 53 DSP Mode A Example

Figure 54 shows an example of DSP Mode B format. Six enabled audio channels are shown, with timeslots 4 and 5 unused.

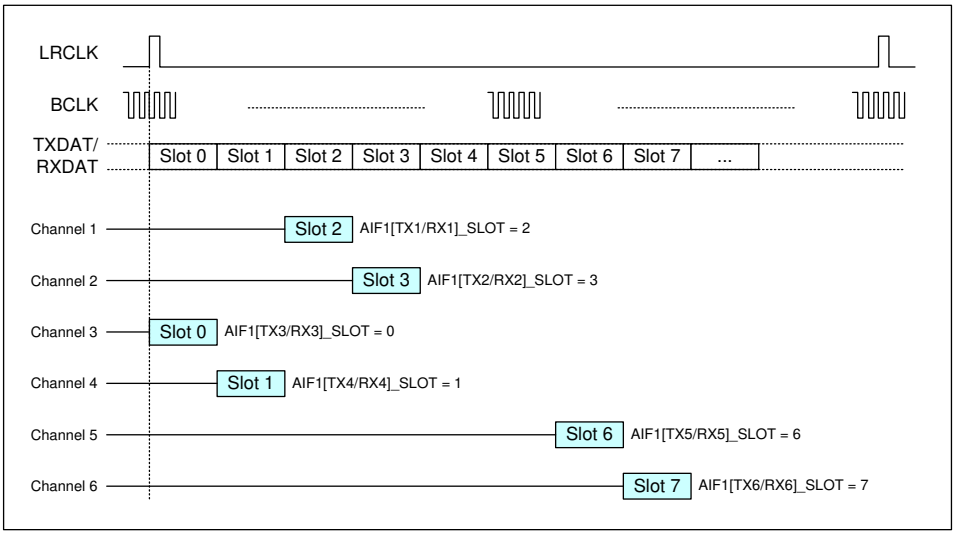


Figure 54 DSP Mode B Example

Figure 55 shows an example of I2S format. Four enabled channels are shown, allocated to timeslots 0 through to 3.

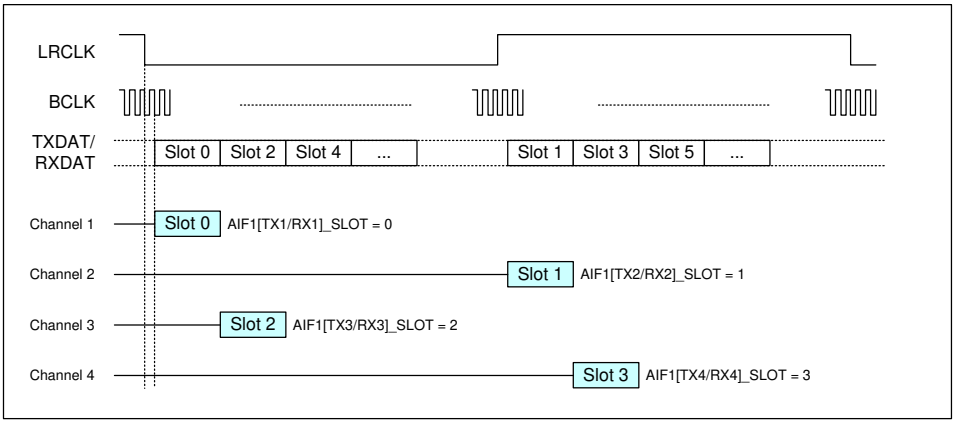


Figure 55 I2S Example

Figure 56 shows an example of Left Justified format. Six enabled channels are shown.

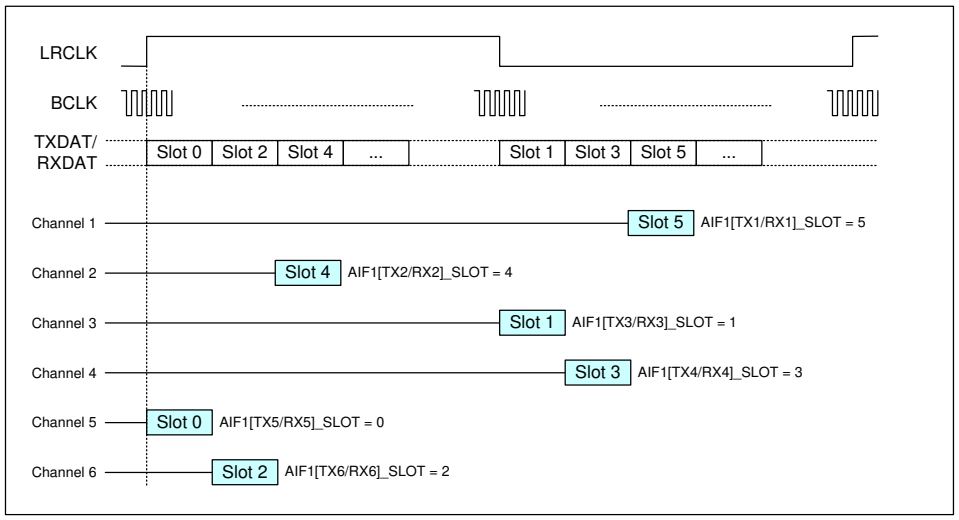


Figure 56 Left Justifed Example

TDM OPERATION BETWEEN THREE OR MORE DEVICES

The AIF operation described above illustrates how multiple audio channels can be interleaved on a single TXDAT or RXDAT pin. The interface uses Time Division Multiplexing (TDM) to allocate time periods to each of the audio channels in turn.

This form of TDM is implemented between two devices, using the electrical connections illustrated in Figure 47 or Figure 48.

It is also possible to implement TDM between three or more devices. This allows one CODEC to receive audio data from two other devices simultaneously on a single audio interface, as illustrated in Figure 57, Figure 58 and Figure 59.

The CS47L85 provides full support for TDM operation. The TXDAT pin can be tri-stated when not transmitting data, in order to allow other devices to transmit on the same wire. The behaviour of the TXDAT pin is configurable, to allow maximum flexibility to interface with other devices in this way.

Typical configurations of TDM operation between three devices are illustrated in Figure 57, Figure 58 and Figure 59.

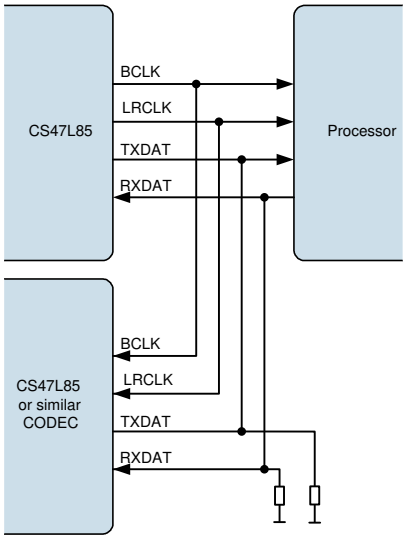


Figure 57 TDM with CS47L85 as Master

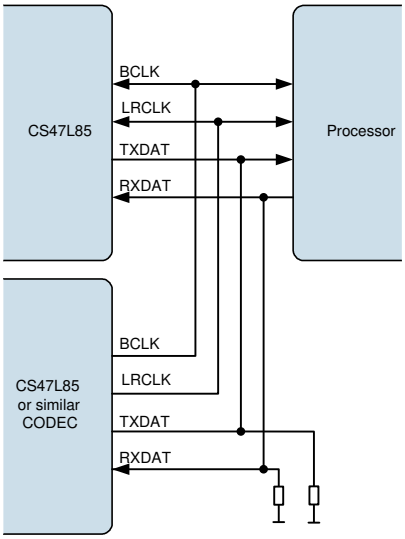


Figure 58 TDM with Other CODEC as Master

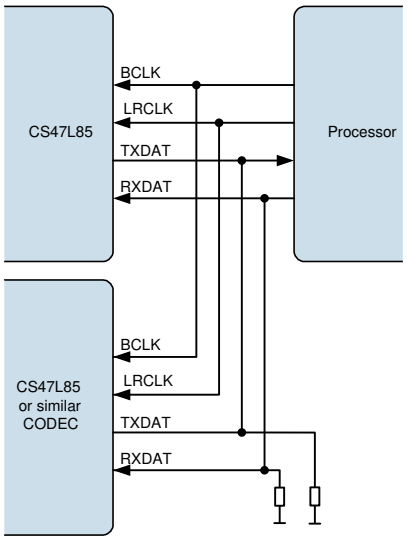


Figure 59 TDM with Processor as Master

Note:

The CS47L85 is a 24-bit device. If the user operates the CS47L85 in 32-bit mode then the 8 LSBs will be ignored on the receiving side and not driven on the transmitting side. It is therefore recommended to add a pull-down resistor if necessary to the RXDAT line and the TXDAT line in TDM mode.

DIGITAL AUDIO INTERFACE CONTROL

This section describes the configuration of the CS47L85 digital audio interface paths.

AIF1 and AIF2 support up to 8 input signal paths and up to 8 output signal paths; AIF3 and AIF4 support up to 2 channels of input and output signal paths. The digital audio interfaces can be configured as Master or Slave interfaces; mixed master/slave configurations are also possible.

Each input and output signal path can be independently enabled or disabled. The AIF output (TX) and AIF input (RX) paths use shared BCLK and LRCLK control signals.

The digital audio interface supports flexible data formats, selectable word-length, configurable timeslot allocations and TDM tri-state control.

The audio interfaces can be re-configured whilst enabled, including changes to the LRCLK frame length and the channel timeslot configurations. Care is required to ensure that any 'on-the-fly' re-configuration does not cause corruption to the active signal paths. Wherever possible, it is recommended to disable all channels before changing the AIF configuration.

As noted in the applicable register descriptions, some of the AIF control fields are locked and cannot be updated whilst AIF channels are enabled; this is to ensure continuity of the respective BCLK and LRCLK signals.

AIF SAMPLE RATE CONTROL

The AIF RX inputs may be selected as input to the digital mixers or signal processing functions within the CS47L85 digital core. The AIF TX outputs are derived from the respective output mixers.

The sample rate for each digital audio interface AIFn is configured using the respective AIFn_RATE register - see Table 22 within the "Digital Core" section.

Note that sample rate conversion is required when routing the AIF paths to any signal chain that is asynchronous and/or configured for a different sample rate.

AIF PIN CONFIGURATION

The external connections associated with each digital audio interface (AIF) are implemented on multi-function GPIO pins, which must be configured for the respective AIF functions when required. The AIF connections are pin-specific alternative functions available on specific GPIO pins. See "General Purpose Input / Output" to configure the GPIO pins for AIF operation.

Integrated pull-up and pull-down resistors can be enabled on the AIFnLRCLK, AIFnBCLK and AIFnRXDAT pins. This is provided as part of the GPIO functionality, and provides a flexible capability for interfacing with other devices.

Each of the pull-up and pull-down resistors can be configured independently using the register bits described in Table 94. When the pull-up and pull-down resistors are both enabled, the CS47L85 provides a 'bus keeper' function on the respective pin. The bus keeper function holds the logic level unchanged whenever the pin is undriven (e.g., if the signal is tri-stated).

AIF MASTER / SLAVE CONTROL

The digital audio interfaces can operate in Master or Slave modes and also in mixed master/slave configurations. In Master mode, the BCLK and LRCLK signals are generated by the CS47L85 when any of the respective digital audio interface channels is enabled. In Slave mode, these outputs are disabled by default to allow another device to drive these pins.

Master mode is selected on the AIFnBCLK pin using the AIFn_BCLK_MSTR register bit. In Master mode, the AIFnBCLK signal is generated by the CS47L85 when one or more AIFn channels is enabled.

When the AIFn_BCLK_FRC bit is set in BCLK master mode, the AIFnBCLK signal is output at all times, including when none of the AIFn channels is enabled. The AIFn_BCLK_FRC bit should be held at 0 if SYSCLK is not enabled. SYSCLK must be present and enabled before setting the AIFn_BCLK_FRC bit. See “Clocking and Sample Rates” for further details (including requirements for reconfiguring SYSCLK while AIF clock signals are enabled).

The AIFnBCLK signal can be inverted in Master or Slave modes using the AIFn_BCLK_INV register.

Master mode is selected on the AIFnLRCLK pin using the AIFn_LRCLK_MSTR register bit. In Master mode, the AIFnLRCLK signal is generated by the CS47L85 when one or more AIFn channels is enabled.

When the AIFn_LRCLK_FRC bit is set in LRCLK master mode, the AIFnLRCLK signal is output at all times, including when none of the AIFn channels is enabled. Note that AIFnLRCLK is derived from AIFnBCLK, and an internal or external AIFnBCLK signal must be present to generate AIFnLRCLK. The AIFn_LRCLK_FRC bit should be held at 0 if SYSCLK is not enabled. SYSCLK must be present and enabled before setting the AIFn_LRCLK_FRC bit. See “Clocking and Sample Rates” for further details (including requirements for reconfiguring SYSCLK while AIF clock signals are enabled).

The AIFnLRCLK signal can be inverted in Master or Slave modes using the AIFn_LRCLK_INV register.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1280 (0500h) AIF1_BCLK_Ctrl	7	AIF1_BCLK_INV	0	AIF1 Audio Interface BCLK Invert 0 = AIF1BCLK not inverted 1 = AIF1BCLK inverted This bit is locked when AIF1 channels are enabled; it can only be changed when all AIF1 channels are disabled.
	6	AIF1_BCLK_FRC	0	AIF1 Audio Interface BCLK Output Control 0 = Normal 1 = AIF1BCLK always enabled in Master mode
	5	AIF1_BCLK_MSTR	0	AIF1 Audio Interface BCLK Master Select 0 = AIF1BCLK Slave mode 1 = AIF1BCLK Master mode This bit is locked when AIF1 channels are enabled; it can only be changed when all AIF1 channels are disabled.
R1282 (0502h) AIF1_Rx_Pin_Ctrl	2	AIF1_LRCLK_INV	0	AIF1 Audio Interface LRCLK Invert 0 = AIF1LRCLK not inverted 1 = AIF1LRCLK inverted This bit is locked when AIF1 channels are enabled; it can only be changed when all AIF1 channels are disabled.
	1	AIF1_LRCLK_FRC	0	AIF1 Audio Interface LRCLK Output Control 0 = Normal 1 = AIF1LRCLK always enabled in Master mode
	0	AIF1_LRCLK_MSTR	0	AIF1 Audio Interface LRCLK Master Select 0 = AIF1LRCLK Slave mode 1 = AIF1LRCLK Master mode This bit is locked when AIF1 channels are enabled; it can only be changed when all AIF1 channels are disabled.

Table 37 AIF1 Master / Slave Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1344 (0540h) AIF2_BCLK_Ctrl	7	AIF2_BCLK_INV	0	AIF2 Audio Interface BCLK Invert 0 = AIF2BCLK not inverted 1 = AIF2BCLK inverted This bit is locked when AIF2 channels are enabled; it can only be changed when all AIF2 channels are disabled.
	6	AIF2_BCLK_FRC	0	AIF2 Audio Interface BCLK Output Control 0 = Normal 1 = AIF2BCLK always enabled in Master mode
	5	AIF2_BCLK_MSTR	0	AIF2 Audio Interface BCLK Master Select 0 = AIF2BCLK Slave mode 1 = AIF2BCLK Master mode This bit is locked when AIF2 channels are enabled; it can only be changed when all AIF2 channels are disabled.
R1346 (0542h) AIF2_Rx_Pin_Ctrl	2	AIF2_LRCLK_INV	0	AIF2 Audio Interface LRCLK Invert 0 = AIF2LRCLK not inverted 1 = AIF2LRCLK inverted This bit is locked when AIF2 channels are enabled; it can only be changed when all AIF2 channels are disabled.
	1	AIF2_LRCLK_FRC	0	AIF2 Audio Interface LRCLK Output Control 0 = Normal 1 = AIF2LRCLK always enabled in Master mode
	0	AIF2_LRCLK_MSTR	0	AIF2 Audio Interface LRCLK Master Select 0 = AIF2LRCLK Slave mode 1 = AIF2LRCLK Master mode This bit is locked when AIF2 channels are enabled; it can only be changed when all AIF2 channels are disabled.

Table 38 AIF2 Master / Slave Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1408 (0580h) AIF3_BCLK_Ctrl	7	AIF3_BCLK_INV	0	AIF3 Audio Interface BCLK Invert 0 = AIF3BCLK not inverted 1 = AIF3BCLK inverted This bit is locked when AIF3 channels are enabled; it can only be changed when all AIF3 channels are disabled.
	6	AIF3_BCLK_FRC	0	AIF3 Audio Interface BCLK Output Control 0 = Normal 1 = AIF3BCLK always enabled in Master mode
	5	AIF3_BCLK_MSTR	0	AIF3 Audio Interface BCLK Master Select 0 = AIF3BCLK Slave mode 1 = AIF3BCLK Master mode This bit is locked when AIF3 channels are enabled; it can only be changed when all AIF3 channels are disabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1410 (0582h) AIF3_Rx_ Pin_Ctrl	2	AIF3_LRCLK_INV	0	AIF3 Audio Interface LRCLK Invert 0 = AIF3LRCLK not inverted 1 = AIF3LRCLK inverted This bit is locked when AIF3 channels are enabled; it can only be changed when all AIF3 channels are disabled.
	1	AIF3_LRCLK_FRC	0	AIF3 Audio Interface LRCLK Output Control 0 = Normal 1 = AIF3LRCLK always enabled in Master mode
	0	AIF3_LRCLK_MSTR	0	AIF3 Audio Interface LRCLK Master Select 0 = AIF3LRCLK Slave mode 1 = AIF3LRCLK Master mode This bit is locked when AIF3 channels are enabled; it can only be changed when all AIF3 channels are disabled.

Table 39 AIF3 Master / Slave Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1440 (05A0h) AIF4_BCLK_Ctrl	7	AIF4_BCLK_INV	0	AIF43 Audio Interface BCLK Invert 0 = AIF4BCLK not inverted 1 = AIF4BCLK inverted This bit is locked when AIF4 channels are enabled; it can only be changed when all AIF4 channels are disabled.
	6	AIF4_BCLK_FRC	0	AIF4 Audio Interface BCLK Output Control 0 = Normal 1 = AIF4BCLK always enabled in Master mode
	5	AIF4_BCLK_MSTR	0	AIF4 Audio Interface BCLK Master Select 0 = AIF4BCLK Slave mode 1 = AIF4BCLK Master mode This bit is locked when AIF4 channels are enabled; it can only be changed when all AIF4 channels are disabled.
R1442 (05A2h) AIF4_Rx_ Pin_Ctrl	2	AIF4_LRCLK_INV	0	AIF4 Audio Interface LRCLK Invert 0 = AIF4LRCLK not inverted 1 = AIF4LRCLK inverted This bit is locked when AIF4 channels are enabled; it can only be changed when all AIF4 channels are disabled.
	1	AIF4_LRCLK_FRC	0	AIF4 Audio Interface LRCLK Output Control 0 = Normal 1 = AIF4LRCLK always enabled in Master mode
	0	AIF4_LRCLK_MSTR	0	AIF4 Audio Interface LRCLK Master Select 0 = AIF4LRCLK Slave mode 1 = AIF4LRCLK Master mode This bit is locked when AIF4 channels are enabled; it can only be changed when all AIF4 channels are disabled.

Table 40 AIF4 Master / Slave Control

AIF SIGNAL PATH ENABLE

The AIF1 and AIF2 interfaces support up to 8 input (RX) channels and up to 8 output (TX) channels. Each of these channels can be enabled or disabled using the register bits defined in Table 41 and Table 42.

The AIF3 and AIF4 interfaces support up to 2 input (RX) channels and up to 2 output (TX) channels. Each of these channels can be enabled or disabled using the register bits defined in Table 43 and Table 44.

The system clock, SYSCLK, must be configured and enabled before any audio path is enabled. The AIF signal paths should be kept disabled (AIF*n*TX*m*_ENA=0, AIF*n*RX*m*_ENA=0) if SYSCLK is not enabled. The ASYNCCLK may also be required, depending on the path configuration. See "Clocking and Sample Rates" for details of the system clocks (including requirements for reconfiguring SYSCLK while audio paths are enabled).

The audio interfaces can be re-configured whilst enabled, including changes to the LRCLK frame length and the channel timeslot configurations. Care is required to ensure that this 'on-the-fly' re-configuration does not cause corruption to the active signal paths. Wherever possible, it is recommended to disable all channels before changing the AIF configuration.

As noted in the applicable register descriptions, some of the AIF control fields are locked and cannot be updated whilst AIF channels are enabled; this is to ensure continuity of the respective BCLK and LRCLK signals.

The CS47L85 performs automatic checks to confirm that the SYSCLK and ASYNCCLK frequencies are high enough to support the commanded signal paths and processing functions. If an attempt is made to enable an AIF signal path, and there are insufficient SYSCLK or ASYNCCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1305 (0519h) AIF1_Tx_ Enables	7	AIF1TX8_ENA	0	AIF1 Audio Interface TX Channel 8 Enable 0 = Disabled 1 = Enabled
	6	AIF1TX7_ENA	0	AIF1 Audio Interface TX Channel 7 Enable 0 = Disabled 1 = Enabled
	5	AIF1TX6_ENA	0	AIF1 Audio Interface TX Channel 6 Enable 0 = Disabled 1 = Enabled
	4	AIF1TX5_ENA	0	AIF1 Audio Interface TX Channel 5 Enable 0 = Disabled 1 = Enabled
	3	AIF1TX4_ENA	0	AIF1 Audio Interface TX Channel 4 Enable 0 = Disabled 1 = Enabled
	2	AIF1TX3_ENA	0	AIF1 Audio Interface TX Channel 3 Enable 0 = Disabled 1 = Enabled
	1	AIF1TX2_ENA	0	AIF1 Audio Interface TX Channel 2 Enable 0 = Disabled 1 = Enabled
	0	AIF1TX1_ENA	0	AIF1 Audio Interface TX Channel 1 Enable 0 = Disabled 1 = Enabled
R1306 (051Ah) AIF1_Rx_ Enables	7	AIF1RX8_ENA	0	AIF1 Audio Interface RX Channel 8 Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6	AIF1RX7_ENA	0	AIF1 Audio Interface RX Channel 7 Enable 0 = Disabled 1 = Enabled
	5	AIF1RX6_ENA	0	AIF1 Audio Interface RX Channel 6 Enable 0 = Disabled 1 = Enabled
	4	AIF1RX5_ENA	0	AIF1 Audio Interface RX Channel 5 Enable 0 = Disabled 1 = Enabled
	3	AIF1RX4_ENA	0	AIF1 Audio Interface RX Channel 4 Enable 0 = Disabled 1 = Enabled
	2	AIF1RX3_ENA	0	AIF1 Audio Interface RX Channel 3 Enable 0 = Disabled 1 = Enabled
	1	AIF1RX2_ENA	0	AIF1 Audio Interface RX Channel 2 Enable 0 = Disabled 1 = Enabled
	0	AIF1RX1_ENA	0	AIF1 Audio Interface RX Channel 1 Enable 0 = Disabled 1 = Enabled

Table 41 AIF1 Signal Path Enable

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1369 (0559h) AIF2_Tx_ Enables	7	AIF2TX8_ENA	0	AIF2 Audio Interface TX Channel 8 Enable 0 = Disabled 1 = Enabled
	6	AIF2TX7_ENA	0	AIF2 Audio Interface TX Channel 7 Enable 0 = Disabled 1 = Enabled
	5	AIF2TX6_ENA	0	AIF2 Audio Interface TX Channel 6 Enable 0 = Disabled 1 = Enabled
	4	AIF2TX5_ENA	0	AIF2 Audio Interface TX Channel 5 Enable 0 = Disabled 1 = Enabled
	3	AIF2TX4_ENA	0	AIF2 Audio Interface TX Channel 4 Enable 0 = Disabled 1 = Enabled
	2	AIF2TX3_ENA	0	AIF2 Audio Interface TX Channel 3 Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1	AIF2TX2_ENA	0	AIF2 Audio Interface TX Channel 2 Enable 0 = Disabled 1 = Enabled
	0	AIF2TX1_ENA	0	AIF2 Audio Interface TX Channel 1 Enable 0 = Disabled 1 = Enabled
R1370 (055Ah) AIF2_Rx_ Enables	7	AIF2RX8_ENA	0	AIF2 Audio Interface RX Channel 8 Enable 0 = Disabled 1 = Enabled
	6	AIF2RX7_ENA	0	AIF2 Audio Interface RX Channel 7 Enable 0 = Disabled 1 = Enabled
	5	AIF2RX6_ENA	0	AIF2 Audio Interface RX Channel 6 Enable 0 = Disabled 1 = Enabled
	4	AIF2RX5_ENA	0	AIF2 Audio Interface RX Channel 5 Enable 0 = Disabled 1 = Enabled
	3	AIF2RX4_ENA	0	AIF2 Audio Interface RX Channel 4 Enable 0 = Disabled 1 = Enabled
	2	AIF2RX3_ENA	0	AIF2 Audio Interface RX Channel 3 Enable 0 = Disabled 1 = Enabled
	1	AIF2RX2_ENA	0	AIF2 Audio Interface RX Channel 2 Enable 0 = Disabled 1 = Enabled
	0	AIF2RX1_ENA	0	AIF2 Audio Interface RX Channel 1 Enable 0 = Disabled 1 = Enabled

Table 42 AIF2 Signal Path Enable

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1433 (0599h) AIF3_Tx_ Enables	1	AIF3TX2_ENA	0	AIF3 Audio Interface TX Channel 2 Enable 0 = Disabled 1 = Enabled
	0	AIF3TX1_ENA	0	AIF3 Audio Interface TX Channel 1 Enable 0 = Disabled 1 = Enabled
R1434 (059Ah) AIF3_Rx_ Enables	1	AIF3RX2_ENA	0	AIF3 Audio Interface RX Channel 2 Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	AIF3RX1_ENA	0	AIF3 Audio Interface RX Channel 1 Enable 0 = Disabled 1 = Enabled

Table 43 AIF3 Signal Path Enable

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1465 (05B9h) AIF4_Tx_ Enables	1	AIF4TX2_ENA	0	AIF4 Audio Interface TX Channel 2 Enable 0 = Disabled 1 = Enabled
	0	AIF4TX1_ENA	0	AIF4 Audio Interface TX Channel 1 Enable 0 = Disabled 1 = Enabled
R1466 (05BAh) AIF4_Rx_ Enables	1	AIF4RX2_ENA	0	AIF4 Audio Interface RX Channel 2 Enable 0 = Disabled 1 = Enabled
	0	AIF4RX1_ENA	0	AIF4 Audio Interface RX Channel 1 Enable 0 = Disabled 1 = Enabled

Table 44 AIF4 Signal Path Enable

AIF BCLK AND LRCLK CONTROL

The AIFnBCLK frequency is selected by the AIFn_BCLK_FREQ register. For each value of this register, the actual frequency depends upon whether AIFn is configured for a 48kHz-related sample rate or a 44.1kHz-related sample rate, as described below.

If AIFn_RATE<1000 (see Table 22), then AIFn is referenced to the SYSCLK clocking domain and the applicable frequency depends upon the SAMPLE_RATE_1, SAMPLE_RATE_2 or SAMPLE_RATE_3 registers.

If AIFn_RATE≥1000, then AIFn is referenced to the ASYNCCLK clocking domain and the applicable frequency depends upon the ASYNC_SAMPLE_RATE_1 or ASYNC_SAMPLE_RATE_2 registers.

The selected AIFnBCLK rate must be less than or equal to SYSCLK/2, or ASYNCCLK/2, as applicable. See “Clocking and Sample Rates” for details of SYSCLK and ASYNCCLK domains, and the associated control registers.

The AIFnLRCLK frequency is controlled relative to AIFnBCLK by the AIFn_BCPF divider.

Note that the BCLK rate must be configured in Master or Slave modes, using the AIFn_BCLK_FREQ registers. The LRCLK rate(s) only require to be configured in Master mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1280 (0500h) AIF1_BCLK_Ctrl	4:0	AIF1_BCLK_FREQ [4:0]	01100	AIF1BCLK Rate 00000 = Reserved 00001 = Reserved 00010 = 64kHz (58.8kHz) 00011 = 96kHz (88.2kHz) 00100 = 128kHz (117.6kHz) 00101 = 192kHz (176.4kHz) 00110 = 256kHz (235.2kHz) 00111 = 384kHz (352.8kHz) 01000 = 512kHz (470.4kHz) 01001 = 768kHz (705.6kHz) 01010 = 1.024MHz (940.8kHz) 01011 = 1.536MHz (1.4112MHz) 01100 = 2.048MHz (1.8816MHz) 01101 = 3.072MHz (2.8824MHz) 01110 = 4.096MHz (3.7632MHz) 01111 = 6.144MHz (5.6448MHz) 10000 = 8.192MHz (7.5264MHz) 10001 = 12.288MHz (11.2896MHz) 10010 = 24.576MHz (22.5792MHz) The frequencies in brackets apply for 44.1kHz-related sample rates only. If AIF1_RATE<1000, then AIF1 is referenced to SYSCLK and the 44.1kHz-related frequencies apply if SAMPLE_RATE_n = 01XXX. If AIF1_RATE>=1000, then AIF1 is referenced to ASYNCCLK and the 44.1kHz-related frequencies apply if ASYNC_SAMPLE_RATE_n = 01XXX. The AIF1BCLK rate must be less than or equal to SYSCLK/2, or ASYNCCLK/2, as applicable. This field is locked when AIF1 channels are enabled; it can only be changed when all AIF1 channels are disabled.
R1286 (0506h) AIF1_Rx_BCLK_Rate	12:0	AIF1_BCPF [12:0]	0040h	AIF1LRCLK Rate This register selects the number of BCLK cycles per AIF1LRCLK frame. AIF1LRCLK clock = AIF1BCLK / AIF1_BCPF Integer (LSB = 1), Valid from 8..8191

Table 45 AIF1 BCLK and LRCLK Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1344 (0540h) AIF2_BCLK_Ctrl	4:0	AIF2_BCLK_FREQ [4:0]	01100	AIF2BCLK Rate 00000 = Reserved 00001 = Reserved 00010 = 64kHz (58.8kHz) 00011 = 96kHz (88.2kHz) 00100 = 128kHz (117.6kHz) 00101 = 192kHz (176.4kHz) 00110 = 256kHz (235.2kHz) 00111 = 384kHz (352.8kHz) 01000 = 512kHz (470.4kHz) 01001 = 768kHz (705.6kHz) 01010 = 1.024MHz (940.8kHz) 01011 = 1.536MHz (1.4112MHz) 01100 = 2.048MHz (1.8816MHz) 01101 = 3.072MHz (2.8824MHz) 01110 = 4.096MHz (3.7632MHz) 01111 = 6.144MHz (5.6448MHz) 10000 = 8.192MHz (7.5264MHz) 10001 = 12.288MHz (11.2896MHz) 10010 = 24.576MHz (22.5792MHz) The frequencies in brackets apply for 44.1kHz-related sample rates only. If AIF2_RATE<1000, then AIF2 is referenced to SYSCLK and the 44.1kHz-related frequencies apply if SAMPLE_RATE_n = 01XXX. If AIF2_RATE>=1000, then AIF2 is referenced to ASYNCCLK and the 44.1kHz-related frequencies apply if ASYNC_SAMPLE_RATE_n = 01XXX. The AIF2BCLK rate must be less than or equal to SYSCLK/2, or ASYNCCLK/2, as applicable. This field is locked when AIF2 channels are enabled; it can only be changed when all AIF2 channels are disabled.
R1350 (0546h) AIF2_Rx_BCLK_Rate	12:0	AIF2_BCPF [12:0]	0040h	AIF2LRCLK Rate This register selects the number of BCLK cycles per AIF2LRCLK frame. AIF2LRCLK clock = AIF2BCLK / AIF2_BCPF Integer (LSB = 1), Valid from 8..8191

Table 46 AIF2 BCLK and LRCLK Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1408 (0580h) AIF3_BCLK_Ctrl	4:0	AIF3_BCLK_FREQ [4:0]	01100	AIF3BCLK Rate 00000 = Reserved 00001 = Reserved 00010 = 64kHz (58.8kHz) 00011 = 96kHz (88.2kHz) 00100 = 128kHz (117.6kHz) 00101 = 192kHz (176.4kHz) 00110 = 256kHz (235.2kHz) 00111 = 384kHz (352.8kHz) 01000 = 512kHz (470.4kHz) 01001 = 768kHz (705.6kHz) 01010 = 1.024MHz (940.8kHz) 01011 = 1.536MHz (1.4112MHz) 01100 = 2.048MHz (1.8816MHz) 01101 = 3.072MHz (2.8824MHz) 01110 = 4.096MHz (3.7632MHz) 01111 = 6.144MHz (5.6448MHz) 10000 = 8.192MHz (7.5264MHz) 10001 = 12.288MHz (11.2896MHz) 10010 = 24.576MHz (22.5792MHz) The frequencies in brackets apply for 44.1kHz-related sample rates only. If AIF3_RATE<1000, then AIF3 is referenced to SYSCLK and the 44.1kHz-related frequencies apply if SAMPLE_RATE_n = 01XXX. If AIF3_RATE>=1000, then AIF3 is referenced to ASYNCCLK and the 44.1kHz-related frequencies apply if ASYNC_SAMPLE_RATE_n = 01XXX. The AIF3BCLK rate must be less than or equal to SYSCLK/2, or ASYNCCLK/2, as applicable. This field is locked when AIF3 channels are enabled; it can only be changed when all AIF3 channels are disabled.
R1414 (0586h) AIF3_Rx_BCLK_Rate	12:0	AIF3_BCPF [12:0]	0040h	AIF3LRCLK Rate This register selects the number of BCLK cycles per AIF3LRCLK frame. AIF3LRCLK clock = AIF3BCLK / AIF3_BCPF Integer (LSB = 1), Valid from 8..8191

Table 47 AIF3 BCLK and LRCLK Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1440 (05A0h) AIF4_BCLK_Ctrl	4:0	AIF4_BCLK_FREQ [4:0]	01100	AIF4BCLK Rate 00000 = Reserved 00001 = Reserved 00010 = 64kHz (58.8kHz) 00011 = 96kHz (88.2kHz) 00100 = 128kHz (117.6kHz) 00101 = 192kHz (176.4kHz) 00110 = 256kHz (235.2kHz) 00111 = 384kHz (352.8kHz) 01000 = 512kHz (470.4kHz) 01001 = 768kHz (705.6kHz) 01010 = 1.024MHz (940.8kHz) 01011 = 1.536MHz (1.4112MHz) 01100 = 2.048MHz (1.8816MHz) 01101 = 3.072MHz (2.8824MHz) 01110 = 4.096MHz (3.7632MHz) 01111 = 6.144MHz (5.6448MHz) 10000 = 8.192MHz (7.5264MHz) 10001 = 12.288MHz (11.2896MHz) 10010 = 24.576MHz (22.5792MHz) The frequencies in brackets apply for 44.1kHz-related sample rates only. If AIF4_RATE<1000, then AIF3 is referenced to SYSCLK and the 44.1kHz-related frequencies apply if SAMPLE_RATE_n = 01XXX. If AIF4_RATE>=1000, then AIF3 is referenced to ASYNCCLK and the 44.1kHz-related frequencies apply if ASYNC_SAMPLE_RATE_n = 01XXX. The AIF4BCLK rate must be less than or equal to SYSCLK/2, or ASYNCCLK/2, as applicable. This field is locked when AIF4 channels are enabled; it can only be changed when all AIF4 channels are disabled.
R1446 (05A6h) AIF4_Rx_BCLK_Rate	12:0	AIF4_BCPF [12:0]	0040h	AIF4LRCLK Rate This register selects the number of BCLK cycles per AIF4LRCLK frame. AIF4LRCLK clock = AIF4BCLK / AIF4_BCPF Integer (LSB = 1), Valid from 8..8191

Table 48 AIF4 BCLK and LRCLK Control

AIF DIGITAL AUDIO DATA CONTROL

The register bits controlling the audio data format, word lengths and slot configurations for AIF1, AIF2, AIF3 and AIF4 are described in Table 49, Table 50, Table 51 and Table 52 respectively.

Note that Left-Justified and DSP-B modes are valid in Master mode only (i.e., BCLK and LRCLK are outputs from the CS47L85).

The AIFn Slot Length is the number of BCLK cycles in one timeslot within the overall LRCLK frame. The Word Length is the number of valid data bits within each timeslot. (If the word length is less than the slot length, then there will be unused BCLK cycles at the end of each timeslot.) The AIFn word length and slot length is independently selectable for the input (RX) and output (TX) paths.

For each AIF input (RX) and AIF output (TX) channel, the position of the audio data sample within the LRCLK frame is configurable. The _SLOT registers define the timeslot position of the audio sample for the associated audio channel. Valid selections are Slot 0 upwards. The timeslots are numbered as illustrated in Figure 53 through to Figure 56.

Note that, in DSP modes, the timeslots are ordered consecutively from the start of the LRCLK frame. In I2S and Left-Justified modes, the even-numbered timeslots are arranged in the first half of the LRCLK frame, and the odd-numbered timeslots are arranged in the second half of the frame.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1284 (0504h) AIF1_Format	2:0	AIF1_FMT [2:0]	000	AIF1 Audio Interface Format 000 = DSP Mode A 001 = DSP Mode B 010 = I²S mode 011 = Left Justified mode Other codes are Reserved This field is locked when AIF1 channels are enabled; it can only be changed when all AIF1 channels are disabled.
R1287 (0507h) AIF1_Frame_Ctrl_1	13:8	AIF1TX_WL [5:0]	18h	AIF1 TX Word Length (Number of valid data bits per slot) Integer (LSB = 1); Valid from 16 to 32
	7:0	AIF1TX_SLOT_LEN [7:0]	18h	AIF1 TX Slot Length (Number of BCLK cycles per slot) Integer (LSB = 1); Valid from 16 to 128
R1288 (0508h) AIF1_Frame_Ctrl_2	13:8	AIF1RX_WL [5:0]	18h	AIF1 RX Word Length (Number of valid data bits per slot) Integer (LSB = 1); Valid from 16 to 32
	7:0	AIF1RX_SLOT_LEN [7:0]	18h	AIF1 RX Slot Length (Number of BCLK cycles per slot) Integer (LSB = 1); Valid from 16 to 128
R1289 (0509h) to R1296 (0510h)	5:0	AIF1TX1_SLOT [5:0]	0h	AIF1 TX Channel n Slot position Defines the TX timeslot position of the Channel n audio sample Integer (LSB=1); Valid from 0 to 63
	5:0	AIF1TX2_SLOT [5:0]	1h	
	5:0	AIF1TX3_SLOT [5:0]	2h	
	5:0	AIF1TX4_SLOT [5:0]	3h	
	5:0	AIF1TX5_SLOT [5:0]	4h	
	5:0	AIF1TX6_SLOT [5:0]	5h	
	5:0	AIF1TX7_SLOT [5:0]	6h	
	5:0	AIF1TX8_SLOT [5:0]	7h	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1297 (0511h) to R1304 (0518h)	5:0	AIF1RX1_SLOT [5:0]	0h	AIF1 RX Channel n Slot position Defines the RX timeslot position of the Channel n audio sample Integer (LSB=1); Valid from 0 to 63
	5:0	AIF1RX2_SLOT [5:0]	1h	
	5:0	AIF1RX3_SLOT [5:0]	2h	
	5:0	AIF1RX4_SLOT [5:0]	3h	
	5:0	AIF1RX5_SLOT [5:0]	4h	
	5:0	AIF1RX6_SLOT [5:0]	5h	
	5:0	AIF1RX7_SLOT [5:0]	6h	
	5:0	AIF1RX8_SLOT [5:0]	7h	

Table 49 AIF1 Digital Audio Data Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1348 (0544h) AIF2_Format	2:0	AIF2_FMT [2:0]	000	AIF2 Audio Interface Format 000 = DSP Mode A 001 = DSP Mode B 010 = I^2S mode 011 = Left Justified mode Other codes are Reserved This field is locked when AIF2 channels are enabled; it can only be changed when all AIF2 channels are disabled.
R1351 (0547h) AIF2_Frame_Ctrl_1	13:8	AIF2TX_WL [5:0]	18h	AIF2 TX Word Length (Number of valid data bits per slot) Integer (LSB = 1); Valid from 16 to 32
	7:0	AIF2TX_SLOT_LEN [7:0]	18h	AIF2 TX Slot Length (Number of BCLK cycles per slot) Integer (LSB = 1); Valid from 16 to 128
R1352 (0548h) AIF2_Frame_Ctrl_2	13:8	AIF2RX_WL [5:0]	18h	AIF2 RX Word Length (Number of valid data bits per slot) Integer (LSB = 1); Valid from 16 to 32
	7:0	AIF2RX_SLOT_LEN [7:0]	18h	AIF2 RX Slot Length (Number of BCLK cycles per slot) Integer (LSB = 1); Valid from 16 to 128

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1353 (0549h) to R1360 (0550h)	5:0	AIF2TX1_SLOT [5:0]	0h	AIF2 TX Channel n Slot position Defines the TX timeslot position of the Channel n audio sample Integer (LSB=1); Valid from 0 to 63
	5:0	AIF2TX2_SLOT [5:0]	1h	
	5:0	AIF2TX3_SLOT [5:0]	2h	
	5:0	AIF2TX4_SLOT [5:0]	3h	
	5:0	AIF2TX5_SLOT [5:0]	4h	
	5:0	AIF2TX6_SLOT [5:0]	5h	
	5:0	AIF2TX7_SLOT [5:0]	6h	
	5:0	AIF2TX8_SLOT [5:0]	7h	
R1361 (0551h) to R1368 (0558h)	5:0	AIF2RX1_SLOT [5:0]	0h	AIF2 RX Channel n Slot position Defines the RX timeslot position of the Channel n audio sample Integer (LSB=1); Valid from 0 to 63
	5:0	AIF2RX2_SLOT [5:0]	1h	
	5:0	AIF2RX3_SLOT [5:0]	2h	
	5:0	AIF2RX4_SLOT [5:0]	3h	
	5:0	AIF2RX5_SLOT [5:0]	4h	
	5:0	AIF2RX6_SLOT [5:0]	5h	
	5:0	AIF2RX7_SLOT [5:0]	6h	
	5:0	AIF2RX8_SLOT [5:0]	7h	

Table 50 AIF2 Digital Audio Data Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1412 (0584h) AIF3_Format	2:0	AIF3_FMT [2:0]	000	AIF3 Audio Interface Format 000 = DSP Mode A 001 = DSP Mode B 010 = I^2S mode 011 = Left Justified mode Other codes are Reserved This field is locked when AIF3 channels are enabled; it can only be changed when all AIF3 channels are disabled.
R1415 (0587h) AIF3_Frame_Ctrl_1	13:8	AIF3TX_WL [5:0]	18h	AIF3 TX Word Length (Number of valid data bits per slot) Integer (LSB = 1); Valid from 16 to 32
	7:0	AIF3TX_SLOT_LEN [7:0]	18h	AIF3 TX Slot Length (Number of BCLK cycles per slot) Integer (LSB = 1); Valid from 16 to 128
R1416 (0588h) AIF3_Fra	13:8	AIF3RX_WL [5:0]	18h	AIF3 RX Word Length (Number of valid data bits per slot) Integer (LSB = 1); Valid from 16 to 32

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
me_Ctrl_2	7:0	AIF3RX_SLOT_LEN [7:0]	18h	AIF3 RX Slot Length (Number of BCLK cycles per slot) Integer (LSB = 1); Valid from 16 to 128
R1417 (0589h) AIF3_Frame_Ctrl_3	5:0	AIF3TX1_SLOT [5:0]	0h	AIF3 TX Channel 1 Slot position Defines the TX timeslot position of the Channel 1 audio sample Integer (LSB=1); Valid from 0 to 63
R1418 (058Ah) AIF3_Frame_Ctrl_4	5:0	AIF3TX2_SLOT [5:0]	1h	AIF3 TX Channel 2 Slot position Defines the TX timeslot position of the Channel 2 audio sample Integer (LSB=1); Valid from 0 to 63
R1425 (0591h) AIF3_Frame_Ctrl_11	5:0	AIF3RX1_SLOT [5:0]	0h	AIF3 RX Channel 1 Slot position Defines the RX timeslot position of the Channel 1 audio sample Integer (LSB=1); Valid from 0 to 63
R1426 (0592h) AIF3_Frame_Ctrl_12	5:0	AIF3RX2_SLOT [5:0]	1h	AIF3 RX Channel 2 Slot position Defines the RX timeslot position of the Channel 2 audio sample Integer (LSB=1); Valid from 0 to 63

Table 51 AIF3 Digital Audio Data Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1444 (05A4h) AIF4_Format	2:0	AIF4_FMT [2:0]	000	AIF4 Audio Interface Format 000 = DSP Mode A 001 = DSP Mode B 010 = I^2S mode 011 = Left Justified mode Other codes are Reserved This field is locked when AIF4 channels are enabled; it can only be changed when all AIF4 channels are disabled.
R1447 (05A7h) AIF4_Frame_Ctrl_1	13:8	AIF4TX_WL [5:0]	18h	AIF4 TX Word Length (Number of valid data bits per slot) Integer (LSB = 1); Valid from 16 to 32
	7:0	AIF4TX_SLOT_LEN [7:0]	18h	AIF4 TX Slot Length (Number of BCLK cycles per slot) Integer (LSB = 1); Valid from 16 to 128
R1448 (05A8h) AIF4_Frame_Ctrl_2	13:8	AIF4RX_WL [5:0]	18h	AIF4 RX Word Length (Number of valid data bits per slot) Integer (LSB = 1); Valid from 16 to 32
	7:0	AIF4RX_SLOT_LEN [7:0]	18h	AIF4 RX Slot Length (Number of BCLK cycles per slot) Integer (LSB = 1); Valid from 16 to 128
R1449 (05A9h) AIF4_Frame_Ctrl_3	5:0	AIF4TX1_SLOT [5:0]	0h	AIF4 TX Channel 1 Slot position Defines the TX timeslot position of the Channel 1 audio sample Integer (LSB=1); Valid from 0 to 63
R1450 (05AAh) AIF4_Frame_Ctrl_4	5:0	AIF4TX2_SLOT [5:0]	1h	AIF4 TX Channel 2 Slot position Defines the TX timeslot position of the Channel 2 audio sample Integer (LSB=1); Valid from 0 to 63

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1457 (05B1h) AIF4_Frame_Ctrl_11	5:0	AIF4RX1_SLOT [5:0]	0h	AIF4 RX Channel 1 Slot position Defines the RX timeslot position of the Channel 1 audio sample Integer (LSB=1); Valid from 0 to 63
R1458 (05B2h) AIF4_Frame_Ctrl_12	5:0	AIF4RX2_SLOT [5:0]	1h	AIF4 RX Channel 2 Slot position Defines the RX timeslot position of the Channel 2 audio sample Integer (LSB=1); Valid from 0 to 63

Table 52 AIF4 Digital Audio Data Control

AIF TDM AND TRI-STATE CONTROL

The AIFn output pins are tri-stated when the AIFn_TRI register is set. Note that this function only affects output pins that have been configured for the respective AIFn function. Any GPIO pin that is configured for a different function will not be affected by the AIFn_TRI register. See “General Purpose Input / Output” to configure the GPIO pins.

Under default conditions, the AIFnTXDAT output is held at logic 0 when the CS47L85 is not transmitting data (i.e., during timeslots that are not enabled for output by the CS47L85). When the AIFnTX_DAT_TRI register is set, the CS47L85 tri-states the respective AIFnTXDAT pin when not transmitting data, allowing other devices to drive the AIFnTXDAT connection.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1281 (0501h) AIF1_Tx_Pin_Ctrl	5	AIF1TX_DAT_TRI	0	AIF1TXDAT Tri-State Control 0 = Logic 0 during unused timeslots 1 = Tri-stated during unused timeslots
R1283 (0503h) AIF1_Rate_Ctrl	6	AIF1_TRI	0	AIF1 Audio Interface Tri-State Control 0 = Normal 1 = AIF1 Outputs are tri-stated Note that this bit only affects output pins that have been configured for the respective AIF1 function.

Table 53 AIF1 TDM and Tri-State Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1345 (0541h) AIF2_Tx_Pin_Ctrl	5	AIF2TX_DAT_TRI	0	AIF2TXDAT Tri-State Control 0 = Logic 0 during unused timeslots 1 = Tri-stated during unused timeslots
R1347 (0543h) AIF2_Rate_Ctrl	6	AIF2_TRI	0	AIF2 Audio Interface Tri-State Control 0 = Normal 1 = AIF2 Outputs are tri-stated Note that this bit only affects output pins that have been configured for the respective AIF2 function.

Table 54 AIF2 TDM and Tri-State Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1409 (0581h) AIF3_Tx_ Pin_Ctrl	5	AIF3TX_DAT_TRI	0	AIF3TXDAT Tri-State Control 0 = Logic 0 during unused timeslots 1 = Tri-stated during unused timeslots
R1411 (0583h) AIF3_Rate _Ctrl	6	AIF3_TRI	0	AIF3 Audio Interface Tri-State Control 0 = Normal 1 = AIF3 Outputs are tri-stated Note that this bit only affects output pins that have been configured for the respective AIF3 function.

Table 55 AIF3 TDM and Tri-State Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1441 (05A1h) AIF4_Tx_ Pin_Ctrl	5	AIF4TX_DAT_TRI	0	AIF4TXDAT Tri-State Control 0 = Logic 0 during unused timeslots 1 = Tri-stated during unused timeslots
R1443 (05A3h) AIF4_Rate _Ctrl	6	AIF4_TRI	0	AIF4 Audio Interface Tri-State Control 0 = Normal 1 = AIF4 Outputs are tri-stated Note that this bit only affects output pins that have been configured for the respective AIF4 function.

Table 56 AIF4 TDM and Tri-State Control

SLIMBUS INTERFACE

The SLIMbus protocol is highly configurable and adaptable, supporting multiple audio signal paths, and mixed sample rates simultaneously. It also supports control messaging and associated communications between devices.

SLIMBUS DEVICES

The SLIMbus components comprise different device classes (Manager, Framer, Interface, Generic). Each component on the bus has an Interface Device, which provides bus management services for the respective component. One or more components on the bus will provide Manager and Framer Device functions; the Manager has the capabilities to administer the bus, whilst the Framer is responsible for driving the CLK line and for driving the DATA required to establish the Frame Structure on the bus. Note that only one Manager and one Framer Device will be active at any time. The Framer function can be transferred between Devices when required. Generic Devices provide the basic SLIMbus functionality for the associated Port(s), and for the Transport Protocol by which audio signal paths are established on the bus.

SLIMBUS FRAME STRUCTURE

The SLIMbus bit stream is formatted within a defined structure of Cells, Slots, Subframes, Frames, and Superframes:

- A single data bit is known as a Cell
- 4 Cells make a Slot
- 192 Slots make a Frame
- 8 Frames make a Superframe

The bit stream structure is configurable to some extent, but the Superframe definition always comprises 1536 slots. The transmitted/received bit rate is not fixed; it can be configured according to system requirements, and can be changed dynamically without interruption to active audio paths.

The SLIMbus CLK frequency (also the bus bit rate) is defined by a *Root Frequency (RF)* and a *Clock Gear (CG)*. In the top Clock Gear (Gear 10), the CLK frequency is equal to the Root Frequency. Each reduction in the Clock Gear halves the CLK frequency, and doubles the duration of the Superframe.

The SLIMbus bandwidth will typically comprise Control space (for bus messages, synchronisation etc.) and Data space (for audio paths). The precise allocation is configurable, and can be entirely Control space, if required.

The Subframe definition comprises the number of Slots per Subframe (6, 8, 24 or 32 Slots), and the number of these Slots (per Subframe) allocated as Control space. The applicable combination of Subframe length and Control space width are defined by the *Subframe Mode (SM)* parameter.

The SLIMbus Frame always comprises 192 Slots, regardless of the Subframe definition. A number of Slots are allocated to Control space, as noted above; the remaining Slots are allocated to Data space. Some of the Control space is required for Framing Information and for the Guide Channel (described below); the remainder of the Control space are allocated to the Message Channel.

CONTROL SPACE

Framing Information is provided in Slots 0 and 96 of every Frame. Slot 0 contains a 4-bit synchronisation code; Slot 96 contains the 32-bit Framing Information, transmitted 4 bits at a time over the 8 Frames that make up the SLIMbus Superframe. The Clock Gear, Root Frequency, Subframe configuration, along with some other parameters, are encoded within the Framing Information.

The Guide Channel occupies two Slots within Frame 0. This provides the necessary information for a SLIMbus component to acquire and verify the frame synchronisation. The Guide Channel occupies the first two Control space Slots within the first Frame of the bit stream, excluding the Framing Information Slots. Note that the exact Slot allocation will depend upon the applicable Subframe mode.

The Message Channel is allocated all of the Control space not used by the Framing Information or the Guide Channel. The Message Channel enables SLIMbus devices to communicate with each other, using a priority-based mechanism defined in the MIPI specification.

Messages may be broadcast to all devices on the bus, or can be addressed to specific devices using their allocated *Logical Address (LA)* or *Enumeration Address (EA)*. Note that, device-specific messages are directed to a particular device (i.e., Manager, Framer, Interface or Generic) within a component on the bus.

DATA SPACE

The Data space can be organised into a maximum of 256 Data Channels. Each Channel, identified by a unique *Channel Number (CN)*, is a stream of one or more contiguous Slots, organised in a consistent data structure that repeats at a fixed interval.

A Data Channel is defined by its *Segment Length (SL)* (number of contiguous Slots allocated), Segment Interval (spacing between the first Slots of successive Segments), and Segment Offset (the Slot Number of the first allocated Slot within the Superframe). The Segment Interval and Segment Offset are collectively defined by a *Segment Distribution (SD)*, by which the SLIMbus Manager may configure (or re-configure) any Data Channel.

Each Segment may comprise TAG, AUX and DATA portions. Any of these portions may be 0-length; the exact composition depends on the *Transport Protocol (TP)* for the associated Channel (see below). The DATA portion must be wide enough to accommodate one full word of the Data Channel contents (data words cannot be spread across multiple segments).

The Segment Interval for each Data Channel represents the minimum spacing between consecutive data samples for that Channel. (Note - the minimum spacing applies if every allocated segment is populated with new data; in many cases, additional bandwidth is allocated, as described below, and not every allocated segment is used.)

The Segment Interval gives rise to Segment Windows for each Data Channel, aligned to the start of every Superframe. The Segment Window boundaries define the times within which each new data sample must be buffered, ready for transmission - adherence to these fixed boundaries allows Slot allocations to be moved within a Segment Window, without altering the signal latency. The Segment Interval may be either shorter or longer than the Frame length, but there is always an integer number of Segment Windows per Superframe.

The *Transport Protocol (TP)* defines the flow control or handshaking method used by the Ports associated with a Data Channel. The applicable flow control mode(s) depend on the relationship between the audio sample rate (flow rate) and the SLIMbus CLK frequency. If the two rates are synchronised and integer-related, then no flow control is needed; in other cases, the flow may be regulated by the use of a 'Presence' bit. The Presence bit can either be set by the source Device ('pushed' protocol), or by the sink Device ('pulled' protocol).

The Data Channel structure is defined in terms of the *Transport Protocol (TP)*, *Segment Distribution (SD)*, and the *Segment Length (SL)* parameters. Each of these is described above.

The Data Channel content definition includes a *Presence Rate (PR)* parameter (describing the nominal sample rate for the audio channel) and a *Frequency Locked (FL)* bit (identifying whether the data source is synchronised to the SLIMbus CLK). The *Data Length (DL)* parameter defines the size of each data sample (number of Slots). The *Auxiliary Bits Format (AF)* and *Data Type (DT)* parameters provide support for non-PCM encoded data channels; the *Channel Link (CL)* parameter is an indicator that channel CN is related to the previous channel, CN-1.

For a given Root Frequency and Clock Gear, the *Segment Length (SL)* and *Segment Distribution (SD)* parameters define the amount of SLIMbus bandwidth that is allocated to a given Data Channel. The minimum bandwidth requirements of a Data Channel are represented by the *Presence Rate (PR)* and *Data Length (DL)* parameters. The allocated SLIMbus bandwidth must be equal to or greater than the bandwidth of the data to be transferred.

The Segment Interval defines the repetition rate of the SLIMbus Slots allocated to consecutive data samples for a given Data Channel. The *Presence Rate (PR)* is the nominal sample rate of the audio path. The Segment Rate (determined by the Segment Interval) must be equal to or greater than the Presence Rate for a given data channel. The following constraints must be observed, when configuring a SLIMbus channel:

- If Pushed or Pulled Transport Protocol is selected, then Segment Rate must be greater than the Presence Rate, to ensure samples are not dropped as a result of clock drift.
- If Isochronous Transport Protocol is selected, the Segment Rate must be equal to the Presence Rate. Isochronous Transport Protocol should only be selected if the data source is frequency-locked to the SLIMbus CLK (ie. the data source is synchronised to the SLIMbus Framer device).

SLIMBUS CONTROL SEQUENCES

This section describes the messages and general protocol associated with most aspects of the SLIMbus system.

Note that the SLIMbus specification permits some flexibility in Core Message support for different components. See "SLIMbus Interface Control" for details of which message(s) are supported on each of the SLIMbus devices that are present on the CS47L85.

DEVICE MANAGEMENT & CONFIGURATION

This section describes the SLIMbus messages associated with configuring all devices on the SLIMbus interface.

When the SLIMbus interface starts up, it is required that one (and only one) of the components provides the Manager and Framer Device functions. Other devices can request connection to the bus after they have gained synchronisation.

The **REPORT_PRESENT (DC, DCV)** message may be issued by devices attempting to connect to the bus. The payload of this message contains the *Device Class (DC)* and *Device Class Version (DCV)* parameters, describing the type of device that is attempting to connect. This message may be issued autonomously by the connecting device, or else in response to a **REQUEST_SELF_ANNOUNCEMENT** message from the Manager Device.

After positively acknowledging the REPORT_PRESENT message, the Manager Device will then issue the **ASSIGN_LOGICAL_ADDRESS (LA)** message to allow the other device to connect to the bus. The payload of this message contains the *Logical Address (LA)* parameter only; this is the unique address by which the connected device will send and receive SLIMbus messages. The device is then said to be 'enumerated'.

Once a device has been successfully connected to the bus, the Logical Address (LA) parameter can be changed at any time using the **CHANGE_LOGICAL_ADDRESS (LA)** message.

The **RESET_DEVICE** message commands an individual SLIMbus device to perform its reset procedure. As part of the reset, all associated ports will be reset, and any associated Data Channels will be cancelled. Note that, if the RESET_DEVICE command is issued to an Interface Device, it will cause a Component Reset (i.e., all Devices within the associated component are reset). Under a Component Reset, every associated Device will release its Logical Address, and the Component will become disconnected from the bus.

INFORMATION MANAGEMENT

A memory map of Information Elements is defined for each Device. This is arranged in 3 x 1kByte blocks, comprising Core Value elements, Device Class-specific Value elements, and User Value elements respectively, as described in the MIPI specification. Note that the contents of the User Information portion for each CS47L85 SLIMbus Device are reserved.

Read/Write access is implemented using the messages described below. Specific elements within the Information Map are identified using the *Element Code (EC)* parameter. In the case of Read access, a unique *Transaction ID (TID)* is assigned to each message relating to a particular read/write request.

The **REQUEST_INFORMATION (TID, EC)** message is used to instruct a device to respond with the indicated information. The payload of this message contains the *Transaction ID (TID)* and the *Element Code (EC)*.

The **REQUEST_CLEAR_INFORMATION (TID, EC, CM)** message is used to instruct a device to respond with the indicated information, and also to clear all, or parts, of the same information slice. The payload of this message contains the *Transaction ID (TID), Element Code (EC)*, and *Clear Mask (CM)*. The Clear Mask field is used to select which element(s) are to be cleared as part of the instruction.

The **REPLY_INFORMATION (TID, IS)** message is used to provide readback of a requested parameter. The payload of this message contains the *Transaction ID (TID)* and the *Information Slice (IS)*. The Information Slice byte(s) contain the value of the requested parameter.

The **CLEAR_INFORMATION (EC, CM)** message is used to clear all, or parts, of the indicated information slice. The payload of this message contains the *Element Code (EC)* and *Clear Mask (CM)*. The Clear Mask field is used to select which element(s) are to be cleared as part of the instruction.

The **REPORT_INFORMATION (EC, IS)** message is used to inform other devices about a change in a specified element in the Information Map. The payload of this message contains the *Element Code (EC)* and the *Information Slice (IS)*. The Information Slice byte(s) contain the new value of the applicable parameter.

VALUE MANAGEMENT (INCLUDING REGISTER ACCESS)

A memory map of Value Elements is defined for each Device. This is arranged in 3 x 1kByte blocks, comprising Core Value elements, Device Class-specific Value elements, and User Value elements respectively, as described in the MIPI specification. These elements are typically parameters used to configure Device behaviour.

The User Value elements of the Interface Device are used on CS47L85 to support Read/Write access to the Register Map. Details of how to access specific registers are described in the “SLIMbus Interface Control” section.

Note that, with the exception of the User Value elements of the Interface Device, the contents of the User Value portion for each CS47L85 SLIMbus Device are reserved.

Read/Write access is implemented using the messages described below. Specific elements within the Value Map are identified using the *Element Code (EC)* parameter. In the case of Read access, a unique *Transaction ID (TID)* is assigned to each message relating to a particular read/write request.

The **REQUEST_VALUE (TID, EC)** message is used to instruct a device to respond with the indicated information. The payload of this message contains the *Transaction ID (TID)* and the *Element Code (EC)*.

The **REPLY_VALUE (TID, VS)** message is used to provide readback of a requested parameter. The payload of this message contains the *Transaction ID (TID)* and the *Value Slice (VS)*. The Value Slice byte(s) contain the value of the requested parameter.

The **CHANGE_VALUE (EC, VU)** message is used to write data to a specified element in the Value Map. The payload of this message contains the *Element Code (EC)* and the *Value Update (VU)*. The Value Update byte(s) contain the new value of the applicable parameter.

FRAME & CLOCKING MANAGEMENT

This section describes the SLIMbus messages associated with changing the Frame or Clocking configuration. One or more configuration messages may be issued as part of a Reconfiguration Sequence; all of the updated parameters become active at once, when the Reconfiguration boundary is reached.

The **BEGIN_RECONFIGURATION** message is issued to define a Reconfiguration Boundary point: subsequent NEXT_* messages will become active at the first valid Superframe boundary following receipt of the **RECONFIGURE_NOW** message. (A valid boundary must be at least two Slots after the end of the RECONFIGURE_NOW message.) Both of these messages have no payload content.

The **NEXT_ACTIVE_FRAMER (LAIF, NCo, NCi)** message is used to select a new device as the active Framer. The payload of this message includes the *Logical Address, Incoming Framer (LAIF)*. Two other fields (NCo, NCi) define the number of clock cycles for which the CLK line shall be inactive during the handover.

The **NEXT_SUBFRAME_MODE (SM)** and **NEXT_CLOCK_GEAR (CG)** messages are used to re-configure the SLIMbus clocking or framing definition. The payload of each is the respective *Subframe Mode (SM) or Clock Gear (CG)* respectively.

The **NEXT_PAUSE_CLOCK (RT)** message instructs the active Framer to pause the bus. The payload of the message contains the Restart Time (RT), which indicates whether the interruption is to be of a specified time and/or phase duration.

The **NEXT_RESET_BUS** message instructs all components on the bus to be reset. In this case, all Devices on the bus are reset and are disconnected from the bus. Subsequent re-connection to the bus follows the same process as when the bus is first initialised.

The **NEXT_SHUTDOWN_BUS** message instructs all devices that the bus is to be shut down.

DATA CHANNEL CONFIGURATION

This section describes the procedure for configuring a SLIMbus Data Channel. Note that the Manager Device is responsible for allocating the available bandwidth as required for each Data Channel.

The **CONNECT_SOURCE (PN, CN)** and **CONNECT_SINK (PN, CN)** messages are issued to the respective devices, defining the Port(s) between which a Data Channel is to be established. Note that multiple destinations (sinks) can be configured for a channel, if required. The payload of each message contains the *Port Number (PN)* and the *Channel Number (CN)* parameters.

The **BEGIN_RECONFIGURATION** message is issued to define a Reconfiguration Boundary point: subsequent NEXT_* messages will become active at the first valid Superframe boundary following receipt of the **RECONFIGURE_NOW** message. (A valid boundary must be at least two Slots after the end of the RECONFIGURE_NOW message.)

The **NEXT_DEFINE_CHANNEL (CN, TP, SD, SL)** message informs the associated devices of the structure of the Data Channel. The payload of this message contains the *Channel Number (CN)*, *Transport Protocol (TP)*, *Segment Distribution (SD)*, and the *Segment Length (SL)* parameters for the Data Channel.

The **NEXT_DEFINE_CONTENT (CN, FL, PR, AF, DT, CL, DL)**, or **CHANGE_CONTENT (CN, FL, PR, AF, DT, CL, DL)**

message provides more detailed information about the Data Channel contents. The payload of this message contains the *Channel Number (CN)*, *Frequency Locked (FL)*, *Presence Rate (PR)*, *Auxiliary Bits Format (AF)*, *Data Type (DT)*, *Channel Link (CL)*, and *Data Length (DL)* parameters.

The **NEXT_ACTIVATE_CHANNEL (CN)** message instructs the channel to be activated at the next Reconfiguration boundary. The payload of this message contains the *Channel Number (CN)* only.

The **RECONFIGURE_NOW** message completes the Reconfiguration sequence, causing all of the 'NEXT_' messages since the BEGIN_RECONFIGURATION to become active at the next valid Superframe boundary. (A valid boundary must be at least two Slots after the end of the RECONFIGURE_NOW message.)

Active channels can be reconfigured using the **CHANGE_CONTENT**, **NEXT_DEFINE_CONTENT**, or **NEXT_DEFINE_CHANNEL** messages. Note that these changes can be effected without interrupting the data channel; the **NEXT_DEFINE_CHANNEL**, for example, may be used to change a Segment Distribution, in order to reallocate the SLIMbus bandwidth.

An active channel can be paused using the **NEXT_DEACTIVATE_CHANNEL** message, and re-instated using the **NEXT_ACTIVATE_CHANNEL** message.

Data channels can be disconnected using the **DISCONNECT_PORT** or **NEXT_REMOVE_CHANNEL** messages. These messages provide equivalent functionality, but use different parameters (PN or CN respectively) to identify the affected signal path.

SLIMBUS INTERFACE CONTROL

The CS47L85 features a MIPI-compliant SLIMbus interface, providing 8 channels of audio input and 8 channels of audio output. Mixed audio sample rates are supported on the SLIMbus interface. The SLIMbus interface also supports read/write access to the CS47L85 control registers.

The SLIMbus interface on CS47L85 comprises a Generic Device, Framer Device, and Interface Device. A maximum of 16 Ports can be configured, providing up to 8 input (RX) channels and up to 8 output (TX) channels.

The audio paths associated with the SLIMbus interface are described in the "Digital Core" section.

The SLIMbus interface supports read/write access to the CS47L85 control registers, as described later in this section.

The SLIMbus clocking rate and channel allocations are controlled by the Manager Device. The Message Channel and Data Channel bandwidth may be dynamically adjusted according to the application requirements. Note that the Manager Device functions are not implemented on the CS47L85, and these bandwidth allocation requirements are outside the scope of this datasheet.

SLIMBUS DEVICE PARAMETERS

The SLIMbus interface on the CS47L85 comprises three Devices. The Enumeration Address of each Device within the SLIMbus interface is derived from the parameters noted in Table 57.

DESCRIPTION	MANUFACTURER ID	PRODUCT CODE	DEVICE ID	INSTANCE VALUE	ENUMERATION ADDRESS
Generic	0x012F	0x6338	0x00	0x00	012F_6338_0000
Framer	0x012F	0x6338	0x55	0x00	012F_6338_5500
Interface	0x012F	0x6338	0x7F	0x00	012F_6338_7F00

Table 57 SLIMbus Device Parameters

SLIMBUS MESSAGE SUPPORT

The SLIMbus interface on the CS47L85 supports bus messages as noted in Table 58.

Additional notes regarding SLIMbus message support are noted below, and also in Table 59.

MESSAGE CODE MC[6:0]	DESCRIPTION	GENERIC	FRAMER	INTERFACE
Device Management Messages				
0x01	REPORT_PRESENT (DC, DCV)	S	S	S
0x02	ASSIGN_LOGICAL_ADDRESS (LA)	D	D	D
0x04	RESET_DEVICE ()	D	D	D
0x08	CHANGE_LOGICAL_ADDRESS (LA)	D	D	D
0x09	CHANGE_ARBITRATION_PRIORITY (AP)			
0x0C	REQUEST_SELF_ANNOUNCEMENT ()	D	D	D
0x0F	REPORT_ABSENT ()			
Data Channel Management Messages				
0x10	CONNECT_SOURCE (PN, CN)	D		
0x11	CONNECT_SINK (PN, CN)	D		
0x14	DISCONNECT_PORT (PN)	D		
0x18	CHANGE_CONTENT (CN, FL, PR, AF, DT, CL, DL)	D		
Information Management Messages				
0x20	REQUEST_INFORMATION (TID, EC)	D	D	D
0x21	REQUEST_CLEAR_INFORMATION (TID, EC, CM)	D	D	D
0x24	REPLY_INFORMATION (TID, IS)	S	S	S
0x28	CLEAR_INFORMATION (EC, CM)	D	D	D
0x29	REPORT_INFORMATION (EC, IS)			S
Reconfiguration Messages				
0x40	BEGIN_RECONFIGURATION ()	D	D	D
0x44	NEXT_ACTIVE_FRAMER (LAIF, NCo, NCi)		D	
0x45	NEXT_SUBFRAME_MODE (SM)		D	D
0x46	NEXT_CLOCK_GEAR (CG)		D	
0x47	NEXT_ROOT_FREQUENCY (RF)		D	
0x4A	NEXT_PAUSE_CLOCK (RT)		D	
0x4B	NEXT_RESET_BUS ()		D	
0x4C	NEXT_SHUTDOWN_BUS ()		D	
0x50	NEXT_DEFINE_CHANNEL (CN, TP, SD, SL)	D		
0x51	NEXT_DEFINE_CONTENT (CN, FL, PR, AF, DT, CL, DL)	D		
0x54	NEXT_ACTIVATE_CHANNEL (CN)	D		
0x55	NEXT_DEACTIVATE_CHANNEL (CN)	D		
0x58	NEXT_REMOVE_CHANNEL (CN)	D		
0x5F	RECONFIGURE_NOW ()	D	D	D
Value Management Messages				
0x60	REQUEST_VALUE (TID, EC)			D
0x61	REQUEST_CHANGE_VALUE (TID, EC, VU)			
0x64	REPLY_VALUE (TID, VS)			S
0x68	CHANGE_VALUE (EC, VU)			D

Table 58 SLIMbus Message Support

S = supported as a Source Device only. D = supported as a Destination Device only.

The CS47L85 SLIMbus component must be reset prior to scheduling a Hardware Reset or Power-On Reset. This can be achieved using the RESET_DEVICE message (issued to the CS47L85 Interface Device), or else using the NEXT_RESET_BUS message.

PARAMETER CODE	DESCRIPTION	COMMENTS
AF	Auxiliary Bits Format	
CG	Clock Gear	
CL	Channel Link	
CM	Clear Mask	CS47L85 does not fully support this function. The CM bytes of the REQUEST_CLEAR_INFORMATION or CLEAR_INFORMATION messages must not be sent to CS47L85 Devices. When either of these messages is received, all bits within the specified Information Slice will be cleared.
CN	Channel Number	
DC	Device Class	
DCV	Device Class Variation	
DL	Data Length	
DT	Data Type	CS47L85 supports the following DT codes: 0h - Not indicated 1h - LPCM audio Note that 2's complement PCM can be supported with DT=0h.
EC	Element Code	
FL	Frequency Locked	
IS	Information Slice	
LA	Logical Address	
LAIF	Logical Address, Incoming Framer	
NCi	Number of Incoming Framer Clock Cycles	
NCo	Number of Outgoing Framer Clock Cycles	
PN	Port Number	Note that the Port Numbers of the CS47L85 SLIMbus paths are register-configurable, as described in Table 60.
PR	Presence Rate	Note that the Presence Rate must be the same as the Sample Rate selected for the associated CS47L85 SLIMbus path.
RF	Root Frequency	CS47L85 supports the following RF codes as Active Framer: 1h - 24.576MHz 2h - 22.5792MHz All codes are supported when CS47L85 is not the Active Framer.
RT	Restart Time	CS47L85 supports the following RT codes: 0h -Fast Recovery 2h - Unspecified Delay When either of these values is specified, the CS47L85 will resume toggling the CLK line within four cycles of the CLK line frequency.
SD	Segment Distribution	Note that any data channels that are assigned the same SAMPLE_RATE_n or ASYNC_SAMPLE_RATE_n value must also be assigned the same Segment Interval.
SL	Segment Length	
SM	Subframe Mode	
TID	Transaction ID	
TP	Transport Protocol	CS47L85 supports the following TP codes for TX channels: 0h - Isochronous Protocol 1h - Pushed Protocol CS47L85 supports the following TP codes for RX channels: 0h - Isochronous Protocol 2h - Pulled Protocol
VS	Value Slice	
VU	Value Update	

Table 59 SLIMbus Parameter Support

SLIMBUS PORT NUMBER CONTROL

The CS47L85 SLIMbus interface supports up to 8 input (RX) channels and up to 8 output (TX) channels. The SLIMbus port numbers for these audio channels are configurable using the registers described in Table 60.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1490 (05D2h) SLIMbus_ RX_Ports0	13:8	SLIMRX2_PORT _ADDR [5:0]	1	SLIMbus RX Channel n Port number Valid from 0..31
	5:0	SLIMRX1_PORT _ADDR [5:0]	0	
R1491 (05D3h) SLIMbus_ RX_Ports1	13:8	SLIMRX4_PORT _ADDR [5:0]	3	
	5:0	SLIMRX3_PORT _ADDR [5:0]	2	
R1492 (05D4h) SLIMbus_ RX_Ports2	13:8	SLIMRX6_PORT _ADDR [5:0]	5	
	5:0	SLIMRX5_PORT _ADDR [5:0]	4	
R1493 (05D5h) SLIMbus_ RX_Ports3	13:8	SLIMRX8_PORT _ADDR [5:0]	7	
	5:0	SLIMRX7_PORT _ADDR [5:0]	6	
R1494 (05D6h) SLIMbus_ TX_Ports0	13:8	SLIMTX2_PORT _ADDR [5:0]	9	SLIMbus TX Channel n Port number Valid from 0..31
	5:0	SLIMTX1_PORT _ADDR [5:0]	8	
R1495 (05D7h) SLIMbus_ TX_Ports1	13:8	SLIMTX4_PORT _ADDR [5:0]	11	
	5:0	SLIMTX3_PORT _ADDR [5:0]	10	
R1496 (05D8h) SLIMbus_ TX_Ports2	13:8	SLIMTX6_PORT _ADDR [5:0]	13	
	5:0	SLIMTX5_PORT _ADDR [5:0]	12	
R1497 (05D9h) SLIMbus_ TX_Ports3	13:8	SLIMTX8_PORT _ADDR [5:0]	15	
	5:0	SLIMTX7_PORT _ADDR [5:0]	14	

Table 60 SLIMbus Port Number Control

SLIMBUS SAMPLE RATE CONTROL

The SLIMbus RX inputs may be selected as input to the digital mixers or signal processing functions within the CS47L85 digital core. The SLIMbus TX outputs are derived from the respective output mixers.

The sample rate for each SLIMbus channel is configured using the SLIMRXn_RATE and SLIMTXn_RATE registers - see Table 22 within the “Digital Core” section.

Note that the SLIMbus interface provides simultaneous support for SYSCLK-referenced and ASYNCCLK-referenced sample rates on different channels. For example, 48kHz and 44.1kHz SLIMbus audio paths can be simultaneously supported.

Sample rate conversion is required when routing the SLIMbus paths to any signal chain that is asynchronous and/or configured for a different sample rate.

SLIMBUS SIGNAL PATH ENABLE

The SLIMbus interface supports up to 8 input (RX) channels and up to 8 output (TX) channels. Each of these channels can be enabled or disabled using the register bits defined in Table 61.

Note that the SLIMbus audio channels can only be supported when the corresponding ports have been enabled by the Manager Device (i.e., in addition to setting the respective enable bits). The status bits in Registers R1527 and R1528 indicate the status of each of the SLIMbus ports.

The system clock, SYSCLK, must be configured and enabled before any audio path is enabled. The SLIMbus audio paths should be kept disabled (SLIMRX*n*_ENA=0, SLIMTX*n*_ENA=0) if SYSCLK is not enabled. The ASYNCCLK may also be required, depending on the path configuration. See "Clocking and Sample Rates" for details of the system clocks (including requirements for reconfiguring SYSCLK while audio paths are enabled).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1525 (05F5h) SLIMbus_RX_Channel_Enable	7	SLIMRX8_ENA	0	SLIMbus RX Channel n Enable 0 = Disabled 1 = Enabled
	6	SLIMRX7_ENA	0	
	5	SLIMRX6_ENA	0	
	4	SLIMRX5_ENA	0	
	3	SLIMRX4_ENA	0	
	2	SLIMRX3_ENA	0	
	1	SLIMRX2_ENA	0	
	0	SLIMRX1_ENA	0	
R1526 (05F6h) SLIMbus_TX_Channel_Enable	7	SLIMTX8_ENA	0	SLIMbus TX Channel n Enable 0 = Disabled 1 = Enabled
	6	SLIMTX7_ENA	0	
	5	SLIMTX6_ENA	0	
	4	SLIMTX5_ENA	0	
	3	SLIMTX4_ENA	0	
	2	SLIMTX3_ENA	0	
	1	SLIMTX2_ENA	0	
	0	SLIMTX1_ENA	0	
R1527 (05F7h) SLIMbus_RX_Port_Status	7	SLIMRX8_PORT_STS	0	SLIMbus RX Channel n Port Status (Read only) 0 = Disabled 1 = Configured and active
	6	SLIMRX7_PORT_STS	0	
	5	SLIMRX6_PORT_STS	0	
	4	SLIMRX5_PORT_STS	0	
	3	SLIMRX4_PORT_STS	0	
	2	SLIMRX3_PORT_STS	0	
	1	SLIMRX2_PORT_STS	0	
	0	SLIMRX1_PORT_STS	0	
R1528 (05F8h) SLIMbus_TX_Port_Status	7	SLIMTX8_PORT_STS	0	SLIMbus TX Channel n Port Status (Read only) 0 = Disabled 1 = Configured and active
	6	SLIMTX7_PORT_STS	0	
	5	SLIMTX6_PORT_STS	0	
	4	SLIMTX5_PORT_STS	0	
	3	SLIMTX4_PORT_STS	0	
	2	SLIMTX3_PORT_STS	0	
	1	SLIMTX2_PORT_STS	0	
	0	SLIMTX1_PORT_STS	0	

Table 61 SLIMbus Signal Path Enable

SLIMBUS CONTROL REGISTER ACCESS

Control register access is supported via the SLIMbus interface. Full read/write access to all registers is possible, via the "User Value Elements" portion of the Value Map.

If the SLIMbus interface is used to access the DSP firmware memory registers, then a system clocking constraint must be observed: the DSPCLK frequency, if enabled, must be greater than 1.3 x RF, where RF is the SLIMbus Root Frequency. Note that, if DSPCLK is disabled (DSP_CLK_ENA=0), or if accessing other areas of the Register Map, the timing constraint is not applicable. See "DSP Firmware Control" for details of the DSP Firmware memory. See "Clocking and Sample Rates" for details of the DSPCLK signal.

Register Write operations are implemented using the "CHANGE_VALUE" message. A maximum of two messages may be required, depending on circumstances: the first "CHANGE_VALUE" message selects the register page (bits [23:8] of the Control Register address); the second message contains the data and bits [7:0] of the register address. The first message may be omitted if the register page is unchanged from the previous Read or Write operation.

The required SLIMbus parameters are described in Table 62 and Table 63, for the generic case of writing the value 0xVVVV to control register address 0xYYYYZZ. Note that it is also possible to write blocks of up to 16 bytes (to consecutive register addresses), as described below.

Write Message 1 – CHANGE_VALUE		
PARAMETER	**VALUE**	**DESCRIPTION**
Source Address	0xSS	'SS' is the 8-bit Logical Address of the message source. This could be any active device on the bus, but is typically the Manager Device (0xFF).
Destination Address	0xLL	'LL' is the 8-bit Logical Address of the message destination (i.e., the CS47L85 SLIMbus Interface Device). The value is assigned by the SLIMbus Manager Device.
Access Mode	0b1	Selects Byte-based access mode.
Byte Address	0x800	Identifies the User Value element for selecting the Control Register page address.
Slice Size	0b001	Selects 2-byte slice size
Value Update	0xYYYY	'YYYY' is bits [23:8] of the applicable Control Register address.

Table 62 Register Write Message (1)

Write Message 2 – CHANGE_VALUE		
PARAMETER	**VALUE**	**DESCRIPTION**
Source Address	0xSS	'SS' is the 8-bit Logical Address of the message source. This could be any active device on the bus, but is typically the Manager Device (0xFF).
Destination Address	0xLL	'LL' is the 8-bit Logical Address of the message destination (i.e., the CS47L85 SLIMbus Interface Device). The value is assigned by the SLIMbus Manager Device.
Access Mode	0b1	Selects Byte-based access mode.
Byte Address	0xUUU	Specifies the Value Map address, calculated as 0xA00 + (2 x 0xZZ), where 'ZZ' is bits [7:0] of the applicable Control Register address.
Slice Size	0b001	Selects 2-byte slice size
Value Update	0xVVVV	'VVVV' is the 16-bit data to be written.

Table 63 Register Write Message (2)

Note that the first message may be omitted if its contents are unchanged from the previous CHANGE_VALUE message sent to the CS47L85.

Write transfers of up to 16 bytes can be configured using the 'Slice Size' parameter in the second message (see Table 63). Additional 'Value Update' words can be appended to the message in this case, with the applicable data contents. For compatibility with the CS47L85 register map, the selected number of bytes must always be an even number.

When a 2-byte transfer is selected, these bytes are written to the register address 0xYYYYZZ (using the same naming conventions as above). When more than 2 bytes are written in a single transfer, the destination register address is auto-incremented as described in Table 64.

Note that, register addresses from R12288 (0x3000) upwards are formatted as 32-bit words. When writing to these addresses, the Slice Size should be a multiple of 4 bytes, and the Byte Address should be aligned with the 32-bit data word boundaries (i.e., an even number). The byte ordering for these register addresses is described in Table 65.

REGISTER ADDRESS (< 0x3000)	BYTE SEQUENCE
Base Address (0xYYYYZZ)	Bytes 2 and 1 (0xVVVV)
Base Address + 1	Bytes 4 and 3
Base Address + 2	Bytes 6 and 5
Base Address + 3	Bytes 8 and 7
Base Address + 4	Bytes 10 and 9
Base Address + 5	Bytes 12 and 11
Base Address + 6	Bytes 14 and 13
Base Address + 7	Bytes 16 and 15

Table 64 SLIMbus Register Write Sequence - 16-bit Register Space (< 0x3000)

REGISTER ADDRESS (≥ 0x3000)	BYTE SEQUENCE
Base Address (0xYYYYZZ)	Bytes 4, 3, 2, 1
Base Address + 2	Bytes 8, 7, 6, 5
Base Address + 4	Bytes 12, 11, 10, 9
Base Address + 6	Bytes 16, 15, 14, 13

Table 65 SLIMbus Register Write Sequence - 32-bit Register Space (≥ 0x3000)

Register Read operations are implemented using the “CHANGE_VALUE” and “REQUEST_VALUE” messages. A maximum of two messages may be required, depending on circumstances: the “CHANGE_VALUE” message selects the register page (bits [23:8] of the Control Register address); the “REQUEST_VALUE” message contains bits [7:0] of the register address. The first message may be omitted if the register page is unchanged from the previous Read or Write operation.

The required SLIMbus parameters are described in Table 66 and Table 67, for the generic case of reading the contents of control register address 0xYYYYZZ.

The CS47L85 SLIMbus interface supports Register Read operations of 2-bytes (i.e., one 16-bit data word) only. Register addresses from R12288 (0x3000) upwards are formatted as 32-bit words; when reading from these addresses, the 2-byte data slice will represent the 2 lower bytes of the selected 32-bit word. The 2 upper bytes of the respective register can be accessed by adding ‘2’ to the Byte Address value described in Table 67.

Read Message 1 – CHANGE_VALUE		
PARAMETER	**VALUE**	**DESCRIPTION**
Source Address	0xSS	‘SS’ is the 8-bit Logical Address of the message source. This could be any active device on the bus, but is typically the Manager Device (0xFF).
Destination Address	0xLL	‘LL’ is the 8-bit Logical Address of the message destination (i.e., the CS47L85 SLIMbus Interface Device). The value is assigned by the SLIMbus Manager Device.
Access Mode	0b1	Selects Byte-based access mode.
Byte Address	0x800	Identifies the User Value element for selecting the Control Register page address.
Slice Size	0b001	Selects 2-byte slice size
Value Update	0xYYYY	‘YYYY’ is bits [23:8] of the applicable Control Register address.

Table 66 Register Read Message (1)

Read Message 2 – REQUEST_VALUE		
PARAMETER	**VALUE**	**DESCRIPTION**
Source Address	0xSS	'SS' is the 8-bit Logical Address of the message source. This could be any active device on the bus, but is typically the Manager Device (0xFF).
Destination Address	0xLL	'LL' is the 8-bit Logical Address of the message destination (i.e., the CS47L85 SLIMbus Interface Device). The value is assigned by the SLIMbus Manager Device.
Access Mode	0b1	Selects Byte-based access mode.
Byte Address	0xUUU	Specifies the Value Map address, calculated as 0xA00 + (2 x 0xZZ), where 'ZZ' is bits [7:0] of the applicable Control Register address.
Slice Size	0b001	Selects 2-byte slice size
Transaction ID	0xTTTT	'TTTT' is the 16-bit Transaction ID for the message. The value is assigned by the SLIMbus Manager Device.

Table 67 Register Read Message (2)

Note that the first message may be omitted if its contents are unchanged from the previous CHANGE_VALUE message sent to the CS47L85.

The CS47L85 will respond to the Register Read commands in accordance with the normal SLIMbus protocols.

Note that the CS47L85 assumes that sufficient Control Space Slots are available in which to provide its response before the next REQUEST_VALUE message is received. The CS47L85 response is made using a REPLY_VALUE message; the SLIMbus Manager should wait until the REPLY_VALUE message has been received before sending the next REQUEST_VALUE message. If additional REQUEST_VALUE message(s) are received before the CS47L85 response has been made, then the earlier REQUEST_VALUE message(s) will be ignored (i.e., only the last REQUEST_VALUE message will be serviced).

SLIMBUS CLOCKING CONTROL

The clock frequency of the SLIMbus interface is not fixed, and may be set according to the application requirements. The clock frequency can be reconfigured dynamically as required.

The CS47L85 SLIMbus interface includes a Framer Device. When configured as the active Framer, the SLIMbus clock (SLIMCLK) is an output from the CS47L85. At other times, SLIMCLK is an input. The Framer function can be transferred from one device to another; this is known as Framer Handover, and is controlled by the Manager Device.

The supported Root Frequencies in Active Framer mode are 24.576MHz or 22.5792MHz only. At other times, the supported Root Frequencies are as defined in the MIPI Alliance specification for SLIMbus.

Under normal operating conditions, the SLIMbus interface operates with a fixed Root Frequency (RF); dynamic updates to the bus rate are applied using a selectable Clock Gear (CG) function. The Root Frequency and the Clock Gear setting are controlled by the Manager Device; these parameters are transmitted in every SLIMbus superframe to all devices on the bus.

In Gear 10 (the highest Clock Gear setting), the SLIMCLK input (or output) frequency is equal to the Root Frequency. In lower gears, the SLIMCLK frequency is reduced by increasing powers of 2.

The Clock Gear definition is shown in Table 68. Note that 24.576MHz Root Frequency is an example only; other frequencies are also supported.

CLOCK GEAR	DESCRIPTION	SLIMCLK FREQUENCY (assuming 24.576MHz Root Frequency)
10	Divide by 1	24.576MHz
9	Divide by 2	12.288MHz
8	Divide by 4	6.144MHz
7	Divide by 8	3.072MHz
6	Divide by 16	1.536MHz
5	Divide by 32	768kHz
4	Divide by 64	384kHz
3	Divide by 128	192kHz
2	Divide by 256	96kHz
1	Divide by 512	48kHz

Table 68 SLIMbus Clock Gear Selection

When the CS47L85 is the active Framer, the SLIMCLK output is synchronised to the SYSCLK or ASYNCCLK system clock, as selected by the SLIMCLK_SRC register bit.

The applicable system clock must be enabled, and configured at the SLIMbus Root Frequency, whenever the CS47L85 is the active Framer. The system clock must not be interrupted or reconfigured if the CS47L85 is the active Framer. See "Clocking and Sample Rates" for details of the SYSCLK and ASYNCCLK system clocks.

When the CS47L85 is not configured as the active Framer device, then the SLIMCLK input can be used to provide a reference source for the Frequency Locked Loops (FLLs). The frequency of this reference is controlled using the SLIMCLK_REF_GEAR register, as described in Table 69.

The SLIMbus clock reference is generated using an adaptive divider on the SLIMCLK input. The divider automatically adapts to the SLIMbus Clock Gear (CG).

Note that, if the Clock Gear (CG) on the bus is lower than the SLIMCLK_REF_GEAR, then the selected reference frequency cannot be supported, and the SLIMbus clock reference is disabled.

The SLIMbus clock reference is selected as input to the FLLs using the FLLn_REFCLK_SRC registers. See "Clocking and Sample Rates" for details of system clocking and the FLLs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1507 (05E3h) SLIMbus_ Framer_R ef_Gear	4	SLIMCLK_SRC	0	SLIMbus Clock source Selects the SLIMbus reference clock in Active Framer mode. 0 = SYSCLK 1 = ASYNCCLK Note that the applicable clock must be enabled, and configured at the SLIMbus Root Frequency, in Active Framer mode.
	3:0	SLIMCLK_REF_ GEAR [3:0]	4h	SLIMbus Clock Reference control. Sets the SLIMbus reference clock relative to the SLIMbus Root Frequency (RF). 0h = Clock stopped 1h = Gear 1 (RF / 512) 2h = Gear 2 (RF / 256) 3h = Gear 3 (RF / 128) 4h = Gear 4 (RF / 64) 5h = Gear 5 (RF / 32) 6h = Gear 6 (RF / 16) 7h = Gear 7 (RF / 8) 8h = Gear 8 (RF / 4) 9h = Gear 9 (RF / 2) Ah = Gear 10 (RF) All other codes are Reserved

Table 69 SLIMbus Clock Reference Control

OUTPUT SIGNAL PATH

The CS47L85 provides six stereo pairs of audio output signal paths. These outputs comprise ground-referenced headphone drivers, differential speaker drivers and digital output interfaces suitable for external speaker drivers. The output signal paths are summarised in Table 70.

SIGNAL PATH	DESCRIPTIONS	OUTPUT PINS
OUT1L, OUT1R	Ground-referenced headphone output	HPOUT1L, HPOUT1R
OUT2L, OUT2R	Ground-referenced headphone output	HPOUT2L, HPOUT2R
OUT3L, OUT3R	Ground-referenced headphone output	HPOUT3L, HPOUT3R
OUT4L, OUT4R	Differential speaker output	SPKOUTLN, SPKOUTLP, SPKOUTRP, SPKOUTRN
OUT5L, OUT5R	Digital speaker (PDM) output	SPKDAT1, SPKCLK1
OUT6L, OUT6R	Digital speaker (PDM) output	SPKDAT2, SPKCLK2

Table 70 Output Signal Path Summary

The analogue output paths incorporate high performance 24-bit sigma-delta DACs.

Under default conditions, the headphone drivers provide a stereo, single-ended output. A mono mode is also available on each headphone output pair, providing a differential (BTL) configuration. The ground-referenced headphone output paths incorporate a common mode feedback path for rejection of system-related noise. These outputs support direct connection to headphone loads, with no requirement for AC coupling capacitors.

The speaker output paths are configured to drive a stereo pair of differential (BTL) outputs. The Class D design offers high efficiency at large signal levels. With a suitable choice of external speaker, the Class D output can drive loudspeakers directly, without any additional filter components.

The digital output paths provide two stereo Pulse Density Modulation (PDM) output interfaces, for connection to external audio devices. A total of four digital output channels are provided.

Digital filters can be enabled in the output signal paths, supporting audiophile-quality DAC playback options. These Hi-Fi filters allow user selection of the preferred characteristics, e.g., linear phase, anti-aliasing or apodizing filter responses.

Digital volume control is available on all outputs (analogue and digital), with programmable ramp control for smooth, glitch-free operation. A configurable noise gate function is available on each of the output signal paths. Any two of the output signal paths may be selected as input to the Acoustic Echo Cancellation (AEC) loopback paths.

The CS47L85 incorporates thermal protection functions, and provides short-circuit detection on the Class D speaker and headphone output paths. The General Purpose Timers (see “DSP Peripheral Control”) can also be used as a Watchdog function, to trigger a shutdown of the Class D speaker drivers. For further details, refer to the “Thermal Shutdown and Short Circuit Protection” section.

The Class D speaker outputs are designed to support monitoring of external loudspeakers, giving real-time feedback for algorithms such as Cirrus Logic’s Speaker Protection software, running on one of the DSP cores. This enables loudspeakers to be protected against damage from excessive signal levels and other electro-mechanical constraints. This feature requires additional external component connections, as described later in this document.

The CS47L85 output signal paths are illustrated in Figure 60.

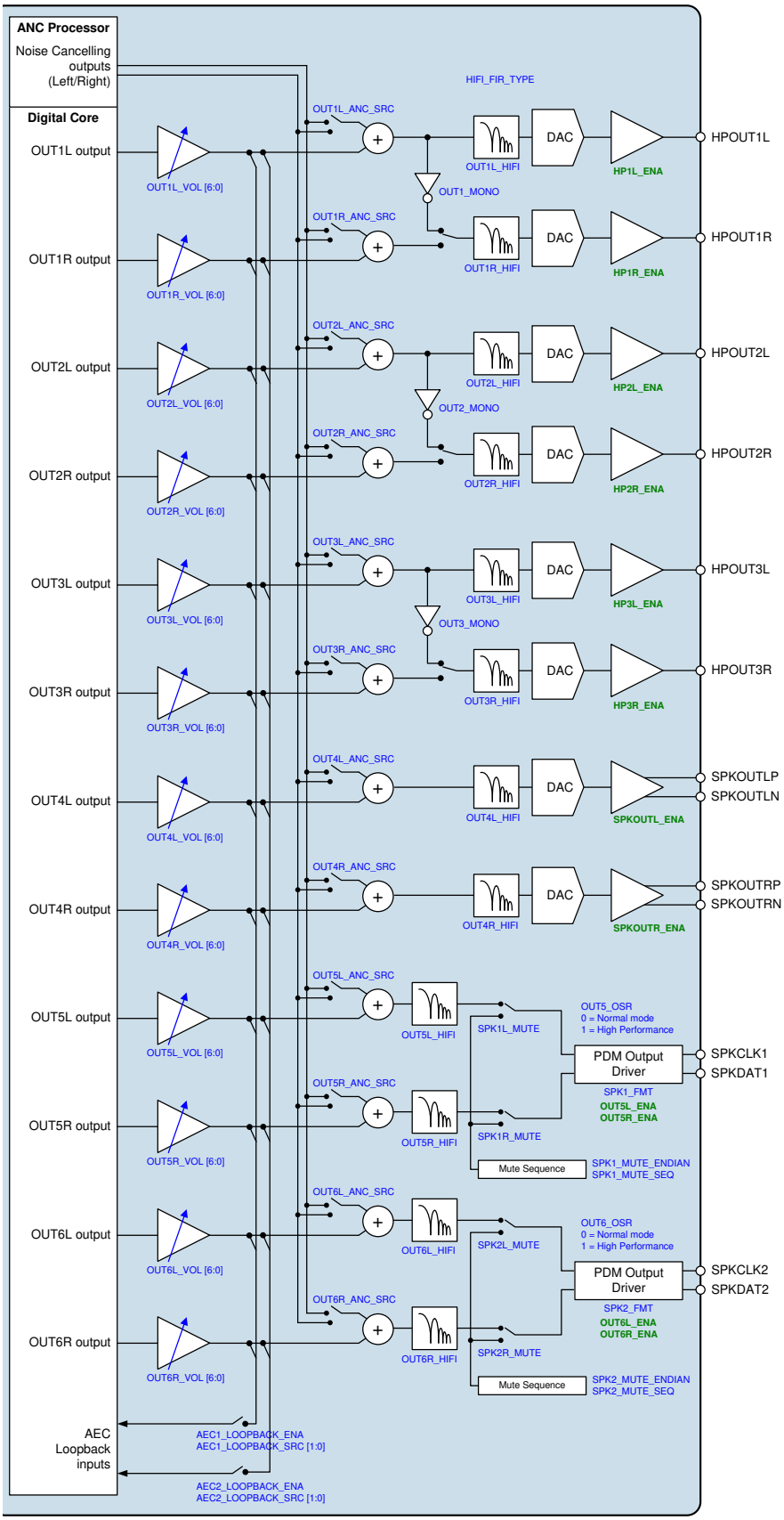


Figure 60 Output Signal Paths

OUTPUT SIGNAL PATH ENABLE

The output signal paths are enabled using the register bits described in Table 71. The respective bit(s) must be enabled for analogue or digital output on the respective output path(s).

The output signal paths are muted by default. It is recommended that de-selecting the mute should be the final step of the path enable control sequence. Similarly, the mute should be selected as the first step of the path disable control sequence. The output signal path mute functions are controlled using the register bits described in Table 76.

The supply rails for outputs (OUT1, OUT2 and OUT3) are generated using an integrated dual-mode Charge Pump, CP1. The Charge Pump is enabled automatically by the CS47L85 when required by the output drivers. See the “Charge Pumps, Regulators and Voltage Reference” section for further details.

The CS47L85 schedules a pop-suppressed control sequence to enable or disable the OUT1, OUT2 OUT3 and OUT4 signal paths. This is automatically managed in response to setting the respective HPnx_ENA or SPKOUTx_ENA register bits. See “Control Write Sequencer” for further details.

The output signal path enable/disable control sequences are inputs to the Interrupt circuit, and can be used to trigger an Interrupt event when a sequence completes. See “Interrupts” for further details.

The system clock, SYSCLK, must be configured and enabled before any audio path is enabled. The output signal paths should be kept disabled (HP*nx*_ENA=0, SPKOUT*x*_ENA=0, OUT*nx*_ENA=0) if SYSCLK is not enabled. The ASYNCCLK may also be required, depending on the path configuration. See “Clocking and Sample Rates” for details of the system clocks (including requirements for reconfiguring SYSCLK while audio paths are enabled).

The CS47L85 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the output signal paths and associated DACs. If an attempt is made to enable an output signal path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The status bits in Register R1025 and R1030 indicate the status of each of the output signal paths. If an Underclocked Error condition occurs, then these bits provide readback of which signal path(s) have been successfully enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1024 (0400h) Output_Enables_1	11	OUT6L_ENA	0	Output Path 6 (Left) Enable 0 = Disabled 1 = Enabled
	10	OUT6R_ENA	0	Output Path 6 (Right) Enable 0 = Disabled 1 = Enabled
	9	OUT5L_ENA	0	Output Path 5 (Left) Enable 0 = Disabled 1 = Enabled
	8	OUT5R_ENA	0	Output Path 5 (Right) Enable 0 = Disabled 1 = Enabled
	7	SPKOUTL_ENA	0	Output Path 4 (Left) Enable 0 = Disabled 1 = Enabled
	6	SPKOUTR_ENA	0	Output Path 4 (Right) Enable 0 = Disabled 1 = Enabled
	5	HP3L_ENA	0	Output Path 3 (Left) Enable 0 = Disabled 1 = Enabled
	4	HP3R_ENA	0	Output Path 3 (Right) Enable 0 = Disabled 1 = Enabled
	3	HP2L_ENA	0	Output Path 2 (Left) Enable 0 = Disabled 1 = Enabled
	2	HP2R_ENA	0	Output Path 2 (Right) Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1	HP1L_ENA	0	Output Path 1 (Left) Enable 0 = Disabled 1 = Enabled
	0	HP1R_ENA	0	Output Path 1 (Right) Enable 0 = Disabled 1 = Enabled
R1025 (0401h) Output_Status_1	11	OUT6L_ENA_STS	0	Output Path 6 (Left) Enable Status 0 = Disabled 1 = Enabled
	10	OUT6R_ENA_STS	0	Output Path 6 (Right) Enable Status 0 = Disabled 1 = Enabled
	9	OUT5L_ENA_STS	0	Output Path 5 (Left) Enable Status 0 = Disabled 1 = Enabled
	8	OUT5R_ENA_STS	0	Output Path 5 (Right) Enable Status 0 = Disabled 1 = Enabled
	7	OUT4L_ENA_STS	0	Output Path 4 (Left) Enable Status 0 = Disabled 1 = Enabled
	6	OUT4R_ENA_STS	0	Output Path 4 (Right) Enable Status 0 = Disabled 1 = Enabled
R1030 (0406h) Raw_Output_Status_1	5	OUT3L_ENA_STS	0	Output Path 3 (Left) Enable Status 0 = Disabled 1 = Enabled
	4	OUT3R_ENA_STS	0	Output Path 3 (Right) Enable Status 0 = Disabled 1 = Enabled
	3	OUT2L_ENA_STS	0	Output Path 2 (Left) Enable Status 0 = Disabled 1 = Enabled
	2	OUT2R_ENA_STS	0	Output Path 2 (Right) Enable Status 0 = Disabled 1 = Enabled
	1	OUT1L_ENA_STS	0	Output Path 1 (Left) Enable Status 0 = Disabled 1 = Enabled
	0	OUT1R_ENA_STS	0	Output Path 1 (Right) Enable Status 0 = Disabled 1 = Enabled

Table 71 Output Signal Path Enable

OUTPUT SIGNAL PATH SAMPLE RATE CONTROL

The output signal paths are derived from the respective output mixers within the CS47L85 digital core. The sample rate for the output signal paths is configured using the OUT_RATE register - see Table 22 within the “Digital Core” section.

Note that sample rate conversion is required when routing the output signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

OUTPUT SIGNAL PATH CONTROL

The SPKCLKn frequency of the PDM output paths (OUT5 and OUT6) is controlled by the respective OUT*n*_OSR register, as described in Table 72. When the OUT*n*_OSR bit is set, the audio performance is improved, but power consumption is also increased.

Note that the SPKCLK*n* frequencies noted in Table 72 assume that the SYSCLK frequency is a multiple of 6.144MHz (SYSCLK_FRAC=0). If the SYSCLK frequency is a multiple of 5.6448MHz (SYSCLK_FRAC=1), then the SPKCLK*n* frequencies will be scaled accordingly.

CONDITION	SPKCLKn FREQUENCY
OUT*n*_OSR = 0	3.072MHz
OUT*n*_OSR = 1	6.144MHz

Table 72 SPKCLK Frequency

The CS47L85 incorporates a stereo Ambient Noise Cancellation (ANC) processor which can provide noise reduction in many different operating conditions. The noise cancellation signals can be mixed into any of the output signal paths using the _ANC_SRC registers, as described in Table 73. See “Ambient Noise Cancellation” for further details of the ANC function.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1040 (0410h) Output_Path_Config_1L	11:10	OUT1L_ANC_SRC [1:0]	00	OUT1L ANC Source Select 00 = Disabled 01 = ANC Left Channel 10 = ANC Right Channel 11 = Reserved
R1044 (0414h) Output_Path_Config_1R	11:10	OUT1R_ANC_SRC [1:0]	00	OUT1R ANC Source Select 00 = Disabled 01 = ANC Left Channel 10 = ANC Right Channel 11 = Reserved
R1048 (0418h) Output_Path_Config_2L	11:10	OUT2L_ANC_SRC [1:0]	00	OUT2L ANC Source Select 00 = Disabled 01 = ANC Left Channel 10 = ANC Right Channel 11 = Reserved
R1052 (041Ch) Output_Path_Config_2R	11:10	OUT2R_ANC_SRC [1:0]	00	OUT2R ANC Source Select 00 = Disabled 01 = ANC Left Channel 10 = ANC Right Channel 11 = Reserved
R1056 (0420h) Output_Path_Config_3L	11:10	OUT3L_ANC_SRC [1:0]	00	OUT3L ANC Source Select 00 = Disabled 01 = ANC Left Channel 10 = ANC Right Channel 11 = Reserved
R1060 (0424h) Output_Path_Config_3R	11:10	OUT3R_ANC_SRC [1:0]	00	OUT3R ANC Source Select 00 = Disabled 01 = ANC Left Channel 10 = ANC Right Channel 11 = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1064 (0428h) Output_Path_Config_4L	11:10	OUT4L_ANC_SRC [1:0]	00	OUT4L ANC Source Select 00 = Disabled 01 = ANC Left Channel 10 = ANC Right Channel 11 = Reserved
R1068 (042Ch) Output_Path_Config_4R	11:10	OUT4R_ANC_SRC [1:0]	00	OUT4R ANC Source Select 00 = Disabled 01 = ANC Left Channel 10 = ANC Right Channel 11 = Reserved
R1072 (0430h) Output_Path_Config_5L	13	OUT5_OSR	0	Output Path 5 Oversample Rate 0 = Normal mode 1 = High Performance mode
	11:10	OUT5L_ANC_SRC [1:0]	00	OUT5L ANC Source Select 00 = Disabled 01 = ANC Left Channel 10 = ANC Right Channel 11 = Reserved
R1076 (0434h) Output_Path_Config_5R	11:10	OUT5R_ANC_SRC [1:0]	00	OUT5R ANC Source Select 00 = Disabled 01 = ANC Left Channel 10 = ANC Right Channel 11 = Reserved
R1080 (0438h) Output_Path_Config_6L	13	OUT6_OSR	0	Output Path 6 Oversample Rate 0 = Normal mode 1 = High Performance mode
	11:10	OUT6L_ANC_SRC [1:0]	00	OUT6L ANC Source Select 00 = Disabled 01 = ANC Left Channel 10 = ANC Right Channel 11 = Reserved
R1084 (043Ch) Output_Path_Config_6R	11:10	OUT6R_ANC_SRC [1:0]	00	OUT6R ANC Source Select 00 = Disabled 01 = ANC Left Channel 10 = ANC Right Channel 11 = Reserved

Table 73 Output Signal Path Control

OUTPUT SIGNAL PATH DIGITAL FILTER CONTROL

An integrated signal processing engine on the CS47L85 supports digital filter requirements for range of Hi-Fi applications. Preset filter coefficients are held in on-board ROM, and can be configured and enabled as required. The Hi-Fi filters are tailored to specific sample rates, and provide options relating to passband frequency, stopband attenuation, and phase response characteristics.

The filter type is selected using the HIFI_FIR_TYPE register field. The available filters are each described in Table 74. The digital filter can be enabled in any output path, using the respective OUTnx_HIFI control bits.

Note that only one filter type can be selected at any time, but the applicable filter can be enabled on any number of output paths simultaneously. The supported sample rates for each filter type are noted in Table 74; the selected filter must be consistent with the output sample rate (OUT_RATE) setting.

The digital filter can be enabled or disabled independently in any output path. A short interruption to the playback if the filter type is changed whilst the Hi-Fi filters are enabled on any output path.

The Hi-Fi digital filters are described in Table 74.

TYPE	SAMPLE RATE	DESCRIPTION	PASSBAND	STOPBAND	PASSBAND RIPPLE	STOPBAND ATTENUATION
0	48 kHz, 44.1 kHz	Deep stopband, Linear Phase	0.454 fs	0.546 fs	0.001 dB	120 dB
1		Deep stopband, Minimum Phase	0.454 fs	0.546 fs	0.001 dB	120 dB
2		Anti-alias, Linear Phase	0.417 fs	0.5 fs	0.001 dB	110 dB
3		Anti-alias, Minimum Phase	0.417 fs	0.5 fs	0.001 dB	110 dB
4	96 kHz, 88.2 kHz	Non-apodizing, Linear Phase	0.227 fs	0.5 fs	0.001 dB	120 dB
5		Non-apodizing, Minimum Phase	0.227 fs	0.5 fs	0.001 dB	120 dB
6		Apodising, Linear Phase	0.227 fs	0.454 fs	0.001 dB	120 dB
7		Apodising, Minimum Phase	0.227 fs	0.454 fs	0.001 dB	120 dB
8	192 kHz, 176.4 kHz	Non-apodizing, Linear Phase	0.114 fs	0.5 fs	0.001 dB	125 dB
9		Non-apodizing, Minimum Phase	0.114 fs	0.5 fs	0.001 dB	125 dB
10		Apodising, Linear Phase	0.114 fs	0.454 fs	0.001 dB	125 dB
11		Apodising, Minimum Phase	0.114 fs	0.454 fs	0.001 dB	125 dB

Table 74 Output Signal Path Digital Filter Types

At 48kHz (or 44.1kHz) sample rate, the key parameters of the Hi-Fi digital filters are the stopband attenuation and phase response. The stopband characteristics are noted in Table 74.

The choice between linear phase and minimum phase filters determines time-domain effects of the filter transfer function. Linear phase offers zero group delay, and equal levels of pre- and post-ringing. Minimum phase offers minimum pre-ringing and latency, but higher levels of post-ringing and group delay distortion.

For sample rates above 48kHz, a choice between apodizing and non-apodizing filters is available. Apodizing filters have the capability to reduce time-domain distortion – this can be used to eliminate 'time smear' effects introduced by other filters in the signal chain, provided the other filters have a flat frequency response throughout the apodizing filter's cut-off region. The cut-off (stopband) frequency of the apodizing filters are slightly lower than the respective non-apodizing filter response.

The Hi-Fi digital filter control registers are described in Table 75.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1040 (410h)	14	OUT1L_HIFI	0	Output Path 1 (Left) Hi-Fi Filter Enable 0 = Disabled 1 = Enabled
R1044 (414h)	14	OUT1R_HIFI	0	Output Path 1 (Right) Hi-Fi Filter Enable 0 = Disabled 1 = Enabled
R1048 (418h)	14	OUT2L_HIFI	0	Output Path 2 (Left) Hi-Fi Filter Enable 0 = Disabled 1 = Enabled
R1052 (41Ch)	14	OUT2R_HIFI	0	Output Path 2 (Right) Hi-Fi Filter Enable 0 = Disabled 1 = Enabled
R1056 (420h)	14	OUT3L_HIFI	0	Output Path 3 (Left) Hi-Fi Filter Enable 0 = Disabled 1 = Enabled
R1060 (424h)	14	OUT3R_HIFI	0	Output Path 3 (Right) Hi-Fi Filter Enable 0 = Disabled 1 = Enabled
R1064 (428h)	14	OUT4L_HIFI	0	Output Path 4 (Left) Hi-Fi Filter Enable 0 = Disabled 1 = Enabled
R1068 (42Ch)	14	OUT4R_HIFI	0	Output Path 4 (Right) Hi-Fi Filter Enable 0 = Disabled 1 = Enabled
R1072 (430h)	14	OUT5L_HIFI	0	Output Path 5 (Left) Hi-Fi Filter Enable 0 = Disabled 1 = Enabled
R1076 (434h)	14	OUT5R_HIFI	0	Output Path 5 (Right) Hi-Fi Filter Enable 0 = Disabled 1 = Enabled
R1080 (438h)	14	OUT6L_HIFI	0	Output Path 6 (Left) Hi-Fi Filter Enable 0 = Disabled 1 = Enabled
R1084 (43Ch)	14	OUT6R_HIFI	0	Output Path 6 (Right) Hi-Fi Filter Enable 0 = Disabled 1 = Enabled
R1102 (44Eh)	3:0	HIFI_FIR_TYPE [3:0]	0000	Output Path Hi-Fi Filter Select 0h = 48kHz Deep stopband, Linear phase 1h = 48kHz Deep stopband, Minimum phase 2h = 48kHz Anti-alias, Linear phase 3h = 48kHz Anti-alias, Minimum phase 4h = 96kHz Non-apodizing, Linear phase 5h = 96kHz Non-apodizing, Minimum phase 6h = 96kHz Apodizing, Linear phase 7h = 96kHz Apodizing, Minimum phase 8h = 192kHz Non-apodizing, Linear phase 9h = 192kHz Non-apodizing, Minimum phase Ah = 192kHz Apodizing, Linear phase Bh = 192kHz Apodizing, Minimum phase All other codes are Reserved

Table 75 Output Signal Path Digital Filter Control

OUTPUT SIGNAL PATH DIGITAL VOLUME CONTROL

A digital volume control is provided on each of the output signal paths, providing -64dB to +31.5dB gain control in 0.5dB steps. An independent mute control is also provided for each output signal path.

Whenever the gain or mute setting is changed, the signal path gain is ramped up or down to the new settings at a programmable rate. For increasing gain (or un-mute), the rate is controlled by the OUT_VI_RAMP register. For decreasing gain (or mute), the rate is controlled by the OUT_VD_RAMP register. Note that the OUT_VI_RAMP and OUT_VD_RAMP registers should not be changed while a volume ramp is in progress.

The OUT_VU bits control the loading of the output signal path digital volume and mute controls. When OUT_VU is set to 0, the digital volume and mute settings will be loaded into the respective control register, but will not actually change the signal path gain. The digital volume and mute settings on all of the output signal paths are updated when a 1 is written to OUT_VU. This makes it possible to update the gain of multiple signal paths simultaneously.

Note that, although the digital volume control registers provide 0.5dB steps, the internal circuits provide signal gain adjustment in 0.125dB steps. This allows a very high degree of gain control, and smooth volume ramping under all operating conditions.

The 0dBFS level of the OUT5/OUT6 digital output paths is not equal to the 0dBFS level of the CS47L85 digital core. The maximum digital output level is -6dBFS (see “Electrical Characteristics”). Under 0dBFS gain conditions, a 0dBFS output from the digital core corresponds to a -6dBFS level in the PDM output.

The digital volume control register fields are described in Table 76 and Table 77.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1033 (0409h) Output_Volume_Ramp	6:4	OUT_VD_RAMP [2:0]	010	Output Volume Decreasing Ramp Rate (seconds/6dB) 000 = 0ms 001 = 0.5ms 010 = 1ms 011 = 2ms 100 = 4ms 101 = 8ms 110 = 15ms 111 = 30ms This register should not be changed while a volume ramp is in progress.
	2:0	OUT_VI_RAMP [2:0]	010	Output Volume Increasing Ramp Rate (seconds/6dB) 000 = 0ms 001 = 0.5ms 010 = 1ms 011 = 2ms 100 = 4ms 101 = 8ms 110 = 15ms 111 = 30ms This register should not be changed while a volume ramp is in progress.
R1041 (0411h) DAC_Digital_Volume_1L	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT1L_MUTE	1	Output Path 1 (Left) Digital Mute 0 = Un-mute 1 = Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	OUT1L_VOL [7:0]	80h	Output Path 1 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 77 for volume range)
R1045 (0415h) DAC_Digital_Volume_1R	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT1R_MUTE	1	Output Path 1 (Right) Digital Mute 0 = Un-mute 1 = Mute
	7:0	OUT1R_VOL [7:0]	80h	Output Path 1 (Right) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 77 for volume range)
R1049 (0419h) DAC_Digital_Volume_2L	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT2L_MUTE	1	Output Path 2 (Left) Digital Mute 0 = Un-mute 1 = Mute
	7:0	OUT2L_VOL [7:0]	80h	Output Path 2 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 77 for volume range)
R1053 (041Dh) DAC_Digital_Volume_2R	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT2R_MUTE	1	Output Path 2 (Right) Digital Mute 0 = Un-mute 1 = Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	OUT2R_VOL [7:0]	80h	Output Path 2 (Right) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 77 for volume range)
R1057 (0421h) DAC_Digital_Volume_3L	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT3L_MUTE	1	Output Path 3 (Left) Digital Mute 0 = Un-mute 1 = Mute
	7:0	OUT3L_VOL [7:0]	80h	Output Path 3 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 77 for volume range)
R1061 (0425h) DAC_Digital_Volume_3R	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT3R_MUTE	1	Output Path 3 (Right) Digital Mute 0 = Un-mute 1 = Mute
	7:0	OUT3R_VOL [7:0]	80h	Output Path 3 (Right) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 77 for volume range)
R1065 (0429h) DAC_Digital_Volume_4L	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT4L_MUTE	1	Output Path 4 (Left) Digital Mute 0 = Un-mute 1 = Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	OUT4L_VOL [7:0]	80h	Output Path 4 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 77 for volume range)
R1069 (042Dh) DAC_Digital_Volume_4R	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT4R_MUTE	1	Output Path 4 (Right) Digital Mute 0 = Un-mute 1 = Mute
	7:0	OUT4R_VOL [7:0]	80h	Output Path 4 (Right) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 77 for volume range)
R1073 (0431h) DAC_Digital_Volume_5R	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT5L_MUTE	1	Output Path 5 (Left) Digital Mute 0 = Un-mute 1 = Mute
	7:0	OUT5L_VOL [7:0]	80h	Output Path 5 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 77 for volume range)
R1077 (0435h) DAC_Digital_Volume_5R	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT5R_MUTE	1	Output Path 5 (Right) Digital Mute 0 = Un-mute 1 = Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	OUT5R_VOL [7:0]	80h	Output Path 5 (Right) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 77 for volume range)
R1081 (0439h) DAC_Digital_Volume_6L	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT6L_MUTE	1	Output Path 6 (Left) Digital Mute 0 = Un-mute 1 = Mute
	7:0	OUT6L_VOL [7:0]	80h	Output Path 6 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 77 for volume range)
R1085 (043Dh) DAC_Digital_Volume_6R	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT6R_MUTE	1	Output Path 6 (Right) Digital Mute 0 = Un-mute 1 = Mute
	7:0	OUT6R_VOL [7:0]	80h	Output Path 6 (Right) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 77 for volume range)

Table 76 Output Signal Path Digital Volume Control

Output Volume Register	Volume (dB)	Output Volume Register	Volume (dB)	Output Volume Register	Volume (dB)	Output Volume Register	Volume (dB)
00h	-64.0	40h	-32.0	80h	0.0	C0h	Reserved
01h	-63.5	41h	-31.5	81h	0.5	C1h	Reserved
02h	-63.0	42h	-31.0	82h	1.0	C2h	Reserved
03h	-62.5	43h	-30.5	83h	1.5	C3h	Reserved
04h	-62.0	44h	-30.0	84h	2.0	C4h	Reserved
05h	-61.5	45h	-29.5	85h	2.5	C5h	Reserved
06h	-61.0	46h	-29.0	86h	3.0	C6h	Reserved
07h	-60.5	47h	-28.5	87h	3.5	C7h	Reserved
08h	-60.0	48h	-28.0	88h	4.0	C8h	Reserved
09h	-59.5	49h	-27.5	89h	4.5	C9h	Reserved
0Ah	-59.0	4Ah	-27.0	8Ah	5.0	CAh	Reserved
0Bh	-58.5	4Bh	-26.5	8Bh	5.5	CBh	Reserved
0Ch	-58.0	4Ch	-26.0	8Ch	6.0	CCh	Reserved
0Dh	-57.5	4Dh	-25.5	8Dh	6.5	CDh	Reserved
0Eh	-57.0	4Eh	-25.0	8Eh	7.0	CEh	Reserved
0Fh	-56.5	4Fh	-24.5	8Fh	7.5	CFh	Reserved
10h	-56.0	50h	-24.0	90h	8.0	D0h	Reserved
11h	-55.5	51h	-23.5	91h	8.5	D1h	Reserved
12h	-55.0	52h	-23.0	92h	9.0	D2h	Reserved
13h	-54.5	53h	-22.5	93h	9.5	D3h	Reserved
14h	-54.0	54h	-22.0	94h	10.0	D4h	Reserved
15h	-53.5	55h	-21.5	95h	10.5	D5h	Reserved
16h	-53.0	56h	-21.0	96h	11.0	D6h	Reserved
17h	-52.5	57h	-20.5	97h	11.5	D7h	Reserved
18h	-52.0	58h	-20.0	98h	12.0	D8h	Reserved
19h	-51.5	59h	-19.5	99h	12.5	D9h	Reserved
1Ah	-51.0	5Ah	-19.0	9Ah	13.0	DAh	Reserved
1Bh	-50.5	5Bh	-18.5	9Bh	13.5	DBh	Reserved
1Ch	-50.0	5Ch	-18.0	9Ch	14.0	DCh	Reserved
1Dh	-49.5	5Dh	-17.5	9Dh	14.5	DDh	Reserved
1Eh	-49.0	5Eh	-17.0	9Eh	15.0	DEh	Reserved
1Fh	-48.5	5Fh	-16.5	9Fh	15.5	DFh	Reserved
20h	-48.0	60h	-16.0	A0h	16.0	E0h	Reserved
21h	-47.5	61h	-15.5	A1h	16.5	E1h	Reserved
22h	-47.0	62h	-15.0	A2h	17.0	E2h	Reserved
23h	-46.5	63h	-14.5	A3h	17.5	E3h	Reserved
24h	-46.0	64h	-14.0	A4h	18.0	E4h	Reserved
25h	-45.5	65h	-13.5	A5h	18.5	E5h	Reserved
26h	-45.0	66h	-13.0	A6h	19.0	E6h	Reserved
27h	-44.5	67h	-12.5	A7h	19.5	E7h	Reserved
28h	-44.0	68h	-12.0	A8h	20.0	E8h	Reserved
29h	-43.5	69h	-11.5	A9h	20.5	E9h	Reserved
2Ah	-43.0	6Ah	-11.0	AAh	21.0	EAh	Reserved
2Bh	-42.5	6Bh	-10.5	ABh	21.5	EBh	Reserved
2Ch	-42.0	6Ch	-10.0	ACh	22.0	ECh	Reserved
2Dh	-41.5	6Dh	-9.5	ADh	22.5	EDh	Reserved
2Eh	-41.0	6Eh	-9.0	AEh	23.0	EEh	Reserved
2Fh	-40.5	6Fh	-8.5	AFh	23.5	EFh	Reserved
30h	-40.0	70h	-8.0	B0h	24.0	F0h	Reserved
31h	-39.5	71h	-7.5	B1h	24.5	F1h	Reserved
32h	-39.0	72h	-7.0	B2h	25.0	F2h	Reserved
33h	-38.5	73h	-6.5	B3h	25.5	F3h	Reserved
34h	-38.0	74h	-6.0	B4h	26.0	F4h	Reserved
35h	-37.5	75h	-5.5	B5h	26.5	F5h	Reserved
36h	-37.0	76h	-5.0	B6h	27.0	F6h	Reserved
37h	-36.5	77h	-4.5	B7h	27.5	F7h	Reserved
38h	-36.0	78h	-4.0	B8h	28.0	F8h	Reserved
39h	-35.5	79h	-3.5	B9h	28.5	F9h	Reserved
3Ah	-35.0	7Ah	-3.0	BAh	29.0	FAh	Reserved
3Bh	-34.5	7Bh	-2.5	BBh	29.5	FBh	Reserved
3Ch	-34.0	7Ch	-2.0	BCh	30.0	FCh	Reserved
3Dh	-33.5	7Dh	-1.5	BDh	30.5	FDh	Reserved
3Eh	-33.0	7Eh	-1.0	BEh	31.0	FEh	Reserved
3Fh	-32.5	7Fh	-0.5	BFh	31.5	FFh	Reserved

Table 77 Output Signal Path Digital Volume Range

OUTPUT SIGNAL PATH NOISE GATE CONTROL

The CS47L85 provides a digital noise gate function for each of the output signal paths. The noise gate ensures best noise performance when the signal path is idle. When the noise gate is enabled, and the applicable signal level is below the noise gate threshold, then the noise gate is activated, causing the signal path to be muted.

The noise gate function is enabled using the NGATE_ENA register, as described in Table 78.

For each output path, the noise gate may be associated with one or more of the signal path threshold detection functions using the _NGATE_SRC register fields. When more than one signal threshold is selected, then the output path noise gate is only activated (i.e., muted) when all of the respective signal thresholds are satisfied.

For example, if the OUT1L noise gate is associated with the OUT1L and OUT1R signal paths, then the OUT1L signal path will only be muted if both the OUT1L and OUT1R signal levels are below the respective thresholds.

The noise gate threshold (the signal level below which the noise gate is activated) is set using NGATE_THR. Note that, for each output path, the noise gate threshold represents the signal level at the respective output pin(s) - the threshold is therefore independent of the digital volume and PGA gain settings.

Note that, although there is only one noise gate threshold level (NGATE_THR), each of the output path noise gates may be activated independently, according to the respective signal content and the associated threshold configuration(s).

To prevent erroneous triggering, a time delay is applied before the gate is activated; the noise gate is only activated (i.e., muted) when the output levels are below the applicable signal level threshold(s) for longer than the noise gate 'hold time'. The 'hold time' is set using the NGATE_HOLD register.

When the noise gate is activated, the CS47L85 gradually attenuates the respective signal path at the rate set by the OUT_VD_RAMP register (see Table 76). When the noise gate is de-activated, the output volume increases at the rate set by the OUT_VI_RAMP register.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1043 (0413h) Noise_Gate_Select_1L	11:0	OUT1L_NGATE_SRC [11:0]	001h	Output Signal Path Noise Gate Source Enables one of more signal paths as inputs to the respective noise gate. If more than one signal path is enabled as an input, the noise gate is only activated (i.e., muted) when all of the respective signal thresholds are satisfied. [11] = OUT6R [10] = OUT6L [9] = OUT5R [8] = OUT5L [7] = OUT4R [6] = OUT4L [5] = OUT3R [4] = OUT3L [3] = OUT2R [2] = OUT2L [1] = OUT1R [0] = OUT1L Each bit is coded as: 0 = Disabled 1 = Enabled
R1047 (0417h) Noise_Gate_Select_1R	11:0	OUT1R_NGATE_SRC [11:0]	002h	
R1051 (041Bh) Noise_Gate_Select_2L	11:0	OUT2L_NGATE_SRC [11:0]	004h	
R1055 (041Fh) Noise_Gate_Select_2R	11:0	OUT2R_NGATE_SRC [11:0]	008h	
R1059 (0423h) Noise_Gate_Select_3L	11:0	OUT3L_NGATE_SRC [11:0]	010h	
R1063 (0427h) Noise_Gate_Select_3R	11:0	OUT3R_NGATE_SRC [11:0]	020h	
R1067 (042Bh) Noise_Gate_Select_4L	11:0	OUT4L_NGATE_SRC [11:0]	040h	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1071 (042Fh) Noise_Gate_Select_4R	11:0	OUT4R_NGATE_SRC [11:0]	080h	
R1075 (0433h) Noise_Gate_Select_5L	11:0	OUT5L_NGATE_SRC [11:0]	100h	
R1079 (0437h) Noise_Gate_Select_5R	11:0	OUT5R_NGATE_SRC [11:0]	200h	
R1083 (043Bh) Noise_Gate_Select_6L	11:0	OUT6L_NGATE_SRC [11:0]	400h	
R1087 (043Fh) Noise_Gate_Select_6R	11:0	OUT6R_NGATE_SRC [11:0]	800h	
R1112 (0458h) Noise_Gate_Control	5:4	NGATE_HOLD [1:0]	00	Output Signal Path Noise Gate Hold Time (delay before noise gate is activated) 00 = 30ms 01 = 120ms 10 = 250ms 11 = 500ms
	3:1	NGATE_THR [2:0]	000	Output Signal Path Noise Gate Threshold 000 = -78dB 001 = -84dB 010 = -90dB 011 = -96dB 100 = -102dB 101 = -108dB 110 = -114dB 111 = -120dB
	0	NGATE_ENA	0	Output Signal Path Noise Gate Enable 0 = Disabled 1 = Enabled

Table 78 Output Signal Path Noise Gate Control

OUTPUT SIGNAL PATH AEC LOOPBACK

The CS47L85 incorporates two loopback signal paths, which are ideally suited as a reference for Acoustic Echo Cancellation (AEC) processing. Any two of the output signal paths may be selected as the AEC loopback sources.

When configured with suitable DSP firmware, the CS47L85 can provide an integrated AEC capability. The AEC loopback feature also enables convenient hook-up to an external device for implementing the required signal processing algorithms.

The AEC Loopback source is connected after the respective digital volume controls, as illustrated in Figure 60. The AEC Loopback signals can be selected as input to any of the digital mixers within the CS47L85 digital core. The sample rate for the AEC Loopback paths is configured using the OUT_RATE register - see Table 22 within the “Digital Core” section.

The AEC loopback function is enabled using the AEC*n*_LOOPBACK_ENA register bits, (where ‘n’ identifies the applicable path, AEC1 or AEC2). The source signals for the Transmit Path AEC function are selected using the AEC*n*_LOOPBACK_SRC bits.

The CS47L85 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the AEC Loopback function. If an attempt is made to enable this function, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The AEC*n*_ENA_STS register bits indicate the status of the AEC Loopback functions. If an Underclocked Error condition occurs, then these bits can provide indication of whether the AEC Loopback function has been successfully enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1104 (0450h) DAC_AEC_Control_1	5:2	AEC1_LOOPBACK_SRC [3:0]	0000	Input source for Tx AEC1 function 0000 = OUT1L 0001 = OUT1R 0010 = OUT2L 0011 = OUT2R 0100 = OUT3 0110 = OUT4L 0111 = OUT4R 1000 = OUT5L 1001 = OUT5R 1010 = OUT6L 1011 = OUT6R All other codes are Reserved
	1	AEC1_ENA_STS	0	Transmit (Tx) Path AEC1 Control Status 0 = Disabled 1 = Enabled
	0	AEC1_LOOPBACK_ENA	0	Transmit (Tx) Path AEC1 Control 0 = Disabled 1 = Enabled
R1105 (0451h) DAC_AEC_Control_2	5:2	AEC2_LOOPBACK_SRC [3:0]	0000	Input source for Tx AEC2 function 0000 = OUT1L 0001 = OUT1R 0010 = OUT2L 0011 = OUT2R 0100 = OUT3 0110 = OUT4L 0111 = OUT4R 1000 = OUT5L 1001 = OUT5R 1010 = OUT6L 1011 = OUT6R All other codes are Reserved
	1	AEC2_ENA_STS	0	Transmit (Tx) Path AEC2 Control Status 0 = Disabled 1 = Enabled
	0	AEC2_LOOPBACK_ENA	0	Transmit (Tx) Path AEC2 Control 0 = Disabled 1 = Enabled

Table 79 Output Signal Path AEC Loopback Control

HEADPHONE OUTPUTS AND MONO MODE

The headphone drivers can provide a mono differential (BTL) output; this is ideal for driving an earpiece or hearing aid coil. The mono differential (BTL) configuration is selected using the OUTn_MONO register bits.

When the OUTn_MONO bit is set, then the respective Right channel output is an inverted copy of the Left channel output signal; this creates a differential output between the respective OUTnL and OUTnR signal paths. The Left and Right channel output drivers must both be enabled in Mono mode; both channels should be enabled simultaneously using the register bits described in Table 71.

The mono (BTL) signal paths are illustrated in Figure 60. Note that, in mono configuration, the effective gain of the signal path is increased by 6dB.

The OUT1L and OUT1R output signal paths are associated with the analogue outputs HPOUT1L and HPOUT1R respectively.

The OUT2L and OUT2R output signal paths are associated with the analogue outputs HPOUT2L and HPOUT2R respectively.

The OUT3L and OUT3R output signal paths are associated with the analogue outputs HPOUT3L and HPOUT3R respectively.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1040 (0410h) Output_Path_Config_1L	12	OUT1_MONO	0	Output Path 1 Mono Mode (Configures HPOUT1L and HPOUT1R as a mono differential output.) 0 = Disabled 1 = Enabled The gain of the signal path is increased by 6dB in differential (mono) mode.
R1048 (0418h) Output_Path_Config_2L	12	OUT2_MONO	0	Output Path 2 Mono Mode (Configures HPOUT2L and HPOUT2R as a mono differential output.) 0 = Disabled 1 = Enabled The gain of the signal path is increased by 6dB in differential (mono) mode.
R1056 (0420h) Output_Path_Config_3L	12	OUT3_MONO	0	Output Path 3 Mono Mode (Configures HPOUT3L and HPOUT3R as a mono differential output.) 0 = Disabled 1 = Enabled The gain of the signal path is increased by 6dB in differential (mono) mode.

Table 80 Headphone Driver Mono Mode Control

The headphone driver outputs HPOUT1L, HPOUT1R, HPOUT2L, HPOUT2R, HPOUT3L and HPOUT3R are suitable for direct connection to external headphones and earpieces. The outputs are ground-referenced, eliminating any requirement for AC coupling capacitors.

The headphone outputs incorporate a common mode, or ground loop, feedback path which provides rejection of system-related ground noise. The feedback pins must be connected to ground for normal operation of the headphone outputs.

Note that the feedback pins should be connected to GND close to the respective headphone jack, as illustrated in Figure 61. In mono (differential) mode, the feedback pin(s) should be connected to the ground plane that is physically closest to the earpiece output PCB tracks.

The ground feedback path for HPOUT1L and HPOUT1R is provided via the HPOUT1FB1 or HPOUT1FB2 pins; the applicable connection must be selected using the ACCDET_SRC register, as described in Table 81.

The ground feedback path for HPOUT2L and HPOUT2R is provided via the HPOUT2FB pin. No register configuration is required for the HPOUT2FB connection.

The ground feedback path for HPOUT3L and HPOUT3R is provided via the HPOUT3FB pin. No register configuration is required for the HPOUT3FB connection.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R659 (0293h) Accessory _Detect_M ode_1	13	ACCDET_SRC	0	Accessory Detect / Headphone Feedback pin select 0 = Accessory detect on MICDET1, Headphone ground feedback on HPOUT1FB1 1 = Accessory detect on MICDET2, Headphone ground feedback on HPOUT1FB2

Table 81 Headphone Output (HPOUT1) Ground Feedback Control

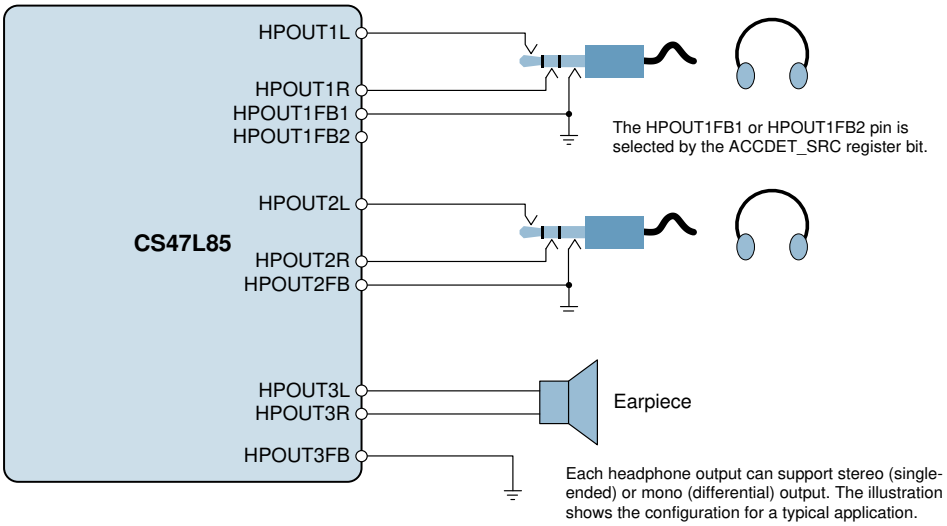


Figure 61 Headphone and Earpiece Connection

SPEAKER OUTPUTS (ANALOGUE)

The speaker driver outputs SPKOUTLP, SPKOUTLN, SPKOUTLP and SPKOUTLN provide two differential (BTL) outputs suitable for direct connection to external loudspeakers. The integrated Class D speaker driver provides high efficiency at large signal levels.

The speaker driver signal paths incorporate a boost function which shifts the signal levels between the AVDD and SPKVDD voltage domains. The boost is pre-configured (+12dB) for the recommended AVDD and SPKVDD operating voltages (see “Recommended Operating Conditions”).

Ultra-low leakage and high PSRR allow the speaker supply SPKVDD to be connected directly to a lithium battery. Note that SPKVDDL powers the Left Speaker driver, and SPKVDDR powers the Right Speaker driver; it is assumed that SPKVDDL = SPKVDDR = SPKVDD.

Note that SYSCLK must be present and enabled when using the Class D speaker output; see “Clocking and Sample Rates” for details of SYSCLK and the associated register control fields.

The OUT4L and OUT4R output signal paths are associated with the analogue outputs SPKOUTLP, SPKOUTLN, SPKOUTLP and SPKOUTLN.

The Class D speaker output is a pulse width modulated signal, and requires external filtering in order to recreate the audio signal. With a suitable choice of external speakers, the speakers themselves can provide the necessary filtering. See “Applications Information” for further information on Class D speaker connections.

The external speaker connection is illustrated in Figure 62, assuming suitable speakers are chosen to provide the PWM filtering.

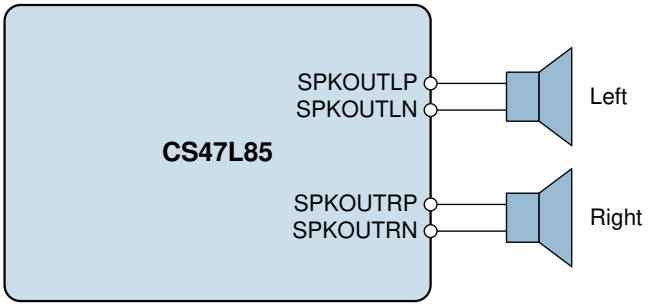


Figure 62 Speaker Connection

The speaker output paths are designed to support monitoring of external loudspeakers, giving real-time feedback for algorithms such as Cirrus Logic's Speaker Protection software. Specific external connections are necessary when using this feature, as detailed below.

The Speaker Protection software, implemented on one of the integrated DSP cores, enables loudspeakers to be protected from excessive signal levels and other electro-mechanical constraints. The monitoring circuit enables the operational limits to be continually optimised for the particular loudspeaker and the prevailing conditions. Factors such as cone excursion, resonance, and thermal behaviour of the loudspeaker are modelled in the Speaker Protection software. As a result, the maximum audio output can be achieved, whilst ensuring the loudspeakers are also fully protected from damage.

Separate P/N ground connections are provided for each speaker driver channel; these pins relate to the positive/negative output transistors respectively, to allow comprehensive current monitoring in the output paths, as an input to the speaker protection algorithms.

The external speaker connections, incorporating the output current monitoring requirements, are illustrated in Figure 63. Note that, if output current monitoring is not required on one or more speaker channels, then the respective ground connections should be tied directly to ground on the PCB.

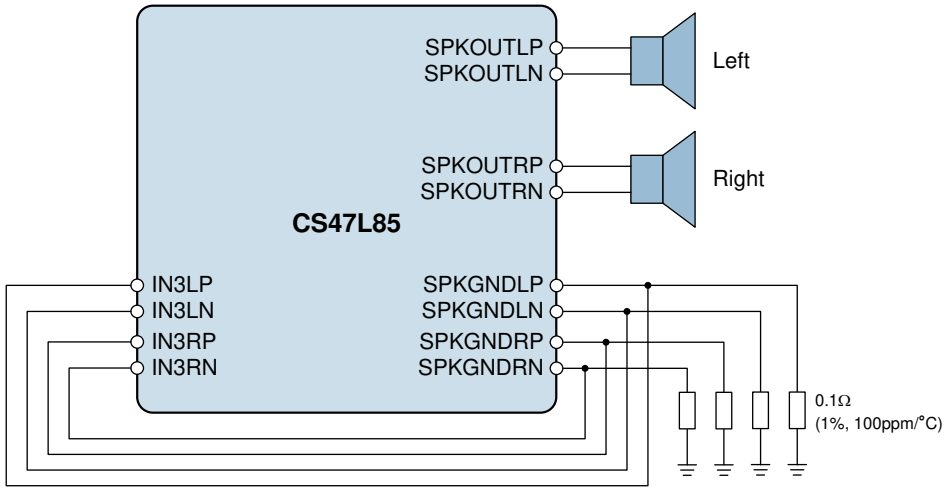


Figure 63 Speaker Output Current Monitoring Connections (Speaker Protection)

Please contact your local Cirrus Logic representative for further information on the Speaker Protection software.

SPEAKER OUTPUTS (DIGITAL PDM)

The CS47L85 supports a four-channel Pulse Density Modulation (PDM) digital speaker interface; the PDM outputs are associated with the OUT5L, OUT5R, OUT6L and OUT6R output signal paths.

The PDM digital speaker interface comprises two stereo interfaces; the operation of one interface is illustrated in Figure 64.

The external connections associated with the PDM outputs are implemented on multi-function GPIO pins, which must be configured for the respective PDM functions when required. The PDM output connections are pin-specific alternative functions available on specific GPIO pins. See “General Purpose Input / Output” to configure the GPIO pins for the PDM output.

The OUT5L and OUT5R output signal paths are interleaved on the SPKDAT1 output, and clocked using SPKCLK1. The OUT6L and OUT6R output signal paths are interleaved on the SPKDAT2 output, and clocked using SPKCLK2.

Note that the PDM interface supports two different operating modes; these are selected using the SPK1_FMT and SPK2_FMT register bits. See “Signal Timing Requirements” for detailed timing information in both modes.

When SPK*n*_FMT = 0 (Mode A), then the Left PDM channel is valid at the rising edge of SPKCLK; the Right PDM channel is valid at the falling edge of SPKCLK.

When SPK*n*_FMT = 1 (Mode B), then the Left PDM channel is valid during the low phase of SPKCLK; the Right PDM channel is valid during the high phase of SPKCLK.

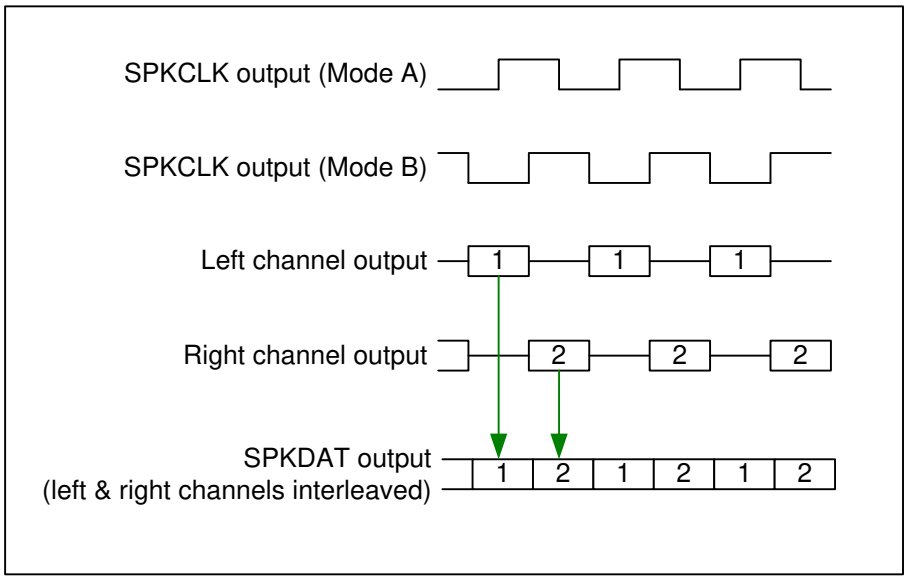


Figure 64 Digital Speaker (PDM) Interface Timing

Clocking for the PDM interface is derived from SYSCLK. Note that the SYSCLK_ENA register must also be set. See “Clocking and Sample Rates” for further details of the system clocks and control registers.

When the OUT5L or OUT5R output signal path is enabled, the PDM interface clock signal is output on the SPKCLK1 pin.

When the OUT6L or OUT6R output signal path is enabled, the PDM interface clock signal is output on the SPKCLK2 pin.

The output signal paths support normal and high performance operating modes, as described in the “Output Signal Path” section. The SPKCLK*n* frequency is set according to the operating mode of the relevant output path, as described in Table 82. The OUT5_OSR and OUT6_OSR register bits are defined in Table 73.

Note that the SPKCLK*n* frequencies noted in Table 82 and Table 83 assume that the SYSCLK frequency is a multiple of 6.144MHz (SYSCLK_FRAC=0). If the SYSCLK frequency is a multiple of 5.6448MHz (SYSCLK_FRAC=1), then the SPKCLK*n* frequencies will be scaled accordingly.

OUT5_OSR	DESCRIPTION	SPKCLK1 FREQUENCY
0	Normal mode	3.072MHz
1	High Performance mode	6.144MHz

Table 82 SPKCLK1 Frequency

OUT6_OSR	DESCRIPTION	SPKCLK2 FREQUENCY
0	Normal mode	3.072MHz
1	High Performance mode	6.144MHz

Table 83 SPKCLK2 Frequency

The PDM output channels can be independently muted. When muted, the default output on each channel is a DSD-compliant silent stream (0110_1001b). The mute output code can be programmed to other values if required, using the SPK*n*_MUTE_SEQ register fields. The mute output code can be transmitted MSB-first or LSB-first; this is selectable using the SPK*n*_MUTE_ENDIAN register.

Note that the PDM Mute function is not a soft-mute; the audio output is interrupted immediately when the PDM mute is asserted. It is recommended to use the Output Signal Path mute function before applying the PDM mute. See Table 76 for details of the OUT*n*L_MUTE and OUT*n*R_MUTE registers.

The PDM output interface registers are described in Table 84.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1168 (0490h) PDM_SPK 1_CTRL_1	13	SPK1R_MUTE	0	PDM Speaker Output 1 (Right) Mute 0 = Audio output (OUT5R) 1 = Mute Sequence output
	12	SPK1L_MUTE	0	PDM Speaker Output 1 (Left) Mute 0 = Audio output (OUT5L) 1 = Mute Sequence output
	8	SPK1_MUTE_ENDIAN	0	PDM Speaker Output 1 Mute Sequence Control 0 = Mute sequence is LSB first 1 = Mute sequence output is MSB first
	7:0	SPK1_MUTE_SEQ [7:0]	69h	PDM Speaker Output 1 Mute Sequence Defines the 8-bit code that is output on SPKDAT1 (left) or SPKDAT1 (right) when muted.
R1169 (0491h) PDM_SPK 1_CTRL_2	0	SPK1_FMT	0	PDM Speaker Output 1 timing format 0 = Mode A (PDM data is valid at the rising/falling edges of SPKCLK1) 1 = Mode B (PDM data is valid during the high/low phase of SPKCLK1)
R1170 (0492h) PDM_SPK 2_CTRL_1	13	SPK2R_MUTE	0	PDM Speaker Output 2 (Right) Mute 0 = Audio output (OUT6R) 1 = Mute Sequence output
	12	SPK2L_MUTE	0	PDM Speaker Output 2 (Left) Mute 0 = Audio output (OUT6L) 1 = Mute Sequence output
	8	SPK2_MUTE_ENDIAN	0	PDM Speaker Output 2 Mute Sequence Control 0 = Mute sequence is LSB first 1 = Mute sequence output is MSB first
	7:0	SPK2_MUTE_SEQ [7:0]	69h	PDM Speaker Output 2 Mute Sequence Defines the 8-bit code that is output on SPKDAT2 (left) or SPKDAT2 (right) when muted.
R1171 (0493h) PDM_SPK 2_CTRL_2	0	SPK2_FMT	0	PDM Speaker Output 2 timing format 0 = Mode A (PDM data is valid at the rising/falling edges of SPKCLK2) 1 = Mode B (PDM data is valid during the high/low phase of SPKCLK2)

Table 84 Digital Speaker (PDM) Output Control

The digital speaker (PDM) outputs SPKDAT*n* and SPKCLK*n* are intended for direct connection to a compatible external speaker driver. A typical configuration is illustrated in Figure 65.

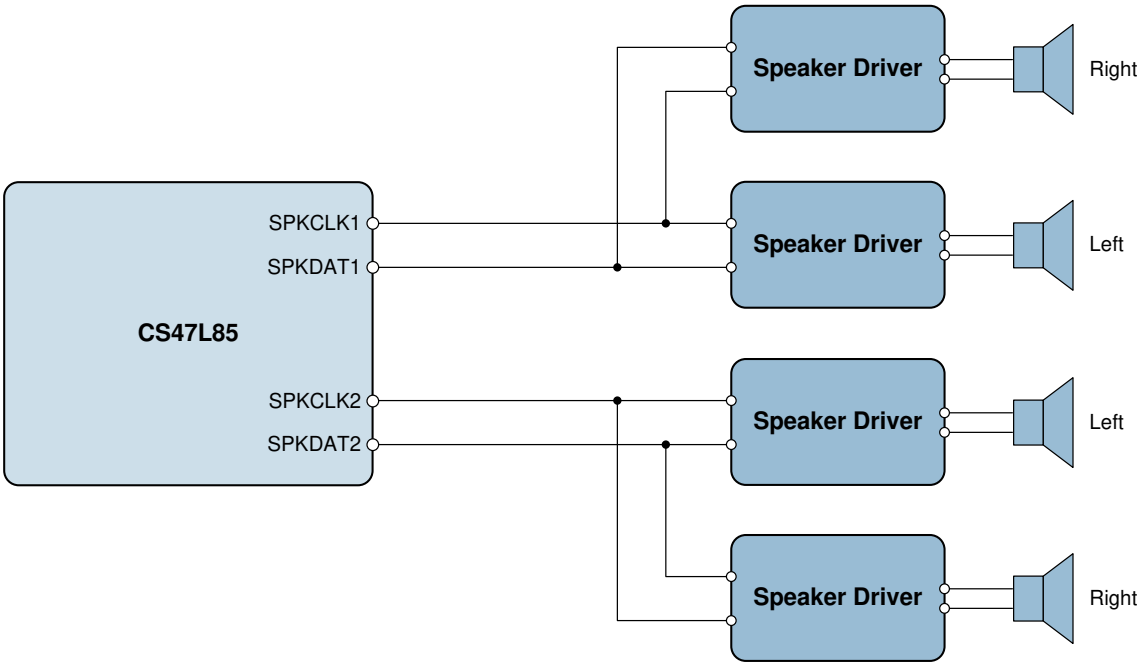


Figure 65 Digital Speaker (PDM) Connection

EXTERNAL ACCESSORY DETECTION

The CS47L85 provides external accessory detection functions which can sense the presence and impedance of external components. This can be used to detect the insertion or removal of an external headphone or headset, and to provide an indication of key/button push events.

Jack insertion is detected using the JACKDET1 and JACKDET2 pins, which must be connected to a switch contact within the jack socket(s). An Interrupt event is generated whenever a jack insertion or jack removal event is detected.

Suppression of pops and clicks caused by jack insertion or removal is provided using the MICDET clamp function. This function can also be used to trigger interrupt events, and/or to trigger the Control Write Sequencer. The integrated General Purpose Switch can be synchronised with the MICDET clamp, to provide additional pop suppression capability.

Microphones, push-buttons and other accessories can be detected via the MICDET1 or MICDET2 pins. The presence of a microphone, and the status of a hookswitch can be detected. This feature can also be used to detect push-button operation.

Headphone impedance can be detected via the HPDETL and HPDETR pins; this can be used to set different gain levels or other configuration settings according to the type of load connected. For example, different settings may be applicable to Headphone or Line output loads.

The MICVDD power domain must be enabled when using the Microphone Detect function. (Note that MICVDD is not required for the Jack Detect or Headphone Detect functions.) The MICVDD power domain is provided using an internal Charge Pump (CP2) and LDO Regulator (LDO2). See “Charge Pumps, Regulators and Voltage Reference” for details of these circuits.

The internal 32kHz clock must be present and enabled when using the Microphone Detect or Headphone Detect functions; the 32kHz clock is also required for the Jack Detect function, assuming input de-bounce is enabled. See “Clocking and Sample Rates” for details of the internal 32kHz clock and associated register control fields.

JACK DETECT

The CS47L85 provides support for jack insertion switch detection. The jack insertion status can be read using the relevant register status bits. A jack insertion or removal can also be used to trigger an interrupt (IRQ) event.

The jack detect interrupt (IRQ) functionality is maintained in Sleep mode (see “Low Power Sleep Configuration”). This enables a jack insertion event to be used to trigger a Wake-Up of the CS47L85.

Jack insertion and removal is detected using the JACKDET1 and JACKDET2 pins. The recommended external connections are illustrated in Figure 66. The logic thresholds associated with the JACKDETn pins are the same, as noted in the “Electrical Characteristics” section. Note that an external resistor (e.g., 500kΩ) connected to JACKDET2 is recommended, in order to reduce leakage current.

The jack detect feature is enabled using the JD*n*_ENA register bits (where *n* = 1 or 2 for JACKDET1 or JACKDET2 respectively); the jack insertion status can be read using the JD*n*_STSx register bits.

The jack detect input de-bounce is selected using the JD*n*_DB register bits, as described in Table 85. Note that, under normal operating conditions, the de-bounce circuit uses the 32kHz clock, which must be enabled whenever input de-bounce functions are required. Input de-bounce is not provided in Sleep mode; the JD*n*_DB register bits have no effect in Sleep mode.

Note that the Jack Detect signals, JD1 and JD2, can be used as inputs to the MICDET Clamp function. This provides additional functionality relating to jack insertion or jack removal events.

An Interrupt Request (IRQ) event is generated whenever a jack insertion or jack removal is detected (see “Interrupts”). Separate ‘mask’ bits are provided, to allow IRQ events on the rising and/or falling edges of the JD1 or JD2 signals.

The control registers associated with the Jack Detect function are described in Table 85.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R723 (02D3h) Jack_detect _analogue	1	JD2_ENA	0	JACKDET2 enable 0 = Disabled 1 = Enabled
	0	JD1_ENA	0	JACKDET1 enable 0 = Disabled 1 = Enabled
R6278 (1886h) IRQ1_Raw_ Status_7	2	JD2_STS1	0	JACKDET2 input status 0 = Jack not detected 1 = Jack is detected (Assumes the JACKDET2 pin is pulled 'low' on Jack insertion.)
	0	JD1_STS1	0	JACKDET1 input status 0 = Jack not detected 1 = Jack is detected (Assumes the JACKDET1 pin is pulled 'low' on Jack insertion.)
R6534 (1986h) IRQ2_Raw_ Status_7	2	JD2_STS2	0	JACKDET2 input status 0 = Jack not detected 1 = Jack is detected (Assumes the JACKDET2 pin is pulled 'low' on Jack insertion.)
	0	JD1_STS2	0	JACKDET1 input status 0 = Jack not detected 1 = Jack is detected (Assumes the JACKDET1 pin is pulled 'low' on Jack insertion.)
R6662 (1A06h) Interrupt_De bounce_7	2	JD2_DB	0	JACKDET2 input de-bounce 0 = Disabled 1 = Enabled
	0	JD1_DB	0	JACKDET1 input de-bounce 0 = Disabled 1 = Enabled

Table 85 Jack Detect Control

A recommended connection circuit, including headphone output on HPOUT1 and microphone connections, is shown in Figure 66. See "Applications Information" for details of recommended external components.

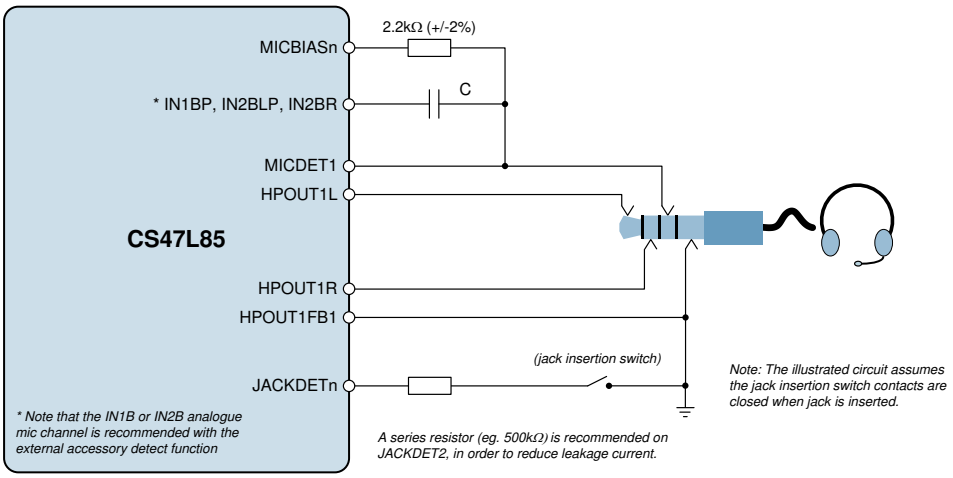


Figure 66 Jack Detect and External Accessory Connections

The internal comparator circuit used to detect the JACKDETn status is illustrated in Figure 67.

The threshold voltages for the jack detect circuit are noted in the “Electrical Characteristics”. Note that separate thresholds are defined for jack insertion and jack removal.

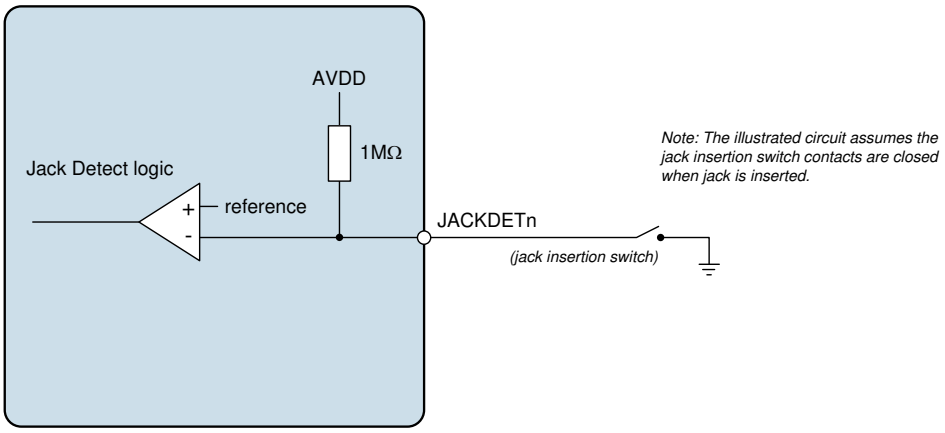


Figure 67 Jack Detect Comparator

JACK POP SUPPRESSION (MICDET CLAMP AND GP SWITCH)

Under typical configuration of a 3.5mm headphone/accessory jack connection, there is a risk of pops and clicks arising from jack insertion or removal. This can occur when the headphone load makes momentary contact with the MICBIAS output when the jack is not fully inserted, as illustrated in Figure 68.

The CS47L85 provides a MICDET Clamp function to suppress pops and clicks caused by jack insertion or removal. The clamp can be controlled directly, or can be activated by a configurable logic function derived from external logic inputs. The clamp status can be read using the relevant register status bit. The clamp status can also be used to trigger an interrupt (IRQ) event or to trigger the Control Write Sequencer.

The MICDET Clamp function can be configured using the MICD_CLAMP_MODE register field; the selectable logic conditions (derived from the JD1 and/or JD2 signals - see Table 85) provide support for different jack detect circuit configurations. The MICD_CLAMP_OVD bit, when set, will activate the MICDET Clamp, regardless of other conditions.

Note that the MICD_CLAMP_OVD bit is enabled by default; the MICDET Clamp is always active following Power-On Reset (POR), Hardware Reset, or Software Reset.

The MICDET Clamp functionality (including the external IRQ) is maintained in Sleep mode (see “Low Power Sleep Configuration”). This enables a jack insertion event to be used to trigger a Wake-Up of the CS47L85.

A summary of the Jack Detect and MICDET Clamp functionality, and their recommended usage in typical applications, is described in the next section.

When the MICDET Clamp is active, the MICDET1/HPOUT1FB2 and HPOUT1FB1/MICDET2 pins are short-circuited together. The grounding of the MICDET pin is achieved via the applicable HPOUT1FB pin; note that it is assumed that the HPOUT1FB connection is grounded externally, as shown in Figure 68.

The configurable logic provides flexibility in selecting the appropriate conditions for activating the MICDET Clamp. The clamp status can be read using the MICD_CLAMP_STS register.

The MICDET Clamp de-bounce is selected using the MICD_CLAMP_DB register, as described in Table 86. Note that, under normal operating conditions, the de-bounce circuit uses the 32kHz clock, which must be enabled whenever input de-bounce functions are required. Input de-bounce is not provided in Sleep mode; the MICD_CLAMP_DB register bit has no effect in Sleep mode.

An Interrupt Request (IRQ) event is generated whenever the MICDET Clamp is asserted or de-asserted (see “Interrupts”). Separate ‘mask’ bits are provided to enable IRQ events on the rising and/or falling edge of the MICDET Clamp status.

The Control Write Sequencer can be triggered by the MICDET Clamp status. This is enabled using the WSEQ_ENA_MICD_CLAMP_FALL and WSEQ_ENA_MICD_CLAMP_RISE register bits. See “Control Write Sequencer” for further details.

The MICDET Clamp function is illustrated in Figure 68. Note that the jack plug is shown partially removed, with the MICDET1 pin in contact with the headphone load.

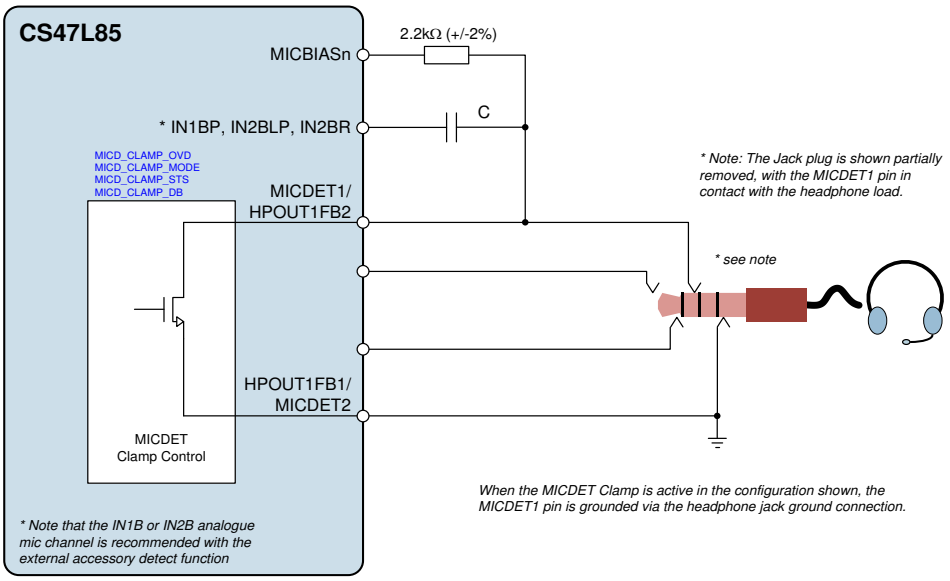


Figure 68 MICDET Clamp circuit

In applications where a large decoupling capacitance is present on the MICBIAS output, the MICDET Clamp function alone may be unable to discharge the capacitor sufficiently to eliminate pops and clicks associated with jack insertion and removal. In this case, it may be desirable to use the General Purpose Switch within the CS47L85 to provide isolation from the MICBIAS output; an example circuit is shown in Figure 69.

The General Purpose Switch is configured using SW1_MODE. This register allows the switch to be disabled, enabled, or synchronised to the MICDET Clamp status, as described in Table 86.

For jack pop suppression, it is recommended to set SW1_MODE=11. In this case, the switch contacts are open whenever the MICDET Clamp is active, and the switch contacts are closed whenever the MICDET Clamp is inactive.

Normal accessory functions are supported when the switch contacts (GPSWP and GPSWN) are closed, and the MICDET Clamp is inactive. Ground clamping of MICDET, and isolation of MICBIAS are achieved when the switch contacts are open, and the MICDET Clamp is active.

Note that the MICDET Clamp function must also be configured appropriately when using this method of pop suppression control.

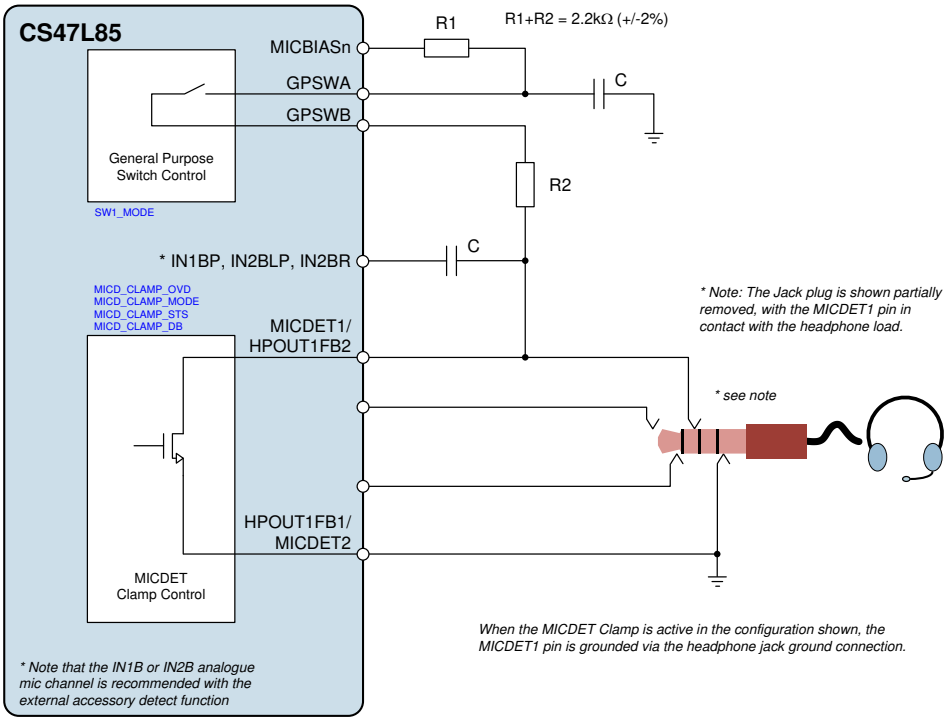


Figure 69 General Purpose Switch circuit

The control registers associated with the MICDET Clamp and General Purpose Switch functions are described in Table 86.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R65 (0041h) Sequence_control	7	WSEQ_ENA_MICD_CLAMP_FALL	0	MICDET Clamp (Falling) Write Sequencer Select 0 = Disabled 1 = Enabled
	6	WSEQ_ENA_MICD_CLAMP_RISE	0	MICDET Clamp (Rising) Write Sequencer Select 0 = Disabled 1 = Enabled
R710 (02C6h) Micd_Clamp_control	4	MICD_CLAMP_OVD	1	MICDET Clamp Override 0 = Disabled 1 = Enabled (Clamp active)
	3:0	MICD_CLAMP_MODE [3:0]	0000	MICDET Clamp Mode 0h = Disabled 1h = Active (MICDET1 and MICDET2 are shorted together) 2h = Reserved 3h = Reserved 4h = Active when JD1=0 5h = Active when JD1=1 6h = Active when JD2=0 7h = Active when JD2=1 8h = Active when JD1=0 or JD2=0 9h = Active when JD1=0 or JD2=1 Ah = Active when JD1=1 or JD2=0 Bh = Active when JD1=1 or JD2=1 Ch = Active when JD1=0 and JD2=0 Dh = Active when JD1=0 and JD2=1 Eh = Active when JD1=1 and JD2=0 Fh = Active when JD1=1 and JD2=1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R712 (02C8h) GP_Switch_1	1:0	SW1_MODE [1:0]	00	General Purpose Switch control 00 = Disabled (open) 01 = Enabled (closed) 10 = Enabled when MICDET Clamp is active 11 = Enabled when MICDET Clamp is not active
R6278 (1886h) IRQ1_Raw_Status_7	4	MICD_CLAMP_STS1	0	MICDET Clamp status 0 = Clamp not active 1 = Clamp active
R6534 (1986h) IRQ2_Raw_Status_7	4	MICD_CLAMP_STS2	0	MICDET Clamp status 0 = Clamp not active 1 = Clamp active
R6662 (1A06h) Interrupt_Debounce_7	4	MICD_CLAMP_DB	0	MICDET Clamp de-bounce 0 = Disabled 1 = Enabled

Table 86 MICDET Clamp and General Purpose Switch control

CONTROL SEQUENCE FOR JACK DETECT & MICDET CLAMP

A summary of the Jack Detect and MICDET Clamp functionality, and their recommended usage in typical applications, is described below.

On device power-up, and following reset, the MICDET Clamp will be active, due to the default setting of MICD_CLAMP_OVD; this ensures no spurious output can occur during jack insertion.

It is recommended to keep the MICDET Clamp active (MICD_CLAMP_OVD = 1) until after a jack insertion has been detected.

The MICDET_CLAMP_MODE field should be set according to the applicable JD1/JD2 signal configuration (configured to assert the clamp when jack is removed).

Jack insertion is indicated using the JD1/JD2 signals; the associated status bits can be read directly, or associated signals can be unmasked as inputs to the Interrupt controller.

After jack insertion has been detected, the applicable headset functions (headphone, microphone, accessory detect) may then be enabled.

If the headset function requires MICBIAS to be enabled on the respective jack, then the MICDET Clamp should be disabled (MICD_CLAMP_OVD = 0) immediately before enabling the MICBIAS (or immediately before enabling MICD_ENA). Note that, if MICBIAS is not required on the respective jack, then the clamp should not be disabled (e.g., for headphone-only operation).

Assuming that the MICDET_CLAMP_MODE field has been correctly set for the applicable JD1/JD2 signal configuration, the clamp controller will provide indication of a jack removal. (The status bits can be read directly, or can be unmasked as inputs to the Interrupt controller.) The clamp will also ensure fast and automatic silencing of the jack outputs.

Under typical use cases, the respective MICBIAS generator and headset audio paths should all be disabled following jack removal.

Lastly, the MICD Clamp override bit should be asserted (MICD_CLAMP_OVD = 1), to make the system ready for a jack insertion.

The recommended control sequence for Jack Detect and MICDET Clamp is summarised in Table 87.

EVENT	DEVICE ACTIONS	RECOMMENDED USER ACTIONS
Initial condition	Clamp asserted by default	Configure MICDET_CLAMP_MODE
Jack insertion	Jack insertion signalled via IRQ	**For headphone-only operation:** Enable output signal paths **For other use cases:** Disable clamp MICD_CLAMP_OVD = 0 Enable MICBIAS / MICDET Enable input / output signal paths
Jack removal	Jack removal signalled via IRQ Clamp asserted automatically	Disable MICBIAS / MICDET Disable input / output signal paths Enable clamp MICD_CLAMP_OVD = 1

Table 87 Control Sequence for Jack Detect and MICDET Clamp

MICROPHONE DETECT

The CS47L85 microphone detection circuit measures the impedance of an external load connected to one of the MICDET pins. This feature can be used to detect the presence of a microphone, and the status of the associated hookswitch. It can also be used to detect push-button status or the connection of other external accessories.

The microphone detection circuit measures the impedance connected to MICDET1 or MICDET2. In the discrete measurement mode (ACCDET_MODE=000), the function reports whether the measured impedance lies within one of 8 pre-defined levels. In the ADC measurement mode (ACCDET_MODE=111), a more specific result is provided in the form of a 7-bit ADC output.

The microphone detection circuit typically uses one of the MICBIAS outputs as a reference. The CS47L85 will automatically enable the appropriate MICBIAS when required in order to perform the detection function; this allows the detection function to be supported in low-power standby operating conditions.

Note that the MICVDD power domain must be enabled when using the microphone detection function. This power domain is provided using an internal Charge Pump (CP2) and LDO Regulator (LDO2). See “Charge Pumps, Regulators and Voltage Reference” for details of these circuits. The internal 32kHz clock must be present and enabled when using the microphone detection function: see “Clocking and Sample Rates” for details.

To select microphone detection on one of the MICDET pins, the ACCDET_MODE register must be set to 000 or 111 (depending on the desired measurement mode). The ACCDET_MODE register is defined in Table 88.

The CS47L85 can only support one headphone or microphone detection function at any time. When the detection function is not in use, it is recommended to set ACCDET_MODE=000.

The microphone detection circuit can be enabled on the MICDET1 pin or the MICDET2 pin, selected by the ACCDET_SRC register.

The microphone detection circuit uses MICVDD, MICBIAS1, MICBIAS2 or MICBIAS3 as a reference. The applicable source is configured using the MICD_BIAS_SRC register. Note that MICBIAS4 is not a valid reference source for the microphone detection function.

When ACCDET_MODE is set to 000 or 111, then Microphone detection is enabled by setting MICD_ENA.

When microphone detection is enabled, the CS47L85 performs a number of measurements in order to determine the MICDET impedance. The measurement process is repeated at a cyclic rate controlled by MICD_RATE. (The MICD_RATE register selects the delay between completion of one measurement and the start of the next.) When the microphone detection result has settled, the CS47L85 indicates valid data by setting the MICD_VALID bit.

When the discrete measurement mode is selected (ACCDET_MODE=000), the measured impedance is only deemed valid after more than one successive measurement has produced the same result. The MICD_DBTIME register provides control of the de-bounce period; this can be either 2 measurements or 4 measurements.

When the microphone detection result has settled (i.e., after the applicable de-bounce period), the CS47L85 indicates valid data by setting the MICD_VALID bit. The measured impedance is indicated using the MICD_LVL and MICD_STS register bits, as described in Table 88.

The MICD_VALID bit, when set, remains asserted for as long as the microphone detection function is enabled (i.e., while MICD_ENA = 1). If the detected impedance changes, then the MICD_LVL and MICD_STS fields will change, but the MICD_VALID bit will remain set, indicating valid data at all times.

The 8 pre-defined impedance levels (including the ‘no accessory detected’ level) allow detection of a typical microphone

and up to 6 push-buttons. Each measurement level can be enabled or disabled independently; this provides flexibility according to the required thresholds, and offers a faster measurement time in some applications. The MICD_LVL_SEL register is described in detail later in this section.

Note that the impedance levels quoted in the MICD_LVL description assume that a microphone (475Ω to 30kΩ impedance) is also present on the MICDET pin. The limits quoted in the “Electrical Characteristics” refer to the combined effective impedance on the MICDET pin. Typical external components are described in the “Applications Information” section.

When the ADC measurement mode is selected (ACCDET_MODE=111), the detection function must be disabled before the measurement can be read. When the CS47L85 indicates valid data (MICD_VALID=1), the detection must be disabled by setting MICD_ENA=0.

The ADC measurement mode generates two output results, contained within the MICDET_ADCVAL and MICDET_ADCVAL_DIFF registers. These registers contain the most recent measurement value (MICDET_ADCVAL) and the measurement difference value (MICDET_ADCVAL_DIFF). The difference value indicates the difference between the latest measurement and the previous measurement; this can be used to determine whether the measurement is stable and reliable.

Note that the MICDET_ADCVAL and MICDET_ADCVAL_DIFF registers do not follow a linear coding. The appropriate test condition for accepting the measurement value (or for re-scheduling the measurement) will vary depending on the application requirements, and depending on the expected impedance value.

The microphone detection function is an input to the Interrupt control circuit and can be used to trigger an Interrupt event every time an accessory insertion, removal or impedance change is detected. See “Interrupts” for further details.

The register fields associated with Microphone Detection (or other accessories) are described in Table 88. The external circuit configuration is illustrated in Figure 70.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R659 (0293h) Accessory_ Detect_Mode_1	13	ACCDET_SRC	0	Accessory Detect / Headphone Feedback pin select 0 = Accessory detect on MICDET1, Headphone ground feedback on HPOUT1FB1 1 = Accessory detect on MICDET2, Headphone ground feedback on HPOUT1FB2
	2:0	ACCDET_MODE [2:0]	000	Accessory Detect Mode Select 000 = Microphone detect (MICDETn, discrete mode) 001 = Headphone detect (HPDETL) 010 = Headphone detect (HPDETR) 011 = Reserved 100 = Headphone detect (MICDETn) 101 = Reserved 110 = Reserved 111 = Microphone detect (MICDETn, ADC mode) Note that the MICDETn measurements are implemented on either the MICDET1 or MICDET2 pins, depending on the ACCDET_SRC register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R675 (02A3h) Mic_Detect_1	15:12	MICD_BIAS_STARTTIME [3:0]	0001	Mic Detect Bias Startup Delay (If MICBIAS is not enabled already, this field selects the delay time allowed for MICBIAS to startup prior to performing the MICDET function.) 0000 = 0ms (continuous) 0001 = 0.25ms 0010 = 0.5ms 0011 = 1ms 0100 = 2ms 0101 = 4ms 0110 = 8ms 0111 = 16ms 1000 = 32ms 1001 = 64ms 1010 = 128ms 1011 = 256ms 1100 to 1111 = 512ms
	11:8	MICD_RATE [3:0]	0001	Mic Detect Rate (Selects the delay between successive MICDET measurements.) 0000 = 0ms (continuous) 0001 = 0.25ms 0010 = 0.5ms 0011 = 1ms 0100 = 2ms 0101 = 4ms 0110 = 8ms 0111 = 16ms 1000 = 32ms 1001 = 64ms 1010 = 128ms 1011 = 256ms 1100 to 1111 = 512ms
	6:4	MICD_BIAS_SRC [2:0]	000	Accessory Detect (MICDET) reference select 000 = MICVDD 001 = MICBIAS1 010 = MICBIAS2 011 = MICBIAS3 All other codes are Reserved
	1	MICD_DBTIME	1	Mic Detect De-bounce 0 = 2 measurements 1 = 4 measurements Only valid when ACCDET_MODE=000.
	0	MICD_ENA	0	Mic Detect Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R676 (02A4h) Mic_Detect_2	7:0	MICD_LVL_SEL [7:0]	1001_1111	Mic Detect Level Select (enables Mic/Accessory Detection in specific impedance ranges) [7] = Enable >475 ohm detection [6] = Not used - must be set to 0 [5] = Not used - must be set to 0 [4] = Enable 375 ohm detection [3] = Enable 155 ohm detection [2] = Enable 73 ohm detection [1] = Enable 40 ohm detection [0] = Enable 18 ohm detection Note that the impedance values quoted assume that a microphone (475ohm-30kohm) is also present on the MICDET pin. Only valid when ACCDET_MODE=000.
R677 (02A5h) Mic_Detect_3	10:2	MICD_LVL [8:0]	0_0000_0000	Mic Detect Level (indicates the measured impedance) [8] = >475 ohm, <30k ohm [7] = Not used [6] = Not used [5] = 375 ohm [4] = 155 ohm [3] = 73 ohm [2] = 40 ohm [1] = 18 ohm [0] = <3 ohm Note that the impedance values quoted assume that a microphone (475ohm-30kohm) is also present on the MICDET pin. Only valid when ACCDET_MODE=000.
	1	MICD_VALID	0	Mic Detect Data Valid 0 = Not Valid 1 = Valid
	0	MICD_STS	0	Mic Detect Status 0 = No Mic/Accessory present (impedance is >30k ohm) 1 = Mic/Accessory is present (impedance is <30k ohm) Only valid when ACCDET_MODE=000.
R683 02ABh Mic_Detect_4	15:8	MICDET_ADCVAL_DIFF [7:0]	00h	Mic Detect ADC Level (Difference) Only valid when ACCDET_MODE=111.
	6:0	MICDET_ADCVAL [6:0]	00h	Mic Detect ADC Level Only valid when ACCDET_MODE=111.

Table 88 Microphone Detect Control

The external connections for the Microphone Detect circuit are illustrated in Figure 70. In typical applications, it can be used to detect a microphone or button press.

Note that, when using the Microphone Detect circuit, it is recommended to use the IN1B or IN2B analogue microphone input paths, to ensure best immunity to electrical transients arising from the external accessory.

The voltage reference for the microphone detection is configured using the MICD_BIAS_SRC register, as described in Table 88. The microphone detection function will automatically enable the applicable reference when required for MICDET impedance measurement.

If the selected reference (MICBIAS*n*) is not already enabled (i.e., if MICB*n*_ENA = 0, where *n* is 1, 2, 3 or 4 as appropriate), then the applicable MICBIAS source will be enabled for short periods of time only, every time the impedance measurement is scheduled. To allow time for the MICBIAS source to start-up, a time delay is applied before the measurement is performed; this is configured using the MICD_BIAS_STARTTIME register, as described in Table 88.

The MICD_BIAS_STARTTIME register should be set to 16ms or more if MICB*n*_RATE = 1 (pop-free start-up / shut-down).
The MICD_BIAS_STARTTIME register should be set to 0.25ms or more if MICB*n*_RATE = 0 (fast start-up / shut-down).

If the selected reference is not enabled continuously (i.e., if MICB*n*_ENA = 0), then the applicable MICBIAS discharge bit (MICB*n*_DISCH) should be set to 0.

The MICBIAS sources are configured using the registers described in the "Charge Pumps, Regulators and Voltage Reference" section.

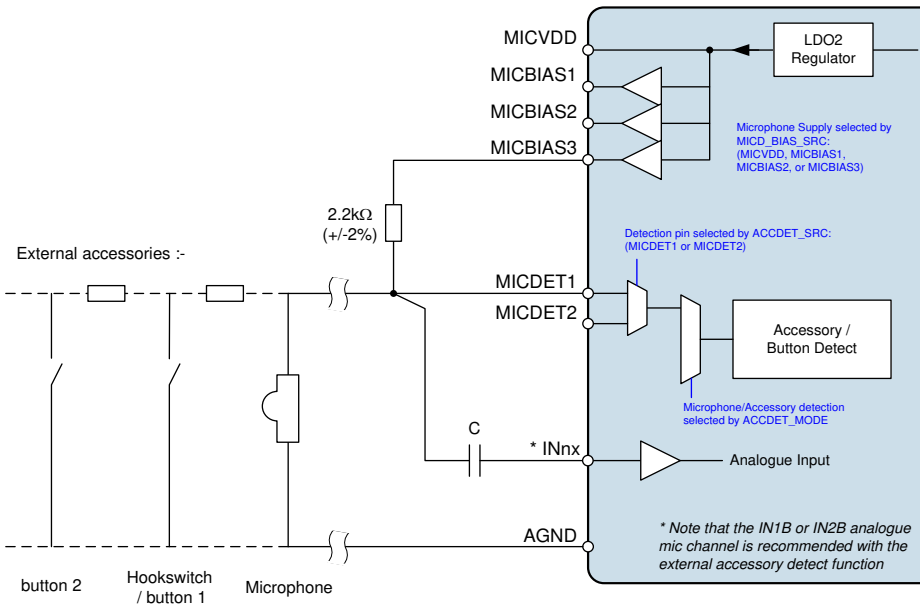


Figure 70 Microphone and Accessory Detect Interface

When the discrete measurement mode is selected (ACCDET_MODE=000), the MICD_LVL_SEL [7:0] register bits allow each of the impedance measurement levels to be enabled or disabled independently. This allows the function to be tailored to the particular application requirements.

If one or more bits within the MICD_LVL_SEL register is set to 0, then the corresponding impedance level will be disabled. Any measured impedance which lies in a disabled level will be reported as the next lowest, enabled level.

For example, the MICD_LVL_SEL [2] bit enables the detection of impedances around 73Ω. If MICD_LVL_SEL [2] = 0, then an external impedance of 73Ω will not be indicated as 73Ω but will be indicated as 40Ω; this would be reported in the MICD_LVL register as MICD_LVL [2] = 1.

With all measurement levels enabled, the CS47L85 can detect the presence of a typical microphone and up to 6 push-buttons. The microphone detect function is specifically designed to detect a video accessory (typical 75Ω) load if required.

See "Applications Information" for typical recommended external components for microphone, video or push-button accessory detection.

The accuracy of the microphone detect function is assured whenever the connected load is within the applicable limits specified in the "Electrical Characteristics". It is required that a 2.2kΩ (2%) resistor must also be connected between MICDET and the selected MICBIAS reference; note that different resistor values will lead to inaccuracy in the impedance measurement.

Note that the connection of a microphone will change the measured impedance on the MICDET pin; see "Applications Information" for recommended components for typical applications.

The measurement time varies between 100µs and 500µs according to the impedance of the external load. A high impedance will be measured faster than a low impedance.

The timing of the microphone detect function is illustrated in Figure 71. Two different cases are shown, according to whether MICBIAS*n* is enabled periodically by the impedance measurement function (MICB*n*_ENA=0), or is enabled at all times (MICB*n*_ENA=1).

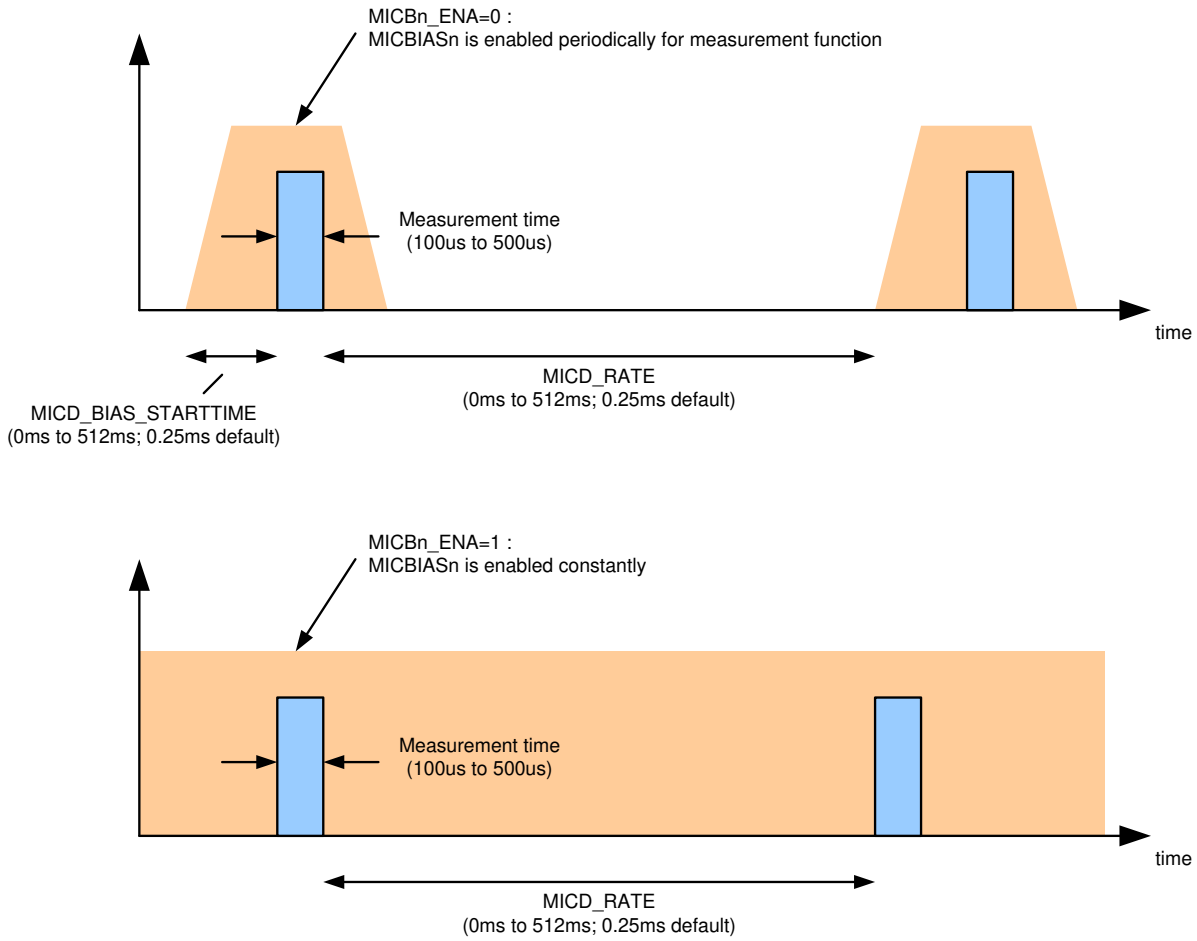


Figure 71 Microphone and Accessory Detect Timing

HEADPHONE DETECT

The CS47L85 headphone detection circuit measures the impedance of an external headphone load. This feature can be used to set different gain levels or to apply other configuration settings according to the type of load connected. Separate monitor pins are provided for headphone detection on the left and right channels of HPOUT1.

Headphone detection can be enabled on the HPDETL pin or the HPDETR pin. Under recommended configuration, these pins provide measurement of the HPOUT1L and HPOUT1R loads respectively.

The headphone detect function can also be enabled on the MICDET1 pin or the MICDET2 pin. Note that, in this configuration, any MICBIAS output that is connected to the selected MICDET pin must be disabled and floating (MICBn_ENA=0, MICBn_DISCH=0).

The applicable headphone detection pin is selected using the ACCDET_MODE register. When MICDETn is selected (ACCDET_MODE=100), the applicable MICDETn pin is determined by the ACCDET_SRC register, as described in Table 91.

The CS47L85 can only support one headphone or microphone detection function at any time. When the detection function is not in use, it is recommended to set ACCDET_MODE=000.

Headphone detection on the selected channel is commanded by writing a ‘1’ to the HP_POLL register bit. The impedance measurement range is configured using the HP_IMPEDANCE_RANGE register. This register should be set in accordance with the expected load impedance.

Note that a number of separate measurements (for different impedance ranges) are typically required in order to determine the load impedance; the recommended control sequence is described below.

Note that setting the HP_IMPEDANCE_RANGE register is not required for detection on the MICDETn pins (ACCDET_MODE=100). Note also that the impedance measurement range, and measurement accuracy, in this mode are different to the HPDETL and HPDETR measurement modes.

For correct operation, the respective output driver(s) must be disabled when headphone detection is commanded on HPOUT1L or HPOUT1R. The required register settings are shown in Table 89.

See Table 71 for details of the HP1L_ENA and HP1R_ENA register bits. The applicable headphone output(s) configuration must be maintained until after the headphone detection has completed.

DESCRIPTION	REQUIREMENT
HPOUT1L Impedance measurement	HP1L_ENA = 0
HPOUT1R Impedance measurement	HP1R_ENA = 0

Table 89 Output Configuration for Headphone Detect

When headphone detection is commanded, the CS47L85 uses an adjustable current source to determine the connected impedance. A sweep of measurement currents is applied. The rate of this sweep can be adjusted using the HP_CLK_DIV and HP_RATE registers.

The headphone detection process will typically comprise a number of separate measurements (for different impedance ranges). Completion of each measurement is indicated by the HP_DONE register bit. When this bit is set, the measurement result can be read from the HP_DACVAL and HP_DACVAL_DOWN fields, and subsequently decoded as described below.

$$\text{Impedance } (\Omega) = \frac{C_0 + (C_1 \times \mathit{Offset})}{\left[\frac{(((\text{HP\_DACVAL} + \text{HP\_DACVAL\_DOWN}) / 2) + 0.5)}{C_2}\right] - \left[\frac{1}{C_3\,(1 + (C_4 \times \mathit{Gradient}))}\right]} - C_5$$

The associated parameters for decoding the measurement result are defined in Table 90. The applicable values are dependent on the HP_IMPEDANCE_RANGE setting in each case. The 'Offset' and 'Gradient' values are derived from register fields which are factory-calibrated for each device.

PARAMETER	HP_IMPEDANCE_ RANGE=00	HP_IMPEDANCE_ RANGE=01	HP_IMPEDANCE_ RANGE=10	HP_IMPEDANCE_ RANGE=11
C_0	1.007	1.007	9.696	100.684
C_1	-0.0072	-0.0072	-0.0795	-0.9494
C_2	4003	7975	7300	7300
C_3	69.3	69.6	62.9	63.2
C_4	0.0055	0.0055	0.0055	0.0055
C_5	0.25	0.25	0.25	0.25
Offset	HP_OFFSET_00	HP_OFFSET_01	HP_OFFSET_10	HP_OFFSET_11
Gradient	HP_GRADIENT_0X	HP_GRADIENT_0X	HP_GRADIENT_1X	HP_GRADIENT_1X

Table 90 Headphone Measurement Decode parameters

Note that, to achieve the specified measurement accuracy, the above equation must be calculated to an accuracy of at least 5 decimal places throughout.

The impedance measurement result is valid when 169 ≤ HP_DACVAL ≤ 1019. (In case of any contradiction with the HP_IMPEDANCE_RANGE description, the HP_DACVAL validity takes precedence.)

If the external impedance is entirely unknown (i.e., it could lie in any of the HP_IMPEDANCE_RANGE regions), then it is recommended to test initially with HP_IMPEDANCE_RANGE=00. If the resultant HP_DACVAL is < 169, then the impedance is higher than the selected measurement range, so the test should be scheduled again, after incrementing HP_IMPEDANCE_RANGE.

Each measurement is triggered by writing '1' to the HP_POLL bit. Completion of each measurement is indicated by the HP_DONE register bit. Note that, after the HP_DONE bit has been asserted, it will remain asserted until the next measurement has been commanded.

A simpler, but less accurate, procedure for headphone impedance measurement is also supported, using the HP_LVL

register. When the HP_DONE bit is set, indicating completion of a measurement, the impedance can be read directly from the HP_LVL field, provided that the value lies within the range of the applicable HP_IMPEDANCE_RANGE setting.

Note that, for detection using one of the MICDETn pins, the HP_LVL field is the only supported readback option. The HP_IMPEDANCE_RANGE field is not valid for detection on the MICDETn pins. See Table 91 for further description of the HP_LVL field.

The headphone detection function is an input to the Interrupt control circuit and can be used to trigger an Interrupt event on completion of the headphone detection - see “Interrupts”.

The register fields associated with Headphone Detection are described in Table 91. The external circuit configuration is illustrated in Figure 72.

Note that 32-bit register addressing is used from R12888 (3000h) upwards; 16-bit format is used otherwise. The registers noted in Table 91 contain a mixture of 16-bit and 32-bit register addresses.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R13304 (33F8h) OTP_HPDET_Cal_1	31:24	HP_OFFSET_11 [7:0]		Headphone Detect Calibration field. Signed number, LSB=0.25. Range is -31.75 to +31.75. Default value is factory-set per device.
	23:16	HP_OFFSET_10 [7:0]		Headphone Detect Calibration field. Signed number, LSB=0.25. Range is -31.75 to +31.75. Default value is factory-set per device.
	15:8	HP_OFFSET_01 [7:0]		Headphone Detect Calibration field. Signed number, LSB=0.25. Range is -31.75 to +31.75. Default value is factory-set per device.
	7:0	HP_OFFSET_00 [7:0]		Headphone Detect Calibration field. Signed number, LSB=0.25. Range is -31.75 to +31.75. Default value is factory-set per device.
R13306 (33FAh) OTP_HPDET_Cal_2	15:8	HP_GRADIENT_1X [7:0]		Headphone Detect Calibration field. Signed number, LSB=0.25. Range is -31.75 to +31.75. Default value is factory-set per device.
	7:0	HP_GRADIENT_0X [7:0]		Headphone Detect Calibration field. Signed number, LSB=0.25. Range is -31.75 to +31.75. Default value is factory-set per device.
R659 (0293h) Accessory_Detect_Mode_1	13	ACCDET_SRC	0	Accessory Detect / Headphone Feedback pin select 0 = Accessory detect on MICDET1, Headphone ground feedback on HPOUT1FB1 1 = Accessory detect on MICDET2, Headphone ground feedback on HPOUT1FB2
	2:0	ACCDET_MODE [2:0]	00	Accessory Detect Mode Select 000 = Microphone detect (MICDETn, discrete mode) 001 = Headphone detect (HPDETL) 010 = Headphone detect (HPDETR) 011 = Reserved 100 = Headphone detect (MICDETn) 101 = Reserved 110 = Reserved 111 = Microphone detect (MICDETn, ADC mode) Note that the MICDETn measurements are implemented on either the MICDET1 or MICDET2 pins, depending on the ACCDET_SRC register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R667 (029Bh) Headphone _Detect_1	10:9	HP_IMPEDANCE _RANGE [1:0]	00	Headphone Detect Range 00 = 4 ohms to 30 ohms 01 = 8 ohms to 100 ohms 10 = 100 ohms to 1k ohms 11 = 1k ohms to 10k ohms Only valid when ACCDET_MODE=001 or ACCDET_MODE=010.
	4:3	HP_CLK_DIV [1:0]	00	Headphone Detect Clock Rate (Selects the clocking rate of the headphone detect adjustable current source. Decreasing the clock rate will give a slower measurement time.) 00 = 32kHz 01 = 16kHz 10 = 8kHz 11 = 4kHz
	2:1	HP_RATE [1:0]	00	Headphone Detect Sweep Rate (Selects the step size between successive measurements. Increasing the step size will give a faster measurement time.) 00 = 1 01 = 2 10 = 4 11 = Reserved
	0	HP_POLL	0	Headphone Detect Enable Write 1 to start HP Detect function
R668 (029Ch) Headphone _Detect_2	15	HP_DONE	0	Headphone Detect Status 0 = HP Detect not complete 1 = HP Detect done
	14:0	HP_LVL [14:0]	0000h	Headphone Detect Level LSB = 0.5ohm 8 = 4ohm or less 9 = 4.5 ohm 10 = 5 ohm 11 = 5.5 ohm …. 20,000 = 10k ohm or more When ACCDET_MODE=001 or 010, this field is valid from 4ohm to10k ohm. When ACCDET_MODE=100, this field is valid from 400ohm to 6k ohm. Note that, when ACCDET_MODE=001 or 010, the HP_LVL readback is only valid within the range selected by HP_IMPEDANCE_RANGE. If HP_LVL reports a value outside the selected range, then the range should be adjusted and the measurement repeated. A result of 0 ohms may be reported if the measurement is less than the minimum value for the selected range.
R669 (029Dh) Headphone _Detect_3	9:0	HP_DACVAL [9:0]	000h	Headphone Detect Level (Coded as integer, LSB=1. See separate description for full decode information.)
R671 (029Fh) Headphone _Detect_5	9:0	HP_DACVAL_DO WN [9:0]	000h	Headphone Detect Level (Coded as integer, LSB=1. See separate description for full decode information.)

Table 91 Headphone Detect Control

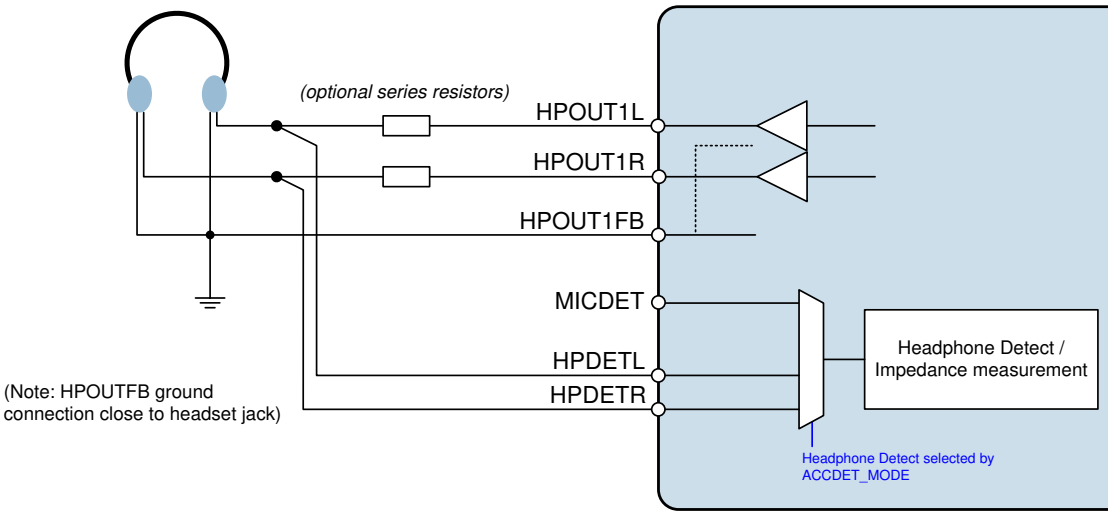


Figure 72 Headphone Detect Interface

The external connections for the Headphone Detect circuit are illustrated in Figure 72. Note that only the HPOUT1L or HPOUT1R headphone outputs should be connected to HPDETL or HPDETR pins - impedance measurement is not supported on HPOUT2L, HPOUT2R, HPOUT3L or HPOUT3R.

Note that, where external resistors are connected in series with the headphone load, as illustrated, it is recommended that the HPDET*n* connection is to the headphone side of the resistors. If the HPDET*n* connection is made to the CS47L85 'end' of these resistors, this will lead to a corresponding offset in the measured impedance.

Under default conditions, the measurement time varies between 17ms and 244ms, depending on the impedance of the external load. A high impedance will be measured faster than a low impedance.

LOW POWER SLEEP CONFIGURATION

The CS47L85 supports a low-power 'Sleep' mode, where most functions are disabled, and power consumption is minimised.

The CS47L85 enters Sleep mode when the DCVDD supply is removed. In a typical application, this is controlled via the LDOENA pin, which enables/disables the LDO1 regulator, thus enabling/disabling the DCVDD supply.

Whilst in the Sleep mode, the CS47L85 can generate an Interrupt Event in response to a change in voltage on the JACKDET1 or JACKDET2 pins. This enables a jack insertion event (or other digital logic transition) to be used to trigger a Wake-Up of the CS47L85.

Note that the AVDD, DBVDD1 supplies must be present throughout the Sleep mode duration. When LDO1 is used to provide the DCVDD supply, then LDOVDD must also be present in Sleep mode.

The system clocks (SYSCLK, ASYNCCLK, DSPCLK) should each be disabled before selecting Sleep mode. The external clock input (MCLKn) may also be stopped, if desired.

Access to the CS47L85 register map using any of the Control Interfaces should be ceased before selecting Sleep mode.

Selected functions and control registers are maintained via an 'Always-On' internal supply domain in Sleep mode. The 'Always-On' control registers are listed in Table 92. These registers are maintained (i.e., not reset) in Sleep mode.

Note that the Control Interface is not supported in Sleep mode. Read/Write access to the 'Always-On' registers is not possible in Sleep mode.

REGISTER ADDRESS	LABEL	REFERENCE
R710 (02C6h)	MICD_CLAMP_OVD	See "External Accessory Detection"
	MICD_CLAMP_MODE [3:0]	
R723 (02D3h)	JD2_ENA	
	JD1_ENA	
R6150 (1806h)	MICD_CLAMP_FALL_EINT1	See "Interrupts"
	MICD_CLAMP_RISE_EINT1	
	JD2_FALL_EINT1	
	JD2_RISE_EINT1	
	JD1_FALL_EINT1	
	JD1_RISE_EINT1	
R6214 (1846h)	IM_MICD_CLAMP_FALL_EINT1	
	IM_MICD_CLAMP_RISE_EINT1	
	IM_JD2_FALL_EINT1	
	IM_JD2_RISE_EINT1	
	IM_JD1_FALL_EINT1	
	IM_JD1_RISE_EINT1	
R6784 (1A80h)	IM_IRQ1	
	IRQ_POL	
	IRQ_OP_CFG	
R6864 (1AD0h)	RESET_PU	See "Hardware Reset, Software Reset, Wake-Up, and Device ID"
	RESET_PD	

Table 92 Sleep Mode 'Always-On' Control Registers

The ‘Always-On’ digital input / output pins are listed in Table 93. All other digital input pins have no effect in Sleep mode; all other digital output pins are undriven (floating).

The IRQ output is normally de-asserted in Sleep mode. Note that, in Sleep mode, the IRQ output can only be asserted in response to the JACKDET1 or JACKDET2 inputs, as described below. If the IRQ output is asserted in Sleep mode, it can only be de-asserted after a Wake-Up transition.

Output drivers and bus keepers are disabled in Sleep Mode, for all pins not on the always-on domain; this means that the logic level on these pins is undefined. If a defined logic level is required during Sleep Mode (e.g., as input to another device), an external pull resistor may be required. If an external pull resistor is connected to a pin that also supports a bus keeper function, the pull resistance should be chosen carefully, taking into account the resistance of the bus keeper. See “General Purpose Input / Output” for specific notes concerning the GPIO pins.

PIN NAME	DESCRIPTION	REFERENCE
IRQ	Interrupt Request (IRQ) output	See “Interrupts”
JACKDET1	Jack Detect input 1	See “External Accessory Detection”
JACKDET2	Jack Detect input 2	See “External Accessory Detection”
LDOENA	Enable pin for LDO1	See “Charge Pumps, Regulators and Voltage Reference”
RESET	Digital Reset input (active low)	See “Hardware Reset, Software Reset, Wake-Up, and Device ID”

Table 93 Sleep Mode ‘Always-On’ Digital Input Pins

The ‘Always-On’ functionality includes the JD1 and JD2 control signals, which provide support for the low-power Sleep mode. The MICDET Clamp status signal is also supported; this is controlled by a selectable logic function, derived from JD1 and/or JD2.

The JD1, JD2 and MICDET Clamp status signals are derived from the JACKDET1 and JACKDET2 inputs, and can be used to trigger the Interrupt Controller.

The Interrupt (IRQ) functionality associated with these signals is part of the ‘Always-On’ functionality, enabling the CS47L85 to provide indication of jack insertion or jack removal to the host processor in Sleep mode. See “Interrupts” for further details.

Note that the JACKDET1 and JACKDET2 inputs will not result in a Wake-Up transition directly; a Wake-Up transition will only occur by re-application of DCVDD. In a typical application, the JACKDETn inputs will provide a signal to the Applications Processor, via the IRQ output; if a Wake-Up transition is required, this is triggered by the Applications Processor asserting the LDOENA pin.

The JD1 and JD2 signals are derived from the Jack Detect function (see “External Accessory Detection”). These inputs can be used to trigger a response to a jack insertion or jack removal detection.

When these signals are enabled, the JD1 and JD2 signals indicate the status of the JACKDET1 and JACKDET2 input pins respectively. See Table 85 for details of the associated control registers.

The MICDET Clamp status is controlled by the JD1 and/or JD2 signals (see “External Accessory Detection”). The configurable logic provides flexibility in selecting the appropriate conditions for activating the MICDET Clamp. The clamp status can be used to trigger a response to a jack insertion or jack removal detection.

The MICDET Clamp function is configured using the MICD_CLAMP_MODE register, as described in Table 86.

GENERAL PURPOSE INPUT / OUTPUT

The CS47L85 provides a number of GPIO functions to enable interfacing and detection of external hardware and to provide logic outputs to other devices. The GPIO input functions can be used to generate an Interrupt (IRQ) event. The GPIO and Interrupt circuits support the following functions:

- Pin-specific alternative functions for external interfaces (AIF, DMIC, PDM, MIF)
- Logic input / Button detect (GPIO input)
- Logic '1' and logic '0' output (GPIO output)
- Interrupt (IRQ) status output
- Clock output
- Frequency Locked Loop (FLL) status output
- Frequency Locked Loop (FLL) Clock output
- IEC-60958-3 compatible S/PDIF output
- Pulse Width Modulation (PWM) Signal output
- Asynchronous Sample Rate Converter (ASRC) Lock status
- Over-Temperature, Speaker Short Circuit Protection, and Speaker Shutdown status output
- General Purpose Timer status output
- Event Logger FIFO buffer status output

Note that the GPIO pins are referenced to different power domains (DBVDD1, DBVDD2, DBVDD3 or DBVDD4), as noted in the "Pin Description" section.

Logic input and output (GPIO) can be supported in two different ways on the CS47L85. The 'standard' mechanism described in this section provides a comprehensive suite of options including input de-bounce, and selectable output drive configuration. The 'DSP GPIO' circuit is tailored towards more advanced requirements typically demanded by DSP software features. The DSP GPIO functions are described in the "DSP Peripheral Control" section.

The CS47L85 also incorporates a General Purpose Switch feature, which can be used as a controllable analogue switch; details of this are provided at the end of this "General Purpose Input / Output" section.

GPIO CONTROL

For each GPIO, the selected function is determined by the GP*n*_FN field, where n identifies the GPIO pin (1 to 40). The pin direction, set by GP*n*_DIR, must be set according to function selected by GP*n*_FN.

When a pin is configured as a GPIO input (GP*n*_DIR = 1, GP*n*_FN = 001h), the logic level at the pin can be read from the respective GP*n*_LVL bit. Note that GP*n*_LVL is not affected by the GP*n*_POL bit.

A de-bounce circuit can be enabled on any GPIO input, to avoid false event triggers. This is enabled on each pin by setting the respective GP*n*_DB bit. The de-bounce circuit uses the 32kHz clock, which must be enabled whenever input de-bounce functions are required. The de-bounce time is configurable using the GP_DBTIME register. See "Clocking and Sample Rates" for further details of the CS47L85 clocking configuration.

Each of the GPIO pins is an input to the Interrupt control circuit and can be used to trigger an Interrupt event. An interrupt event is triggered on the rising and falling edges of the GPIO input. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See "Interrupts" for more details of the Interrupt event handling.

Integrated pull-up and pull-down resistors are provided on each of the GPIO pins; these can be configured independently using the GP*n*_PU and GP*n*_PD fields. When the pull-up and pull-down control bits are both enabled, the CS47L85 provides a 'bus keeper' function on the respective pin. The bus keeper function holds the logic level unchanged whenever the pin is undriven (e.g., if the signal is tri-stated).

Note that the bus keeper is enabled by default on all GPIO pins and, if not actively driven, may result in either a logic 0 or logic 1 at the respective input on start-up. If an external pull resistor is connected (e.g., to control the logic level in Sleep Mode), the chosen resistance should take account of the bus keeper resistance (see "Electrical Characteristics"). A 'strong' pull resistor (e.g., 10kΩ) is required, if a specific start-up condition is to be forced by the external pull component.

When a pin is configured as a GPIO output (GP*n*_DIR = 0, GP*n*_FN = 001h), its level can be set to logic 0 or logic 1 using the GP*n*_LVL field. Note that the GP*n*_LVL registers are 'write only' when the respective GPIO pin is configured as an output.

When a pin is configured as an output (GP*n*_DIR = 0), the polarity can be inverted using the GP*n*_POL bit. When

GP*n*_POL = 1, then the selected output function is inverted. In the case of Logic Level output (GP*n*_FN = 001h), the external output will be the opposite logic level to GP*n*_LVL when GP*n*_POL = 1. Note that, if GPn_FN=000h or 002h, then the GP*n*_POL bit has no effect on the respective GPIO pin.

A GPIO output can be either CMOS driven or Open Drain. This is selected on each pin using the respective GP*n*_OP_CFG bit. Note that, if GPn_FN=000h or 002h, then the GP*n*_OP_CFG bit has no effect on the respective GPIO pin; see Pin Description" for the output configuration in this case.

The register fields that control the GPIO pins are described in Table 94.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5888 (1700h) GPIO1_CTRL_1 to R5966 (174Eh) GPIO40_CTRL_1	15	GPn_LVL	see notes	GPIOn level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. For output functions only, when GPn_POL is set, the register is the opposite logic level to the external pin. Note that the GP*n*_LVL register is 'write only' when GP*n*_DIR=0.
	14	GPn_OP_CFG	0	GPIOn Output Configuration 0 = CMOS 1 = Open Drain Note that, if GPn_FN=000h or 002h, then this bit has no effect on the GPIOn output.
	13	GPn_DB	1	GPIOn Input De-bounce 0 = Disabled 1 = Enabled
	12	GPn_POL	0	GPIOn Output Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low) Note that, if GPn_FN=000h or 002h, then this bit has no effect on the GPIOn output.
	8:0	GPn_FN [8:0]	001h	GPIOn Pin Function (see Table 95 for details)
R5889 (1701h) GPIO1_CTRL_2 to R5967 (174Fh) GPIO40_CTRL_2	15	GPn_DIR	1	GPIOn Pin Direction 0 = Output 1 = Input The GPn_DIR bit has no effect if GPn_FN=000h or 002h If GPn_FN=000h, then the pin direction is selected by the applicable pin-specific function. If GPn_FN=002h, then the pin direction is set according to the DSP GPIO configuration.
	14	GPn_PU	1	GPIOn Pull-Up Enable 0 = Disabled 1 = Enabled Note - when GPn_PD and GPn_PU are both set to '1', then a 'bus keeper' function is enabled on the respective GPIOn pin.
	13	GPn_PD	1	GPIOn Pull-Down Enable 0 = Disabled 1 = Enabled Note - when GPn_PD and GPn_PU are both set to '1', then a 'bus keeper' function is enabled on the respective GPIOn pin.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6848 (1AC0h) GPIO_Debounce_Config	3:0	GP_DBTIME [3:0]	0000	GPIO Input de-bounce time 0h = 100us 1h = 1.5ms 2h = 3ms 3h = 6ms 4h = 12ms 5h = 24ms 6h = 48ms 7h = 96ms 8h = 192ms 9h = 384ms Ah = 768ms Bh to Fh = Reserved
Notes: 1. *n* is a number (1 to 40) that identifies the individual GPIO. 2. The default value of GP*n*_LVL depends upon whether the pin is actively driven by another device. If the pin is actively driven, the bus-keeper will maintain this logic level. If the pin is not actively driven, the bus-keeper may establish either a logic 1 or logic 0 as the initial input level.				

Table 94 GPIO Control

GPIO FUNCTION SELECT

The available GPIO functions are described in Table 95.

The function of each GPIO is set using the GP*n*_FN register, where n identifies the GPIO pin (1 to 40). Note that the respective GP*n*_DIR must also be set according to whether the function is an input or output.

GPn_FN	DESCRIPTION	COMMENTS
000h	Pin-specific alternate function	Alternate functions supporting Digital Microphone, Digital Audio Interface, Master Control Interface, and PDM output functions.
001h	Button detect input / Logic level output	GPn_DIR = 0: GPIO pin logic level is set by GPn_LVL. GPn_DIR = 1: Button detect or logic level input.
002h	DSP GPIO	Low latency input/output for DSP functions.
003h	IRQ1 Output	Interrupt (IRQ1) output 0 = IRQ1 not asserted 1 = IRQ1 asserted
004h	IRQ2 Output	Interrupt (IRQ2) output 0 = IRQ2 not asserted 1 = IRQ2 asserted
010h	FLL1 Clock	Clock output from FLL1
011h	FLL2 Clock	Clock output from FLL2
012h	FLL3 Clock	Clock output from FLL3
018h	FLL1 Lock	Indicates FLL1 Lock status 0 = Not locked 1 = Locked
019h	FLL2 Lock	Indicates FLL2 Lock status 0 = Not locked 1 = Locked
01Ah	FLL3 Lock	Indicates FLL3 Lock status 0 = Not locked 1 = Locked

GPn_FN	DESCRIPTION	COMMENTS
040h	OPCLK Clock Output	Configurable clock output derived from SYSCLK
041h	OPCLK Async Clock Output	Configurable clock output derived from ASYNCCLK
048h	PWM1 Output	Configurable Pulse Width Modulation output PWM1
049h	PWM2 Output	Configurable Pulse Width Modulation output PWM2
04Ch	S/PDIF Output	IEC-60958-3 compatible S/PDIF output
088h	ASRC1 IN1 Lock	Indicates ASRC1 IN1 Lock status (ASRC IN1 paths convert from the SYSCLK domain to the ASYCNCLK domain.) 0 = Not locked 1 = Locked
089h	ASRC1 IN2 Lock	Indicates ASRC1 IN2 Lock status (ASRC IN2 paths convert from the ASYNCCLK domain to the SYSCLK domain.) 0 = Not locked 1 = Locked
08Ah	ASRC2 IN1 Lock	Indicates ASRC2 IN1 Lock status (ASRC IN1 paths convert from the SYSCLK domain to the ASYCNCLK domain.) 0 = Not locked 1 = Locked
08Bh	ASRC2 IN2 Lock	Indicates ASRC2 IN2Lock status (ASRC IN2 paths convert from the ASYNCCLK domain to the SYSCLK domain.) 0 = Not locked 1 = Locked
0A0h	DSP IRQ1 Flag	DSP Status flag (DSP_IRQn) output A short pulse is output whenever the respective DSP_IRQn_EINTx interrupt is triggered.
0B6h	SPKOUTL Short Circuit Status	SPKOUTL Short Circuit status 0 = Normal 1 = Short Circuit detected
0B7h	SPKOUTR Short Circuit Status	SPKOUTR Short Circuit status 0 = Normal 1 = Short Circuit detected
0E0h	Speaker Shutdown Status	Speaker Shutdown Status 0 = Normal 1 = Speaker Shutdown completed (due to Overheat Temperature, Short Circuit protection, or General Purpose Timer condition)
0E1h	Speaker Overheat Shutdown	Indicates Shutdown Temperature status 0 = Temperature is below shutdown level 1 = Temperature is above shutdown level
0E2h	Speaker Overheat Warning	Indicates Warning Temperature status 0 = Temperature is below warning level 1 = Temperature is above warning level

GPn_FN	DESCRIPTION	COMMENTS
140h	Timer 1 Status	Timer n Status A pulse is output after the respective Timer reaches its final count value.
141h	Timer 2 Status	
142h	Timer 3 Status	
143h	Timer 4 Status	
144h	Timer 5 Status	
145h	Timer 6 Status	
146h	Timer 7 Status	
147h	Timer 8 Status	
150h	Event Log 1 FIFO Not Empty Status	Event Log n FIFO Not Empty status 0 = FIFO Empty 1 = FIFO Not Empty
151h	Event Log 2 FIFO Not Empty Status	
152h	Event Log 3 FIFO Not Empty Status	
153h	Event Log 4 FIFO Not Empty Status	
154h	Event Log 5 FIFO Not Empty Status	
155h	Event Log 6 FIFO Not Empty Status	
156h	Event Log 7 FIFO Not Empty Status	
157h	Event Log 8 FIFO Not Empty Status	

Table 95 GPIO Function Select

PIN-SPECIFIC ALTERNATIVE FUNCTION

GP*n*_FN = 000h.

The CS47L85 provides 8 dedicated GPIO pins (1 to 8). The remaining 32 GPIOs are multiplexed with the pin-specific functions listed in Table 96.

The alternative functions are selected by setting the respective GPn_FN registers to 000h, as described in “GPIO Control”. Note that each of the functions listed in Table 96 is unique to the associated pin, and can only be supported on that pin.

The pin direction (input or output) is set automatically for each pin, whenever the respective GPn_FN register is set to 000h. The GPn_DIR control bit has no effect in this case.

NAME	CONDITION	DESCRIPTION	DIRECTION
AIF1BCLK/GPIO16	GP16_FN = 00h	Audio interface 1 bit clock	digital input / output
AIF1LRCLK/GPIO18	GP18_FN = 00h	Audio interface 1 left / right clock	digital input / output
AIF1RXDAT/GPIO17	GP17_FN = 00h	Audio interface 1 RX digital audio data	digital input
AIF1TXDAT/GPIO15	GP15_FN = 00h	Audio interface 1 TX digital audio data	digital output
AIF2BCLK/GPIO20	GP20_FN = 00h	Audio interface 2 bit clock	digital input / output
AIF2LRCLK/GPIO22	GP22_FN = 00h	Audio interface 2 left / right clock	digital input / output
AIF2RXDAT/GPIO21	GP21_FN = 00h	Audio interface 2 RX digital audio data	digital input
AIF2TXDAT/GPIO19	GP19_FN = 00h	Audio interface 2 TX digital audio data	digital output
AIF3BCLK/GPIO24	GP24_FN = 00h	Audio interface 3 bit clock	digital input / output
AIF3LRCLK/GPIO26	GP26_FN = 00h	Audio interface 3 left / right clock	digital input / output
AIF3RXDAT/GPIO25	GP25_FN = 00h	Audio interface 3 RX digital audio data	digital input
AIF3TXDAT/GPIO23	GP23_FN = 00h	Audio interface 3 TX digital audio data	digital output
AIF4BCLK/GPIO28	GP28_FN = 00h	Audio interface 4 bit clock	digital input / output
AIF4LRCLK/GPIO30	GP30_FN = 00h	Audio interface 4 left / right clock	digital input / output
AIF4RXDAT/GPIO29	GP29_FN = 00h	Audio interface 4 RX digital audio data	digital input
AIF4TXDAT/GPIO27	GP27_FN = 00h	Audio interface 4 TX digital audio data	digital output
DMICCLK4/GPIO31	GP31_FN = 00h	Digital MIC clock 4	digital output
DMICDAT4/GPIO32	GP32_FN = 00h	Digital MIC data 4	digital input
DMICCLK5/GPIO33	GP33_FN = 00h	Digital MIC clock 5	digital output
DMICDAT5/GPIO34	GP34_FN = 00h	Digital MIC data 5	digital input
DMICCLK6/GPIO35	GP35_FN = 00h	Digital MIC clock 6	digital output
DMICDAT6/GPIO36	GP36_FN = 00h	Digital MIC data 6	digital input
MIF1SCLK/GPIO9	GP9_FN = 00h	Master (I2C) Interface 1 clock	digital output
MIF1SDA/GPIO10	GP10_FN = 00h	Master (I2C) Interface 1 data	digital input / output
MIF2SCLK/GPIO11	GP11_FN = 00h	Master (I2C) Interface 2 clock	digital output
MIF2SDA/GPIO12	GP12_FN = 00h	Master (I2C) Interface 2 data	digital input / output
MIF3SCLK/GPIO13	GP13_FN = 00h	Master (I2C) Interface 3 clock	digital output
MIF3SDA/GPIO14	GP14_FN = 00h	Master (I2C) Interface 3 data	digital input / output
SPKCLK1/GPIO37	GP37_FN = 00h	Digital speaker (PDM) 1 clock	digital output
SPKDAT1/GPIO39	GP39_FN = 00h	Digital speaker (PDM) 1 data	digital output
SPKCLK2/GPIO38	GP38_FN = 00h	Digital speaker (PDM) 2 clock	digital output
SPKDAT2/GPIO40	GP40_FN = 00h	Digital speaker (PDM) 2 data	digital output

Table 96 GPIO Alternate Functions

BUTTON DETECT (GPIO INPUT)

GP*n*_FN = 001h.

Button detect functionality can be selected on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. The same functionality can be used to support a Jack Detect input function.

It is recommended to enable the GPIO input de-bounce feature when using GPIOs as button input or Jack Detect input.

The GP*n*_LVL fields may be read to determine the logic levels on a GPIO input, after the selectable de-bounce controls. Note that GP*n*_LVL is not affected by the GP*n*_POL bit.

The de-bounced GPIO signals are also inputs to the Interrupt control circuit. An interrupt event is triggered on the rising and falling edges of the GPIO input. The associated interrupt bits are latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

LOGIC ‘1’ AND LOGIC ‘0’ OUTPUT (GPIO OUTPUT)

GP*n*_FN = 001h.

The CS47L85 can be programmed to drive a logic high or logic low level on a GPIO pin by selecting the “GPIO Output” function as described in “GPIO Control”.

The output logic level is selected using the respective GP*n*_LVL bit. Note that the GP*n*_LVL registers are ‘write only’ when the respective GPIO pin is configured as an output.

The polarity of the GPIO output can be inverted using the GP*n*_POL registers. If GP*n*_POL=1, then the external output will be the opposite logic level to GP*n*_LVL.

DSP GPIO (LOW LATENCY DSP INPUT/OUTPUT)

GP*n*_FN = 002h.

The DSP GPIO function provides an advanced I/O capability, supporting the requirements of the CS47L85 as a multi-purpose sensor hub. The DSP GPIO pins are accessed using maskable sets of I/O control registers; this allows the selected combinations of GPIOs to be controlled with ease, regardless of how the allocation of GPIO pins has been implemented in hardware.

The DSP GPIO function is selected by setting the respective GPIO registers as described in “GPIO Control”.

A full description of the DSP GPIO function is provided in the “DSP Peripheral Control” section.

The pin direction (input or output) is set according to the DSP GPIO configuration for each pin, whenever the respective GPn_FN register is set to 002h. The GPn_DIR control bit has no effect in this case.

INTERRUPT (IRQ) STATUS OUTPUT

GP*n*_FN = 003h, 004h.

The CS47L85 has an Interrupt Controller which can be used to indicate when any selected Interrupt events occur. An interrupt can be generated by any of the events described throughout the GPIO function definition above. Individual interrupts may be masked in order to configure the Interrupt as required. See “Interrupts” for further details.

The Interrupt Controller supports two separate Interrupt Request (IRQ) outputs. The IRQ1 or IRQ2 status may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

Note that the IRQ1 status is output on the IRQ pin at all times.

FREQUENCY LOCKED LOOP (FLL) CLOCK OUTPUT

GP*n*_FN = 010h, 011h, 012h.

Clock outputs derived from the FLLs may be output on a GPIO pin. The GPIO output from each FLLn (where 'n' is 1, 2 or 3) is controlled by the respective FLLn_GPCLK_DIV and FLLn_GPCLK_ENA registers, as described in Table 97.

It is recommended to disable the clock output (FLLn_GPCLK_ENA=0) before making any change to the respective FLLn_GPCLK_DIV register.

Note that the FLLn_GPCLK_DIV and FLLn_GPCLK_ENA registers affect the GPIO outputs only; they do not affect the FLL frequency. The maximum output frequency supported for GPIO output is noted in the "Electrical Characteristics".

The Frequency Locked Loop (FLL) Clock outputs may be output directly on a GPIO pin by setting the respective GPIO registers as described in "GPIO Control".

See "Clocking and Sample Rates" for more details of the CS47L85 system clocking and for details of how to configure the FLLs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R394 (018Ah) FLL1_GPIO _Clock	7:1	FLL1_GPCLK_DIV [6:0]	06h	FLL1 GPIO Clock Divider 00h to 05h = Reserved 06h= Divide by 6 07h = Divide by 7 08h = Divide by 8 09h = Divide by 9 … 7Fh = Divide by 127 (F_{GPIO} = F_{VCO} / FLL1_GPCLK_DIV)
	0	FLL1_GPCLK_ENA	0	FLL1 GPIO Clock Enable 0 = Disabled 1 = Enabled
R426 (01AAh) FLL2_GPIO _Clock	7:1	FLL2_GPCLK_DIV [6:0]	06h	FLL2 GPIO Clock Divider 00h to 05h = Reserved 06h= Divide by 6 07h = Divide by 7 08h = Divide by 8 09h = Divide by 9 … 7Fh = Divide by 127 (F_{GPIO} = F_{VCO} / FLL2_GPCLK_DIV)
	0	FLL2_GPCLK_ENA	0	FLL2 GPIO Clock Enable 0 = Disabled 1 = Enabled
R458 (01CAh) FLL3_GPIO _Clock	7:1	FLL3_GPCLK_DIV [6:0]	06h	FLL3 GPIO Clock Divider 00h to 05h = Reserved 06h= Divide by 6 07h = Divide by 7 08h = Divide by 8 09h = Divide by 9 … 7Fh = Divide by 127 (F_{GPIO} = F_{VCO} / FLL3_GPCLK_DIV)
	0	FLL3_GPCLK_ENA	0	FLL3 GPIO Clock Enable 0 = Disabled 1 = Enabled

Table 97 FLL Clock Output Control

FREQUENCY LOCKED LOOP (FLL) STATUS OUTPUT

GP*n*_FN = 018h, 019h, 01Ah.

The CS47L85 supports FLL status flags, which may be used to control other events. The 'FLL Lock' signals indicate whether FLL Lock has been achieved. See "Clocking and Sample Rates" for more details of the FLL.

The FLL Lock signals may be output directly on a GPIO pin by setting the respective GPIO registers as described in "GPIO Control".

The FLL Lock signals are inputs to the Interrupt Controller circuit. An interrupt event is triggered on the rising and falling edges of these signals. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See "Interrupts" for more details of the Interrupt event handling.

OPCLK AND OPCLK_ASYNC CLOCK OUTPUT

GP*n*_FN = 040h, 041h.

A clock output (OPCLK) derived from SYSCLK can be output on a GPIO pin. The OPCLK frequency is controlled by OPCLK_DIV and OPCLK_SEL. The OPCLK output is enabled using the OPCLK_ENA register, as described in Table 98.

A clock output (OPCLK_ASYNC) derived from ASYNCCLK can be output on a GPIO pin. The OPCLK_ASYNC frequency is controlled by OPCLK_ASYNC_DIV and OPCLK_ASYNC_SEL. The OPCLK_ASYNC output is enabled using the OPCLK_ASYNC_ENA register

It is recommended to disable the clock output (OPCLK_ENA=0 or OPCLK_ASYNC_ENA=0) before making any change to the respective OPCLK_DIV, OPCLK_SEL, OPCLK_ASYNC_DIV or OPCLK_ASYNC_SEL registers.

The OPCLK output should be kept disabled (OPCLK_ENA=0) if SYSCLK is not enabled. SYSCLK must be present and enabled before setting the OPCLK_ENA bit. See "Clocking and Sample Rates" for further details (including requirements for reconfiguring SYSCLK while digital core functions are enabled).

The OPCLK or OPCLK_ASYNC Clock outputs can be output directly on a GPIO pin by setting the respective GPIO registers as described in "GPIO Control".

Note that the OPCLK source frequency cannot be higher than the SYSCLK frequency. The OPCLK_ASYNC source frequency cannot be higher than the ASYNCCLK frequency. The maximum output frequency supported for GPIO output is noted in the "Electrical Characteristics".

See "Clocking and Sample Rates" for more details of the system clocks (SYSCLK and ASYNCCLK).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R329 (0149h) Output_system_clock	15	OPCLK_ENA	0	OPCLK Enable 0 = Disabled 1 = Enabled
	7:3	OPCLK_DIV [4:0]	00h	OPCLK Divider 02h = Divide by 2 04h = Divide by 4 06h = Divide by 6 … (even numbers only) 1Eh = Divide by 30 Note that only even numbered divisions (2, 4, 6, etc.) are valid selections. All other codes are Reserved when the OPCLK signal is enabled.
	2:0	OPCLK_SEL [2:0]	000	OPCLK Source Frequency 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) All other codes are Reserved The frequencies in brackets apply for 44.1kHz-related SYSCLK rates only (i.e., SAMPLE_RATE_n = 01XXX). The OPCLK Source Frequency must be less than or equal to the SYSCLK frequency.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R330 (014Ah) Output_async _lock	15	OPCLK_ASYNC_ENA	0	OPCLK_ASYNC Enable 0 = Disabled 1 = Enabled
	7:3	OPCLK_ASYNC_DIV [4:0]	00h	OPCLK_ASYNC Divider 02h = Divide by 2 04h = Divide by 4 06h = Divide by 6 … (even numbers only) 1Eh = Divide by 30 Note that only even numbered divisions (2, 4, 6, etc.) are valid selections. All other codes are Reserved when the OPCLK_ASYNC signal is enabled.
	2:0	OPCLK_ASYNC_SEL [2:0]	000	OPCLK_ASYNC Source Frequency 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) All other codes are Reserved The frequencies in brackets apply for 44.1kHz-related ASYNCCLK rates only (i.e., ASYNC_SAMPLE_RATE_n = 01XXX). The OPCLK_ASYNC Source Frequency must be less than or equal to the ASYNCCLK frequency.

Table 98 OPCLK and OPCLK_ASYNC Control

PULSE WIDTH MODULATION (PWM) SIGNAL OUTPUT

GP*n*_FN = 048h, 049h.

The CS47L85 incorporates two Pulse Width Modulation (PWM) signal generators which can be enabled as GPIO outputs. The duty cycle of each PWM signal can be modulated by an audio source, or can be set to a fixed value using a control register setting.

The Pulse Width Modulation (PWM) outputs may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

See “Digital Core” for details of how to configure the PWM signal generators.

SPDIF AUDIO OUTPUT

GP*n*_FN = 04Ch.

The CS47L85 incorporates an IEC-60958-3 compatible S/PDIF transmitter, which can be selected as a GPIO output. The S/PDIF transmitter supports stereo audio channels, and allows full control over the S/PDIF validity bits and channel status information.

The S/PDIF signal may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

See “Digital Core” for details of how to configure the S/PDIF output generator.

ASYNCHRONOUS SAMPLE RATE CONVERTER (ASRC) LOCK STATUS OUTPUT

GP*n*_FN = 088h, 089h, 08Ah, 08Bh.

The CS47L85 maintains a flag indicating the lock status of the Asynchronous Sample Rate Converters (ASRCs), which may be used to control other events if required. See “Digital Core” for more details of the ASRCs.

The ASRC Lock signals may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

The ASRC Lock signals are inputs to the Interrupt control circuit. An interrupt event is triggered on the rising and falling edges of the ASRC Lock signals. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

OVER-TEMPERATURE, SHORT CIRCUIT PROTECTION, AND SPEAKER SHUTDOWN STATUS OUTPUT

GP*n*_FN = 0B6h, 0B7h, 0E0h, 0E1h, 0E2h.

The CS47L85 incorporates a temperature sensor which detects when the device temperature is within normal limits or if the device is approaching a hazardous temperature condition.

The temperature status may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. A GPIO pin can be used to indicate either an Overheat Warning Temperature event or an Overheat Shutdown Temperature event.

The CS47L85 provides short circuit protection on the Class D speaker outputs, and on each of the headphone output paths.

The status of the Class D speaker short circuit detection circuits may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

If the Overheat Shutdown Temperature is exceeded, or if a short circuit is detected on the Class D speaker outputs, then the Class D speaker outputs will automatically be disabled in order to protect the device. The General Purpose Timers can be used as a Watchdog function to trigger a shutdown of the Class D speaker drivers. Further details of the Speaker Shutdown functions are described in the “Thermal Shutdown and Short Circuit Protection” section. When the speaker driver shutdown is complete, the Speaker Shutdown signal will be asserted. The speaker driver shutdown status can also be output directly on a GPIO pin.

The Overtemperature, Short Circuit protection, and Speaker Shutdown status flags are inputs to the Interrupt control circuit. An interrupt event may be triggered on the applicable edges of these signals. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

GENERAL PURPOSE TIMER STATUS OUTPUT

GP*n*_FN = 140h, 141h, 142h, 143h, 144h, 145h, 146h, 147h.

The General Purpose Timers can count up or down, and support continuous or single count modes. Status outputs indicating the progress of these timers are provided. See “DSP Peripheral Control” for details of the General Purpose Timers.

A logic signal from the General Purpose Timers may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. This logic signal is pulsed high whenever the respective Timer reaches its final count value.

The General Purpose Timers also provide inputs to the Interrupt control circuit. An interrupt event is triggered whenever the respective Timer reaches its final count value. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

EVENT LOGGER FIFO BUFFER STATUS OUTPUT

GP*n*_FN = 150h, 151h, 152h, 153h, 154h, 155h, 156h, 157h.

The Event Loggers are each provided with a 16-stage FIFO buffer, in which any detected events (signal transitions) are recorded. Status outputs for each FIFO buffer are provided. See “DSP Peripheral Control” for details of the Event Loggers.

A logic signal from the Event Loggers may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. This logic signal is set high whenever the ‘FIFO Not Empty’ condition is true.

The Event Loggers also provide inputs to the Interrupt control circuit. An interrupt event is triggered whenever the respective FIFO condition occurs. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

GENERAL PURPOSE SWITCH

The CS47L85 provides a General Purpose Switch, which can be used as a controllable analogue switch for external functions. The switch is implemented between the GPSWP and GPSWN pins. Note that this feature is entirely independent to the GPIOn pins.

The General Purpose Switch is configured using SW1_MODE. This register allows the switch to be disabled, enabled, or synchronised to the MICDET Clamp status, as described in Table 99.

The switch is a bi-directional analogue switch, offering flexibility in the potential circuit applications. Refer to the “Absolute Maximum Ratings” and “Electrical Characteristics” for further details.

The switch can be used in conjunction with the MICDET Clamp function, in order suppress pops and clicks associated with jack insertion and removal. An example circuit is shown in Figure 69, within the “External Accessory Detection” section. Note that the MICDET Clamp function must also be configured appropriately when using this method of pop suppression control.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R712 (02C8h) GP_Switch_1	1:0	SW1_MODE [1:0]	00	General Purpose Switch control 00 = Disabled (open) 01 = Enabled (closed) 10 = Enabled when MICDET Clamp is active 11 = Enabled when MICDET Clamp is not active

Table 99 General Purpose Switch control

INTERRUPTS

The Interrupt Controller has multiple inputs. These include the Jack Detect and GPIO input pins, DSP_IRQn flags, headphone / accessory detection, FLL / ASRC Lock detection, and status flags from DSP peripheral functions. (See Table 100 and Table 101 for a full definition of the Interrupt Controller inputs.) Any combination of these inputs can be used to trigger an Interrupt Request (IRQ) event.

The Interrupt Controller supports two sets of interrupt registers. This allows two separate Interrupt Request (IRQ) outputs to be generated, and for each IRQ to report a different set of input or status conditions.

For each Interrupt Request (IRQ1 and IRQ2) output, there is an Interrupt register field associated with each of the interrupt inputs. These fields are asserted whenever a logic edge is detected on the respective input. Some inputs are triggered on rising edges only; some are triggered on both edges. Separate rising and falling interrupt registers are provided for the JD1 and JD2 signals. The Interrupt register fields for IRQ1 are described in Table 100. The Interrupt register fields for IRQ2 are described in Table 101. The Interrupt flags can be polled at any time, or else in response to the Interrupt Request (IRQ) output being signalled via the IRQ pin or a GPIO pin.

All of the Interrupts are edge-triggered, as noted above. Many of these are triggered on both the rising and falling edges and, therefore, the Interrupt registers cannot indicate which edge has been detected. The “Raw Status” fields described in Table 100 and Table 101 provide readback of the current value of the corresponding inputs to the Interrupt Controller. Note that the “Raw Status” bits associated with IRQ1 and IRQ2 both provide the same readback information. The status of any GPIO (or DSP GPIO) inputs can also be read using the GPIO (or DSP GPIO) control registers, as described in Table 94 and Table 36.

Individual mask bits can enable or disable different functions from the Interrupt controller. The mask bits are described in Table 100 (for IRQ1) and Table 101 (for IRQ2). Note that a masked interrupt input will not assert the corresponding interrupt register field, and will not cause the associated Interrupt Request (IRQ) output to be asserted.

The Interrupt Request (IRQ) outputs represent the logical ‘OR’ of the associated interrupt registers. (IRQ1 is derived from the _EINT1 registers; IRQ2 is derived from the _EINT2 registers). The Interrupt register fields are latching fields and, once they are set, they are not reset until a ‘1’ is written to the respective register bit(s). The Interrupt Request (IRQ) outputs are not reset until each of the associated interrupts has been reset.

A de-bounce circuit can be enabled on any GPIO input, to avoid false event triggers. This is enabled on each pin using the register bits described in Table 94. The GPIO de-bounce circuit uses the 32kHz clock, which must be enabled whenever the GPIO de-bounce function is required.

A de-bounce circuit is always enabled on the FLL status inputs; either the 32kHz clock, or the SYSCLK signal, must be enabled to trigger an Interrupt from the FLL status inputs. Note that the “Raw Status” fields (described in Table 100 and Table 101), are valid without clocking, and can be used to provide FLL status readback when system clocks are not available.

The IRQ outputs can be globally masked using the IM_IRQ1 and IM_IRQ2 register bits. When not masked, the IRQ status can be read from IRQ1_STS and IRQ2_STS for the respective IRQ outputs.

The IRQ1 output is provided externally on the IRQ pin. Under default conditions, this output is ‘Active Low’. The polarity can be inverted using the IRQ_POL register. The IRQ output can be either CMOS driven or Open Drain; this is selected using the IRQ_OP_CFG register. Note that the IRQ output is referenced to the DBVDD1 power domain.

The IRQ2 status can be used to trigger DSP firmware execution - see “DSP Firmware Control”. This allows the DSP firmware execution to be linked to external events (e.g., Jack detection, or GPIO input), or to any of the status conditions flagged by the Interrupt registers.

The IRQ1 and IRQ2 signals may be output on a GPIO pin - see “General Purpose Input / Output”.

The CS47L85 Interrupt Controller circuit is illustrated in Figure 73. (Note that not all interrupt inputs are shown.) The control fields associated with IRQ1 and IRQ2 are described in Table 100 and Table 101 respectively. The global interrupt mask bits, status bits, and output configuration register are described in Table 102.

Note that, under default register conditions, the ‘Boot Done’ status is the only un-masked interrupt source; a falling edge on the IRQ pin will indicate completion of the Boot Sequence.

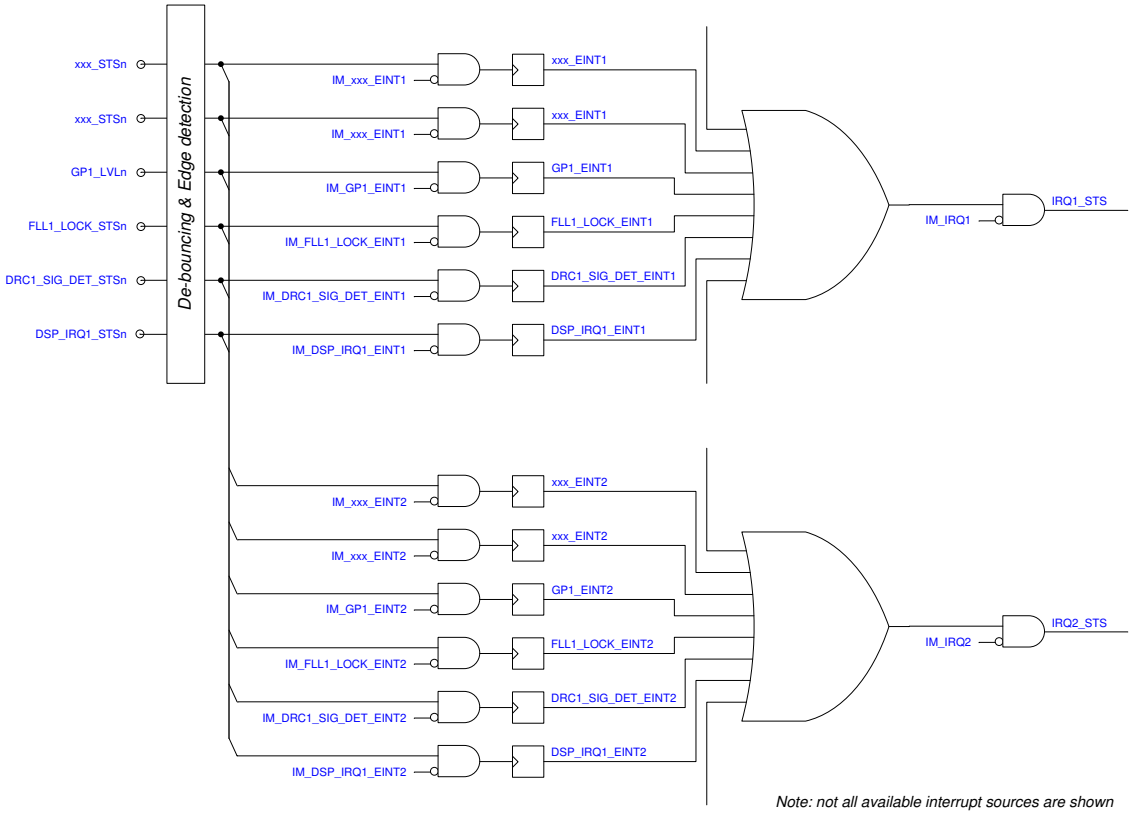


Figure 73 Interrupt Controller

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6144 (1800h) IRQ1_Status_1	15	DSP_SHARED_WR_COLL_EINT1	0	DSP Shared Memory Collision Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	12	CTRLIF_ERR_EINT1	0	Control Interface Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	9	SYSCLK_FAIL_EINT1	0	SYSCLK Fail Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	7	BOOT_DONE_EINT1	0	Boot Done Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6145 (1801h) IRQ1_Status_2	10	FLL3_LOCK_EINT1	0	FLL3 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	9	FLL2_LOCK_EINT1	0	FLL2 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	8	FLL1_LOCK_EINT1	0	FLL1 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R6149 (1805h) IRQ1_Status_6	8	MICDET_EINT1	0	Microphone / Accessory Detect Interrupt (Detection event triggered) Note: Cleared when a '1' is written.
	0	HPDET_EINT1	0	Headphone Detect Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6150 (1806h) IRQ1_Status_7	5	MICD_CLAMP_FALL_EINT1	0	MICDET Clamp Interrupt (Falling edge triggered) Note: Cleared when a '1' is written.
	4	MICD_CLAMP_RISE_EINT1	0	MICDET Clamp Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	JD2_FALL_EINT1	0	JD2 Interrupt (Falling edge triggered) Note: Cleared when a '1' is written.
	2	JD2_RISE_EINT1	0	JD2 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	JD1_FALL_EINT1	0	JD1 Interrupt (Falling edge triggered) Note: Cleared when a '1' is written.
	0	JD1_RISE_EINT1	0	JD1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6152 (1808h) IRQ1_Status_9	11	ASRC2_IN2_LOCK_EINT1	0	ASRC2 IN2 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	10	ASRC2_IN1_LOCK_EINT1	0	ASRC2 IN1 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	9	ASRC1_IN2_LOCK_EINT1	0	ASRC1 IN2 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	8	ASRC1_IN1_LOCK_EINT1	0	ASRC1 IN1 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	1	DRC2_SIG_DET_EINT1	0	DRC2 Signal Detect Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	0	DRC1_SIG_DET_EINT1	0	DRC1 Signal Detect Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R6154 (180Ah) IRQ1_Status_11	15	DSP_IRQ16_EINT1	0	DSP IRQ16 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	14	DSP_IRQ15_EINT1	0	DSP IRQ15 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	13	DSP_IRQ14_EINT1	0	DSP IRQ14 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	12	DSP_IRQ13_EINT1	0	DSP IRQ13 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	11	DSP_IRQ12_EINT1	0	DSP IRQ12 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	10	DSP_IRQ11_EINT1	0	DSP IRQ11 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	9	DSP_IRQ10_EINT1	0	DSP IRQ10 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	8	DSP_IRQ9_EINT1	0	DSP IRQ9 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	7	DSP_IRQ8_EINT1	0	DSP IRQ8 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	6	DSP_IRQ7_EINT1	0	DSP IRQ7 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	DSP_IRQ6_EINT1	0	DSP IRQ6 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	DSP_IRQ5_EINT1	0	DSP IRQ5 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	DSP_IRQ4_EINT1	0	DSP IRQ4 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	DSP_IRQ3_EINT1	0	DSP IRQ3 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	DSP_IRQ2_EINT1	0	DSP IRQ2 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	DSP_IRQ1_EINT1	0	DSP IRQ1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6155 (180Bh) IRQ1_Status_12	7	SPKOUTR_SC_EINT1	0	SPKOUTR Short Circuit Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	6	SPKOUTL_SC_EINT1	0	SPKOUTL Short Circuit Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	5	HP3R_SC_EINT1	0	HPOUT3R Short Circuit Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	HP3L_SC_EINT1	0	HPOUT3L Short Circuit Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	HP2R_SC_EINT1	0	HPOUT2R Short Circuit Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	HP2L_SC_EINT1	0	HPOUT2L Short Circuit Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	HP1R_SC_EINT1	0	HPOUT1R Short Circuit Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	HP1L_SC_EINT1	0	HPOUT1L Short Circuit Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6156 (180Ch) IRQ1_Status_13	7	SPKOUTR_ENABLE_DONE_EINT1	0	SPKOUTR Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	6	SPKOUTL_ENABLE_DONE_EINT1	0	SPKOUTL Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	5	HP3R_ENABLE_DONE_EINT1	0	HPOUT3R Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	HP3L_ENABLE_DONE_EINT1	0	HPOUT3L Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	HP2R_ENABLE_DONE_EINT1	0	HPOUT2R Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	HP2L_ENABLE_DONE_EINT1	0	HPOUT2L Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	HP1R_ENABLE_DONE_EINT1	0	HPOUT1R Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	HP1L_ENABLE_DONE_EINT1	0	HPOUT1L Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6157 (180Dh) IRQ1_Status_14	7	SPKOUTR_DISABLE_DONE_EINT1	0	SPKOUTR Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	6	SPKOUTL_DISABLE_DONE_EINT1	0	SPKOUTL Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	HP3R_DISABLE_DONE_EINT1	0	HPOUT3R Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	HP3L_DISABLE_DONE_EINT1	0	HPOUT3L Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	HP2R_DISABLE_DONE_EINT1	0	HPOUT2R Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	HP2L_DISABLE_DONE_EINT1	0	HPOUT2L Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	HP1R_DISABLE_DONE_EINT1	0	HPOUT1R Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	HP1L_DISABLE_DONE_EINT1	0	HPOUT1L Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6158 (180Eh) IRQ1_Status_15	2	SPK_OVERHEAT_WARN_EINT1	0	Speaker Overheat Warning Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	SPK_OVERHEAT_EINT1	0	Speaker Overheat Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	SPK_SHUTDOWN_EINT1	0	Speaker Shutdown Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R6160 (1810h) IRQ1_Status_17	15	GP16_EINT1	0	GPIO16 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	14	GP15_EINT1	0	GPIO15 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	13	GP14_EINT1	0	GPIO14 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	12	GP13_EINT1	0	GPIO13 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	11	GP12_EINT1	0	GPIO12 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	10	GP11_EINT1	0	GPIO11 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	9	GP10_EINT1	0	GPIO10 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	8	GP9_EINT1	0	GPIO9 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	7	GP8_EINT1	0	GPIO8 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	6	GP7_EINT1	0	GPIO7 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	5	GP6_EINT1	0	GPIO6 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	4	GP5_EINT1	0	GPIO5 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	3	GP4_EINT1	0	GPIO4 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	2	GP3_EINT1	0	GPIO3 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	1	GP2_EINT1	0	GPIO2 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	0	GP1_EINT1	0	GPIO1 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R6161 (1811h) IRQ1_Status_18	15	GP32_EINT1	0	GPIO32 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	14	GP31_EINT1	0	GPIO31 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	13	GP30_EINT1	0	GPIO30 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	12	GP29_EINT1	0	GPIO29 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	11	GP28_EINT1	0	GPIO28 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	10	GP27_EINT1	0	GPIO27 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	9	GP26_EINT1	0	GPIO26 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	8	GP25_EINT1	0	GPIO25 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	7	GP24_EINT1	0	GPIO24 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	6	GP23_EINT1	0	GPIO23 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	5	GP22_EINT1	0	GPIO22 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	4	GP21_EINT1	0	GPIO21 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	3	GP20_EINT1	0	GPIO20 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	2	GP19_EINT1	0	GPIO19 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	1	GP18_EINT1	0	GPIO18 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	0	GP17_EINT1	0	GPIO17 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R6162 (1812h) IRQ1_Status_19	7	GP40_EINT1	0	GPIO40 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	6	GP39_EINT1	0	GPIO39 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	5	GP38_EINT1	0	GPIO38 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	4	GP37_EINT1	0	GPIO37 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	3	GP36_EINT1	0	GPIO36 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	2	GP35_EINT1	0	GPIO35 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	1	GP34_EINT1	0	GPIO34 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	0	GP33_EINT1	0	GPIO33 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6164 (1814h) IRQ1_Status_21	7	TIMER8_EINT1	0	Timer 8 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	6	TIMER7_EINT1	0	Timer 7 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	TIMER6_EINT1	0	Timer 6 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	TIMER5_EINT1	0	Timer 5 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	TIMER4_EINT1	0	Timer 4 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	TIMER3_EINT1	0	Timer 3 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	TIMER2_EINT1	0	Timer 2 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	TIMER1_EINT1	0	Timer 1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6165 (1815h) IRQ1_Status_22	7	EVENT8_NOT_EMPTY_EINT1	0	Event Log 8 FIFO Not Empty Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	6	EVENT7_NOT_EMPTY_EINT1	0	Event Log 7 FIFO Not Empty Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	EVENT6_NOT_EMPTY_EINT1	0	Event Log 6 FIFO Not Empty Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	EVENT5_NOT_EMPTY_EINT1	0	Event Log 5 FIFO Not Empty Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	EVENT4_NOT_EMPTY_EINT1	0	Event Log 4 FIFO Not Empty Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	EVENT3_NOT_EMPTY_EINT1	0	Event Log 3 FIFO Not Empty Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	EVENT2_NOT_EMPTY_EINT1	0	Event Log 2 FIFO Not Empty Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	EVENT1_NOT_EMPTY_EINT1	0	Event Log 1 FIFO Not Empty Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6166 (1816h) IRQ1_Status_23	7	EVENT8_FULL_EINT1	0	Event Log 8 FIFO Full Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	6	EVENT7_FULL_EINT1	0	Event Log 7 FIFO Full Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	EVENT6_FULL_EINT1	0	Event Log 6 FIFO Full Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	4	EVENT5_FULL_EINT1	0	Event Log 5 FIFO Full Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	EVENT4_FULL_EINT1	0	Event Log 4 FIFO Full Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	EVENT3_FULL_EINT1	0	Event Log 3 FIFO Full Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	EVENT2_FULL_EINT1	0	Event Log 2 FIFO Full Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	EVENT1_FULL_EINT1	0	Event Log 1 FIFO Full Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6167 (1817h) IRQ1_Status_24	7	EVENT8_WMARK_EINT1	0	Event Log 8 FIFO Watermark Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	6	EVENT7_WMARK_EINT1	0	Event Log 7 FIFO Watermark Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	EVENT6_WMARK_EINT1	0	Event Log 6 FIFO Watermark Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	EVENT5_WMARK_EINT1	0	Event Log 5 FIFO Watermark Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	EVENT4_WMARK_EINT1	0	Event Log 4 FIFO Watermark Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	EVENT3_WMARK_EINT1	0	Event Log 3 FIFO Watermark Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	EVENT2_WMARK_EINT1	0	Event Log 2 FIFO Watermark Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	EVENT1_WMARK_EINT1	0	Event Log 1 FIFO Watermark Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6168 (1818h) IRQ1_Status_25	6	DSP7_DMA_EINT1	0	DSP7 DMA Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	DSP6_DMA_EINT1	00	DSP6 DMA Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	DSP5_DMA_EINT1	00	DSP5 DMA Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	DSP4_DMA_EINT1	00	DSP4 DMA Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	DSP3_DMA_EINT1	00	DSP3 DMA Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	DSP2_DMA_EINT1	00	DSP2 DMA Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	DSP1_DMA_EINT1	00	DSP1 DMA Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6170 (181Ah) IRQ1_Status_27	6	DSP7_START1_EINT1	0	DSP7 Start 1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	DSP6_START1_EINT1	0	DSP6 Start 1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	DSP5_START1_EINT1	0	DSP5 Start 1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	DSP4_START1_EINT1	0	DSP4 Start 1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	DSP3_START1_EINT1	0	DSP3 Start 1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	DSP2_START1_EINT1	0	DSP2 Start 1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	DSP1_START1_EINT1	0	DSP1 Start 1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6171 (181Bh) IRQ1_Status_28	6	DSP7_START2_EINT1	0	DSP7 Start 2 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	DSP6_START2_EINT1	0	DSP6 Start 2 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	DSP5_START2_EINT1	0	DSP5 Start 2 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	DSP4_START2_EINT1	0	DSP4 Start 2 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	DSP3_START2_EINT1	0	DSP3 Start 2 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	DSP2_START2_EINT1	0	DSP2 Start 2 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	DSP1_START2_EINT1	0	DSP1 Start 2 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6173 (181Dh) IRQ1_Status_30	6	DSP7_BUSY_EINT1	0	DSP7 Busy Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	DSP6_BUSY_EINT1	0	DSP6 Busy Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	DSP5_BUSY_EINT1	0	DSP5 Busy Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	DSP4_BUSY_EINT1	0	DSP4 Busy Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2	DSP3_BUSY_EINT1	0	DSP3 Busy Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	DSP2_BUSY_EINT1	0	DSP2 Busy Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	DSP1_BUSY_EINT1	0	DSP1 Busy Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6174 (181Eh) IRQ1_Status_31	2	MIF3_DONE_EINT1	0	MIF3 Done Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	MIF2_DONE_EINT1	0	MIF2 Done Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	MIF1_DONE_EINT1	0	MIF1 Done Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6175 (181Fh) IRQ1_Status_32	2	MIF3_BLOCK_EINT1	0	MIF3 Block Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	MIF2_BLOCK_EINT1	0	MIF2 Block Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	MIF1_BLOCK_EINT1	0	MIF1 Block Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6208 (1840h) to R6239 (185Fh)		IM_*	(see note)	For each *_EINT1 interrupt register in R6144 to R6175, a corresponding mask bit (IM_*) is provided in R6208 to R6239. The mask bits are coded as: 0 = Do not mask interrupt 1 = Mask interrupt
		Note : The BOOT_DONE_EINT1 interrupt is '0' (un-masked) by default; all other interrupts are '1' (masked) by default.		
R6272 (1880h) IRQ1_Raw_Status_1	12	CTRLIF_ERR_STS1	0	Control Interface Error Status 0 = Normal 1 = Control Interface Error
	7	BOOT_DONE_STS1	0	Boot Status 0 = Busy (boot sequence in progress) 1 = Idle (boot sequence completed) Control register writes should not be attempted until Boot Sequence has completed.
R6273 (1881h) IRQ1_Raw_Status_2	10	FLL3_LOCK_STS1	0	FLL3 Lock Status 0 = Not locked 1 = Locked
	9	FLL2_LOCK_STS1	0	FLL2 Lock Status 0 = Not locked 1 = Locked
	8	FLL1_LOCK_STS1	0	FLL1 Lock Status 0 = Not locked 1 = Locked
R6278 (1886h) IRQ1_Raw	4	MICD_CLAMP_STS1	0	MICDET Clamp status 0 = Clamp not active 1 = Clamp active

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
_Status_7	2	JD2_STS1	0	JACKDET2 input status 0 = Jack not detected 1 = Jack is detected (Assumes the JACKDET2 pin is pulled 'low' on Jack insertion.)
	0	JD1_STS1	0	JACKDET1 input status 0 = Jack not detected 1 = Jack is detected (Assumes the JACKDET1 pin is pulled 'low' on Jack insertion.)
R6280 (1888h) IRQ1_Raw _Status_9	11	ASRC2_IN2_LOCK_STS1	0	ASRC2 IN2 Lock Status 0 = Not locked 1 = Locked
	10	ASRC2_IN1_LOCK_STS1	0	ASRC2 IN1 Lock Status 0 = Not locked 1 = Locked
	9	ASRC1_IN2_LOCK_STS1	0	ASRC1 IN2 Lock Status 0 = Not locked 1 = Locked
	8	ASRC1_IN1_LOCK_STS1	0	ASRC1 IN1 Lock Status 0 = Not locked 1 = Locked
	1	DRC2_SIG_DET_STS1	0	DRC2 Signal Detect Status 0 = Normal 1 = Signal detected
	0	DRC1_SIG_DET_STS1	0	DRC1 Signal Detect Status 0 = Normal 1 = Signal detected
R6283 (188Bh) IRQ1_Raw _Status_12	7	SPKOUTR_SC_STS1	0	SPKOUTR Short Circuit Status 0 = Normal 1 = Short Circuit detected
	6	SPKOUTL_SC_STS1	0	SPKOUTL Short Circuit Status 0 = Normal 1 = Short Circuit detected
	5	HP3R_SC_STS1	0	HPOUT3R Short Circuit Status 0 = Normal 1 = Short Circuit detected
	4	HP3L_SC_STS1	0	HPOUT3L Short Circuit Status 0 = Normal 1 = Short Circuit detected
	3	HP2R_SC_STS1	0	HPOUT2R Short Circuit Status 0 = Normal 1 = Short Circuit detected
	2	HP2L_SC_STS1	0	HPOUT2L Short Circuit Status 0 = Normal 1 = Short Circuit detected
	1	HP1R_SC_STS1	0	HPOUT1R Short Circuit Status 0 = Normal 1 = Short Circuit detected
	0	HP1L_SC_STS1	0	HPOUT1L Short Circuit Status 0 = Normal 1 = Short Circuit detected
R6284 (188Ch) IRQ1_Raw	7	SPKOUTR_ENABLE_DONE_STS1	0	SPKOUTR Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
_Status_13	6	SPKOUTL_ENABLE_DONE_STS1	0	SPKOUTL Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	5	HP3R_ENABLE_DONE_STS1	0	HPOUT3R Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	4	HP3L_ENABLE_DONE_STS1	0	HPOUT3L Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	3	HP2R_ENABLE_DONE_STS1	0	HPOUT2R Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	2	HP2L_ENABLE_DONE_STS1	0	HPOUT2L Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	1	HP1R_ENABLE_DONE_STS1	0	HPOUT1R Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	0	HP1L_ENABLE_DONE_STS1	0	HPOUT1L Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
R6285 (188Dh) IRQ1_Raw_Status_14	7	SPKOUTR_DISABLE_DONE_STS1	0	SPKOUTR Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	6	SPKOUTL_DISABLE_DONE_STS1	0	SPKOUTL Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	5	HP3R_DISABLE_DONE_STS1	0	HPOUT3R Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	4	HP3L_DISABLE_DONE_STS1	0	HPOUT3L Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	3	HP2R_DISABLE_DONE_STS1	0	HPOUT2R Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	2	HP2L_DISABLE_DONE_STS1	0	HPOUT2L Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	1	HP1R_DISABLE_DONE_STS1	0	HPOUT1R Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	0	HP1L_DISABLE_DONE_STS1	0	HPOUT1L Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
R6286 (188Eh) IRQ1_Raw_Status_15	2	SPK_OVERHEAT_WARN_STS1	0	Speaker Overheat Warning Status 0 = Normal 1 = Warning temperature exceeded
	1	SPK_OVERHEAT_STS1	0	Speaker Overheat Status 0 = Normal 1 = Shutdown temperature exceeded
	0	SPK_SHUTDOWN_STS1	0	Speaker Shutdown Status 0 = Normal 1 = Speaker Shutdown completed (due to Overheat Temperature or Short Circuit condition)
R6288	15	GP16_STS1	0	GPIOn Input status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
(1890h) IRQ1_Raw _Status_17	14	GP15_STS1	0	Reads back the logic level of GPIOn. Only valid for pins configured as GPIO input (does not include DSPGPIO inputs).
	13	GP14_STS1	0	
	12	GP13_STS1	0	
	11	GP12_STS1	0	
	10	GP11_STS1	0	
	9	GP10_STS1	0	
	8	GP9_STS1	0	
	7	GP8_STS1	0	
	6	GP7_STS1	0	
	5	GP6_STS1	0	
	4	GP5_STS1	0	
	3	GP4_STS1	0	
	2	GP3_STS1	0	
	1	GP2_STS1	0	
	0	GP1_STS1	0	
R6289 (1891h) IRQ1_Raw _Status_18	15	GP32_STS1	0	GPIOn Input status Reads back the logic level of GPIOn. Only valid for pins configured as GPIO input (does not include DSPGPIO inputs).
	14	GP31_STS1	0	
	13	GP30_STS1	0	
	12	GP29_STS1	0	
	11	GP28_STS1	0	
	10	GP27_STS1	0	
	9	GP26_STS1	0	
	8	GP25_STS1	0	
	7	GP24_STS1	0	
	6	GP23_STS1	0	
	5	GP22_STS1	0	
	4	GP21_STS1	0	
	3	GP20_STS1	0	
	2	GP19_STS1	0	
	1	GP18_STS1	0	
	0	GP17_STS1	0	
R6290 (1892h) IRQ1_Raw _Status_19	7	GP40_STS1	0	GPIOn Input status Reads back the logic level of GPIOn. Only valid for pins configured as GPIO input (does not include DSPGPIO inputs).
	6	GP39_STS1	0	
	5	GP38_STS1	0	
	4	GP37_STS1	0	
	3	GP36_STS1	0	
	2	GP35_STS1	0	
	1	GP34_STS1	0	
	0	GP33_STS1	0	
R6293 (1895h) IRQ1_Raw _Status_22	7	EVENT8_NOT_E MPTY_STS1	0	Event Log n FIFO Not Empty status 0 = FIFO Empty 1 = FIFO Not Empty
	6	EVENT7_NOT_E MPTY_STS1	0	
	5	EVENT6_NOT_E MPTY_STS1	0	
	4	EVENT5_NOT_E MPTY_STS1	0	
	3	EVENT4_NOT_E MPTY_STS1	0	
	2	EVENT3_NOT_E MPTY_STS1	0	
	1	EVENT2_NOT_E MPTY_STS1	0	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	EVENT1_NOT_EMPTY_STS1	0	
R6294 (1896h) IRQ1_Raw_Status_23	7	EVENT8_FULL_STS1	0	Event Log n FIFO Full status 0 = FIFO Not Full 1 = FIFO Full
	6	EVENT7_FULL_STS1	0	
	5	EVENT6_FULL_STS1	0	
	4	EVENT5_FULL_STS1	0	
	3	EVENT4_FULL_STS1	0	
	2	EVENT3_FULL_STS1	0	
	1	EVENT2_FULL_STS1	0	
	0	EVENT1_FULL_STS1	0	
R6295 (1897h) IRQ1_Raw_Status_24	7	EVENT8_WMARK_STS1	0	Event Log n FIFO Watermark status 0 = FIFO Watermark not reached 1 = FIFO Watermark reached
	6	EVENT7_WMARK_STS1	0	
	5	EVENT6_WMARK_STS1	0	
	4	EVENT5_WMARK_STS1	0	
	3	EVENT4_WMARK_STS1	0	
	2	EVENT3_WMARK_STS1	0	
	1	EVENT2_WMARK_STS1	0	
	0	EVENT1_WMARK_STS1	0	
R6296 (1898h) IRQ1_Raw_Status_25	6	DSP7_DMA_STS1	0	DSPn DMA status 0 = Normal 1 = All enabled WDMA buffers filled, and all enabled RDMA buffers emptied
	5	DSP6_DMA_STS1	00	
	4	DSP5_DMA_STS1	00	
	3	DSP4_DMA_STS1	00	
	2	DSP3_DMA_STS1	00	
	1	DSP2_DMA_STS1	00	
	0	DSP1_DMA_STS1	00	
R6301 (189Dh) IRQ1_Raw_Status_30	6	DSP7_BUSY_STS1	0	DSPn Busy status 0 = DSP Idle 1 = DSP Busy
	5	DSP6_BUSY_STS1	0	
	4	DSP5_BUSY_STS1	0	
	3	DSP4_BUSY_STS1	0	
	2	DSP3_BUSY_STS1	0	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1	DSP2_BUSY_STS1	0	
	0	DSP1_BUSY_STS1	0	

Table 100 Interrupt 1 Control Registers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6400 (1900h) IRQ2_Status_1	15	DSP_SHARED_WR_COLL_EINT2	0	DSP Shared Memory Collision Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	12	CTRLIF_ERR_EINT2	0	Control Interface Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	9	SYSCLK_FAIL_EINT2	0	SYSCLK Fail Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	7	BOOT_DONE_EINT2	0	Boot Done Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6401 (1901h) IRQ2_Status_2	10	FLL3_LOCK_EINT2	0	FLL3 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	9	FLL2_LOCK_EINT2	0	FLL2 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	8	FLL1_LOCK_EINT2	0	FLL1 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R6405 (1905h) IRQ2_Status_6	8	MICDET_EINT2	0	Microphone / Accessory Detect Interrupt (Detection event triggered) Note: Cleared when a '1' is written.
	0	HPDET_EINT2	0	Headphone Detect Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6406 (1906h) IRQ2_Status_7	5	MICD_CLAMP_FALL_EINT2	0	MICDET Clamp Interrupt (Falling edge triggered) Note: Cleared when a '1' is written.
	4	MICD_CLAMP_RISE_EINT2	0	MICDET Clamp Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	JD2_FALL_EINT2	0	JD2 Interrupt (Falling edge triggered) Note: Cleared when a '1' is written.
	2	JD2_RISE_EINT2	0	JD2 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	JD1_FALL_EINT2	0	JD1 Interrupt (Falling edge triggered) Note: Cleared when a '1' is written.
	0	JD1_RISE_EINT2	0	JD1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6408 (1908h) IRQ2_Statu	11	ASRC2_IN2_LOCK_EINT2	0	ASRC2 IN2 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
s_9	10	ASRC2_IN1_LOCK_EINT2	0	ASRC2 IN1 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	9	ASRC1_IN2_LOCK_EINT2	0	ASRC1 IN2 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	8	ASRC1_IN1_LOCK_EINT2	0	ASRC1 IN1 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	1	DRC2_SIG_DET_EINT2	0	DRC2 Signal Detect Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	0	DRC1_SIG_DET_EINT2	0	DRC1 Signal Detect Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R6410 (190Ah) IRQ2_Status_11	15	DSP_IRQ16_EINT2	0	DSP IRQ16 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	14	DSP_IRQ15_EINT2	0	DSP IRQ15 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	13	DSP_IRQ14_EINT2	0	DSP IRQ14 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	12	DSP_IRQ13_EINT2	0	DSP IRQ13 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	11	DSP_IRQ12_EINT2	0	DSP IRQ12 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	10	DSP_IRQ11_EINT2	0	DSP IRQ11 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	9	DSP_IRQ10_EINT2	0	DSP IRQ10 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	8	DSP_IRQ9_EINT2	0	DSP IRQ9 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	7	DSP_IRQ8_EINT2	0	DSP IRQ8 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	6	DSP_IRQ7_EINT2	0	DSP IRQ7 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	DSP_IRQ6_EINT2	0	DSP IRQ6 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	DSP_IRQ5_EINT2	0	DSP IRQ5 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	DSP_IRQ4_EINT2	0	DSP IRQ4 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	DSP_IRQ3_EINT2	0	DSP IRQ3 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1	DSP_IRQ2_EINT2	0	DSP IRQ2 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	DSP_IRQ1_EINT2	0	DSP IRQ1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6411 (190Bh) IRQ2_Status_12	7	SPKOUTR_SC_EINT2	0	SPKOUTR Short Circuit Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	6	SPKOUTL_SC_EINT2	0	SPKOUTL Short Circuit Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	5	HP3R_SC_EINT2	0	HPOUT3R Short Circuit Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	HP3L_SC_EINT2	0	HPOUT3L Short Circuit Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	HP2R_SC_EINT2	0	HPOUT2R Short Circuit Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	HP2L_SC_EINT2	0	HPOUT2L Short Circuit Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	HP1R_SC_EINT2	0	HPOUT1R Short Circuit Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	HP1L_SC_EINT2	0	HPOUT1L Short Circuit Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6412 (190Ch) IRQ2_Status_13	7	SPKOUTR_ENABLE_DONE_EINT2	0	SPKOUTR Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	6	SPKOUTL_ENABLE_DONE_EINT2	0	SPKOUTL Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	HP3R_ENABLE_DONE_EINT2	0	HPOUT3R Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	HP3L_ENABLE_DONE_EINT2	0	HPOUT3L Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	HP2R_ENABLE_DONE_EINT2	0	HPOUT2R Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	HP2L_ENABLE_DONE_EINT2	0	HPOUT2L Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	HP1R_ENABLE_DONE_EINT2	0	HPOUT1R Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	HP1L_ENABLE_DONE_EINT2	0	HPOUT1L Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6413 (190Dh) IRQ2_Statu	7	SPKOUTR_DISABLE_DONE_EINT2	0	SPKOUTR Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
s_14	6	SPKOUTL_DISABLE_DONE_EINT2	0	SPKOUTL Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	HP3R_DISABLE_DONE_EINT2	0	HPOUT3R Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	HP3L_DISABLE_DONE_EINT2	0	HPOUT3L Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	HP2R_DISABLE_DONE_EINT2	0	HPOUT2R Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	HP2L_DISABLE_DONE_EINT2	0	HPOUT2L Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	HP1R_DISABLE_DONE_EINT2	0	HPOUT1R Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	HP1L_DISABLE_DONE_EINT2	0	HPOUT1L Disable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6414 (190Eh) IRQ2_Status_15	2	SPK_OVERHEAT_WARN_EINT2	0	Speaker Overheat Warning Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	SPK_OVERHEAT_EINT2	0	Speaker Overheat Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	SPK_SHUTDOWN_EINT2	0	Speaker Shutdown Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R6416 (1910h) IRQ2_Status_17	15	GP16_EINT2	0	GPIO16 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	14	GP15_EINT2	0	GPIO15 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	13	GP14_EINT2	0	GPIO14 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	12	GP13_EINT2	0	GPIO13 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	11	GP12_EINT2	0	GPIO12 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	10	GP11_EINT2	0	GPIO11 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	9	GP10_EINT2	0	GPIO10 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	8	GP9_EINT2	0	GPIO9 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	7	GP8_EINT2	0	GPIO8 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6	GP7_EINT2	0	GPIO7 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	5	GP6_EINT2	0	GPIO6 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	4	GP5_EINT2	0	GPIO5 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	3	GP4_EINT2	0	GPIO4 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	2	GP3_EINT2	0	GPIO3 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	1	GP2_EINT2	0	GPIO2 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	0	GP1_EINT2	0	GPIO1 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R6417 (1911h) IRQ2_Status_18	15	GP32_EINT2	0	GPIO32 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	14	GP31_EINT2	0	GPIO31 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	13	GP30_EINT2	0	GPIO30 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	12	GP29_EINT2	0	GPIO29 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	11	GP28_EINT2	0	GPIO28 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	10	GP27_EINT2	0	GPIO27 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	9	GP26_EINT2	0	GPIO26 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	8	GP25_EINT2	0	GPIO25 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	7	GP24_EINT2	0	GPIO24 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	6	GP23_EINT2	0	GPIO23 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	5	GP22_EINT2	0	GPIO22 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	4	GP21_EINT2	0	GPIO21 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3	GP20_EINT2	0	GPIO20 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	2	GP19_EINT2	0	GPIO19 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	1	GP18_EINT2	0	GPIO18 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	0	GP17_EINT2	0	GPIO17 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R6418 (1912h) IRQ2_Status_19	7	GP40_EINT2	0	GPIO40 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	6	GP39_EINT2	0	GPIO39 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	5	GP38_EINT2	0	GPIO38 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	4	GP37_EINT2	0	GPIO37 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	3	GP36_EINT2	0	GPIO36 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	2	GP35_EINT2	0	GPIO35 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	1	GP34_EINT2	0	GPIO34 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	0	GP33_EINT2	0	GPIO33 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R6420 (1914h) IRQ2_Status_21	7	TIMER8_EINT2	0	Timer 8 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	6	TIMER7_EINT2	0	Timer 7 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	TIMER6_EINT2	0	Timer 6 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	TIMER5_EINT2	0	Timer 5 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	TIMER4_EINT2	0	Timer 4 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	TIMER3_EINT2	0	Timer 3 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	TIMER2_EINT2	0	Timer 2 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	TIMER1_EINT2	0	Timer 1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6421 (1915h) IRQ2_Status_22	7	EVENT8_NOT_EMPTY_EINT2	0	Event Log 8 FIFO Not Empty Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	6	EVENT7_NOT_EMPTY_EINT2	0	Event Log 7 FIFO Not Empty Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	EVENT6_NOT_EMPTY_EINT2	0	Event Log 6 FIFO Not Empty Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	EVENT5_NOT_EMPTY_EINT2	0	Event Log 5 FIFO Not Empty Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	EVENT4_NOT_EMPTY_EINT2	0	Event Log 4 FIFO Not Empty Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	EVENT3_NOT_EMPTY_EINT2	0	Event Log 3 FIFO Not Empty Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	EVENT2_NOT_EMPTY_EINT2	0	Event Log 2 FIFO Not Empty Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	EVENT1_NOT_EMPTY_EINT2	0	Event Log 1 FIFO Not Empty Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6422 (1916h) IRQ2_Status_23	7	EVENT8_FULL_EINT2	0	Event Log 8 FIFO Full Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	6	EVENT7_FULL_EINT2	0	Event Log 7 FIFO Full Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	EVENT6_FULL_EINT2	0	Event Log 6 FIFO Full Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	EVENT5_FULL_EINT2	0	Event Log 5 FIFO Full Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	EVENT4_FULL_EINT2	0	Event Log 4 FIFO Full Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	EVENT3_FULL_EINT2	0	Event Log 3 FIFO Full Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	EVENT2_FULL_EINT2	0	Event Log 2 FIFO Full Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	EVENT1_FULL_EINT2	0	Event Log 1 FIFO Full Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6423 (1917h) IRQ2_Status_24	7	EVENT8_WMARK_EINT2	0	Event Log 8 FIFO Watermark Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	6	EVENT7_WMARK_EINT2	0	Event Log 7 FIFO Watermark Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	5	EVENT6_WMARK_EINT2	0	Event Log 6 FIFO Watermark Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	EVENT5_WMARK_EINT2	0	Event Log 5 FIFO Watermark Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	EVENT4_WMARK_EINT2	0	Event Log 4 FIFO Watermark Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	EVENT3_WMARK_EINT2	0	Event Log 3 FIFO Watermark Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	EVENT2_WMARK_EINT2	0	Event Log 2 FIFO Watermark Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	EVENT1_WMARK_EINT2	0	Event Log 1 FIFO Watermark Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6424 (1918h) IRQ2_Status_25	6	DSP7_DMA_EINT2	0	DSP7 DMA Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	DSP6_DMA_EINT2	00	DSP6 DMA Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	DSP5_DMA_EINT2	00	DSP5 DMA Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	DSP4_DMA_EINT2	00	DSP4 DMA Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	DSP3_DMA_EINT2	00	DSP3 DMA Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	DSP2_DMA_EINT2	00	DSP2 DMA Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	DSP1_DMA_EINT2	00	DSP1 DMA Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6426 (191Ah) IRQ2_Status_27	6	DSP7_START1_EINT2	0	DSP7 Start 1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	DSP6_START1_EINT2	0	DSP6 Start 1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	DSP5_START1_EINT2	0	DSP5 Start 1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	DSP4_START1_EINT2	0	DSP4 Start 1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	DSP3_START1_EINT2	0	DSP3 Start 1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	DSP2_START1_EINT2	0	DSP2 Start 1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	DSP1_START1_EINT2	0	DSP1 Start 1 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6427 (191Bh) IRQ2_Status_28	6	DSP7_START2_EINT2	0	DSP7 Start 2 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	DSP6_START2_EINT2	0	DSP6 Start 2 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	DSP5_START2_EINT2	0	DSP5 Start 2 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	DSP4_START2_EINT2	0	DSP4 Start 2 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	DSP3_START2_EINT2	0	DSP3 Start 2 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	DSP2_START2_EINT2	0	DSP2 Start 2 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	DSP1_START2_EINT2	0	DSP1 Start 2 Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6429 (191Dh) IRQ2_Status_30	6	DSP7_BUSY_EINT2	0	DSP7 Busy Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	DSP6_BUSY_EINT2	0	DSP6 Busy Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	4	DSP5_BUSY_EINT2	0	DSP5 Busy Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	DSP4_BUSY_EINT2	0	DSP4 Busy Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	2	DSP3_BUSY_EINT2	0	DSP3 Busy Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	DSP2_BUSY_EINT2	0	DSP2 Busy Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	DSP1_BUSY_EINT2	0	DSP1 Busy Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6430 (191Eh) IRQ2_Status_31	2	MIF3_DONE_EINT2	0	MIF3 Done Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	MIF2_DONE_EINT2	0	MIF2 Done Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	MIF1_DONE_EINT2	0	MIF1 Done Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6431 (191Fh) IRQ2_Statu	2	MIF3_BLOCK_EINT2	0	MIF3 Block Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
s_32	1	MIF2_BLOCK_EINT2	0	MIF2 Block Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	MIF1_BLOCK_EINT2	0	MIF1 Block Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R6464 (1940h) to R6495 (195Fh)		IM_*	1	For each *_EINT2 interrupt register in R6400 to R6431, a corresponding mask bit (IM_*) is provided in R6464 to R6495. The mask bits are coded as: 0 = Do not mask interrupt 1 = Mask interrupt
R6528 (1980h) IRQ2_Raw_Status_1	12	CTRLIF_ERR_STS2	0	Control Interface Error Status 0 = Normal 1 = Control Interface Error
	7	BOOT_DONE_STS2	0	Boot Status 0 = Busy (boot sequence in progress) 1 = Idle (boot sequence completed) Control register writes should not be attempted until Boot Sequence has completed.
R6529 (1981h) IRQ2_Raw_Status_2	10	FLL3_LOCK_STS2	0	FLL3 Lock Status 0 = Not locked 1 = Locked
	9	FLL2_LOCK_STS2	0	FLL2 Lock Status 0 = Not locked 1 = Locked
	8	FLL1_LOCK_STS2	0	FLL1 Lock Status 0 = Not locked 1 = Locked
R6534 (1986h) IRQ2_Raw_Status_7	4	MICD_CLAMP_STS2	0	MICDET Clamp status 0 = Clamp not active 1 = Clamp active
	2	JD2_STS2	0	JACKDET2 input status 0 = Jack not detected 1 = Jack is detected (Assumes the JACKDET2 pin is pulled 'low' on Jack insertion.)
	0	JD1_STS2	0	JACKDET1 input status 0 = Jack not detected 1 = Jack is detected (Assumes the JACKDET1 pin is pulled 'low' on Jack insertion.)
R6536 (1988h) IRQ2_Raw_Status_9	11	ASRC2_IN2_LOCK_STS2	0	ASRC2 IN2 Lock Status 0 = Not locked 1 = Locked
	10	ASRC2_IN1_LOCK_STS2	0	ASRC2 IN1 Lock Status 0 = Not locked 1 = Locked
	9	ASRC1_IN2_LOCK_STS2	0	ASRC1 IN2 Lock Status 0 = Not locked 1 = Locked
	8	ASRC1_IN1_LOCK_STS2	0	ASRC1 IN1 Lock Status 0 = Not locked 1 = Locked
	1	DRC2_SIG_DET_STS2	0	DRC2 Signal Detect Status 0 = Normal 1 = Signal detected

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	DRC1_SIG_DET_STS2	0	DRC1 Signal Detect Status 0 = Normal 1 = Signal detected
R6539 (198Bh) IRQ2_Raw_Status_12	7	SPKOUTR_SC_STS2	0	SPKOUTR Short Circuit Status 0 = Normal 1 = Short Circuit detected
	6	SPKOUTL_SC_STS2	0	SPKOUTL Short Circuit Status 0 = Normal 1 = Short Circuit detected
	5	HP3R_SC_STS2	0	HPOUT3R Short Circuit Status 0 = Normal 1 = Short Circuit detected
	4	HP3L_SC_STS2	0	HPOUT3L Short Circuit Status 0 = Normal 1 = Short Circuit detected
	3	HP2R_SC_STS2	0	HPOUT2R Short Circuit Status 0 = Normal 1 = Short Circuit detected
	2	HP2L_SC_STS2	0	HPOUT2L Short Circuit Status 0 = Normal 1 = Short Circuit detected
	1	HP1R_SC_STS2	0	HPOUT1R Short Circuit Status 0 = Normal 1 = Short Circuit detected
	0	HP1L_SC_STS2	0	HPOUT1L Short Circuit Status 0 = Normal 1 = Short Circuit detected
R6540 (198Ch) IRQ2_Raw_Status_13	7	SPKOUTR_ENABLE_DONE_STS2	0	SPKOUTR Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	6	SPKOUTL_ENABLE_DONE_STS2	0	SPKOUTL Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	5	HP3R_ENABLE_DONE_STS2	0	HPOUT3R Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	4	HP3L_ENABLE_DONE_STS2	0	HPOUT3L Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	3	HP2R_ENABLE_DONE_STS2	0	HPOUT2R Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	2	HP2L_ENABLE_DONE_STS2	0	HPOUT2L Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	1	HP1R_ENABLE_DONE_STS2	0	HPOUT1R Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	0	HP1L_ENABLE_DONE_STS2	0	HPOUT1L Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
R6541 (198Dh) IRQ2_Raw_Status_14	7	SPKOUTR_DISABLE_DONE_STS2	0	SPKOUTR Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	6	SPKOUTL_DISABLE_DONE_STS2	0	SPKOUTL Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	5	HP3R_DISABLE_DONE_STS2	0	HPOUT3R Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	4	HP3L_DISABLE_DONE_STS2	0	HPOUT3L Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	3	HP2R_DISABLE_DONE_STS2	0	HPOUT2R Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	2	HP2L_DISABLE_DONE_STS2	0	HPOUT2L Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	1	HP1R_DISABLE_DONE_STS2	0	HPOUT1R Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	0	HP1L_DISABLE_DONE_STS2	0	HPOUT1L Disable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
R6542 (198Eh) IRQ2_Raw_Status_15	2	SPK_OVERHEAT_WARN_STS2	0	Speaker Overheat Warning Status 0 = Normal 1 = Warning temperature exceeded
	1	SPK_OVERHEAT_STS2	0	Speaker Overheat Status 0 = Normal 1 = Shutdown temperature exceeded
	0	SPK_SHUTDOWN_STS2	0	Speaker Shutdown Status 0 = Normal 1 = Speaker Shutdown completed (due to Overheat Temperature or Short Circuit condition)
R6544 (1990h) IRQ2_Raw_Status_17	15	GP16_STS2	0	GPIOn Input status Reads back the logic level of GPIOn. Only valid for pins configured as GPIO input (does not include DSPGPIO inputs).
	14	GP15_STS2	0	
	13	GP14_STS2	0	
	12	GP13_STS2	0	
	11	GP12_STS2	0	
	10	GP11_STS2	0	
	9	GP10_STS2	0	
	8	GP9_STS2	0	
	7	GP8_STS2	0	
	6	GP7_STS2	0	
	5	GP6_STS2	0	
	4	GP5_STS2	0	
	3	GP4_STS2	0	
	2	GP3_STS2	0	
	1	GP2_STS2	0	
	0	GP1_STS2	0	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6545 (1991h) IRQ2_Raw _Status_18	15	GP32_STS2	0	GPIOn Input status Reads back the logic level of GPIOn. Only valid for pins configured as GPIO input (does not include DSPGPIO inputs).
	14	GP31_STS2	0	
	13	GP30_STS2	0	
	12	GP29_STS2	0	
	11	GP28_STS2	0	
	10	GP27_STS2	0	
	9	GP26_STS2	0	
	8	GP25_STS2	0	
	7	GP24_STS2	0	
	6	GP23_STS2	0	
	5	GP22_STS2	0	
	4	GP21_STS2	0	
	3	GP20_STS2	0	
	2	GP19_STS2	0	
	1	GP18_STS2	0	
	0	GP17_STS2	0	
R6546 (1992h) IRQ2_Raw _Status_19	7	GP40_STS2	0	GPIOn Input status Reads back the logic level of GPIOn. Only valid for pins configured as GPIO input (does not include DSPGPIO inputs).
	6	GP39_STS2	0	
	5	GP38_STS2	0	
	4	GP37_STS2	0	
	3	GP36_STS2	0	
	2	GP35_STS2	0	
	1	GP34_STS2	0	
	0	GP33_STS2	0	
R6549 (1995h) IRQ2_Raw _Status_22	7	EVENT8_NOT_EMPTY_STS2	0	Event Log n FIFO Not Empty status 0 = FIFO Empty 1 = FIFO Not Empty
	6	EVENT7_NOT_EMPTY_STS2	0	
	5	EVENT6_NOT_EMPTY_STS2	0	
	4	EVENT5_NOT_EMPTY_STS2	0	
	3	EVENT4_NOT_EMPTY_STS2	0	
	2	EVENT3_NOT_EMPTY_STS2	0	
	1	EVENT2_NOT_EMPTY_STS2	0	
	0	EVENT1_NOT_EMPTY_STS2	0	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6550 (1996h) IRQ2_Raw _Status_23	7	EVENT8_FULL_ STS2	0	Event Log n FIFO Full status 0 = FIFO Not Full 1 = FIFO Full
	6	EVENT7_FULL_ STS2	0	
	5	EVENT6_FULL_ STS2	0	
	4	EVENT5_FULL_ STS2	0	
	3	EVENT4_FULL_ STS2	0	
	2	EVENT3_FULL_ STS2	0	
	1	EVENT2_FULL_ STS2	0	
	0	EVENT1_FULL_ STS2	0	
R6551 (1997h) IRQ2_Raw _Status_24	7	EVENT8_WMAR K_STS2	0	Event Log n FIFO Watermark status 0 = FIFO Watermark not reached 1 = FIFO Watermark reached
	6	EVENT7_WMAR K_STS2	0	
	5	EVENT6_WMAR K_STS2	0	
	4	EVENT5_WMAR K_STS2	0	
	3	EVENT4_WMAR K_STS2	0	
	2	EVENT3_WMAR K_STS2	0	
	1	EVENT2_WMAR K_STS2	0	
	0	EVENT1_WMAR K_STS2	0	
R6552 (1998h) IRQ2_Raw _Status_25	6	DSP7_DMA_STS 2	0	DSPn DMA status 0 = Normal 1 = All enabled WDMA buffers filled, and all enabled RDMA buffers emptied
	5	DSP6_DMA_STS 2	00	
	4	DSP5_DMA_STS 2	00	
	3	DSP4_DMA_STS 2	00	
	2	DSP3_DMA_STS 2	00	
	1	DSP2_DMA_STS 2	00	
	0	DSP1_DMA_STS 2	00	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6557 (199Dh) IRQ2_Raw _Status_30	6	DSP7_BUSY_ST S2	0	DSPn Busy status 0 = DSP Idle 1 = DSP Busy
	5	DSP6_BUSY_ST S2	0	
	4	DSP5_BUSY_ST S2	0	
	3	DSP4_BUSY_ST S2	0	
	2	DSP3_BUSY_ST S2	0	
	1	DSP2_BUSY_ST S2	0	
	0	DSP1_BUSY_ST S2	0	

Table 101 Interrupt 2 Control Registers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6784 (1A80h) IRQ1_CTR L	11	IM_IRQ1	0	IRQ1 Output Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt.
	10	IRQ_POL	1	IRQ Output Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)
	9	IRQ_OP_CFG	0	IRQ Output Configuration 0 = CMOS 1 = Open Drain
R6786 (1A82h) IRQ2_CTR L	11	IM_IRQ2	0	IRQ2 Output Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt.
R6816 (1AA0h) Interrupt_R aw_Status_ 1	1	IRQ2_STS	0	IRQ2 Status IRQ2_STS is the logical 'OR' of all unmasked _EINT2 interrupts. 0 = Not asserted 1 = Asserted
	0	IRQ1_STS	0	IRQ1 Status IRQ1_STS is the logical 'OR' of all unmasked _EINT1 interrupts. 0 = Not asserted 1 = Asserted

Table 102 Interrupt Control Registers

CLOCKING AND SAMPLE RATES

The CS47L85 requires a clock reference for its internal functions and also for the input (ADC) paths, output (DAC) paths and digital audio interfaces. Under typical clocking configurations, all commonly-used audio sample rates can be derived directly from the external reference; for additional flexibility, the CS47L85 incorporates three Frequency Locked Loop (FLL) circuits to perform frequency conversion and filtering.

External clock signals may be connected via MCLK1 and MCLK2. (These inputs are referenced to the DBVDD1 and DBVDD2 power domains respectively.) In AIF Slave modes, the BCLK signals may be used as a reference for the system clocks. The SLIMbus interface can provide the clock reference, when used as the input to one of the FLLs. To avoid audible glitches, all clock configurations must be set up before enabling playback.

SYSTEM CLOCKING

The CS47L85 supports three primary clock domains - SYSCLK, ASYNCLK, and DSPCLK.

The SYSCLK and ASYNCCLK clock domains are the reference clocks for all the audio signal paths on the CS47L85. Up to five different sample rates may be independently selected for specific audio interfaces and other input/output signal paths; each selected sample rate must be synchronised either to SYSCLK or to ASYNCCLK, as described later.

The SYSCLK and ASYNCCLK clock domains are independent (i.e., not synchronised). Stereo full-duplex sample rate conversion is supported, allowing asynchronous audio data to be mixed and to be routed between independent interfaces. See “Digital Core” for further details.

The DSPCLK clock domain is the reference clock for the programmable DSP Cores on the CS47L85. A wide range of DSPCLK frequencies can be supported, and a programmable clock divider is provided for each DSP Core, allowing the DSP clocking (and power consumption) to be optimised according to the applicable processing requirements of each DSP Core. See “DSP Firmware Control” for further details.

Note that there is no requirement for DSPCLK to be synchronised to SYSCLK or ASYNCCLK. The DSPCLK controls the software execution in the DSP Cores; audio outputs from the DSP Cores may be synchronised either to SYSCLK or ASYNCCLK, regardless of the applicable DSPCLK rate.

Excluding the DSP Cores, each subsystem within the CS47L85 digital core is clocked at a dynamically-controlled rate, limited by the SYSCLK (or ASYNCCLK) frequency, as applicable. For maximum signal mixing and processing capacity, it is recommended that the highest possible SYSCLK and ASYNCCLK frequencies are configured.

The DSP Cores are clocked at the DSPCLK rate (or supported divisions of the DSPCLK frequency). The DSPCLK configuration must ensure that sufficient clock cycles are available for the processing requirements of each DSP Core. The requirements will vary, according to the particular software that is in use.

SAMPLE RATE CONTROL

The CS47L85 supports two independent clock domains for the audio signal paths, referenced to SYSCLK and ASYNCCLK respectively.

Different sample rates may be selected for each of the audio interfaces (AIF1, AIF2, AIF3, AIF4, SLIMbus), and for the input (ADC) and output (DAC) paths. Each of these must be referenced either to SYSCLK or to ASYNCCLK. (Note that the SLIMbus interface supports multiple sample rates, selected independently for each input or output channel.)

The CS47L85 can support a maximum of five different sample rates at any time. The supported sample rates range from 8kHz to 192kHz.

Up to three different sample rates can be selected using the SAMPLE_RATE_1, SAMPLE_RATE_2 and SAMPLE_RATE_3 registers. These must each be numerically related to each other and to the SYSCLK frequency (further details of these requirements are provided in Table 103 and the accompanying text).

The remaining two sample rates can be selected using the ASYNC_SAMPLE_RATE_1 and ASYNC_SAMPLE_RATE_2 registers. These sample rates must be numerically related to each other and to the ASYNCCLK frequency (further details of these requirements are provided in Table 104 and the accompanying text),

Each of the audio interfaces, input paths and output paths is associated with one of the sample rates selected by the SAMPLE_RATE_n or ASYNC_SAMPLE_RATE_n registers.

Note that if any two interfaces are operating at the same sample rate, but are not synchronised, then one of these must be referenced to the ASYNCCLK domain, and the other to the SYSCLK domain.

Note that, when any of the SAMPLE_RATE_n or ASYNC_SAMPLE_RATE_n registers is written to, the activation of the new setting is automatically synchronised by the CS47L85 to ensure continuity of all active signal paths. The SAMPLE_RATE_n_STS and ASYNC_SAMPLE_RATE_n_STS registers provide readback of the sample rate selections that have been implemented.

There are some restrictions to be observed regarding the sample rate control configuration, as noted below:

- The input (ADC / Digital Microphone) and output (DAC) signal paths must always be associated with the SYSCLK clocking domain.
- All external clock references (MCLK input or Slave mode AIF input) must be within 1% of the applicable register setting(s).
- The input (ADC / DMIC) sample rate is valid from 8kHz to 192kHz. If 384kHz or 768kHz DMIC clock rate is selected on any of the input paths, then the supported sample rate is valid only up to 48kHz or 96kHz respectively.
- The S/PDIF sample rate is valid from 32kHz to 192kHz.
- The Asynchronous Sample Rate Converters (ASRCs) support sample rates 8kHz to 192kHz. For each ASRC, the ratio of the two sample rates must not exceed 6.
- The Isochronous Sample Rate Converters (ISRCs) support sample rates 8kHz to 192kHz. For each ISRC, the higher sample rate must be an integer multiple of the lower rate.

AUTOMATIC SAMPLE RATE DETECTION

The CS47L85 supports automatic sample rate detection on the digital audio interfaces (AIF1, AIF2, AIF3 and AIF4). Note that this is only possible when the respective interface is operating in Slave mode (i.e., when LRCLK and BCLK are inputs to the CS47L85).

Automatic sample rate detection is enabled using the RATE_EST_ENA register bit. The LRCLK input pin selected for sample rate detection is set using the LRCLK_SRC register.

Up to four audio sample rates can be configured for automatic detection; these sample rates are selected using the SAMPLE_RATE_DETECT_n registers. Note that the function will only detect sample rates that match one of the SAMPLE_RATE_DETECT_n registers.

If one of the selected audio sample rates is detected on the selected LRCLK input, then a Control Write Sequence will be triggered. A unique sequence of actions may be programmed for each of the detected sample rates. Note that the applicable control sequences must be programmed by the user for each detection outcome. See “Control Write Sequencer” for further details.

The TRIG_ON_STARTUP register controls whether the sample rate detection circuit responds to the initial detection of the applicable interface (i.e., when the AIFn interface starts up).

When TRIG_ON_STARTUP=0, then the detection circuit will only respond (i.e., trigger the Control Write Sequencer) to a change in the detected sample rate - the initial sample rate detection will be ignored. (Note that the ‘initial sample rate detection’ is the first detection of a sample rate that matches one of the SAMPLE_RATE_DETECT_n registers.)

When TRIG_ON_STARTUP=1, then the detection circuit will trigger the Control Write Sequencer whenever a selected sample rate is detected, including when the AIF interface starts up, or when the sample rate detection is first enabled.

As described above, setting TRIG_ON_STARTUP=0 is designed to inhibit any response to the initial detection of a sample rate that matches one of the SAMPLE_RATE_DETECT_n registers. Note that, if the LRCLK_SRC setting is changed, or if the detection function is disabled and re-enabled, then a subsequent detection of a matching sample rate may trigger the Control Write Sequencer, regardless of the TRIG_ON_STARTUP setting.

There are some restrictions to be observed regarding the automatic sample rate detection, as noted below:

- The same sample rate must not be selected on more than one of the SAMPLE_RATE_DETECT_n registers.
- Sample rates 192kHz and 176.4kHz must not be selected concurrently.
- Sample rates 96kHz and 88.2kHz must not be selected concurrently.

The control registers associated with the automatic sample rate detection function are described in Table 105.

SYSCLK AND ASYNCCLK CONTROL

The SYSCLK and ASYNCCLK clocks may be provided directly from external inputs (MCLK, or slave mode BCLK inputs). Alternatively, the SYSCLK and ASYNCCLK clocks can be derived using the integrated FLL(s), with MCLK, BCLK, LRCLK or SLIMCLK as a reference.

The required SYSCLK frequency is dependent on the SAMPLE_RATE_n registers. Table 103 illustrates the valid SYSCLK frequencies for every supported sample rate.

The SYSCLK_FREQ and SYSCLK_FRAC registers are used to identify the applicable SYSCLK frequency. It is recommended that the highest possible SYSCLK frequency is selected.

The chosen SYSCLK frequency must be valid for all of the SAMPLE_RATE_n registers. It follows that all of the SAMPLE_RATE_n registers must select numerically-related values, i.e., all from the same cell as represented in Table 103.

Sample Rate	SAMPLE_RATE_n	SYSCLK Frequency	SYSCLK_FREQ	SYSCLK_FRAC
12kHz 24kHz 48kHz 96kHz 192kHz 8kHz 16kHz 32kHz	01h 02h 03h 04h 05h 11h 12h 13h	6.144MHz, 12.288MHz, 24.576MHz, 49.152MHz, or 98.304MHz	000, 001, 010, 011, or 100	0
11.025kHz 22.05kHz 44.1kHz 88.2kHz 176.4kHz	09h 0Ah 0Bh 0Ch 0Dh	5.6448MHz, 11.2896MHz, 22.5792MHz, 45.1584MHz, or 90.3168MHz	000, 001, 010, 011, or 100	1
Note that each of the SAMPLE_RATE_n registers must select a sample rate value from the same group in the two lists above.				

Table 103 SYSCLK Frequency Selection

The required ASYNCCLK frequency is dependent on the ASYNC_SAMPLE_RATE_n registers. Table 104 illustrates the valid ASYNCCLK frequencies for every supported sample rate.

The ASYNC_CLK_FREQ register is used to identify the applicable ASYNCCLK frequency. It is recommended that the highest possible ASYNCCLK frequency is selected.

Note that, if all the sample rates in the system are synchronised to SYSCLK, then the ASYNCCLK may not be required at all. In this case, the ASYNCCLK should be disabled (see Table 105), and the associated register values are not important.

Sample Rate	ASYNC_SAMPLE_RATE_n	ASYNCCLK Frequency	ASYNC_CLK_FREQ
12kHz 24kHz 48kHz 96kHz 192kHz 8kHz 16kHz 32kHz	01h 02h 03h 04h 05h 11h 12h 13h	6.144MHz, 12.288MHz, 24.576MHz, 49.152MHz or 98.304MHz	000, 001, 010, 011 or 100
11.025kHz 22.05kHz 44.1kHz 88.2kHz 176.4kHz	09h 0Ah 0Bh 0Ch 0Dh	5.6448MHz, 11.2896MHz, 22.5792MHz, 45.1584MHz or 90.3168MHz	000, 001, 010, 011 or 100
Note that each of the ASYNC_SAMPLE_RATE_n registers must select a sample rate value from the same group in the two lists above.			

Table 104 ASYNCCLK Frequency Selection

The CS47L85 supports automatic clocking configuration. The programmable dividers associated with the ADCs, DACs and all DSP functions are configured automatically, with values determined from the SYSCLK_FREQ, SAMPLE_RATE_n, ASYNC_CLK_FREQ and ASYNC_SAMPLE_RATE_n fields.

Note that the digital audio interface (AIF) clocking rates must be configured separately.

The sample rates of each AIF, the input (ADC) paths, output (DAC) paths and DSP functions are selected as described in the respective sections. Stereo full-duplex sample rate conversion is supported in multiple configurations to allow digital audio to be routed between interfaces and for asynchronous audio data to be mixed. See “Digital Core” for further details.

The SYSCLK_SRC register is used to select the SYSCLK source, as described in Table 105. The source may be MCLKn, AIFnBCLK or FLLn. If one of the Frequency Locked Loop (FLL) circuits is selected as the source, then the relevant FLL must be enabled and configured, as described later.

The SYSCLK_FREQ and SYSCLK_FRAC registers are set according to the frequency of the selected SYSCLK source. Note that the FLLn oscillator frequency is divided by three, when used as the SYSCLK source, as shown in Figure 74 and Figure 76. Accordingly, the FLLs can support SYSCLK frequencies in the range 90MHz to 100MHz.

The SYSCLK-referenced circuits within the digital core are clocked at a dynamically-controlled rate, limited by the SYSCLK frequency itself. For maximum signal mixing and processing capacity, it is recommended that the highest possible SYSCLK frequency is configured.

The SAMPLE_RATE_n registers are set according to the sample rate(s) that are required by one or more of the CS47L85 audio interfaces. The CS47L85 supports sample rates ranging from 8kHz to 192kHz.

The SYSCLK signal is enabled by the register bit SYSCLK_ENA. The applicable clock source (MCLKn, AIFnBCLK or FLLn) must be enabled before setting SYSCLK_ENA=1. This bit must be cleared to 0 when reconfiguring the SYSCLK source or frequency. The SYSCLK_ENA bit should also be cleared to 0 before stopping or removing the applicable clock source.

The SYSCLK signal is the reference clock for many different subsystems on the CS47L85. All of the SYSCLK-dependent subsystems should be disabled if SYSCLK is not enabled. The SYSCLK_ENA bit must be set to 1 before enabling any SYSCLK-dependent function, and all the dependent functions should be disabled before clearing the SYSCLK_ENA bit to 0.

The SYSCLK-dependent subsystems are referenced below; if one or more of the following conditions is met, then the SYSCLK signal is required, and should not be interrupted or reconfigured.

- Input signal path enabled (INnx_ENA=1)
- Output signal path enabled (OUTnx_ENA=1, SPKOUTx_ENA=1, HPnx_ENA=1)
- Digital Core Mixer enabled (*_SRCn>00h)
- EQ, DRC, or LHPF processor enabled (EQn_ENA=1, DRCnx_ENA=1, LHPFn_ENA=1)
- SPDIF output enabled (SPD1_ENA=1)
- Tone generator enabled (TONEn_ENA=1)
- Noise generator enabled (NOISE_GEN_ENA=1)
- Haptic generator enabled (HAP_CTRL>00)
- PWM generator enabled (PWMn_ENA=1)
- ASRC channel enabled (ASRCn_INmL_ENA=1, ASRCn_INmR_ENA=1)
- ISRC channel enabled (ISRCn_INTm_ENA=1, ISRCn_DECm_ENA=1)
- Digital audio interface path enabled (AIFnTXm_ENA=1, AIFnRXm_ENA=1)
- Digital audio interface clocks enabled (AIFn_BCLK_FRC=1, AIFn_LRCLK_FRC=1)
- SLIMbus framer mode enabled (note - only applies if SLIMCLK_SRC=0)
- SLIMbus data channel enabled (SLIMTXn_ENA=1, SLIMRXn_ENA=1)
- DSP Core firmware requires access to registers below 0x40000
- Timer enabled, with SYSCLK as clock source (TIMERn_RUNNING_STS=1 and TIMERn_REFCLK_SRC=8h)
- ANC processor enabled (CLK_L_ENA_SET=1, CLK_NG_ENA=1, CLK_R_ENA_SET=1)
- OPCLK enabled for GPIO output (OPCLK_ENA=1)

If reconfiguration of the SYSCLK source or frequency is required, and it is not possible to disable all of the SYSCLK-dependent subsystems, then the Control Write Sequencer must be used for the reconfiguration of SYSCLK. The control sequence should apply the following actions:

- Clear SYSCLK_ENA to 0
- Write updates to SYSCLK_SRC, SYSCLK_FREQ, and SYSCLK_FRAC
- Set SYSCLK_ENA to 1

The ASYNC_CLK_SRC register is used to select the ASYNCCLK source, as described in Table 105. The source may be MCLKn, AIFnBCLK or FLLn. If one of the Frequency Locked Loop (FLL) circuits is selected as the source, then the relevant FLL must be enabled and configured, as described later.

The ASYNC_CLK_FREQ register is set according to the frequency of the selected ASYNCCLK source. Note that the FLLn output frequency is divided by three, when used as the ASYNCCLK source. The FLLs can support ASYNCCLK frequencies in the range 90MHz to 100MHz.

The ASYNCCLK-referenced circuits within the digital core are clocked at a dynamically-controlled rate, limited by the ASYNCCLK frequency itself. For maximum signal mixing and processing capacity, it is recommended that the highest possible ASYNCCLK frequency is configured.

The ASYNC_SAMPLE_RATE_n registers are set according to the sample rate(s) of any audio interface that is not synchronised to the SYSCLK clock domain.

The ASYNCCLK signal is enabled by the register bit ASYNC_CLK_ENA. The applicable clock source (MCLKn, AIFnBCLK or FLLn) must be enabled before setting ASYNC_CLK_ENA=1. This bit must be cleared to 0 when reconfiguring the ASYNCCLK source or frequency. The ASYNC_CLK_ENA bit should also be cleared to 0 before stopping or removing the applicable clock source.

The SYSCLK (and ASYNCCLK, when applicable) clocks must be configured and enabled before any audio path is enabled.

The CS47L85 performs automatic checks to confirm that the SYSCLK and ASYNCCLK frequencies are high enough to support the commanded signal paths and processing functions. If an attempt is made to enable a signal path or processing function, and there are insufficient SYSCLK or ASYNCCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

DSPCLK CONTROL

The DSPCLK clock may be provided directly from external inputs (MCLK, or slave mode BCLK inputs). Alternatively, DSPCLK can be derived using the integrated FLL(s), with MCLK, BCLK, LRCLK or SLIMCLK as a reference.

Note that a configurable clock divider is provided for each DSP Core, allowing the DSP clocking (and power consumption) to be optimised according to the applicable processing requirements of each DSP Core. See “DSP Firmware Control” for further details.

The DSP Cores are clocked at the DSPCLK rate (or supported divisions of the DSPCLK frequency). The DSPCLK configuration must ensure that sufficient clock cycles are available for the processing requirements of each DSP Core. The requirements will vary, according to the particular software that is in use.

The DSP_CLK_SRC register is used to select the DSPCLK source, as described in Table 105. The source may be MCLKn, AIFnBCLK or FLLn. If one of the Frequency Locked Loop (FLL) circuits is selected as the source, then the relevant FLL must be enabled and configured, as described later.

In most cases, the FLL output frequency is divided by two, when used as the DSPCLK source; this enables DSPCLK frequencies in the range 135MHz to 150MHz. For FLL1 only, a ‘divide by 6’ option is also available, supporting low power DSP operation with DSPCLK frequencies in the range 45MHz to 50MHz.

The DSPCLK signal is enabled by the register bit DSP_CLK_ENA. The applicable clock source (MCLKn, AIFnBCLK or FLLn) must be enabled before setting DSP_CLK_ENA=1. This bit must be cleared to 0 when reconfiguring the clock sources.

The DSP_CLK_FREQ_RANGE register must be configured for the applicable DSPCLK frequency. Note that, if the DSPCLK frequency is equal to one of the threshold frequencies quoted, then the higher range setting should be selected. For example, if the DSPCLK frequency is 37.5MHz, then DSP_CLK_FREQ_RANGE should be set to 011.

In a typical application, DSPCLK and SYSCLK are derived from a single FLL source. In this case, one of the nominal DSPCLK frequencies is likely to be applicable (see Table 105).

Note that there is no requirement for DSPCLK to be synchronised to SYSCLK or ASYNCCLK. The DSPCLK controls the

software execution in the DSP Cores; audio outputs from the DSP Cores may be synchronised either to SYSCLK or ASYNCCLK, regardless of the applicable DSPCLK rate.

The DSPCLK signal is the reference clock for the DSP cores and DSP peripherals on the CS47L85. All of the DSPCLK-dependent functions should be disabled if DSPCLK is not enabled. The DSPCLK_ENA bit must be set to 1 before enabling any DSPCLK-dependent function, and all the dependent functions should be disabled before clearing the DSPCLK_ENA bit to 0.

The DSPCLK-dependent subsystems are referenced below; if one or more of the following conditions is met, then the DSPCLK signal is required, and should not be interrupted or reconfigured.

- DSP core enabled (DSPn_CORE_ENA=1)
- DSP DMA function enabled (DSPn_[WDMA/RDMA]_CHANNEL_ENABLE>00h)
- DSP core in JTAG mode
- Master Interface active (MIFn_BUSY_STS=1)
- Timer enabled (TIMERn_RUNNING_STS=1)

If reconfiguration of the DSPCLK source or frequency is required, and it is not possible to disable all of the DSPCLK-dependent functions, then the following control requirements must be applied to reconfigure DSPCLK:

- Clear DSP_CLK_ENA to 0
- Wait 34us (only required if a Timer is enabled)
- Update DSP_CLK_SRC and DSP_CLK_FREQ_RANGE, and set DSP_CLK_ENA=1. (These must be applied in a single register write operation)
- If a DSP core is enabled, DMA function is enabled, DSP core is in JTAG mode, or a Master Interface is active, then no other register read/write actions (either by Control Interface or by DSP firmware access) can be permitted during this control sequence.
- If a Timer is enabled, but no DSP core, DMA, JTAG, or MIF is active, then DSPCLK can be stopped at any time. The minimum wait time of 34us is required before changing DSP_CLK_SRC or DSP_CLK_FREQ_RANGE, but there are no other constraints on configuring DSPCLK in these circumstances.

  If DSPCLK is the Timer clock source, the Timer pauses when DSPCLK stops, and resumes operation when DSPCLK restarts. If DSPCLK is not the clock source, the Timer operation continues when DSPCLK stops, but the Timer no longer synchronises to DSPCLK.

MISCELLANEOUS CLOCK CONTROLS

The CS47L85 incorporates a 32kHz clock circuit, which is required for input signal de-bounce, Microphone/Accessory detect, and for the Charge Pump 2 (CP2) circuits. The 32kHz clock must be configured and enabled whenever any of these features are in use.

The 32kHz clock can be generated automatically from SYSCLK, or may be input directly as MCLK1 or MCLK2. The 32kHz clock source is selected using the CLK_32K_SRC register. The 32kHz clock is enabled using the CLK_32K_ENA register.

A clock output (OPCLK) derived from SYSCLK can be output on a GPIO pin. See “General Purpose Input / Output” to configure a GPIO pin for this function.

A clock output (OPCLK_ASYNC) derived from ASYNCCLK can be output on a GPIO pin. See “General Purpose Input / Output” to configure a GPIO pin for this function.

The CS47L85 provides integrated pull-down resistors on the MCLK1 and MCLK2 pins. This provides a flexible capability for interfacing with other devices.

The clocking scheme for the CS47L85 is illustrated in Figure 74.

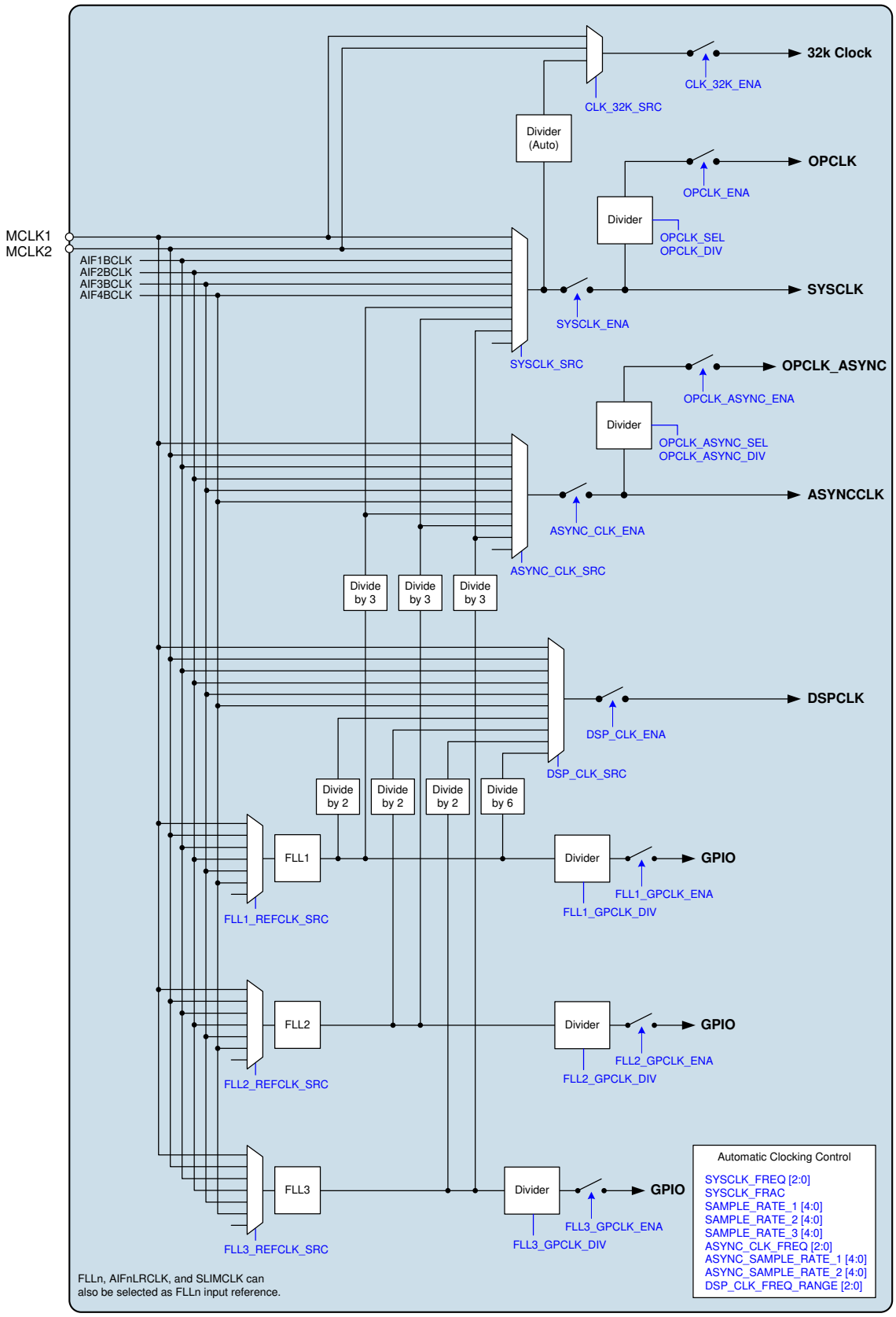


Figure 74 System Clocking

The CS47L85 clocking control registers are described in Table 105.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R256 (0100h) Clock_32k_1	6	CLK_32K_ENA	0	32kHz Clock Enable 0 = Disabled 1 = Enabled
	1:0	CLK_32K_SRC [1:0]	10	32kHz Clock Source 00 = MCLK1 (direct) 01 = MCLK2 (direct) 10 = SYSCLK (automatically divided) 11 = Reserved
R257 (0101h) System_Clock_1	15	SYSCLK_FRAC	0	SYSCLK Frequency 0 = SYSCLK is a multiple of 6.144MHz 1 = SYSCLK is a multiple of 5.6448MHz
	10:8	SYSCLK_FREQ [2:0]	101	SYSCLK Frequency 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) 100 = 98.304MHz (90.3168MHz) All other codes are Reserved The frequencies in brackets apply for 44.1kHz-related sample rates only (i.e., SAMPLE_RATE_n = 01XXX).
	6	SYSCLK_ENA	0	SYSCLK Control 0 = Disabled 1 = Enabled SYSCLK should only be enabled after the applicable clock source has been configured and enabled. Set this bit to 0 when reconfiguring the clock sources. All SYSCLK-dependent functions should be disabled before clearing SYSCLK_ENA=0. Specific control sequences must be followed if reconfiguring SYSCLK while dependent functions are enabled.
	3:0	SYSCLK_SRC [3:0]	0100	SYSCLK Source 0000 = MCLK1 0001 = MCLK2 0100 = FLL1 0101 = FLL2 0110 = FLL3 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK 1011 = AIF4BCLK All other codes are Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R258 (0102h) Sample_rate_1	4:0	SAMPLE_RATE_1 [4:0]	10001	Sample Rate 1 Select 00h = None 01h = 12kHz 02h = 24kHz 03h = 48kHz 04h = 96kHz 05h = 192kHz 09h = 11.025kHz 0Ah = 22.05kHz 0Bh = 44.1kHz 0Ch = 88.2kHz 0Dh = 176.4kHz 11h = 8kHz 12h = 16kHz 13h = 32kHz All other codes are Reserved
R259 (0103h) Sample_rate_2	4:0	SAMPLE_RATE_2 [4:0]	10001	Sample Rate 2 Select *Register coding is same as SAMPLE_RATE_1.*
R260 (0104h) Sample_rate_3	4:0	SAMPLE_RATE_3 [4:0]	10001	Sample Rate 3 Select *Register coding is same as SAMPLE_RATE_1.*
R266 (010Ah) Sample_rate_1_status	4:0	SAMPLE_RATE_1_STS [4:0]	00000	Sample Rate 1 Status (Read only) *Register coding is same as SAMPLE_RATE_1.*
R267 (010Bh) Sample_rate_2_status	4:0	SAMPLE_RATE_2_STS [4:0]	00000	Sample Rate 2 Status (Read only) *Register coding is same as SAMPLE_RATE_1.*
R268 (010Ch) Sample_rate_3_status	4:0	SAMPLE_RATE_3_STS [4:0]	00000	Sample Rate 3 Status (Read only) *Register coding is same as SAMPLE_RATE_1.*
R274 (0112h) Async_clock_1	10:8	ASYNC_CLK_FREQ [2:0]	011	ASYNCCLK Frequency 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) 100 = 98.304MHz (90.3168MHz) All other codes are Reserved The frequencies in brackets apply for 44.1kHz-related sample rates only (i.e., ASYNC_SAMPLE_RATE_n = 01XXX).
	6	ASYNC_CLK_ENA	0	ASYNCCLK Control 0 = Disabled 1 = Enabled ASYNCCLK should only be enabled after the applicable clock source has been configured and enabled. Set this bit to 0 when reconfiguring the clock sources.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:0	ASYNC_CLK_SRC [3:0]	0101	ASYNCCLK Source 0000 = MCLK1 0001 = MCLK2 0010 = Reserved 0011 = Reserved 0100 = FLL1 0101 = FLL2 0110 = FLL3 0111 = Reserved 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK 1011 = AIF4BCLK All other codes are Reserved
R275 (0113h) Async_sample_rate_1	4:0	ASYNC_SAMPLE_RATE_1 [4:0]	10001	ASYNC Sample Rate 1 Select 00h = None 01h = 12kHz 02h = 24kHz 03h = 48kHz 04h = 96kHz 05h = 192kHz 09h = 11.025kHz 0Ah = 22.05kHz 0Bh = 44.1kHz 0Ch = 88.2kHz 0Dh = 176.4kHz 11h = 8kHz 12h = 16kHz 13h = 32kHz All other codes are Reserved
R276 (0114h) Async_sample_rate_2	4:0	ASYNC_SAMPLE_RATE_2 [4:0]	10001	ASYNC Sample Rate 2 Select *Register coding is same as ASYNC_SAMPLE_RATE_1.*
R283 (011Bh) Async_sample_rate_1_status	4:0	ASYNC_SAMPLE_RATE_1_STS [4:0]	00000	ASYNC Sample Rate 1 Status (Read only) *Register coding is same as ASYNC_SAMPLE_RATE_1.*
R284 (011Ch) Async_sample_rate_2_status	4:0	ASYNC_SAMPLE_RATE_2_STS [4:0]	00000	ASYNC Sample Rate 2 Status (Read only) *Register coding is same as ASYNC_SAMPLE_RATE_1.*
R288 (0120h) DSP_Clock_1	10:8	DSP_CLK_FREQ_RANGE [2:0]	000	DSPCLK Frequency 000=5.5MHz to 9.375MHz (9.216MHz) 001=9.375MHz to 18.75MHz (18.432MHz) 010=18.75MHz to 37.5MHz (36.864MHz) 011=37.5MHz to 75MHz (73.728MHz) 100=75MHz to 150MHz (147.456MHz) All other codes are Reserved The frequencies in brackets are the nominal (or typical) frequencies for each setting. If the DSPCLK frequency is equal to one of the threshold frequencies quoted (e.g., 37.5MHz), then the higher range setting (e.g., 011) should be selected.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6	DSP_CLK_ENA	0	DSPCLK Control 0 = Disabled 1 = Enabled DSPCLK should only be enabled after the applicable clock source has been configured and enabled. Set this bit to 0 when reconfiguring the clock sources. All DSPCLK-dependent functions should be disabled before clearing DSP_CLK_ENA=0. Specific control sequences must be followed if reconfiguring DSPCLK while dependent functions are enabled.
	3:0	DSP_CLK_SRC [3:0]	0101	DSPCLK Source 0000 = MCLK1 0001 = MCLK2 0100 = FLL1 0101 = FLL2 0110 = FLL3 0111 = FLL1 DIV6 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK 1011 = AIF4BCLK All other codes are Reserved
R329 (0149h) Output_system_clock	15	OPCLK_ENA	0	OPCLK Enable 0 = Disabled 1 = Enabled
	7:3	OPCLK_DIV [4:0]	00h	OPCLK Divider 02h = Divide by 2 04h = Divide by 4 06h = Divide by 6 … (even numbers only) 1Eh = Divide by 30 Note that only even numbered divisions (2, 4, 6, etc.) are valid selections. All other codes are Reserved when the OPCLK signal is enabled.
	2:0	OPCLK_SEL [2:0]	000	OPCLK Source Frequency 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) All other codes are Reserved The frequencies in brackets apply for 44.1kHz-related SYSCLK rates only (i.e., SAMPLE_RATE_n = 01XXX). The OPCLK Source Frequency must be less than or equal to the SYSCLK frequency.
R330 (014Ah) Output_as	15	OPCLK_ASYNC_ENA	0	OPCLK_ASYNC Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
ync_clock	7:3	OPCLK_ASYNC_DIV [4:0]	00h	OPCLK_ASYNC Divider 02h = Divide by 2 04h = Divide by 4 06h = Divide by 6 … (even numbers only) 1Eh = Divide by 30 Note that only even numbered divisions (2, 4, 6, etc.) are valid selections. All other codes are Reserved when the OPCLK_ASYNC signal is enabled.
	2:0	OPCLK_ASYNC_SEL [2:0]	000	OPCLK_ASYNC Source Frequency 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) All other codes are Reserved The frequencies in brackets apply for 44.1kHz-related ASYNCCLK rates only (i.e., ASYNC_SAMPLE_RATE_n = 01XXX). The OPCLK_ASYNC Source Frequency must be less than or equal to the ASYNCCLK frequency.
R334 (014Eh) Clock_Gen_Pad_Ctrl	8	MCLK2_PD	0	MCLK2 Pull-Down Control 0 = Disabled 1 = Enabled
	7	MCLK1_PD	0	MCLK1 Pull-Down Control 0 = Disabled 1 = Enabled
R338 (0152h) Rate_Estimator_1	4	TRIG_ON_STARTUP	0	Automatic Sample Rate Detection Start-Up select 0 = Do not trigger Write Sequence on initial detection 1 = Always trigger the Write Sequencer on sample rate detection
	3:1	LRCLK_SRC [2:0]	000	Automatic Sample Rate Detection source 000 = AIF1LRCLK 001 = Reserved 010 = AIF2LRCLK 011 = Reserved 100 = AIF3LRCLK 101 = Reserved 110 = AIF4LRCLK 111 = Reserved
	0	RATE_EST_ENA	0	Automatic Sample Rate Detection control 0 = Disabled 1 = Enabled
R339 (0153h) Rate_Estimator_2	4:0	SAMPLE_RATE_DETECT_A [4:0]	00h	Automatic Detection Sample Rate A (Up to four different sample rates can be configured for automatic detection.) *Register coding is same as SAMPLE_RATE_n.*
R340 (0154h) Rate_Estimator_3	4:0	SAMPLE_RATE_DETECT_B [4:0]	00h	Automatic Detection Sample Rate B (Up to four different sample rates can be configured for automatic detection.) *Register coding is same as SAMPLE_RATE_n.*

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R341 (0155h) Rate_Estimator_4	4:0	SAMPLE_RATE_DETECT_C [4:0]	00h	Automatic Detection Sample Rate C (Up to four different sample rates can be configured for automatic detection.) *Register coding is same as SAMPLE_RATE_n.*
R342 (0156h) Rate_Estimator_5	4:0	SAMPLE_RATE_DETECT_D [4:0]	00h	Automatic Detection Sample Rate D (Up to four different sample rates can be configured for automatic detection.) *Register coding is same as SAMPLE_RATE_n.*

Table 105 Clocking Control

In AIF Slave modes, it is important to ensure the applicable clock domain (SYSCLK or ASYNCCLK) is synchronised with the associated external LRCLK. This can be achieved by selecting an MCLK input that is derived from the same reference as the LRCLK, or can be achieved by selecting the external BCLK or LRCLK signal as a reference input to one of the FLLs, as a source for SYSCLK or ASYNCCLK.

If the AIF clock domain is not synchronised with the LRCLK, then clicks arising from dropped or repeated audio samples will occur, due to the inherent tolerances of multiple, asynchronous, system clocks. See “Applications Information” for further details on valid clocking configurations.

BCLK AND LRCLK CONTROL

The digital audio interfaces (AIF1, AIF2, AIF3 and AIF4) use BCLK and LRCLK signals for synchronisation. In master mode, these are output signals, generated by the CS47L85. In slave mode, these are input signals to the CS47L85. It is also possible to support mixed master/slave operation.

The BCLK and LRCLK signals are controlled as illustrated in Figure 75. See the “Digital Audio Interface Control” section for further details of the relevant control registers.

Note that the BCLK and LRCLK signals are synchronised to SYSCLK or ASYNCLK, depending upon the applicable clocking domain for the respective interface. See “Digital Core” for further details.

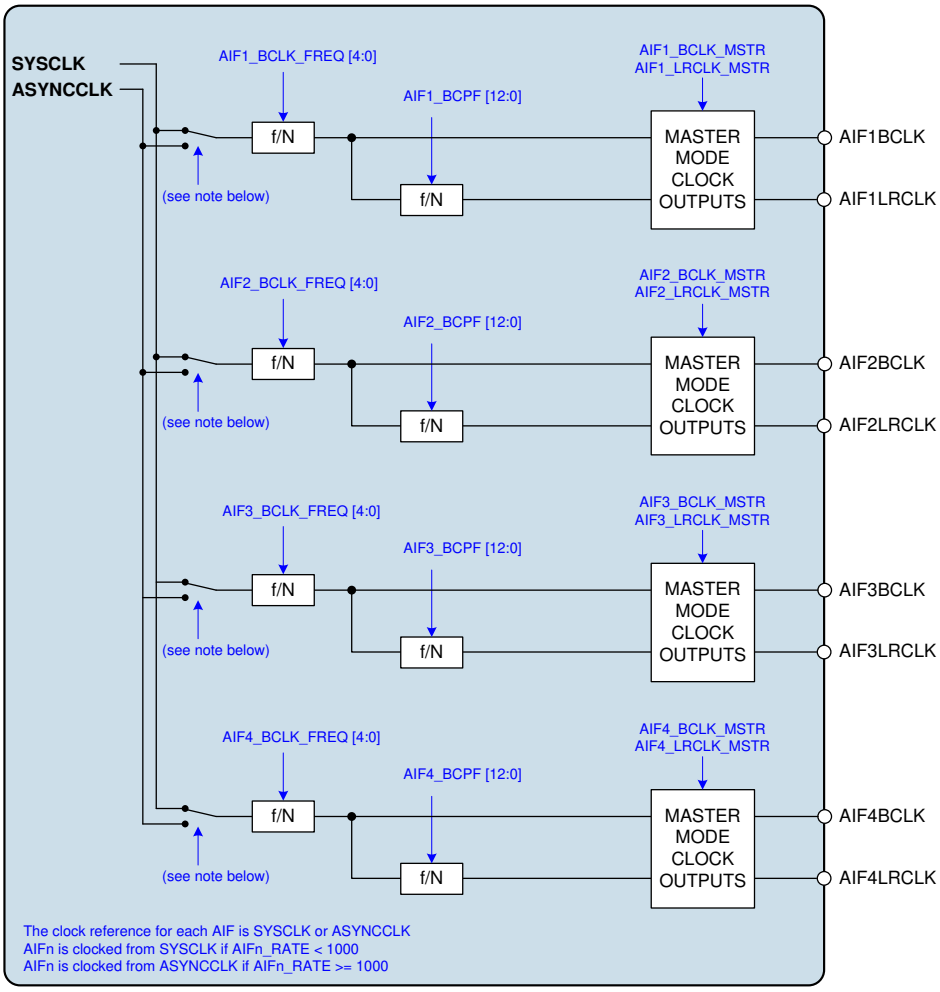


Figure 75 BCLK and LRCLK Control

CONTROL INTERFACE CLOCKING

Register map access is possible with or without a system clock - there is no requirement for SYSCLK, or any other system clock, to be enabled when accessing the register map.

See “Control Interface” for further details of control register access.

FREQUENCY LOCKED LOOP (FLL)

Three integrated FLLs are provided to support the clocking requirements of the CS47L85. These can be enabled and configured independently according to the available reference clocks and the application requirements. The reference clock may be a high frequency (e.g., 12.288MHz) or low frequency (e.g., 32.768kHz).

The FLL is tolerant of jitter and may be used to generate a stable output clock from a less stable input reference. The FLL characteristics are summarised in “Electrical Characteristics”. Note that the FLL can be used to generate a free-running clock in the absence of an external reference source. This is described in the “Free-Running FLL Mode” section below. Configurable spread-spectrum modulation can be applied to the FLL outputs, to control EMI effects.

Each of the FLLs comprises two sub-systems - the ‘main’ loop and the ‘synchroniser’ loop; these can be used together to maintain best frequency accuracy and noise (jitter) performance across multiple use-cases. The two-loop design enables the FLL to synchronise effectively to an input clock that may be intermittent or noisy, whilst also achieving the performance benefits of a stable clock reference that may be asynchronous to the audio data.

The main loop takes a constant and stable clock reference as its input. For best performance, a high frequency (e.g., 12.288MHz) reference is recommended. The main FLL loop will free-run without any clock reference if the input signal is removed; it can also be configured to initiate an output in the absence of any reference signal.

The synchroniser loop takes a separate clock reference as its input. The synchroniser input may be intermittent (e.g., during voice calls only). The FLL uses the synchroniser input, when available, as the frequency reference. To achieve the designed performance advantage, the synchroniser input must be synchronous with the audio data.

Note that, if only a single clock input reference is used, this must be configured as the main FLL input reference. The synchroniser should be disabled in this case.

The synchroniser loop should only be used when the main loop clock reference is present. If the input reference to the main FLL is intermittent, or may be interrupted unexpectedly, then the synchroniser should be disabled.

The FLL is enabled using the FLL*n*_ENA register bit (where *n* = 1, 2 or 3 for the corresponding FLL). The FLL Synchroniser is enabled using the FLL*n*_SYNC_ENA register bit.

Note that the other FLL registers should be configured before enabling the FLL; the FLL*n*_ENA bit should be set as the final step of the FLL*n* enable sequence.

The FLL_SYNC_ENA bit should not be changed if FLL*n*_ENA = 1; the FLLn_ENA bit should be cleared before changing FLL*n*_SYNC_ENA.

The FLL supports configurable free-running operation, using the FLL*n*_FREERUN register bits described in the next section. Note that, once the FLL output has been established, the FLL will always free-run when the input reference clock is stopped, regardless of the FLL*n*_FREERUN bits.

To disable the FLL while the input reference clock has stopped, the respective FLL*n*_FREERUN bit must be set to ‘1’, before setting the FLL*n*_ENA bit to ‘0’.

When changing any of the FLL configuration fields, it is recommended that the digital circuit be disabled via FLL*n*_ENA and then re-enabled after the other register settings have been updated. If the FLL configuration is changed while the FLL is enabled, the respective FLL*n*_FREERUN bit should be set before updating any other FLL fields. A minimum delay of 32µs should be allowed between setting FLL*n*_FREERUN and writing to the required FLL register fields. The FLL*n*_FREERUN bit should remain set until after the FLL has been reconfigured.

Note that, if the FLL*n*_N or FLL*n*_THETA fields are changed while the FLL is enabled, the FLL*n*_CTRL_UPD bit must also be written, as described below. As a general rule, however, it is recommended to configure the FLL (and FLL Synchroniser, if applicable), before setting the corresponding _ENA register bit(s).

The FLL configuration requirements are illustrated in Figure 76.

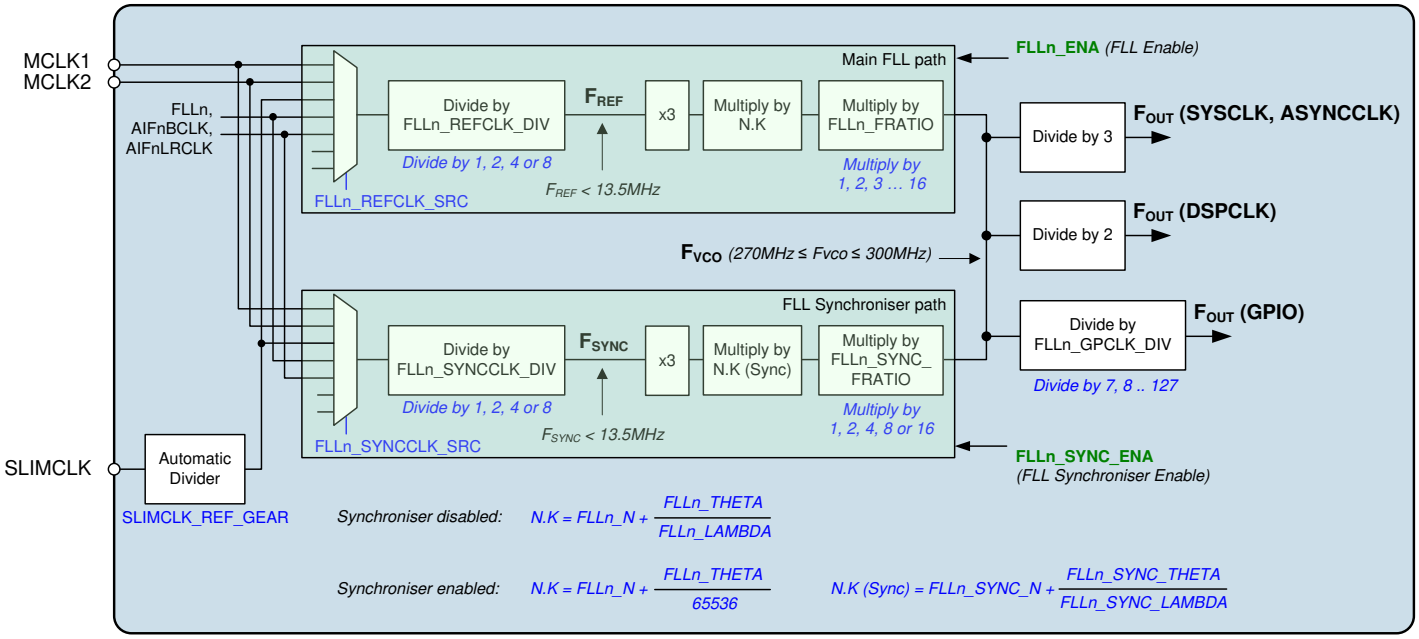


Figure 76 FLL Configuration

The procedure for configuring the FLL is described below. Note that the configuration of the main FLL path and the FLL Synchroniser path are very similar. One or both paths must be configured, depending on the application requirements:

- If a single clock input reference is used, then only the main FLL path should be used.
- If the input reference to the main FLL is intermittent, or may be interrupted unexpectedly, then only the main FLL path should be used.
- If two clock input references are used, then the constant or low-noise clock is configured on the main FLL path, and the high-accuracy clock is configured on the FLL synchroniser path. Note that the synchroniser input must be synchronous with the audio data.

The following description is applicable to FLL1, FLL2 and FLL3. The associated register control fields are described in Table 109, Table 110 and Table 111 respectively.

The main input reference is selected using FLLn_REFCLK_SRC. The synchroniser input reference is selected using FLLn_SYNCCLK_SRC. The available options in each case comprise MCLK1, MCLK2, SLIMCLK, AIFnBCLK, AIFnLRCLK, or the output from another FLL.

The SLIMCLK reference is controlled by an adaptive divider on the external SLIMCLK input. The divider automatically adapts to the SLIMbus Clock Gear, to provide a constant reference frequency for the FLL. See “SLIMbus Interface Control” for details.

The FLL input reference can be generated directly from the output of another FLL. Note that the reference frequency is equal to F_{VCO} / 3 in this case, with respect to the selected FLL source.

The FLL*n*_REFCLK_DIV field controls a programmable divider on the main input reference. The FLL*n*_SYNCCLK_DIV field controls a programmable divider on the synchroniser input reference. Each input can be divided by 1, 2, 4 or 8. These registers should be set to bring each reference down to 13.5MHz or below. For best performance, it is recommended that the highest possible frequency - within the 13.5MHz limit - should be selected. (Note that additional guidelines also apply, as described below.)

The FLL output frequency, relative to the main input reference F_{REF}, is a function of:

- The FLL oscillator frequency, F_{VCO}
- The frequency ratio set by FLL*n*_FRATIO
- The real number represented by N.K. (N=integer; K=fractional portion)

The F_{VCO} frequency must be in the range 270MHz to 300MHz.

When the FLL is selected as SYSCLK or ASYNCCLK source, a fixed divider sets the output frequency equal to F_{VCO} / 3. Therefore, F_{VCO} must be exactly 294.912MHz (for 48kHz-related sample rates) or 270.9504MHz (for 44.1kHz-related sample rates).

When the FLL is selected as DSPCLK source, a fixed divider sets the output frequency equal to F_{VCO} / 2. This enables DSPCLK frequencies in the range 135MHz to 150MHz. For FLL1 only, a 'divide by 6' option is also available, supporting low power DSP operation with DSPCLK frequencies in the range 45MHz to 50MHz. Note that the DSPCLK can be further divided for each DSP.

When the FLL is selected as a GPIO output, a programmable divider supports division ratios in the range 7 through to 127, enabling a wide range of GPIO clock output frequencies.

Note that the chosen F_{VCO} frequency can be used to support multiple outputs simultaneously (e.g., SYSCLK and DSPCLK); each of the FLL clock output paths is controlled by a separate divider function, as illustrated in Figure 76.

The FLL*n*_FRATIO field selects the frequency division ratio of the FLL input. The FLL*n*_GAIN field is used to optimise the FLL, according to the input frequency. As a general guide, these fields should be selected as described in Table 106. (Note that additional guidelines also apply, as described below.)

REFERENCE FREQUENCY F_{REF}	FLL*n*_FRATIO	FLL*n*_GAIN
1MHz - 13.5MHz	0h (divide by 1)	4h (16x gain)
256kHz - 1MHz	1h (divide by 2)	2h (4x gain)
128kHz - 256kHz	3h (divide by 4)	0h (1x gain)
64kHz - 128kHz	7h (divide by 8)	0h (1x gain)
Less than 64kHz	Fh (divide by 16)	0h (1x gain)

Table 106 Selection of FLL*n*_FRATIO and FLL*n*_GAIN

The FLL oscillator frequency, F_{VCO} is set according to the following equation:

$$F_{VCO} = (F_{REF} \times 3 \times N.K \times FLLn\_FRATIO)$$

The value of N.K can thus be determined as follows:

$$N.K = F_{VCO} / (FLLn\_FRATIO \times 3 \times F_{REF})$$

Note that, in the above equations:

F_{REF} is the input frequency, after division by FLL*n*_REFCLK_DIV, where applicable

FLL*n*_FRATIO is the F_{VCO} clock ratio (1, 2, 3 … 16)

If the above equations produce an integer value for N.K, then the value of FLL*n*_FRATIO should be adjusted to a different, odd-number division (e.g., divide by 3), and the value of N.K re-calculated. A non-integer value of N.K is recommended for best performance of the FLL. (If possible, the FLL*n*_FRATIO value should be decreased to the nearest alternative odd-number division. If a suitable lower value does not exist, FLL*n*_FRATIO should be increased to the nearest odd-number division instead.)

After the value of FLL*n*_FRATIO has been determined, the input frequency, F_{REF}, must be compared with the maximum frequency limit noted in Table 107. If the input frequency (after division by FLL*n*_REFCLK_DIV) is higher than the applicable limit, then the FLL*n*_REFCLK_DIV division ratio should be increased, and the value of N.K re-calculated. (Note that the same value of FLL*n*_FRATIO as already calculated should be used, when deriving the new value of N.K.)

FLL*n*_FRATIO	REFERENCE FREQUENCY F_{REF} - MAXIMUM VALUE
0h (divide by 1)	13.5 MHz
1h (divide by 2)	6.144 MHz
2h (divide by 3)	
3h (divide by 4)	3.072 MHz
4h (divide by 5)	
5h (divide by 6)	2.8224 MHz
6h (divide by 7)	
7h (divide by 8)	1.536 MHz
8h (divide by 9)	
9h (divide by 10)	
Ah (divide by 11)	
Bh (divide by 12)	
Ch (divide by 13)	
Dh (divide by 14)	
Eh (divide by 15)	
Fh (divide by 16)	768 kHz

Table 107 Maximum FLL input frequency (function of FLLn_FRATIO)

The value of N is held in the FLL*n*_N register field.

The value of K is determined by the FLL*n*_THETA and FLL*n*_LAMBDA fields, as described later.

The FLL*n*_N, FLL*n*_THETA and FLL*n*_LAMBDA fields are all coded as integers (LSB = 1).

If the FLL*n*_N or FLL*n*_THETA registers are updated while the FLL is enabled (FLL*n*_ENA=1), then the new values will only be effective when a '1' is written to the FLL*n*_CTRL_UPD bit. This makes it possible to update the two registers simultaneously, without disabling the FLL.

Note that, when the FLL is disabled (FLL*n*_ENA=0), then the FLL*n*_N and FLL*n*_THETA registers can be updated without writing to the FLL*n*_CTRL_UPD bit.

The values of FLL*n*_THETA and FLL*n*_LAMBDA can be calculated as described later.

A similar procedure applies for the derivation of the FLL Synchroniser parameters - assuming that this function is used.

The FLL*n*_SYNC_FRATIO field selects the frequency division ratio of the FLL synchroniser input. The FLL*n*_GAIN and FLL*n*_SYNC_DFSAT fields are used to optimise the FLL, according to the input frequency. These fields should be set as described in Table 108.

Note that the FLL*n*_SYNC_FRATIO register coding is not the same as the FLL*n*_FRATIO register.

SYNCHRONISER FREQUENCY F_{SYNC}	FLL*n*_SYNC_FRATIO	FLLn_SYNC_GAIN	FLLn_SYNC_DFSAT
1MHz - 13.5MHz	0h (divide by 1)	4h (16x gain)	0 (wide bandwidth)
256kHz - 1MHz	1h (divide by 2)	2h (4x gain)	0 (wide bandwidth)
128kHz - 256kHz	2h (divide by 4)	0h (1x gain)	0 (wide bandwidth)
64kHz - 128kHz	3h (divide by 8)	0h (1x gain)	1 (narrow bandwidth)
Less than 64kHz	4h (divide by 16)	0h (1x gain)	1 (narrow bandwidth)

Table 108 Selection of FLL*n*_SYNC_FRATIO, FLL*n*_SYNC_GAIN, FLL*n*_SYNC_DFSAT

The FLL oscillator frequency, F_{VCO}, is the same frequency calculated as described above.

The value of N.K (Sync) can then be determined as follows:

$$N.K\ (Sync) = F_{VCO} / (FLLn\_SYNC\_FRATIO \times 3 \times F_{SYNC})$$

Note that, in the above equations:

F_{SYNC} is the synchroniser input frequency, after division by FLL*n*_SYNCCLK_DIV, where applicable

FLL*n*_SYNC_FRATIO is the F_{VCO} clock ratio (1, 2, 4, 8 or 16)

The value of N (Sync) is held in the FLL*n*_SYNC_N register field.

The value of K (Sync) is determined by the FLL*n*_SYNC_THETA and FLL*n*_SYNC_LAMBDA fields.

The FLL*n*_SYNC_N, FLL*n*_SYNC_THETA and FLL*n*_SYNC_LAMBDA fields are all coded as integers (LSB = 1).

In Fractional Mode, with the synchroniser disabled (K > 0, and FLL*n*_SYNC_ENA = 0), the register fields FLL*n*_THETA and FLL*n*_LAMBDA can be calculated as described below.

The equivalent procedure is also used to derive the FLL*n*_SYNC_THETA and FLL*n*_SYNC_LAMBDA register values from the corresponding synchroniser parameters. (This is only required if the synchroniser is enabled.)

Calculate GCD(FLL) using the 'Greatest Common Denominator' function:

GCD(FLL) = GCD(FLL*n*_FRATIO x F_{REF}, F_{VCO} / 3)

where GCD(x, y) is the greatest common denominator of x and y

F_{REF} is the input frequency, after division by FLL*n*_REFCLK_DIV, where applicable.

Next, calculate FLL*n*_THETA and FLL*n*_LAMBDA using the following equations:

FLL*n*_THETA = ((F_{VCO} / 3) - (FLL_N x FLL*n*_FRATIO x F_{REF})) / GCD(FLL)

FLL*n*_LAMBDA = (FLL*n*_FRATIO x F_{REF}) / GCD(FLL)

Note that, in the operating conditions described above, the values of FLL*n*_THETA and FLL*n*_LAMBDA must be co-prime (i.e., not divisible by any common integer). The calculation above ensures that the values will be co-prime. The value of K must be a fraction less than 1 (i.e., FLL*n*_THETA must be less than FLL*n*_LAMBDA).

In Fractional Mode, with the synchroniser enabled (K > 0, and FLLn_SYNC_ENA = 1), the value of FLL*n*_THETA is calculated as described below. The value of FLLn_LAMBDA is ignored in this case.

FLL*n*_THETA = K x 65536

The FLL control registers are described in Table 109, Table 110 and Table 111. Example settings for a variety of reference frequencies and output frequencies are shown in Table 114.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R369 (0171h) FLL1_Control_1	0	FLL1_ENA	0	FLL1 Enable 0 = Disabled 1 = Enabled This should be set as the final step of the FLL1 enable sequence, i.e., after the other FLL registers have been configured.
R370 (0172h) FLL1_Control_2	15	FLL1_CTRL_UPD	0	FLL1 Control Update Write '1' to apply the FLL1_N and FLL1_THETA register settings. (Only valid when FLL1_ENA=1)
	9:0	FLL1_N [9:0]	008h	FLL1 Integer multiply for F_{REF} (LSB = 1) If updated while the FLL is enabled, the new value is only effective when a '1' is written to FLL1_CTRL_UPD.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R371 (0173h) FLL1_Control_3	15:0	FLL1_THETA [15:0]	0018h	FLL1 Fractional multiply for F_{REF} This field sets the numerator (multiply) part of the FLL1_THETA / FLL1_LAMBDA ratio. Coded as LSB = 1. If updated while the FLL is enabled, the new value is only effective when a '1' is written to FLL1_CTRL_UPD.
R372 (0174h) FLL1_Control_4	15:0	FLL1_LAMBDA [15:0]	007Dh	FLL1 Fractional multiply for F_{REF} This field sets the denominator (dividing) part of the FLL1_THETA / FLL1_LAMBDA ratio. Coded as LSB = 1.
R373 (0175h) FLL1_Control_5	11:8	FLL1_FRATIO [3:0]	0h	FLL1 F_{VCO} clock divider 0h = 1 1h = 2 2h = 3 3h = 4 … Fh = 16
R374 (0176h) FLL1_Control_6	7:6	FLL1_REFCLK_DIV [1:0]	00	FLL1 Clock Reference Divider 00 = 1 01 = 2 10 = 4 11 = 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.
	3:0	FLL1_REFCLK_SRC	0000	FLL1 Clock source 0000 = MCLK1 0001 = MCLK2 0011 = SLIMCLK 0100 = FLL1 0101 = FLL2 0110 = FLL3 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK 1011 = AIF4BCLK 1100 = AIF1LRCLK 1101 = AIF2LRCLK 1110 = AIF3LRCLK 1111 = AIF4LRCLK All other codes are Reserved
R377 (0179h) FLL1_Control_7	5:2	FLL1_GAIN [3:0]	0000	FLL1 Gain 0000 = 1 0001 = 2 0010 = 4 0011 = 8 0100 = 16 0101 = 32 0110 = 64 0111 = 128 1000 to 1111 = 256
R385 (0181h) FLL1_Synchroniser_1	0	FLL1_SYNC_ENA	0	FLL1 Synchroniser Enable 0 = Disabled 1 = Enabled This should be set as the final step of the FLL1 synchroniser enable sequence, i.e., after the other synchroniser registers have been configured.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R386 (0182h) FLL1_Synchroniser_2	9:0	FLL1_SYNC_N [9:0]	000h	FLL1 Integer multiply for F_{SYNC} (LSB = 1)
R387 (0183h) FLL1_Synchroniser_3	15:0	FLL1_SYNC_THETA [15:0]	0000h	FLL1 Fractional multiply for F_{SYNC} This field sets the numerator (multiply) part of the FLL1_SYNC_THETA / FLL1_SYNC_LAMBDA ratio. Coded as LSB = 1.
R388 (0184h) FLL1_Synchroniser_4	15:0	FLL1_SYNC_LAMBDA [15:0]	0000h	FLL1 Fractional multiply for F_{SYNC} This field sets the denominator (dividing) part of the FLL1_SYNC_THETA / FLL1_SYNC_LAMBDA ratio. Coded as LSB = 1.
R389 (0185h) FLL1_Synchroniser_5	10:8	FLL1_SYNC_FRATIO [2:0]	000	FLL1 Synchroniser F_{VCO} clock divider 000 = 1 001 = 2 010 = 4 011 = 8 1XX = 16
R390 (0186h) FLL1_Synchroniser_6	7:6	FLL1_SYNCCLK_DIV [1:0]	00	FLL1 Synchroniser Clock Reference Divider 00 = 1 01 = 2 10 = 4 11 = 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.
	3:0	FLL1_SYNCCLK_SRC	0000	FLL1 Synchroniser Clock source 0000 = MCLK1 0001 = MCLK2 0011 = SLIMCLK 0100 = FLL1 0101 = FLL2 0110 = FLL3 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK 1011 = AIF4BCLK 1100 = AIF1LRCLK 1101 = AIF2LRCLK 1110 = AIF3LRCLK 1111 = AIF4LRCLK All other codes are Reserved
R391 (0187h) FLL1_Synchroniser_7	5:2	FLL1_SYNC_GAIN [3:0]	0000	FLL1 Synchroniser Gain 0000 = 1 0001 = 2 0010 = 4 0011 = 8 0100 = 16 0101 = 32 0110 = 64 0111 = 128 1000 to 1111 = 256

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	FLL1_SYNC_DFSAT	1	FLL1 Synchroniser Bandwidth 0 = Wide bandwidth 1 = Narrow bandwidth

Table 109 FLL1 Register Map

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R401 (0191h) FLL2_Control_1	0	FLL2_ENA	0	FLL2 Enable 0 = Disabled 1 = Enabled This should be set as the final step of the FLL2 enable sequence, i.e., after the other FLL registers have been configured.
R402 (0192h) FLL2_Control_2	15	FLL2_CTRL_UPD	0	FLL2 Control Update Write '1' to apply the FLL2_N and FLL2_THETA register settings. (Only valid when FLL2_ENA=1)
	9:0	FLL2_N [9:0]	008h	FLL2 Integer multiply for F_{REF} (LSB = 1) If updated while the FLL is enabled, the new value is only effective when a '1' is written to FLL2_CTRL_UPD.
R403 (0193h) FLL2_Control_3	15:0	FLL2_THETA [15:0]	0018h	FLL2 Fractional multiply for F_{REF} This field sets the numerator (multiply) part of the FLL2_THETA / FLL2_LAMBDA ratio. Coded as LSB = 1. If updated while the FLL is enabled, the new value is only effective when a '1' is written to FLL2_CTRL_UPD.
R404 (0194h) FLL2_Control_4	15:0	FLL2_LAMBDA [15:0]	007Dh	FLL2 Fractional multiply for F_{REF} This field sets the denominator (dividing) part of the FLL2_THETA / FLL2_LAMBDA ratio. Coded as LSB = 1.
R405 (0195h) FLL2_Control_5	11:8	FLL2_FRATIO [3:0]	0h	FLL2 F_{VCO} clock divider 0h = 1 1h = 2 2h = 3 3h = 4 … Fh = 16
R406 (0196h) FLL2_Control_6	7:6	FLL2_REFCLK_DIV [1:0]	00	FLL2 Clock Reference Divider 00 = 1 01 = 2 10 = 4 11 = 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:0	FLL2_REFCLK_SRC	0000	FLL2 Clock source 0000 = MCLK1 0001 = MCLK2 0011 = SLIMCLK 0100 = FLL1 0101 = FLL2 0110 = FLL3 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK 1011 = AIF4BCLK 1100 = AIF1LRCLK 1101 = AIF2LRCLK 1110 = AIF3LRCLK 1111 = AIF4LRCLK All other codes are Reserved
R409 (0199h) FLL2_Control_7	5:2	FLL2_GAIN [3:0]	0000	FLL2 Gain 0000 = 1 0001 = 2 0010 = 4 0011 = 8 0100 = 16 0101 = 32 0110 = 64 0111 = 128 1000 to 1111 = 256
R417 (01A1h) FLL2_Synchroniser_1	0	FLL2_SYNC_ENA	0	FLL2 Synchroniser Enable 0 = Disabled 1 = Enabled This should be set as the final step of the FLL2 synchroniser enable sequence, i.e., after the other synchroniser registers have been configured.
R418 (01A2h) FLL2_Synchroniser_2	9:0	FLL2_SYNC_N [9:0]	000h	FLL2 Integer multiply for F_{SYNC} (LSB = 1)
R419 (01A3h) FLL2_Synchroniser_3	15:0	FLL2_SYNC_THETA [15:0]	0000h	FLL2 Fractional multiply for F_{SYNC} This field sets the numerator (multiply) part of the FLL2_SYNC_THETA / FLL2_SYNC_LAMBDA ratio. Coded as LSB = 1.
R420 (01A4h) FLL2_Synchroniser_4	15:0	FLL2_SYNC_LAMBDA [15:0]	0000h	FLL2 Fractional multiply for F_{SYNC} This field sets the denominator (dividing) part of the FLL2_SYNC_THETA / FLL2_SYNC_LAMBDA ratio. Coded as LSB = 1.
R421 (01A5h) FLL2_Synchroniser_5	10:8	FLL2_SYNC_FRATIO [2:0]	000	FLL2 Synchroniser F_{VCO} clock divider 000 = 1 001 = 2 010 = 4 011 = 8 1XX = 16

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R422 (01A6h) FLL2_Synchroniser_6	7:6	FLL2_SYNCCLK_DIV [1:0]	00	FLL2 Synchroniser Clock Reference Divider 00 = 1 01 = 2 10 = 4 11 = 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.
	3:0	FLL2_SYNCCLK_SRC	0000	FLL2 Synchroniser Clock source 0000 = MCLK1 0001 = MCLK2 0011 = SLIMCLK 0100 = FLL1 0101 = FLL2 0110 = FLL3 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK 1011 = AIF4BCLK 1100 = AIF1LRCLK 1101 = AIF2LRCLK 1110 = AIF3LRCLK 1111 = AIF4LRCLK All other codes are Reserved
R423 (01A7h) FLL2_Synchroniser_7	5:2	FLL2_SYNC_GAIN [3:0]	0000	FLL2 Synchroniser Gain 0000 = 1 0001 = 2 0010 = 4 0011 = 8 0100 = 16 0101 = 32 0110 = 64 0111 = 128 1000 to 1111 = 256
	0	FLL2_SYNC_DFSAT	1	FLL2 Synchroniser Bandwidth 0 = Wide bandwidth 1 = Narrow bandwidth

Table 110 FLL2 Register Map

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R433 (01B1h) FLL3_Control_1	0	FLL3_ENA	0	FLL3 Enable 0 = Disabled 1 = Enabled This should be set as the final step of the FLL3 enable sequence, i.e., after the other FLL registers have been configured.
R434 (01B2h) FLL3_Control_2	15	FLL3_CTRL_UPD	0	FLL3 Control Update Write '1' to apply the FLL3_N and FLL3_THETA register settings. (Only valid when FLL3_ENA=1)
	9:0	FLL3_N [9:0]	008h	FLL3 Integer multiply for F_{REF} (LSB = 1) If updated while the FLL is enabled, the new value is only effective when a '1' is written to FLL3_CTRL_UPD.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R435 (01B3h) FLL3_Control_3	15:0	FLL3_THETA [15:0]	0018h	FLL3 Fractional multiply for F_{REF} This field sets the numerator (multiply) part of the FLL3_THETA / FLL3_LAMBDA ratio. Coded as LSB = 1. If updated while the FLL is enabled, the new value is only effective when a '1' is written to FLL3_CTRL_UPD.
R436 (01B4h) FLL3_Control_4	15:0	FLL3_LAMBDA [15:0]	007Dh	FLL3 Fractional multiply for F_{REF} This field sets the denominator (dividing) part of the FLL3_THETA / FLL3_LAMBDA ratio. Coded as LSB = 1.
R437 (01B5h) FLL3_Control_5	11:8	FLL3_FRATIO [3:0]	0h	FLL3 F_{VCO} clock divider 0h = 1 1h = 2 2h = 3 3h = 4 … Fh = 16
R438 (01B6h) FLL3_Control_6	7:6	FLL3_REFCLK_DIV [1:0]	00	FLL3 Clock Reference Divider 00 = 1 01 = 2 10 = 4 11 = 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.
	3:0	FLL3_REFCLK_SRC	0000	FLL3 Clock source 0000 = MCLK1 0001 = MCLK2 0011 = SLIMCLK 0100 = FLL1 0101 = FLL2 0110 = FLL3 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK 1011 = AIF4BCLK 1100 = AIF1LRCLK 1101 = AIF2LRCLK 1110 = AIF3LRCLK 1111 = AIF4LRCLK All other codes are Reserved
R441 (01B9h) FLL3_Control_7	5:2	FLL3_GAIN [3:0]	0000	FLL3 Gain 0000 = 1 0001 = 2 0010 = 4 0011 = 8 0100 = 16 0101 = 32 0110 = 64 0111 = 128 1000 to 1111 = 256
R449 (01C1h) FLL3_Synchroniser_1	0	FLL3_SYNC_ENA	0	FLL3 Synchroniser Enable 0 = Disabled 1 = Enabled This should be set as the final step of the FLL3 synchroniser enable sequence, i.e., after the other synchroniser registers have been configured.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R450 (01C2h) FLL3_Synchroniser_2	9:0	FLL3_SYNC_N [9:0]	000h	FLL3 Integer multiply for F_{SYNC} (LSB = 1)
R451 (01C3h) FLL3_Synchroniser_3	15:0	FLL3_SYNC_THETA [15:0]	0000h	FLL3 Fractional multiply for F_{SYNC} This field sets the numerator (multiply) part of the FLL3_SYNC_THETA / FLL3_SYNC_LAMBDA ratio. Coded as LSB = 1.
R452 (01C4h) FLL3_Synchroniser_4	15:0	FLL3_SYNC_LAMBDA [15:0]	0000h	FLL3 Fractional multiply for F_{SYNC} This field sets the denominator (dividing) part of the FLL3_SYNC_THETA / FLL3_SYNC_LAMBDA ratio. Coded as LSB = 1.
R453 (01C5h) FLL3_Synchroniser_5	10:8	FLL3_SYNC_FRATIO [2:0]	000	FLL3 Synchroniser F_{VCO} clock divider 000 = 1 001 = 2 010 = 4 011 = 8 1XX = 16
R454 (01C6h) FLL3_Synchroniser_6	7:6	FLL3_SYNCCLK_DIV [1:0]	00	FLL3 Synchroniser Clock Reference Divider 00 = 1 01 = 2 10 = 4 11 = 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.
	3:0	FLL3_SYNCCLK_SRC	0000	FLL3 Synchroniser Clock source 0000 = MCLK1 0001 = MCLK2 0011 = SLIMCLK 0100 = FLL1 0101 = FLL2 0110 = FLL3 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK 1011 = AIF4BCLK 1100 = AIF1LRCLK 1101 = AIF2LRCLK 1110 = AIF3LRCLK 1111 = AIF4LRCLK All other codes are Reserved
R455 (01C7h) FLL3_Synchroniser_7	5:2	FLL3_SYNC_GAIN [3:0]	0000	FLL3 Synchroniser Gain 0000 = 1 0001 = 2 0010 = 4 0011 = 8 0100 = 16 0101 = 32 0110 = 64 0111 = 128 1000 to 1111 = 256

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	FLL3_SYNC_DFSAT	1	FLL3 Synchroniser Bandwidth 0 = Wide bandwidth 1 = Narrow bandwidth

Table 111 FLL3 Register Map

FREE-RUNNING FLL MODE

The FLL can generate a clock signal even when no external reference is available. This may be because the normal input reference has been interrupted, or may be during a standby or start-up period when no initial reference clock is available.

Free-running FLL mode is enabled using the FLLn_FREERUN register. (Note that FLLn_ENA must also be enabled in Free-running FLL mode.)

In Free-running FLL mode, the normal feedback mechanism of the FLL is halted, and the FLL oscillates independently of the external input reference(s).

If the FLL was previously operating normally, (with an input reference clock), then the FLL output frequency will remain unchanged when Free-running FLL mode is enabled. The FLL output will be independent of the input reference while operating in free-running mode with FLLn_FREERUN=1.

The main FLL loop will always continue to free-run if the input reference clock is stopped (regardless of the FLLn_FREERUN setting). If FLLn_FREERUN=0, the FLL will re-lock to the input reference whenever it is available.

In free-running mode, (with FLLn_FREERUN=1), the FLL integrator value (part of the feedback mechanism) can be commanded directly using the FLLn_FRC_INTEG_VAL register. The integrator value in this register is applied to the FLL when a '1' is written to the FLLn_FRC_INTEG_UPD bit.

If the FLL is started up in free-running mode, (i.e., it was not previously running), then the default value of FLLn_FRC_INTEG_VAL will be applied.

The FLL integrator value (part of the feedback mechanism) can be read from the FLLn_INTEG register; the value of this field may be stored for later use. Note that the readback value of the FLLn_INTEG register is only valid when FLLn_FREERUN=1, and the FLLn_INTEG_VALID bit is set.

The FLL integrator setting does not ensure a specific output frequency for the FLL across all devices and operating conditions; some level of variation will apply.

The free-running FLL clock may be selected as the SYSCLK source or ASYNCCLK source as shown Figure 74.

The control registers applicable to Free-running FLL mode are described in Table 112.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R369 (0171h) FLL1_Control_1	1	FLL1_FREERUN	1	FLL1 Free-Running Mode Enable 0 = Disabled 1 = Enabled The FLL feedback mechanism is halted in Free-Running mode, and the latest integrator setting is maintained
R375 (0177h) FLL1_Loop_Filter_Test_1	15	FLL1_FRC_INTEG_UPD	0	Write '1' to apply the FLL1_FRC_INTEG_VAL setting. (Only valid when FLL1_FREERUN=1)
	11:0	FLL1_FRC_INTEG_VAL [11:0]	281h	FLL1 Forced Integrator Value
R376 (0178h) FLL1_NCO_Test_0	15	FLL1_INTEG_VALID	0	FLL1 Integrator Valid Indicates if the FLL1_INTEG register is valid 0 = Not valid 1 = Valid
	11:0	FLL1_INTEG [11:0]	000h	FLL1 Integrator Value (Read-only) Indicates the current FLL1 integrator setting. Only valid when FLL1_INTEG_VALID = 1.
R401 (0191h) FLL2_Control_1	1	FLL2_FREERUN	1	FLL2 Free-Running Mode Enable 0 = Disabled 1 = Enabled The FLL feedback mechanism is halted in Free-Running mode, and the latest integrator setting is maintained

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R407 (0197h) FLL2_Loop_Filter_Test_1	15	FLL2_FRC_INTEG_UPD	0	Write '1' to apply the FLL2_FRC_INTEG_VAL setting. (Only valid when FLL2_FREERUN=1)
	11:0	FLL2_FRC_INTEG_VAL [11:0]	000h	FLL2 Forced Integrator Value
R408 (0198h) FLL2_NCO_Test_0	15	FLL2_INTEG_VALID	0	FLL2 Integrator Valid Indicates if the FLL2_INTEG register is valid 0 = Not valid 1 = Valid
	11:0	FLL2_INTEG [11:0]	000h	FLL2 Integrator Value (Read-only) Indicates the current FLL2 integrator setting. Only valid when FLL2_INTEG_VALID = 1.
R433 (01B1h) FLL3_Control_1	1	FLL3_FREERUN	1	FLL3 Free-Running Mode Enable 0 = Disabled 1 = Enabled The FLL feedback mechanism is halted in Free-Running mode, and the latest integrator setting is maintained
R439 (01B7h) FLL3_Loop_Filter_Test_1	15	FLL3_FRC_INTEG_UPD	0	Write '1' to apply the FLL3_FRC_INTEG_VAL setting. (Only valid when FLL3_FREERUN=1)
	11:0	FLL3_FRC_INTEG_VAL [11:0]	000h	FLL3 Forced Integrator Value
R440 (01B8h) FLL3_NCO_Test_0	15	FLL3_INTEG_VALID	0	FLL3 Integrator Valid Indicates if the FLL3_INTEG register is valid 0 = Not valid 1 = Valid
	11:0	FLL3_INTEG [11:0]	000h	FLL3 Integrator Value (Read-only) Indicates the current FLL3 integrator setting. Only valid when FLL3_INTEG_VALID = 1.

Table 112 Free-Running FLL Mode Control

SPREAD SPECTRUM FLL CONTROL

The CS47L85 can apply modulation to the FLL outputs, using spread spectrum techniques. This can be used to control the EMI characteristics of the circuits that are clocked via the FLLs.

Each of the FLLs can be individually configured for Triangle modulation, Zero Mean Frequency Modulation (ZMFM) or Dither. The amplitude and frequency parameters of the spread spectrum functions is also programmable, using the registers described in Table 113.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R393 (0189h) FLL1_Spread_Spectrum	5:4	FLL1_SS_AMPL [1:0]	00	FLL1 Spread Spectrum Amplitude Controls the extent of the spread-spectrum modulation. 00 = 0.7% (triangle), 0.7% (ZMFM, dither) 01 = 1.1% (triangle), 1.3% (ZMFM, dither) 10 = 2.3% (triangle), 2.6% (ZMFM, dither) 11 = 4.6% (triangle), 5.2% (ZMFM, dither)
	3:2	FLL1_SS_FREQ [1:0]	00	FLL1 Spread Spectrum Frequency Controls the spread spectrum modulation frequency in Triangle mode. 00 = 439kHz 01 = 878kHz 10 = 1.17MHz 11 = 1.76MHz

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1:0	FLL1_SS_SEL [1:0]	00	FLL1 Spread Spectrum Select 00 = Disabled 01 = Zero Mean Frequency (ZMFM) 10 = Triangle 11 = Dither
R425 (01A9h) FLL2_Spread_Spectrum	5:4	FLL2_SS_AMPL [1:0]	00	FLL2 Spread Spectrum Amplitude Controls the extent of the spread-spectrum modulation. 00 = 0.7% (triangle), 0.7% (ZMFM, dither) 01 = 1.1% (triangle), 1.3% (ZMFM, dither) 10 = 2.3% (triangle), 2.6% (ZMFM, dither) 11 = 4.6% (triangle), 5.2% (ZMFM, dither)
	3:2	FLL2_SS_FREQ [1:0]	00	FLL2 Spread Spectrum Frequency Controls the spread spectrum modulation frequency in Triangle mode. 00 = 439kHz 01 = 878kHz 10 = 1.17MHz 11 = 1.76MHz
	1:0	FLL2_SS_SEL [1:0]	00	FLL2 Spread Spectrum Select 00 = Disabled 01 = Zero Mean Frequency (ZMFM) 10 = Triangle 11 = Dither
R457 (01C9h) FLL3_Spread_Spectrum	5:4	FLL3_SS_AMPL [1:0]	00	FLL3 Spread Spectrum Amplitude Controls the extent of the spread-spectrum modulation. 00 = 0.7% (triangle), 0.7% (ZMFM, dither) 01 = 1.1% (triangle), 1.3% (ZMFM, dither) 10 = 2.3% (triangle), 2.6% (ZMFM, dither) 11 = 4.6% (triangle), 5.2% (ZMFM, dither)
	3:2	FLL3_SS_FREQ [1:0]	00	FLL3 Spread Spectrum Frequency Controls the spread spectrum modulation frequency in Triangle mode. 00 = 439kHz 01 = 878kHz 10 = 1.17MHz 11 = 1.76MHz
	1:0	FLL3_SS_SEL [1:0]	00	FLL3 Spread Spectrum Select 00 = Disabled 01 = Zero Mean Frequency (ZMFM) 10 = Triangle 11 = Dither

Table 113 FLL Spread Spectrum Control

FLL INTERRUPTS AND GPIO OUTPUT

For each FLL, the CS47L85 supports an 'FLL Lock' signal which indicates whether FLL Lock has been achieved (i.e., the FLL is locked to the input reference signal).

The FLL Lock signals are inputs to the Interrupt control circuit and can be used to trigger an Interrupt event - see "Interrupts". Note that these Interrupt signals are de-bounced, and require clocking to be present in order to assert the respective Interrupt; either the 32kHz clock, or the SYSCLK signal, must be enabled to trigger an Interrupt from the FLL signals.

The FLL Lock signals can be output directly on a GPIO pin as an external indication of the FLL status. See "General Purpose Input / Output" to configure a GPIO pin for these functions. (These GPIO outputs are not de-bounced, and do not require clocking to be present.)

Clock output signals derived from the FLL can be output on a GPIO pin. See "General Purpose Input / Output" to configure a GPIO pin for this function.

The FLL clocking configuration is illustrated in Figure 76.

EXAMPLE FLL CALCULATION

The following example illustrates how to derive the FLL1 registers to generate an oscillator frequency (F_{VCO}) of 294.912 MHz from a 12.000 MHz reference clock (F_{REF}). This is suitable for generating SYSCLK at 98.304 MHz, and/or DSPCLK at 147.456 MHz.

Note that, for the purposes of this calculation, it is assumed that the synchroniser is disabled.

- Set FLL1_REFCLK_DIV in order to generate F_{REF} <=13.5MHz:
  FLL1_REFCLK_DIV = 00 (divide by 1)
- Set FLL1_FRATIO for the given reference frequency as shown in Table 106:
  F_{REF} = 12MHz, therefore FLL1_FRATIO = 0h (divide by 1)
- Calculate N.K as given by N.K = F_{VCO} / (FLL1_FRATIO x 3 x F_{REF}):
  N.K = 294.912 / (1 x 3 x 12) = 8.192
- Confirm that a non-integer value has been calculated for N.K.
- Confirm that the input frequency, F_{REF}, is less than the applicable limit shown in Table 107.
- Determine FLL1_N from the integer portion of N.K:-
  FLL1_N = 8 (008h)
- Determine GCD(FLL), as given by GCD(FLL) = GCD(FLL1_FRATIO x F_{REF}, F_{VCO} / 3):
  GCD(FLL) = GCD(1 x 12000000, 294912000 / 3) = 96000
- Determine FLL1_THETA, as given by
  FLL1_THETA = ((F_{VCO} / 3) - (FLL1_N x FLL1_FRATIO x F_{REF})) / GCD(FLL):
  FLL1_THETA = ((294912000 / 3) - (8 x 1 x 12000000)) / 96000
  FLL1_THETA = 24 (0018h)
- Determine FLL_LAMBDA, as given by
  FLL1_LAMBDA = (FLL1_FRATIO x F_{REF}) / GCD(FLL):
  FLL1_LAMBDA = (1 x 12000000) / 96000
  FLL1_LAMBDA = 125 (007Dh)

EXAMPLE FLL SETTINGS

Table 114 provides example FLL settings for generating an oscillator frequency (F_{VCO}) of 294.912 MHz from a variety of low and high frequency reference inputs. This is suitable for generating SYSCLK at 98.304 MHz, and/or DSPCLK at 147.456 MHz.

Note that, in these examples, it is assumed that the synchroniser is disabled.

FLL (Main Loop) Settings							
F_{SOURCE}	F_{VCO} (MHz)	F_{REF} Divider	FRATIO	N.K	FLLn_N	FLLn_ THETA	FLLn_ LAMBDA
32.000 kHz	294.912	1	15	204.8	0CCh	0004h	0005h
32.768 kHz	294.912	1	16	187.5	0BBh	0001h	0002h
48 kHz	294.912	1	15	136.5333	088h	0008h	000Fh
128 kHz	294.912	1	7	109.4173	06Dh	0005h	0007h
512 kHz	294.912	1	5	38.4	026h	0002h	0005h
1.536 MHz	294.912	1	3	21.3333	015h	0001h	0003h
3.072 MHz	294.912	1	3	10.6667	00Ah	0002h	0003h
11.2896 MHz	294.912	1	1	8.7075	008h	0068h	0093h
12.000 MHz	294.912	1	1	8.192	008h	0018h	007Dh
12.288 MHz	294.912	2	3	5.3333	005h	0001h	0003h
13.000 MHz	294.912	1	1	7.5618	007h	0391h	0659h
19.200 MHz	294.912	2	1	10.24	00Ah	0006h	0019h
24 MHz	294.912	2	1	8.192	008h	0018h	007Dh
26 MHz	294.912	2	1	7.5618	007h	0391h	0659h
27 MHz	294.912	2	1	7.2818	007h	013Dh	0465h

$F_{VCO} = (F_{SOURCE} / F_{REF}$ Divider) * 3 * N.K * FRATIO
The N.K values are represented in the FLLn_N, FLLn_THETA and FLLn_LAMBDA registers as shown above.
See Table 109, Table 110 and Table 111 for the coding of the FLLn_REFCLK_DIV and FLLn_FRATIO registers.

Table 114 Example FLL Settings – Synchroniser Disabled

Table 115 provides example FLL settings for generating SYSCLK at 98.304 MHz, and/or DSPCLK at 147.456 MHz, with the synchroniser enabled. The main loop and the synchroniser loop must each be configured according to the respective input source.

FLL (Main Loop) Settings							
F_{SOURCE}	F_{VCO} (MHz)	F_{REF} Divider	FRATIO	N.K	FLLn_N	FLLn_ THETA	FLLn_ LAMBDA
32.000 kHz	294.912	1	15	204.8	0CCh	CCCCh	0000h
32.768 kHz	294.912	1	16	187.5	0BBh	8000h	0000h
48 kHz	294.912	1	15	136.5333	088h	8888h	0000h
128 kHz	294.912	1	7	109.7143	06Dh	B6DBh	0000h
512 kHz	294.912	1	5	38.4	026h	6666h	0000h
1.536 MHz	294.912	1	3	21.3333	015h	5555h	0000h
3.072 MHz	294.912	1	3	10.6667	00Ah	AAAAh	0000h
11.2896 MHz	294.912	1	1	8.7075	008h	B51Dh	0000h
12.000 MHz	294.912	1	1	8.192	008h	3126h	0000h
12.288 MHz	294.912	2	3	5.3333	005h	5555h	0000h
13.000 MHz	294.912	1	1	7.5618	007h	8FD5h	0000h
19.200 MHz	294.912	2	1	10.24	00Ah	3D70h	0000h
24 MHz	294.912	2	1	8.192	008h	3126h	0000h
26 MHz	294.912	2	1	7.5618	007h	8FD5h	0000h
27 MHz	294.912	2	1	7.2818	007h	4822h	0000h
FLL (Synchroniser Loop) Settings							
F_{SOURCE}	F_{VCO} (MHz)	F_{SYNC} Divider	FRATIO (SYNC)	N.K (SYNC)	FLLn_ SYNC_N	FLLn_ SYNC_ THETA	FLLn_ SYNC_ LAMBDA
32.000 kHz	294.912	1	16	192	0C0h	0000h	0000h
32.768 kHz	294.912	1	16	187.5	0BBh	0001h	0002h
48 kHz	294.912	1	16	128	080h	0000h	0000h
128 kHz	294.912	1	8	96	060h	0000h	0000h
512 kHz	294.912	1	2	96	060h	0000h	0000h
1.536 MHz	294.912	1	1	64	040h	0000h	0000h
3.072 MHz	294.912	1	1	32	020h	0000h	0000h
11.2896 MHz	294.912	1	1	8.7075	008h	0068h	0093h
12.000 MHz	294.912	1	1	8.192	008h	0018h	007Dh
12.288 MHz	294.912	1	1	8	008h	0000h	0000h
13.000 MHz	294.912	1	1	7.5618	007h	0391h	0659h
19.200 MHz	294.912	2	1	10.24	00Ah	0006h	0019h
24 MHz	294.912	2	1	8.192	008h	0018h	007Dh
26 MHz	294.912	2	1	7.5618	007h	0391h	0659h
27 MHz	294.912	2	1	7.2818	007h	013Dh	0465h

F_{VCO} = (F_{SOURCE} / F_{REF} Divider) * 3 * N.K * FRATIO

See Table 109, Table 110 and Table 111 for details of the FLL configuration fields.

Note that the coding of FLLn_FRATIO is different to FLLn_SYNC_FRATIO.

Table 115 Example FLL Settings – Synchroniser Enabled

CONTROL INTERFACE

The CS47L85 is controlled by writing to its control registers. Readback is available for all registers. Three independent Control Interfaces are provided, giving flexible capability as described below. Note that the SLIMbus interface also supports read/write access to the CS47L85 control registers - see “SLIMbus Interface Control”.

Register access is possible on all of the Control Interfaces (including SLIMbus) simultaneously. Note that the Control Interface function can be supported with or without system clocking - there is no requirement for SYSCLK, or any other system clock, to be enabled when accessing the register map.

The CS47L85 executes a Boot Sequence following Power-On Reset (POR), Hardware Reset, Software Reset or Wake-Up (from Sleep mode). Note that Control Register writes should not be attempted until the Boot Sequence has completed. See “Power-On Reset (POR)” for further details.

A summary of the CS47L85 Control Interfaces is described in Table 116.

CONTROL INTERFACE	DESCRIPTION	PIN FUNCTIONS	POWER DOMAIN
CIF1	4-wire (SPI) interface	CIF1MISO - data output CIF1MOSI - data input CIF1SCLK - interface clock input CIF1SS - ‘slave select’ input	DBVDD1
CIF2	2-wire (I2C) interface	CIF2SCLK - interface clock input CIF2SDA - data input/output	DBVDD1
CIF3	4-wire (SPI) interface	CIF3MISO - data output CIF3MOSI - data input CIF3SCLK - interface clock input CIF3SS - ‘slave select’ input	DBVDD3

Table 116 Control Interface Summary

The CS47L85 provides an integrated pull-down resistor on the CIF1MISO pin. This provides a flexible capability for interfacing with other devices. The pull-down is enabled using the CIF1MISO_PD control bit, as described in Table 117.

Note that there is no pull-down available on the CIF3MISO pin. An external resistor (e.g., 47kΩ) should be used here, if required.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (0008h) Ctrl_IF_CFG_1	7	CIF1MISO_PD	0	CIF1MISO Pull-Down Control 0 = Disabled 1 = Enabled

Table 117 Control Interface Pull-Down

A detailed description of the 2-wire (I2C) interface and 4-wire (SPI) interface modes is provided in the following sections.

4-WIRE (SPI) CONTROL MODE

The 4-wire (SPI) Control Interface mode is supported on CIF1 and CIF3, and uses the corresponding SS, SCLK, MOSI and MISO pins.

In Write operations (R/W=0), the MOSI pin input is driven by the controlling device.

In Read operations (R/W=1), the MOSI pin is ignored following receipt of the valid register address.

When SS is asserted (logic 0), the MISO output is actively driven when outputting data, and is high impedance at other times. When SS is not asserted, the MISO output is high impedance.

The high impedance state of the MISO output allows the pin to be shared with other slaves. An internal pull-down resistor can be enabled on the CIF1MISO pin, as described in Table 117.

Data transfers on CIF1 or CIF3 must use the applicable SPI message format, according to the register address space that is being accessed:

- When accessing register addresses below R12288 (3000h), the applicable SPI protocol comprises a 31-bit register address, and 16-bit data words.
- When accessing register addresses from R12888 (3000h) upwards, the applicable SPI protocol comprises a 31-bit register address, and 32-bit data words.
- Note that, in all cases, the complete SPI message protocol also includes a Read/Write bit, and a 16-bit 'padding' phase (see Figure 77 and Figure 78 below).

Continuous read and write modes enable multiple register operations to be scheduled faster than is possible with single register operations. In these modes, the CS47L85 will automatically increment the register address at the end of each data word, for as long as SS is held low and SCLK is toggled. Successive data words can be input/output every 16 (or 32) clock cycles (depending on the applicable register address space).

The 4-wire (SPI) protocol is illustrated in Figure 77 and Figure 78. Note that 16-bit data words are shown, but the equivalent protocol also applies to 32-bit data words.

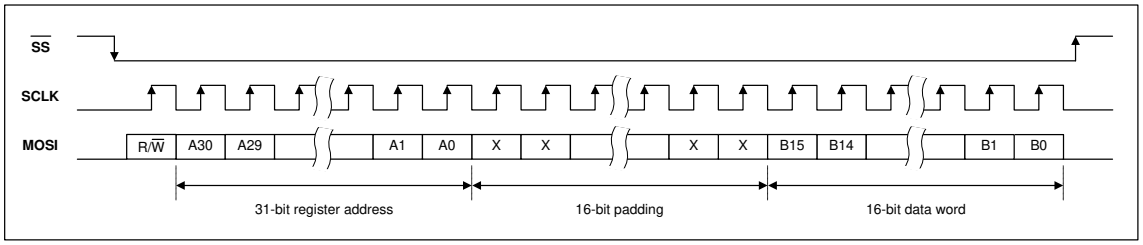


Figure 77 Control Interface 4-wire (SPI) Register Write (16-bit Data Words)

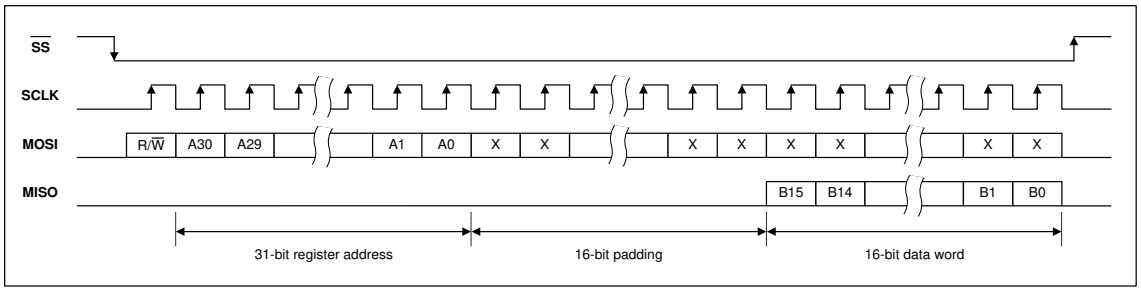


Figure 78 Control Interface 4-wire (SPI) Register Read (16-bit Data Words)

2-WIRE (I2C) CONTROL MODE

The 2-wire (I2C) Control Interface mode is supported on CIF2 only, and uses the corresponding SCLK, SDA pins.

In 2-wire (I2C) mode, the CS47L85 is a slave device on the control interface; SCLK is a clock input, while SDA is a bi-directional data pin. To allow arbitration of multiple slaves (and/or multiple masters) on the same interface, the CS47L85 transmits logic 1 by tri-stating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the logic 1 can be recognised by the master.

In order to allow many devices to share a single 2-wire control bus, every device on the bus has a unique 8-bit device ID (this is not the same as the address of each register in the CS47L85).

The CS47L85 device ID is 0011_0100 (34h). Note that the LSB of the device ID is the Read/Write bit; this bit is set to logic 1 for “Read” and logic 0 for “Write”.

The CS47L85 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDA while SCLK remains high. This indicates that a device ID, and subsequent address/data byte(s), will follow. The CS47L85 responds to the start condition and shifts in the next eight bits on SDA (8-bit device ID, including Read/Write bit, MSB first). If the device ID received matches the device ID of the CS47L85, then the CS47L85 responds by pulling SDA low on the next clock pulse (ACK). If the device ID is not recognised or the R/W bit is set incorrectly, the CS47L85 returns to the idle condition and waits for a new start condition and valid address.

If the device ID matches the device ID of the CS47L85, the data transfer continues as described below. The controller indicates the end of data transfer with a low to high transition on SDA while SCLK remains high. After receiving a complete address and data sequence the CS47L85 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDA changes while SCLK is high), the device returns to the idle condition.

Data transfers on CIF2 must use the applicable I2C message format, according to the register address space that is being accessed:

- When accessing register addresses below R12288 (3000h), the applicable I2C protocol comprises a 32-bit register address, and 16-bit data words.
- When accessing register addresses from R12888 (3000h) upwards, the applicable I2C protocol comprises a 32-bit register address, and 32-bit data words.
- Note that, in all cases, the complete I2C message protocol also includes a Device ID, a Read/Write bit, and other signalling bits (see Figure 79 and Figure 80 below).

The CS47L85 supports the following read and write operations:

- Single write
- Single read
- Multiple write
- Multiple read

Continuous (multiple) read and write modes allow register operations to be scheduled faster than is possible with single register operations. In these modes, the CS47L85 will automatically increment the register address after each data word. Successive data words can be input/output every 2 (or 4) data bytes, depending on the applicable register address space.

The 2-wire (I2C) protocol for a single, 16-bit register write operation is illustrated in Figure 79.

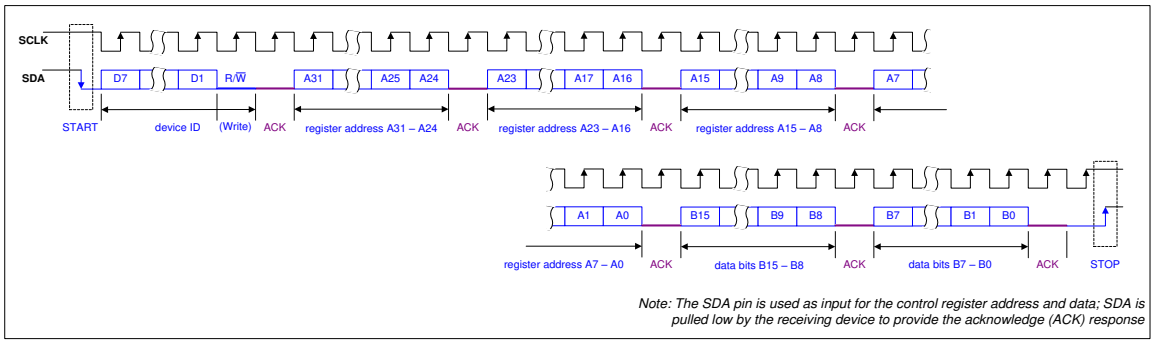


Figure 79 Control Interface 2-wire (I2C) Register Write (16-bit Data Words)

The 2-wire (I2C) protocol for a single, 16-bit register read operation is illustrated in Figure 80.

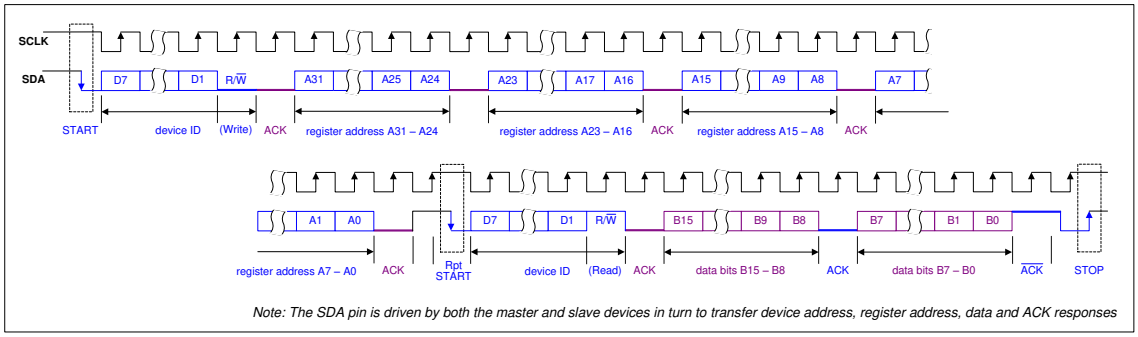


Figure 80 Control Interface 2-wire (I2C) Register Read (16-bit Data Words)

The Control Interface also supports other register operations, as listed above. The interface protocol for these operations is summarised below. The terminology used in the following figures is detailed in Table 118.

Note that 16-bit data words are shown in these illustrations. The equivalent protocol is also applicable to 32-bit words, with 4 data bytes transmitted (or received) instead of 2.

TERMINOLOGY	DESCRIPTION	
S	Start Condition	
Sr	Repeated start	
A	Acknowledge (SDA Low)	
$\overline{A}$	Not Acknowledge (SDA High)	
P	Stop Condition	
R/W	ReadNotWrite	0 = Write 1 = Read
[White field]	Data flow from bus master to CS47L85	
[Grey field]	Data flow from CS47L85 to bus master	

Table 118 Control Interface (I2C) Terminology

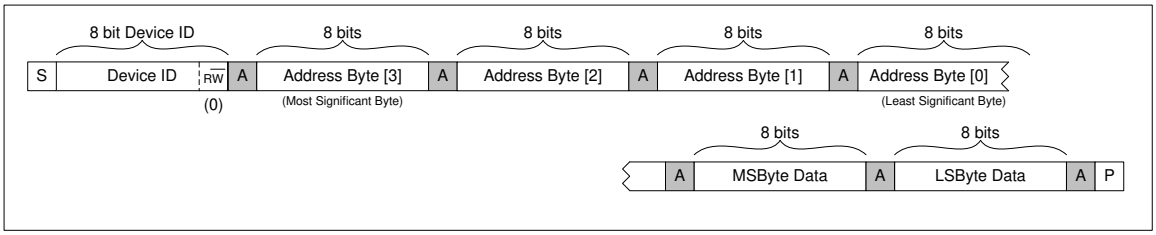


Figure 81 Single Register Write to Specified Address

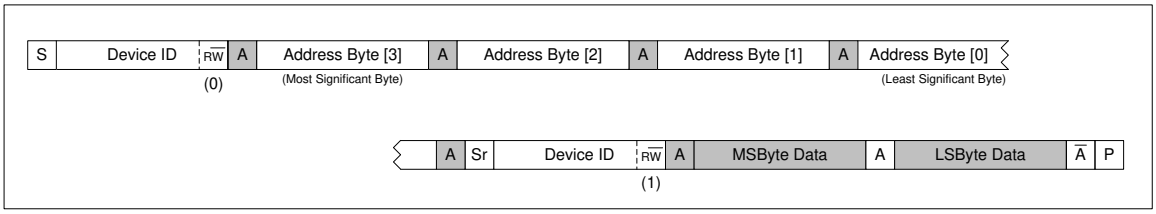


Figure 82 Single Register Read from Specified Address

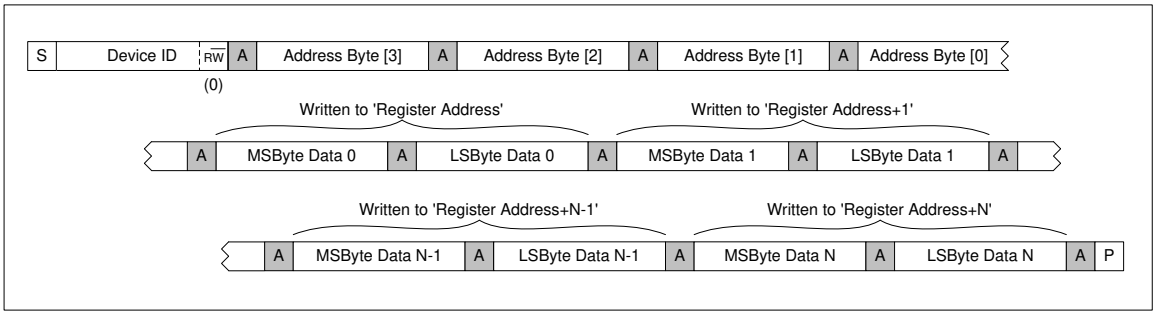


Figure 83 Multiple Register Write to Specified Address

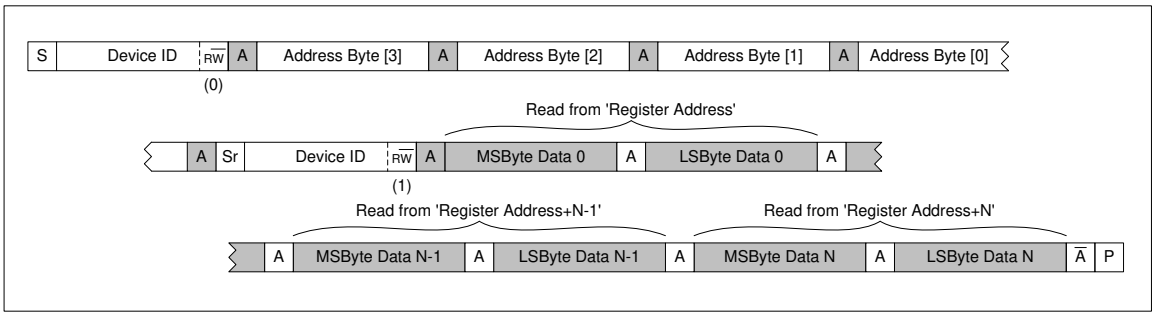


Figure 84 Multiple Register Read from Specified Address

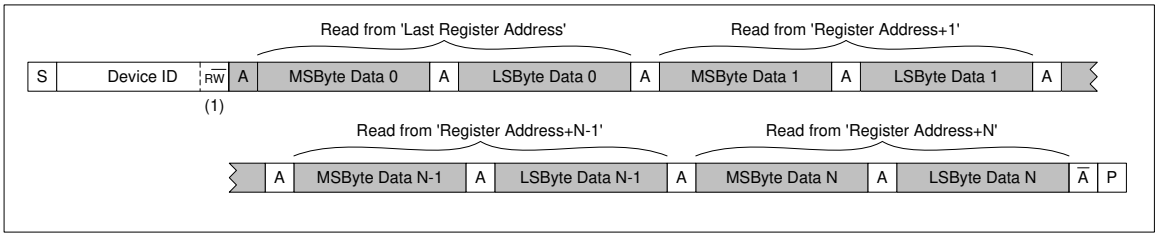


Figure 85 Multiple Register Read from Last Address

CONTROL WRITE SEQUENCER

The Control Write Sequencer is a programmable unit that forms part of the CS47L85 control interface logic. It provides the ability to perform a sequence of register write operations with the minimum of demands on the host processor - the sequence may be initiated by a single operation from the host processor and then left to execute independently.

Default sequences for pop-suppressed start-up and shut-down of each headphone/earpiece output driver are provided (these are scheduled automatically when the respective output paths are enabled or disabled). Other control sequences can be programmed, and may be associated with Sample Rate Detection, DRC, MICDET Clamp, or Event Logger status - these sequences are automatically scheduled whenever a corresponding event is detected.

When a sequence is initiated, the sequencer performs a series of pre-defined register writes. The 'start index' of a control sequence within the sequencer's memory may be commanded directly by the host processor. The applicable 'start index' for each of the sequences associated with Sample Rate Detection, DRC, or MICDET Clamp, or Event Logger status is held in a user-programmed control register.

The Control Write Sequencer may be triggered in a number of ways, as described above. Multiple sequences will be queued if necessary, and each is scheduled in turn.

The Control Write Sequencer can be supported with or without system clocking - there is no requirement for SYSCLK, or any other system clock, to be enabled when using the Control Write Sequencer. The timing accuracy of the sequencer operation will be improved when SYSCLK is present, but the general functionality is supported with or without SYSCLK.

INITIATING A SEQUENCE

The Register fields associated with running the Control Write Sequencer are described in Table 119.

The CS47L85 provides 16 general purpose trigger bits for the Write Sequencer, to allow easy triggering of the associated control sequences. Writing a '1' to the trigger bit will initiate a control sequence, starting at the respective index position within the Control Sequencer memory.

The WSEQ_TRG1_INDEX register defines the sequencer start index corresponding to the WSEQ_TRG1 trigger control bit. Equivalent start index registers are provided for each of the trigger control bits, as described in Table 119. Note that a sequencer start index of 1FFh will cause the respective sequence to be aborted.

The General Purpose control sequences are undefined following Power-On Reset (POR), Hardware Reset, or following a Sleep mode transition. The General Purpose control sequences must be reconfigured by the host processor following any of these events. Note that all control sequences are maintained in the sequencer memory through Software Reset.

The Write Sequencer can also be commanded using control bits in register R22 (16h). In this case, the Write Sequencer is enabled using the WSEQ_ENA bit, and the index location of the first command in the sequence is held in the WSEQ_START_INDEX register. Writing a '1' to the WSEQ_START bit commands the sequencer to execute a control sequence, starting at the specified index position. Note that, if the sequencer is already running, then the WSEQ_START command will be queued, and executed later when the sequencer becomes available.

Note that the mechanism for queuing multiple sequence requests has some limitations, when using the WSEQ_START bit to trigger the write sequencer. If a sequence is initiated using the WSEQ_START bit, no other control sequences should be triggered until the sequence completes. The WSEQ_BUSY bit (described in Table 125) provides an indication of the sequencer status, and can be used to confirm that sequence has completed. Control sequences triggered by another other method are queued if necessary, and scheduled in turn.

The Write Sequencer can be interrupted by writing a '1' to the WSEQ_ABORT bit. Note that this command will only abort a sequence that is currently running; if other sequence commands are pending and not yet started, these sequences will not be aborted by writing to the WSEQ_ABORT bit.

The Write Sequencer stores up to 508 register write commands. These are defined in Registers R12288 (3000h) to R13302 (33F6h). See Table 126 for a description of these registers.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R22 (0016h) Write_Sequencer_Ctrl_0	11	WSEQ_ABORT	0	Writing a 1 to this bit aborts the current sequence.
	10	WSEQ_START	0	Writing a 1 to this bit starts the write sequencer at the index location selected by WSEQ_START_INDEX. At the end of the sequence, this bit will be reset by the Write Sequencer.
	9	WSEQ_ENA	0	Write Sequencer Enable 0 = Disabled 1 = Enabled Only applies to sequences triggered using the WSEQ_START bit.
	8:0	WSEQ_START_INDEX [8:0]	000h	Sequence Start Index This field contains the index location in the sequencer memory of the first command in the selected sequence. Only applies to sequences triggered using the WSEQ_START bit. Valid from 0 to 507 (1FBh).
R66 (0042h) Spare_Triggers	15	WSEQ_TRG16	0	Write Sequence Trigger 16 Write '1' to trigger
	14	WSEQ_TRG15	0	Write Sequence Trigger 15 Write '1' to trigger
	13	WSEQ_TRG14	0	Write Sequence Trigger 14 Write '1' to trigger
	12	WSEQ_TRG13	0	Write Sequence Trigger 13 Write '1' to trigger
	11	WSEQ_TRG12	0	Write Sequence Trigger 12 Write '1' to trigger
	10	WSEQ_TRG11	0	Write Sequence Trigger 11 Write '1' to trigger
	9	WSEQ_TRG10	0	Write Sequence Trigger 10 Write '1' to trigger
	8	WSEQ_TRG9	0	Write Sequence Trigger 9 Write '1' to trigger
	7	WSEQ_TRG8	0	Write Sequence Trigger 8 Write '1' to trigger
	6	WSEQ_TRG7	0	Write Sequence Trigger 7 Write '1' to trigger
	5	WSEQ_TRG6	0	Write Sequence Trigger 6 Write '1' to trigger
	4	WSEQ_TRG5	0	Write Sequence Trigger 5 Write '1' to trigger
	3	WSEQ_TRG4	0	Write Sequence Trigger 4 Write '1' to trigger
	2	WSEQ_TRG3	0	Write Sequence Trigger 3 Write '1' to trigger
	1	WSEQ_TRG2	0	Write Sequence Trigger 2 Write '1' to trigger
	0	WSEQ_TRG1	0	Write Sequence Trigger 1 Write '1' to trigger
R75 (004Bh) Spare_Sequence_Select_1	8:0	WSEQ_TRG1_INDEX [8:0]	1FFh	Write Sequence trigger 1 start index This field contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG1 trigger. Valid from 0 to 507 (1FBh).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R76 (004Ch) Spare_Sequence_Select_2	8:0	WSEQ_TRG2_INDEX [8:0]	1FFh	Write Sequence trigger 1 start index This field contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG2 trigger. Valid from 0 to 507 (1FBh).
R77 (004Dh) Spare_Sequence_Select_3	8:0	WSEQ_TRG3_INDEX [8:0]	1FFh	Write Sequence trigger 1 start index This field contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG3 trigger. Valid from 0 to 507 (1FBh).
R78 (004Eh) Spare_Sequence_Select_4	8:0	WSEQ_TRG4_INDEX [8:0]	1FFh	Write Sequence trigger 1 start index This field contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG4 trigger. Valid from 0 to 507 (1FBh).
R79 (004Fh) Spare_Sequence_Select_5	8:0	WSEQ_TRG5_INDEX [8:0]	1FFh	Write Sequence trigger 1 start index This field contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG5 trigger. Valid from 0 to 507 (1FBh).
R80 (0050h) Spare_Sequence_Select_6	8:0	WSEQ_TRG6_INDEX [8:0]	1FFh	Write Sequence trigger 1 start index This field contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG6 trigger. Valid from 0 to 507 (1FBh).
R89 (0059h) Spare_Sequence_Select_7	8:0	WSEQ_TRG7_INDEX [8:0]	1FFh	Write Sequence trigger 1 start index This field contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG7 trigger. Valid from 0 to 507 (1FBh).
R90 (005Ah) Spare_Sequence_Select_8	8:0	WSEQ_TRG8_INDEX [8:0]	1FFh	Write Sequence trigger 1 start index This field contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG8 trigger. Valid from 0 to 507 (1FBh).
R91 (005Bh) Spare_Sequence_Select_9	8:0	WSEQ_TRG9_INDEX [8:0]	1FFh	Write Sequence trigger 1 start index This field contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG9 trigger. Valid from 0 to 507 (1FBh).
R92 (005Ch) Spare_Sequence_Select_10	8:0	WSEQ_TRG10_INDEX [8:0]	1FFh	Write Sequence trigger 1 start index This field contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG10 trigger. Valid from 0 to 507 (1FBh).
R93 (005Dh) Spare_Sequence_Select_11	8:0	WSEQ_TRG11_INDEX [8:0]	1FFh	Write Sequence trigger 1 start index This field contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG11 trigger. Valid from 0 to 507 (1FBh).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R94 (005Eh) Spare_Sequence_Select_12	8:0	WSEQ_TRG12_INDEX [8:0]	1FFh	Write Sequence trigger 1 start index This field contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG12 trigger. Valid from 0 to 507 (1FBh).
R104 (0068h) Spare_Sequence_Select_13	8:0	WSEQ_TRG13_INDEX [8:0]	1FFh	Write Sequence trigger 1 start index This field contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG13 trigger. Valid from 0 to 507 (1FBh).
R105 (0069h) Spare_Sequence_Select_14	8:0	WSEQ_TRG14_INDEX [8:0]	1FFh	Write Sequence trigger 1 start index This field contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG14 trigger. Valid from 0 to 507 (1FBh).
R106 (006Ah) Spare_Sequence_Select_15	8:0	WSEQ_TRG15_INDEX [8:0]	1FFh	Write Sequence trigger 1 start index This field contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG15 trigger. Valid from 0 to 507 (1FBh).
R107 (006Bh) Spare_Sequence_Select_16	8:0	WSEQ_TRG16_INDEX [8:0]	1FFh	Write Sequence trigger 1 start index This field contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG16 trigger. Valid from 0 to 507 (1FBh).

Table 119 Write Sequencer Control - Initiating a Sequence

AUTOMATIC SAMPLE RATE DETECTION SEQUENCES

The CS47L85 supports automatic sample rate detection on the digital audio interfaces (AIF1, AIF2, AIF3 and AIF4), when operating in AIF Slave mode. Automatic sample rate detection is enabled using the RATE_EST_ENA register bit (see Table 105).

Up to four audio sample rates can be configured for automatic detection; these sample rates are selected using the SAMPLE_RATE_DETECT_n registers. If one of the selected audio sample rates is detected, then the Control Write Sequencer will be triggered. The applicable start index location within the sequencer memory is separately configurable for each detected sample rate.

The WSEQ_SAMPLE_RATE_DETECT_A_INDEX register defines the sequencer start index corresponding to the SAMPLE_RATE_DETECT_A sample rate. Equivalent start index values are defined for the other sample rates, as described in Table 120.

Note that a sequencer start index of 1FFh will cause the respective sequence to be aborted.

The automatic sample rate detection control sequences are undefined following Power-On Reset (POR), Hardware Reset, or following a Sleep mode transition. The automatic sample rate detection control sequences must be reconfigured by the host processor following any of these events. Note that all control sequences are maintained in the sequencer memory through Software Reset.

See “Clocking and Sample Rates” for further details of the automatic sample rate detection function.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R97 (0061h) Sample_Rate_Sequence_Select_1	8:0	WSEQ_SAMPLE_RATE_DETECT_A_INDEX [8:0]	1FFh	Sample Rate A Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with Sample Rate A detection. Valid from 0 to 507 (1FBh).
R98 (0062h) Sample_Rate_Sequence_Select_2	8:0	WSEQ_SAMPLE_RATE_DETECT_B_INDEX [8:0]	1FFh	Sample Rate B Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with Sample Rate B detection. Valid from 0 to 507 (1FBh).
R99 (0063h) Sample_Rate_Sequence_Select_3	8:0	WSEQ_SAMPLE_RATE_DETECT_C_INDEX [8:0]	1FFh	Sample Rate C Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with Sample Rate C detection. Valid from 0 to 507 (1FBh).
R100 (0064h) Sample_Rate_Sequence_Select_4	8:0	WSEQ_SAMPLE_RATE_DETECT_D_INDEX [8:0]	1FFh	Sample Rate D Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with Sample Rate D detection. Valid from 0 to 507 (1FBh).

Table 120 Write Sequencer Control - Automatic Sample Rate Detection

DRC SIGNAL DETECT SEQUENCES

The Dynamic Range Control (DRC) function within the CS47L85 Digital Core provides a configurable signal detect function. This allows the signal level at the DRC input to be monitored and used to trigger other events.

The DRC Signal Detect functions are enabled and configured using the register fields described in Table 14 and Table 15 for DRC1 and DRC2 respectively.

A Control Write Sequence can be associated with a rising edge and/or a falling edge of the DRC1 Signal Detect output. This is enabled using the DRC1_WSEQ_SIG_DET_ENA register bit, as described in Table 14.

Note that signal detection is supported on DRC1 and DRC2, but the triggering of the Control Write Sequencer is available on DRC1 only.

When the DRC Signal Detect sequence is enabled, the Control Write Sequencer will be triggered whenever the DRC1 Signal Detect output transitions (high or low). The applicable start index location within the sequencer memory is separately configurable for each logic condition.

The WSEQ_DRC1_SIG_DET_RISE_SEQ_INDEX register defines the sequencer start index corresponding to a DRC1 Signal Detect Rising Edge event, as described in Table 121. The WSEQ_DRC1_SIG_DET_FALL_SEQ_INDEX register defines the sequencer start index corresponding to a DRC1 Signal Detect Falling Edge event.

Note that a sequencer start index of 1FFh will cause the respective sequence to be aborted.

The DRC Signal Detect sequences cannot be independently enabled for rising and falling edges. Instead, a start index of 1FFh can be used to disable the sequence for either edge, if required.

The DRC Signal Detect control sequences are undefined following Power-On Reset (POR), Hardware Reset, or following a Sleep mode transition. The DRC Signal Detect control sequences must be reconfigured by the host processor following any of these events. Note that all control sequences are maintained in the sequencer memory through Software Reset.

See “Digital Core” for further details of the Dynamic Range Control (DRC) function.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R110 (006Eh) Trigger_Sequence_Select_32	8:0	WSEQ_DRC1_SIG_DET_RISE_INDEX [8:0]	1FFh	DRC1 Signal Detect (Rising) Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with DRC1 Signal Detect (Rising) detection. Valid from 0 to 507 (1FBh).
R111 (006Fh) Trigger_Sequence_Select_33	8:0	WSEQ_DRC1_SIG_DET_FALL_INDEX [8:0]	1FFh	DRC1 Signal Detect (Falling) Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with DRC1 Signal Detect (Falling) detection. Valid from 0 to 507 (1FBh).

Table 121 Write Sequencer Control - DRC Signal Detect

MICDET CLAMP SEQUENCES

The CS47L85 supports external accessory detection functions, including the MICDET Clamp circuit. The MICDET Clamp status can be used to trigger the Control Write Sequencer. The MICDET Clamp is controlled by the JD1 and/or JD2 signals, as described in Table 86.

A Control Write Sequence can be associated with a rising edge and/or a falling edge of the MICDET Clamp status. This is configured using the register bits described in Table 86.

If one of the selected logic conditions is detected, the Control Write Sequencer will be triggered. The applicable start index location within the sequencer memory is separately configurable for the rising and falling edge conditions.

The WSEQ_MICD_CLAMP_RISE_INDEX register defines the sequencer start index corresponding to a MICDET Clamp Rising Edge (Clamp active) event, as described in Table 122. The WSEQ_MICD_CLAMP_FALL_INDEX register defines the sequencer start index corresponding to a MICDET Clamp Falling Edge event.

Note that a sequencer start index of 1FFh will cause the respective sequence to be aborted.

The MICDET Clamp control sequences are undefined following Power-On Reset (POR), Hardware Reset, or following a Sleep mode transition. The MICDET Clamp control sequences must be reconfigured by the host processor following any of these events. Note that all control sequences are maintained in the sequencer memory through Software Reset.

See “External Accessory Detection” for further details of the MICDET Clamp status signals.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R102 (0066h) Always_On_Triggers_Sequence_Select_1	8:0	WSEQ_MICD_CLAMP_RISE_INDEX [8:0]	1FFh	MICDET Clamp (Rising) Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with MICDET Clamp (Rising) detection. Valid from 0 to 507 (1FBh).
R103 (0067h) Always_On_Triggers_Sequence_Select_2	8:0	WSEQ_MICD_CLAMP_FALL_INDEX [8:0]	1FFh	MICDET Clamp (Falling) Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with MICDET Clamp (Falling) detection. Valid from 0 to 507 (1FBh).

Table 122 Write Sequencer Control - MICDET Clamp

EVENT LOGGER SEQUENCES

The CS47L85 provides 8 Event Log functions, for monitoring and recording internal or external signals. The logged events are held in a FIFO buffer, from which the application software can read details of the detected logic transitions.

The Control Write Sequencer is automatically triggered whenever the NOT_EMPTY status of the Event Log buffer is asserted. A different control sequence may be configured for each of the Event Loggers.

The WSEQ_EVENTLOGn_INDEX register defines the sequencer start index corresponding to respective Event Logger (where 'n' is 1 to 8), as described in Table 123.

Note that a sequencer start index of 1FFh will cause the respective sequence to be aborted.

The Event Logger control sequences are undefined following Power-On Reset (POR), Hardware Reset, or following a Sleep mode transition. The Event Logger control sequences must be reconfigured by the host processor following any of these events. Note that all control sequences are maintained in the sequencer memory through Software Reset.

See "DSP Peripheral Control" for further details of the Event Loggers.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R120 (0078h) Eventlog_Sequence_Select_1	8:0	WSEQ_EVENTLOG1_INDEX [8:0]	1FFh	Event Log 1 Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with Event Log 1 'FIFO Not Empty' detection. Valid from 0 to 507 (1FBh).
R121 (0079h) Eventlog_Sequence_Select_2	8:0	WSEQ_EVENTLOG2_INDEX [8:0]	1FFh	Event Log 2 Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with Event Log 2 'FIFO Not Empty' detection. Valid from 0 to 507 (1FBh).
R122 (007Ah) Eventlog_Sequence_Select_3	8:0	WSEQ_EVENTLOG3_INDEX [8:0]	1FFh	Event Log 3 Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with Event Log 3 'FIFO Not Empty' detection. Valid from 0 to 507 (1FBh).
R123 (007Bh) Eventlog_Sequence_Select_4	8:0	WSEQ_EVENTLOG4_INDEX [8:0]	1FFh	Event Log 4 Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with Event Log 4 'FIFO Not Empty' detection. Valid from 0 to 507 (1FBh).
R124 (007Ch) Eventlog_Sequence_Select_5	8:0	WSEQ_EVENTLOG5_INDEX [8:0]	1FFh	Event Log 5 Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with Event Log 5 'FIFO Not Empty' detection. Valid from 0 to 507 (1FBh).
R125 (007Dh) Eventlog_Sequence_Select_6	8:0	WSEQ_EVENTLOG6_INDEX [8:0]	1FFh	Event Log 6 Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with Event Log 6 'FIFO Not Empty' detection. Valid from 0 to 507 (1FBh).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R126 (007Eh) Eventlog_Sequence_Select_7	8:0	WSEQ_EVENTLOG7_INDEX [8:0]	1FFh	Event Log 7 Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with Event Log 7 'FIFO Not Empty' detection. Valid from 0 to 507 (1FBh).
R127 (007Fh) Eventlog_Sequence_Select_8	8:0	WSEQ_EVENTLOG8_INDEX [8:0]	1FFh	Event Log 8 Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with Event Log 8 'FIFO Not Empty' detection. Valid from 0 to 507 (1FBh).

Table 123 Write Sequencer Control - Event Loggers

BOOT SEQUENCE

The CS47L85 executes a Boot Sequence following Power-On Reset (POR), Hardware Reset, Software Reset or Wake-Up (from Sleep mode). The Boot Sequence configures the CS47L85 with factory-set trim (calibration) data.

See "Power-On Reset (POR)" and "Hardware Reset, Software Reset, Wake-Up, and Device ID" for further details.

The start index location of the the Boot Sequence is 384 (180h). See Table 128 for details of the Write Sequencer Memory allocation.

The Boot Sequence can be commanded at any time by writing '1' to the WSEQ_BOOT_START bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (0018h) Write_Sequencer_Ctrl_2	1	WSEQ_BOOT_START	0	Writing a 1 to this bit starts the write sequencer at the index location configured for the Boot Sequence. The Boot Sequence start index is 384 (180h).

Table 124 Write Sequencer Control - Boot Sequence

SEQUENCER STATUS AND READBACK

The status of the Write Sequencer can be read using the WSEQ_BUSY and WSEQ_CURRENT_INDEX registers, as described in Table 125.

When the WSEQ_BUSY bit is asserted, this indicates that the Write Sequencer is busy.

The index address of the most recent Write Sequencer command can be read from the WSEQ_CURRENT_INDEX field. This can be used to provide a precise indication of the Write Sequencer progress.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (0017h) Write_Sequencer_Ctrl_1	9	WSEQ_BUSY (read only)	0	Sequencer Busy flag (Read Only). 0 = Sequencer idle 1 = Sequencer busy
	8:0	WSEQ_CURRENT_INDEX [8:0] (read only)	000h	Sequence Current Index. This indicates the memory location of the most recently accessed command in the write sequencer memory. Coding is the same as WSEQ_START_INDEX.

Table 125 Write Sequencer Control - Status Readback

PROGRAMMING A SEQUENCE

A Control Write Sequence comprises a series of write operations to data bits (or groups of bits) within the control register map. Each write operation is defined by 5 fields, as described below.

The block of 2 registers is replicated 508 times, defining each of the sequencer's 508 possible index addresses. Many sequences can be stored in the sequencer memory at the same time, with each assigned a unique range of index addresses.

The WSEQ_DELAYn register is used to identify the 'end of sequence' position, as described below.

Note that, in the following descriptions, the term '*n*' denotes the sequencer index address (valid from 0 to 507).

WSEQ_DATA_WIDTH*n* is a 3-bit field which identifies the width of the data block to be written. Note that the maximum value of this field selects a width of 8-bits; writing to register fields greater than 8 bits wide must be performed using two separate operations of the Write Sequencer.

WSEQ_ADDR*n* is a 13-bit field containing the register address in which the data should be written.

WSEQ_DELAY*n* is a 4-bit field which controls the waiting time between the current step and the next step in the sequence (i.e., the delay occurs after the write in which it was called). The total delay time per step (including execution) is defined below, giving a useful range of execution/delay times from 3.3µs up to 1s per step. Setting this field to 0xF identifies the step as the last in the sequence.

If WSEQ_DELAYn = 0h or Fh, the step execution time is 3.3µs

For all other values, the step execution time is 61.44µs x ((2 $^{WSEQ\_DELAY}$) - 1)

WSEQ_DATA_START*n* is a 4-bit field which identifies the LSB position within the selected control register to which the data should be written. For example, setting WSEQ_DATA_START*n* = 0100 will select bit 4 as the LSB position of the data to be written.

WSEQ_DATA*n* is an 8-bit field which contains the data to be written to the selected control register. The WSEQ_DATA_WIDTH*n* field determines how many of these bits are written to the selected control register; the most significant bits (above the number indicated by WSEQ_DATA_WIDTH*n*) are ignored.

The register definitions for Step 0 are described in Table 126. The equivalent definitions also apply to Step 1 through to Step 507, in the subsequent register address locations.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12288 (3000h) WSEQ_Sequence_1	31:29	WSEQ_DATA_WIDTH0 [2:0]	000	Width of the data block written in this sequence step. 000 = 1 bit 001 = 2 bits 010 = 3 bits 011 = 4 bits 100 = 5 bits 101 = 6 bits 110 = 7 bits 111 = 8 bits
	28:16	WSEQ_ADDR0 [12:0]	0000h	Control Register Address to be written to in this sequence step.
	15:12	WSEQ_DELAY0 [3:0]	0000	Time delay after executing this step. 00h = 3.3us 01h to 0Eh = 61.44us x ((2^WSEQ_DELAY)-1) Fh = End of sequence marker
	11:8	WSEQ_DATA_START0 [3:0]	0000	Bit position of the LSB of the data block written in this sequence step. 0000 = Bit 0 … 1111 = Bit 15

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	WSEQ_DATA0 [7:0]	00h	Data to be written in this sequence step. When the data width is less than 8 bits, then one or more of the MSBs of WSEQ_DATA*n* are ignored. It is recommended that unused bits be set to 0.

Table 126 Write Sequencer Control - Programming a Sequence

SEQUENCER MEMORY DEFINITION

The Write Sequencer memory defines up to 508 write operations; these are indexed as 0 to 507 in the sequencer memory map.

The Write Sequencer memory will revert to its default contents following Power-On Reset (POR), Hardware Reset, or a Sleep mode transition, In these cases, the sequence memory will contain the Boot Sequence, and the OUT1, OUT2, OUT3, OUT4 signal path enable/disable sequences; the remainder of the sequence memory will be undefined.

User-defined sequences can be programmed after power-up. The user-defined control sequences must be reconfigured by the host processor following Power-On Reset (POR), Hardware Reset, or following a Sleep mode transition. Note that all control sequences are maintained in the sequencer memory through Software Reset. See the “Applications Information” section for a summary of the CS47L85 memory reset conditions.

The default control sequences can be overwritten in the sequencer memory, if required. Note that the headphone and earpiece output path enable registers (HPnx_ENA, SPKOUTx_ENA) will always trigger the Write Sequencer (at the pre-determined start index addresses).

Writing ‘1’ to the WSEQ_LOAD_MEM bit will clear the sequencer memory to the POR state.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (0018h) Write_Sequencer_Ctrl_2	0	WSEQ_LOAD_MEM	0	Writing a 1 to this bit resets the sequencer memory to the POR state.

Table 127 Write Sequencer Control - Load Memory Control

The sequencer memory is summarised in Table 128. User-defined sequences should be assigned space within the allocated portion (‘user space’) of the Write Sequencer memory.

The start index for the user-defined sequences is configured using the registers described in Table 119 through to Table 123.

DESCRIPTION	SEQUENCE INDEX RANGE
Default Sequences	0 to 302
User Space	303 to 383
Boot Sequence	384 to 507

Table 128 Write Sequencer Memory Allocation

CHARGE PUMPS, REGULATORS AND VOLTAGE REFERENCE

The CS47L85 incorporates two Charge Pump circuits and two LDO Regulator circuits to generate supply rails for internal functions and to support external microphone requirements. The CS47L85 also provides four MICBIAS generators which provide low noise reference voltages suitable for biasing electret condenser (ECM) type microphones or powering digital microphones.

Refer to the “Applications Information” section for recommended external components.

The CPVDD domain (1.8V) powers the Charge Pump 1 and Charge Pump 2 circuits. The CPVDD2 power domain (1.2V) is an additional supply used by Charge Pump 1 only.

The DCVDD domain (1.2V) can be supplied externally, or can be provided by the LDO1 Regulator.

Note that the CPVDD2 domain must always be powered externally; the CPVDD2 domain should not be connected to the LDO1 output.

CHARGE PUMPS AND LDO2 REGULATOR

Charge Pump 1 (CP1) is used to generate the positive and negative supply rails for the analogue output drivers. CP1 is enabled automatically by the CS47L85 when required by the output drivers.

Charge Pump 2 (CP2) powers LDO2, which provides the supply rail for analogue input circuits and for the MICBIAS generators. CP2 and LDO2 are enabled using the CP2_ENA register bit.

The 32kHz clock must be configured and enabled when using CP2. See “Clocking and Sample Rates” for details of the system clocks.

When CP2 and LDO2 are enabled, the MICVDD voltage can be selected using the LDO2_VSEL control field. Note that, when one or more of the MICBIAS generators is operating in normal (regulator) mode, then the MICVDD voltage must be at least 200mV greater than the highest selected MICBIASn output voltage(s).

When CP2 and LDO2 are enabled, an internal bypass path may be selected, connecting the MICVDD pin directly to the CPVDD supply. This path is controlled using the CP2_BYPASS register. Note that the bypass path is only supported when CP2 is enabled.

When CP2 is disabled, the CP2VOUT pin can be configured to be floating or to be actively discharged. This is selected using the CP2_DISCH register bit.

When LDO2 is disabled, the MICVDD pin can be configured to be floating or to be actively discharged. This is selected using the LDO2_DISCH register bit.

The MICVDD pin is connected to the output of LDO2. Note that the MICVDD does not support direct connection to an external supply; MICVDD is always powered internally to the CS47L85.

The Charge Pumps and LDO2 Regulator circuits are illustrated in Figure 86. The associated register control bits are descrbed in Table 129.

Note that decoupling capacitors and flyback capacitors are required for these circuits. Refer to the “Applications Information” section for recommended external components.

MICROPHONE BIAS (MICBIAS) CONTROL

There are four MICBIAS generators which provide low noise reference voltages suitable for biasing electret condenser (ECM) type microphones or powering digital microphones. Refer to the “Applications Information” section for recommended external components.

The MICBIAS generators are powered from MICVDD, which is generated by an internal Charge Pump and LDO, as illustrated in Figure 86.

The MICBIAS outputs can be independently enabled using the MICB*n*_ENA register bits (where *n* = 1, 2 3 or 4 for MICBIAS1, 2, 3 or 4 respectively).

When a MICBIAS output is disabled, the output pin can be configured to be floating or to be actively discharged. This is selected using the MICB*n*_DISCH register bits.

The MICBIAS generators can each operate as a voltage regulator or in bypass mode. The applicable mode is selected using the MICB*n*_BYPASS registers.

In Regulator mode (MICB*n*_BYPASS=0), the output voltage is selected using the MICB*n*_LVL register bits. In this mode, MICVDD must be at least 200mV greater than the required MICBIAS output voltages. The MICBIAS outputs are powered

from the MICVDD pin, and use the internal bandgap circuit as a reference.

In Regulator mode, the MICBIAS regulators are designed to operate without external decoupling capacitors. The regulators can be configured to support a capacitive load if required, using the MICB*n*_EXT_CAP register bits. (This may be appropriate for a digital microphone supply.) It is important that the external capacitance is compatible with the applicable MICB*n*_EXT_CAP setting. The compatible load conditions are detailed in the "Electrical Characteristics" section.

In Bypass mode (MICB*n*_BYPASS=1), the output pin (MICBIAS*n*) is connected directly to MICVDD. This enables a low power operating state. Note that the MICB*n*_EXT_CAP register settings are not applicable in Bypass mode; there are no restrictions on the external MICBIAS capacitance in Bypass mode.

The MICBIAS generators incorporate a pop-free control circuit to ensure smooth transitions when the MICBIAS outputs are enabled or disabled in Bypass mode; this feature is enabled using the MICB*n*_RATE registers.

The MICBIAS generators are illustrated in Figure 86. The MICBIAS control register bits are descrbed in Table 129.

The maximum output current for each MICBIAS*n* pin is noted in the "Electrical Characteristics". This limit must be observed on each MICBIAS output, especially if more than one microphone is connected to a single MICBIAS pin. Note that the maximum output current differs between Regulator mode and Bypass mode.

VOLTAGE REFERENCE CIRCUIT

The CS47L85 incorporates a voltage reference circuit, powered by AVDD. This circuit ensures the accuracy of the LDO Regulator and MICBIAS voltage settings.

LDO1 REGULATOR AND DCVDD SUPPLY

The LDO1 voltage regulator is powered by LDOVDD, and is intended for generating the DCVDD domain, which powers the digital core functions on the CS47L85. In this configuration, the LDO output (LDOVOUT) should be connected to the DCVDD pin. Note that the use of the LDO1 regulator to power external circuits cannot be supported by the CS47L85.

LDO1 is enabled when a logic '1' is applied to the LDOENA pin. The logic level is determined with respect to the DBVDD1 voltage domain.

When LDO1 is disabled, the LDOVOUT pin can be configured to be floating or to be actively discharged. This is selected using the LDO1_DISCH register bit.

It is possible to supply DCVDD from an external supply. In this configuration, the LDOVOUT pin should be left floating: it must not be connected to the DCVDD pin. The LDO1 regulator is not used in this case, and must be disabled at all times.

An internal pull-down resistor is enabled by default on the LDOENA pin. This is configurable using the LDO1ENA_PD register bit. A pull-up resistor is also available, as described in Table 129. When the pull-up and pull-down resistors are both enabled, the CS47L85 provides a 'bus keeper' function on the LDOENA pin. The bus keeper function holds the input logic level unchanged whenever the external circuit removes the drive (e.g., if the signal is tri-stated).

If DCVDD is powered from LDO1, then a logic '1' must be applied to the LDOENA pin during power-up, to enable LDO1. The LDO must also be enabled using the LDOENA pin following a Hardware Reset or Software Reset, to allow the device to re-start. (It is recommended that the LDOENA pin is asserted before any reset, and is held at logic '1' until after the reset is complete; this ensures the DSP6 firmware memory contents can be retained, and also allows faster reset time.)

For normal operation following Power-On Reset (POR), Hardware Reset, or Software Reset, LDO1 must be enabled using the LDOENA pin. The 'bus keeper' function can be used during normal operation to keep LDO1 enabled without actively driving the LDOENA pin. Note that the LDOENA pin must always be actively driven following a reset, as the bus keeper function will be disabled in this case.

See "Power-On Reset (POR)" and "Hardware Reset, Software Reset, Wake-Up, and Device ID" for details of CS47L85 Resets. See also "Low Power Sleep Configuration" for details of the Sleep / Wake-up functions.

The LDO1 Regulator circuit is illustrated in Figure 86. The associated register control bits are described in Table 129.

Note that the LDO output requires an external decoupling capacitor; this requirement is typically achieved via decoupling on the DCVDD pins. Refer to the "Applications Information" section for recommended external components.

BLOCK DIAGRAM AND CONTROL REGISTERS

The Charge Pump and Regulator circuits are illustrated in Figure 86. Note that decoupling capacitors and flyback capacitors are required for these circuits. Refer to the “Applications Information” section for recommended external components.

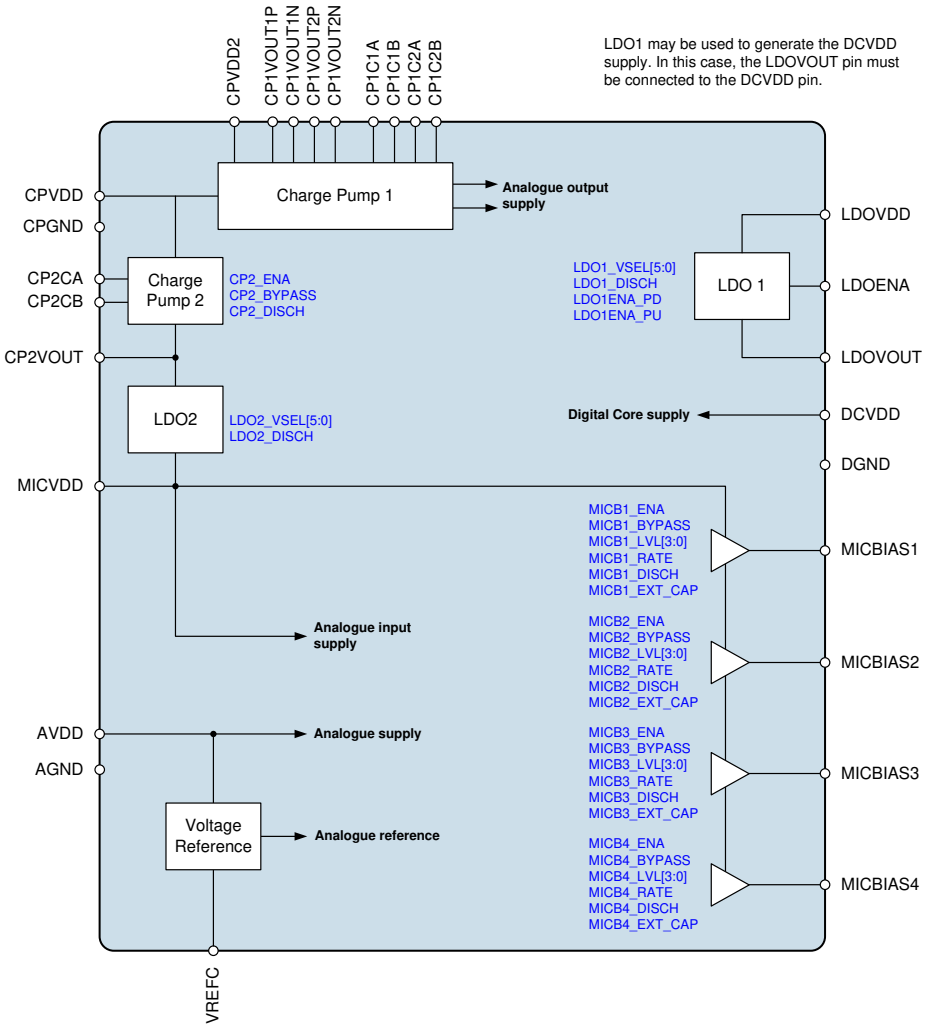


Figure 86 Charge Pumps and Regulators

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R512 (0200h) Mic_Charge_Pump_1	2	CP2_DISCH	1	Charge Pump 2 Discharge 0 = CP2VOUT floating when disabled 1 = CP2VOUT discharged when disabled
	1	CP2_BYPASS	1	Charge Pump 2 and LDO2 Bypass Mode 0 = Normal 1 = Bypass mode In Bypass mode, CPVDD is connected directly to MICVDD. Note that CP2_ENA must also be set.
	0	CP2_ENA	1	Charge Pump 2 and LDO2 Control (Provides analogue input and MICVDD supplies) 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R528 (0210h) LDO1_Control_1	10:5	LDO1_VSEL [5:0]	0Ch	LDO1 Output Voltage Select 0Ch = 1.200V All other codes are Reserved
	2	LDO1_DISCH	1	LDO1 Discharge 0 = LDOVOUT floating when disabled 1 = LDOVOUT discharged when disabled
R531 (0213h) LDO2_Control_1	10:5	LDO2_VSEL [5:0]	1Fh	LDO2 Output Voltage Select 00h = 0.900V 01h = 0.925V 02h = 0.950V … (25mV steps) 13h = 1.375V 14h = 1.400V 15h = 1.500V 16h = 1.600V … (100mV steps) 26h = 3.200V 27h to 3Fh = 3.300V (See Table 130 for voltage range)
	2	LDO2_DISCH	1	LDO2 Discharge 0 = MICVDD floating when disabled 1 = MICVDD discharged when disabled
R536 (218h) Mic_Bias_Ctrl_1	15	MICB1_EXT_CAP	0	Microphone Bias 1 External Capacitor (when MICB1_BYPASS = 0). Configures the MICBIAS1 regulator according to the specified capacitance connected to the MICBIAS1 output. 0 = No external capacitor 1 = External capacitor connected
	8:5	MICB1_LVL [3:0]	7h	Microphone Bias 1 Voltage Control (when MICB1_BYPASS = 0) 0h = 1.5V 1h = 1.6V … (0.1V steps) Ch = 2.7V Dh to Fh = 2.8V
	3	MICB1_RATE	0	Microphone Bias 1 Rate (Bypass mode) 0 = Fast start-up / shut-down 1 = Pop-free start-up / shut-down
	2	MICB1_DISCH	1	Microphone Bias 1 Discharge 0 = MICBIAS1 floating when disabled 1 = MICBIAS1 discharged when disabled
	1	MICB1_BYPASS	1	Microphone Bias 1 Mode 0 = Regulator mode 1 = Bypass mode
	0	MICB1_ENA	0	Microphone Bias 1 Enable 0 = Disabled 1 = Enabled
R537 (219h) Mic_Bias_Ctrl_2	15	MICB2_EXT_CAP	0	Microphone Bias 2 External Capacitor (when MICB2_BYPASS = 0). Configures the MICBIAS2 regulator according to the specified capacitance connected to the MICBIAS2 output. 0 = No external capacitor 1 = External capacitor connected

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	8:5	MICB2_LVL [3:0]	7h	Microphone Bias 2 Voltage Control (when MICB2_BYPASS = 0) 0h = 1.5V 1h = 1.6V … (0.1V steps) Ch = 2.7V Dh to Fh = 2.8V
	3	MICB2_RATE	0	Microphone Bias 2 Rate (Bypass mode) 0 = Fast start-up / shut-down 1 = Pop-free start-up / shut-down
	2	MICB2_DISCH	1	Microphone Bias 2 Discharge 0 = MICBIAS2 floating when disabled 1 = MICBIAS2 discharged when disabled
	1	MICB2_BYPASS	1	Microphone Bias 2 Mode 0 = Regulator mode 1 = Bypass mode
	0	MICB2_ENA	0	Microphone Bias 2 Enable 0 = Disabled 1 = Enabled
R538 (21Ah) Mic_Bias_ Ctrl_3	15	MICB3_EXT_CAP	0	Microphone Bias 3 External Capacitor (when MICB3_BYPASS = 0). Configures the MICBIAS3 regulator according to the specified capacitance connected to the MICBIAS3 output. 0 = No external capacitor 1 = External capacitor connected
	8:5	MICB3_LVL [3:0]	7h	Microphone Bias 3 Voltage Control (when MICB3_BYPASS = 0) 0h = 1.5V 1h = 1.6V … (0.1V steps) Ch = 2.7V Dh to Fh = 2.8V
	3	MICB3_RATE	0	Microphone Bias 3 Rate (Bypass mode) 0 = Fast start-up / shut-down 1 = Pop-free start-up / shut-down
	2	MICB3_DISCH	1	Microphone Bias 3 Discharge 0 = MICBIAS3 floating when disabled 1 = MICBIAS3 discharged when disabled
	1	MICB3_BYPASS	1	Microphone Bias 3 Mode 0 = Regulator mode 1 = Bypass mode
	0	MICB3_ENA	0	Microphone Bias 3 Enable 0 = Disabled 1 = Enabled
R539 (21Bh) Mic_Bias_ Ctrl_4	15	MICB4_EXT_CAP	0	Microphone Bias 4 External Capacitor (when MICB4_BYPASS = 0). Configures the MICBIAS4 regulator according to the specified capacitance connected to the MICBIAS4 output. 0 = No external capacitor 1 = External capacitor connected

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	8:5	MICB4_LVL [3:0]	7h	Microphone Bias 4 Voltage Control (when MICB4_BYPASS = 0) 0h = 1.5V 1h = 1.6V … (0.1V steps) Ch = 2.7V Dh to Fh = 2.8V
	3	MICB4_RATE	0	Microphone Bias 4 Rate (Bypass mode) 0 = Fast start-up / shut-down 1 = Pop-free start-up / shut-down
	2	MICB4_DISCH	1	Microphone Bias 4 Discharge 0 = MICBIAS4 floating when disabled 1 = MICBIAS4 discharged when disabled
	1	MICB4_BYPASS	1	Microphone Bias 4 Mode 0 = Regulator mode 1 = Bypass mode
	0	MICB4_ENA	0	Microphone Bias 4 Enable 0 = Disabled 1 = Enabled
R6864 (1AD0h) AOD_Pad _Ctrl	15	LDO1ENA_PD	1	LDOENA Pull-Down Control 0 = Disabled 1 = Enabled Note - when LDO1ENA_PD and LDO1ENA_PU are both set to '1', then a 'bus keeper' function is enabled on the LDOENA pin.
	14	LDO1ENA_PU	0	LDOENA Pull-Up Control 0 = Disabled 1 = Enabled Note - when LDO1ENA_PD and LDO1ENA_PU are both set to '1', then a 'bus keeper' function is enabled on the LDOENA pin.

Table 129 Charge Pump and LDO Control Registers

LDO2_VSEL [5:0]	LDO OUTPUT	LDO2_VSEL [5:0]	LDO OUTPUT	LDO2_VSEL [5:0]	LDO OUTPUT
00h	0.900V	10h	1.300V	20h	2.600V
01h	0.925V	11h	1.325V	21h	2.700V
02h	0.950V	12h	1.350V	22h	2.800V
03h	0.975V	13h	1.375V	23h	2.900V
04h	1.000V	14h	1.400V	24h	3.000V
05h	1.025V	15h	1.500V	25h	3.100V
06h	1.050V	16h	1.600V	26h	3.200V
07h	1.075V	17h	1.700V	27h	3.300V
08h	1.100V	18h	1.800V	28h to 3Fh	3.300V
09h	1.125V	19h	1.900V		
0Ah	1.150V	1Ah	2.000V		
0Bh	1.175V	1Bh	2.100V		
0Ch	1.200V	1Ch	2.200V		
0Dh	1.225V	1Dh	2.300V		
0Eh	1.250V	1Eh	2.400V		
0Fh	1.275V	1Fh	2.500V		

Table 130 LDO2 Voltage Control

JTAG INTERFACE

The JTAG interface provides test and debug access to the CS47L85 DSP core. The interface comprises 5 pins, as detailed below.

- TCK: Clock input
- TDI: Data input
- TDO: Data output
- TMS: Mode select input
- TRST: Test Access Port reset input (active low)

For normal operation (test and debug access disabled), the JTAG interface should be held in reset (i.e., TRST should be at logic 0). An internal pull-down resistor holds the TRST pin low when not actively driven. External connection to DGND is recommended, if the JTAG interface function is not required.

The other JTAG input pins (TCK, TDI, TMS) should also be held at logic 0 for normal operation. An internal pull-down resistor holds these pins low when not actively driven.

If the JTAG interface is enabled (TRST de-asserted, and TCK active) at the time of Power-On Reset, or any other Reset, then a Software Reset must be scheduled, with the TCK input stopped or TRST asserted (logic '0'), before using the JTAG interface.

As a general rule, it is recommended to always schedule a Software Reset before starting the JTAG clock, or de-asserting the JTAG reset. In this event, the JTAG interface should be held in its reset state until the Software Reset has completed, and the BOOT_DONE_STSx bits have been set.

See "Hardware Reset, Software Reset, Wake-Up, and Device ID" for further details of the CS47L85 Software Reset.

Note that DSPCLK must be present and enabled, if the JTAG interface is enabled. See "Clocking and Sample Rates" for further details of the CS47L85 system clocks.

THERMAL SHUTDOWN AND SHORT CIRCUIT PROTECTION

The CS47L85 incorporates thermal protection functions, and also provides short-circuit detection on the Class D speaker and headphone output paths, as described below.

The temperature sensor detects when the device temperature is within normal limits or if the device is approaching a hazardous temperature condition.

The temperature sensor is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see "Interrupts". A two-stage indication is provided, via the SPK_OVERHEAT_WARN_EINTn and SPK_OVERHEAT_EINTn interrupts.

If the upper temperature threshold (SPK_OVERHEAT_EINTn) is exceeded, then the Class D speaker outputs will automatically be disabled in order to protect the device. When the speaker driver shutdown is complete, a further interrupt, SPK_SHUTDOWN_EINTn, will be asserted.

The short circuit detection function for the Class D speaker outputs is triggered when the respective output drivers are enabled (using the register bits described in Table 71). If a short circuit is detected at this time, then the enable will be unsuccessful, and the respective output driver will not be enabled.

The Class D speaker short circuit detection provides inputs to the Interrupt control circuit and can be used to trigger an Interrupt event - see "Interrupts".

If the Class D speaker short circuit condition is detected, then the respective driver(s) will automatically be disabled in order to protect the device. When the speaker driver shutdown is complete, a further interrupt, SPK_SHUTDOWN_EINTn, will be asserted.

To enable the Class D speaker outputs following a short circuit detection, the host processor must disable and re-enable the output driver(s). Note that the short circuit status bits will always be cleared when the drivers are disabled.

The short circuit detection function for the headphone output paths operates continuously whilst the respective output driver is enabled. If a short circuit is detected on any headphone output, then current limiting is applied, in order to protect

the output driver. Note that the respective output driver will continue to operate, but the output is current-limited.

The headphone output short circuit detection provides inputs to the Interrupt control circuit and can be used to trigger an Interrupt event when a short circuit condition is detected - see “Interrupts”.

The General Purpose Timers (see “DSP Peripheral Control”) can also be used to trigger a shutdown of the Class D speaker drivers. This is configured using the SPK_SHUTDOWN_TIMER_SEL register field, as described in Table 131.

If one of the General Purpose Timers is selected for the Speaker Shutdown function, and the respective Timer reaches its final count value, then the Class D speaker drivers will automatically be disabled. When the driver shutdown is complete, an interrupt event (SPK_SHUTDOWN_EINTn) will be signalled.

To enable the Class D speaker outputs following a Timeout condition, the host processor must disable and re-enable the output driver(s).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R620 (026Dh) SPK_Watchdog_1	3:0	SPK_SHUTDOWN_TIMER_SEL [3:0]	0h	Speaker Shutdown Timer select 0h = Disabled 1h = Timer 1 2h = Timer 2 3h = Timer 3 4h = Timer 4 5h = Timer 5 6h = Timer 6 7h = Timer 7 8h = Timer 8 All other codes are Reserved

Table 131 Speaker Shutdown - Timer Control

The Thermal status, Class D Speaker Short Circuit protection, and Class D Speaker shutdown flags can be output directly on a GPIO pin as an external indication of the associated events. See “General Purpose Input / Output” to configure a GPIO pin for this function.

POWER-ON RESET (POR)

The CS47L85 will remain in the reset state until AVDD, DBVDD1 and DCVDD are all above their respective reset thresholds. Note that specified device performance is not assured outside the voltage ranges defined in the "Recommended Operating Conditions" section.

Refer to "Recommended Operating Conditions" for the CS47L85 power-up sequencing requirements.

If DCVDD is powered from LDO1, then the DCVDD supply must be enabled using the LDOENA pin for the initial power-up. Note that subsequent interruption to DCVDD should only be permitted as part of a control sequence for entering Sleep mode.

After the initial power-up, the Power-On Reset will be re-scheduled following an interruption to the DBVDD1 or AVDD supplies.

If the CS47L85 SLIMbus component is in its operational state, then it must be reset prior to scheduling a Power-On Reset. See "SLIMbus Interface Control" for details of the SLIMbus reset control messages.

Following Power-On Reset (POR), a Boot Sequence is executed. The BOOT_DONE_STSx register is asserted on completion of the Boot Sequence, as described in Table 132. Control register writes should not be attempted until BOOT_DONE_STSx has been asserted.

The BOOT_DONE_STS signal is an input to the Interrupt control circuit and can be used to trigger an Interrupt event on completion of the Boot Sequence - see "Interrupts". Under default register conditions, a falling edge on the IRQ pin will indicate completion of the Boot Sequence.

For details of the Boot Sequence, see "Control Write Sequencer".

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6272 (1880h) IRQ1_Raw_Status_1	7	BOOT_DONE_STS1	0	Boot Status 0 = Busy (boot sequence in progress) 1 = Idle (boot sequence completed) Control register writes should not be attempted until Boot Sequence has completed.
R6528 (1980h) IRQ2_Raw_Status_1	7	BOOT_DONE_STS2	0	Boot Status 0 = Busy (boot sequence in progress) 1 = Idle (boot sequence completed) Control register writes should not be attempted until Boot Sequence has completed.

Table 132 Device Boot-Up Status

The CS47L85 is in Sleep mode when AVDD and DBVDD1 are present, and DCVDD is below its reset threshold. (Note that specific control requirements are also applicable for entering Sleep mode, as described in "Low Power Sleep Configuration".)

In Sleep mode, most of the Digital Core (and control registers) are held in reset; selected functions and control registers are maintained via an 'Always-On' internal supply domain. See "Low Power Sleep Configuration" for details of the 'Always-On' functions.

See "Hardware Reset, Software Reset, Wake-Up, and Device ID" for details of the Wake-Up transition (exit from Sleep mode).

Table 133 describes the default status of the CS47L85 digital I/O pins on completion of Power-On Reset, prior to any register writes. The same default conditions are also applicable on completion of a Hardware Reset or Software Reset (see "Hardware Reset, Software Reset, Wake-Up, and Device ID").

The same default conditions are applicable following a Wake-Up transition, except for the IRQ, LDOENA and RESET pins. These are 'Always-On' pins whose configuration is unchanged in Sleep mode and during a Wake-Up transition.

Note that the default conditions described in Table 133 will not be valid if modified by the Boot Sequence or by a 'Wake-Up' control sequence. See "Control Write Sequencer" for details of these functions.

PIN NO	NAME	TYPE	RESET STATUS
MICVDD power domain			
C4	IN1ALN/DMICCLK1	Analogue Input / Digital Output	Analogue input
B1	IN1RN/DMICDAT1	Analogue input / Digital Input	Analogue input
D4	IN2ALN/DMICCLK2	Analogue Input / Digital Output	Analogue input
C1	IN2ARN/DMICDAT2	Analogue input / Digital Input	Analogue input
E4	IN3LN/DMICCLK3	Analogue Input / Digital Output	Analogue input
D1	IN3RN/DMICDAT3	Analogue input / Digital Input	Analogue input
DBVDD1 power domain			
H13	AIF1BCLK/GPIO16	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
H12	AIF1LRCLK/GPIO18	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
G12	AIF1RXDAT/GPIO17	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
G11	AIF1TXDAT/GPIO15	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
H11	CIF1SS	Digital Input	Digital input
J12	CIF1MISO	Digital Output	Digital output
J11	CIF1MOSI	Digital Input	Digital input
J13	CIF1SCLK	Digital Input	Digital input
K11	CIF2SCLK	Digital Input	Digital input
K13	CIF2SDA	Digital Input / Output	Digital input
G9	GPIO1	Digital Input / Output	Digital input, Bus-keeper enabled
F11	IRQ	Digital Output	Digital output
E13	LDOENA	Digital Input	Digital input, Pull-down to DGND
F12	MCLK1	Digital Input	Digital input
K12	MIF1SCLK/GPIO9	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
L12	MIF1SDA/GPIO10	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
F13	RESET	Digital Input	Digital input, Pull-up to DBVDD1
M14	SLIMCLK	Digital Input / Output	Digital input
L13	SLIMDAT	Digital Input / Output	Digital input
DBVDD2 power domain			
M12	AIF2BCLK/GPIO20	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
L10	AIF2LRCLK/GPIO22	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
N13	AIF2RXDAT/GPIO21	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
L11	AIF2TXDAT/GPIO19	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
J7	GPIO2	Digital Input / Output	Digital input, Bus-keeper enabled
M13	MCLK2	Digital Input	Digital input
M10	MIF2SCLK/GPIO11	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
L9	MIF2SDA/GPIO12	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
N12	SPKCLK1/GPIO37	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
P11	SPKCLK2/GPIO38	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
M11	SPKDAT1/GPIO39	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
N11	SPKDAT2/GPIO40	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
H8	TCK	Digital Input	Digital input, Pull-down to DGND
J9	TDI	Digital Input	Digital input, Pull-down to DGND
H9	TDO	Digital Output	Digital Output
J8	TMS	Digital Input	Digital input, Pull-down to DGND
G8	TRST	Digital Input	Digital input, Pull-down to DGND

PIN NO	NAME	TYPE	RESET STATUS
DBVDD3 power domain			
M4	AIF3BCLK/GPIO24	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
K4	AIF3LRCLK/GPIO26	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
N4	AIF3RXDAT/GPIO25	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
L4	AIF3TXDAT/GPIO23	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
M7	AIF4BCLK/GPIO28	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
N8	AIF4LRCLK/GPIO30	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
P8	AIF4RXDAT/GPIO29	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
L7	AIF4TXDAT/GPIO27	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
L6	CIF3MISO	Digital Output	Digital output
N6	CIF3MOSI	Digital Input	Digital input
N7	CIF3SCLK	Digital Input	Digital input
M6	CIF3SS	Digital Input	Digital input
J4	GPIO3	Digital Input / Output	Digital input, Bus-keeper enabled
H7	GPIO4	Digital Input / Output	Digital input, Bus-keeper enabled
G6	GPIO5	Digital Input / Output	Digital input, Bus-keeper enabled
N5	GPIO6	Digital Input / Output	Digital input, Bus-keeper enabled
H6	GPIO7	Digital Input / Output	Digital input, Bus-keeper enabled
J6	GPIO8	Digital Input / Output	Digital input, Bus-keeper enabled
M5	MIF3SCLK/GPIO13	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
L5	MIF3SDA/GPIO14	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
DBVDD4 power domain			
N10	DMICCLK4/GPIO31	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
N9	DMICCLK5/GPIO33	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
L8	DMICCLK6/GPIO35	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
M9	DMICDAT4/GPIO32	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
P9	DMICDAT5/GPIO34	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled
M8	DMICDAT6/GPIO36	Digital Input / Output	Digital input (GPIO), Bus-keeper enabled

Table 133 CS47L85 Digital I/O Status in Reset

Note that the dual function INnLN/DMICCLKn and INnRN/DMICDATn pins default to their respective analogue input functions after Power-On Reset is completed. The analogue input functions are referenced to the MICVDD power domain.

The power-up condition of the GPIO pins depends upon whether the pin is actively driven by another device when the CS47L85 starts up. If the pin is actively driven, the bus-keeper will maintain this logic level. If the pin is not actively driven, the bus-keeper may establish either a logic 1 or logic 0 as the default input level.

HARDWARE RESET, SOFTWARE RESET, WAKE-UP, AND DEVICE ID

The CS47L85 provides a Hardware Reset function, which is executed whenever the RESET input is asserted (logic 0). The RESET input is active low and is referenced to the DBVDD1 power domain.

A Hardware Reset causes almost all of the CS47L85 control registers to be reset to their default states. The only exception is the contents of the DSP6 firmware memory, which are retained during Hardware Reset, provided DCVDD is held above its reset threshold.

An internal pull-up resistor is enabled by default on the RESET pin; this can be configured using the RESET_PU register bit. A pull-down resistor is also available, as described in Table 134. When the pull-up and pull-down resistors are both enabled, the CS47L85 provides a 'bus keeper' function on the RESET pin. The bus keeper function holds the input logic level unchanged whenever the external circuit removes the drive (e.g., if the signal is tri-stated).

If the CS47L85 SLIMbus component is in its operational state, then it must be reset prior to scheduling a Hardware Reset. See "SLIMbus Interface Control" for details of the SLIMbus reset control messages.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6864 (1AD0h) AOD_Pad _Ctrl	1	RESET_PU	1	RESET Pull-up enable 0 = Disabled 1 = Enabled Note - when RESET_PD and RESET_PU are both set to '1', then a 'bus keeper' function is enabled on the RESET pin.
	0	RESET_PD	0	RESET Pull-down enable 0 = Disabled 1 = Enabled Note - when RESET_PD and RESET_PU are both set to '1', then a 'bus keeper' function is enabled on the RESET pin.

Table 134 Reset Pull-Up Configuration

A Software Reset is executed by writing any value to register R0. A Software Reset causes most of the CS47L85 control registers to be reset to their default states. Note that the Control Write Sequencer memory and the firmware memory contents of DSP6 are retained during Software Reset.

Note that the first register read/write operation following a Software Reset may be unsuccessful, if the register access is attempted via a different Control Interface to the one that commanded the Software Reset. Note that only the first register read/write is affected, and only when using more than one Control Interface.

A Wake-Up transition (from Sleep mode) is similar to a Software Reset, but selected functions and control registers are maintained via an 'Always-On' internal supply domain. The 'Always-On' registers are not reset during Wake-Up. See "Low Power Sleep Configuration" for details of the 'Always-On' functions.

The Control Write Sequencer memory contents will revert to its default contents following Power-On Reset (POR), Hardware Reset, or a Sleep mode transition. The control sequences (including any user-defined sequences) are maintained in the sequencer memory through Software Reset.

The DSP firmware memory contents are cleared following Power-On Reset (POR), or a Sleep mode transition. The firmware memory contents are not affected by Software Reset, provided DCVDD is held above its reset threshold. On DSP1 to DSP5, and on DSP7, the firmware memory contents are cleared under Hardware Reset conditions. On DSP6 only, the firmware memory is retained through Hardware Reset, provided DCVDD is held above its reset threshold.

See the "Applications Information" section for a summary of the CS47L85 memory reset conditions. The DSPn_MEM_ENA register bits are described in Table 27.

If DCVDD is powered from LDO1, it is recommended that the LDOENA pin is asserted (logic 1) before Hardware Reset or Software Reset; this ensures the DSP memory contents can be retained, and also allows faster reset time.

Following Hardware Reset, Software Reset or Wake-Up (from Sleep mode), a Boot Sequence is executed. The BOOT_DONE_STSx register (see Table 132) is de-asserted during Hardware Reset, Software Reset and in Sleep mode. The BOOT_DONE_STSx register is asserted on completion of the Boot Sequence. Control register writes should not be attempted until BOOT_DONE_STSx has been asserted.

The BOOT_DONE_STSx status is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see "Interrupts".

For details of the Boot Sequence, see “Control Write Sequencer”.

The status of the CS47L85 digital I/O pins following Hardware Reset, Software Reset or Wake-Up is described in the “Power-On Reset (POR)” section.

The Device ID can be read back from Register R0. The Hardware Revision can be read back from Register R1.

The Software Revision can be read back from Register R2. The Software Revision code is incremented if software driver compatibility or software feature support is changed.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (0000h) Software_Reset	15:0	SW_RST_DEV_ID [15:0]	6338h	Writing to this register resets all registers to their default state. Reading from this register will indicate Device ID 6338h.
R1 (0001h) Hardware_Revision	7:0	HW_REVISION [7:0]		Hardware Device revision. (incremented for every new revision of the device)
R2 (0002h) Software_Revision	6:0	SW_REVISION [6:0]		Software Device revision. (incremented if software driver compatibility or software feature support is changed)

Table 135 Device Reset and ID

REGISTER MAP

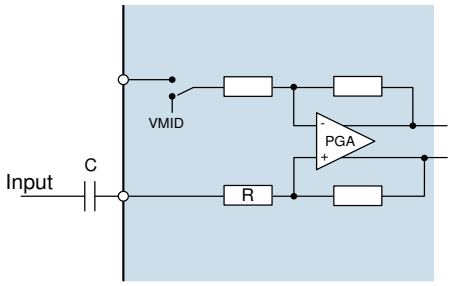
The CS47L85 Register Map listing is contained within Technical Note WTN0573.
Please contact your local Cirrus Logic representative for more details.

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

ANALOGUE INPUT PATHS

The CS47L85 provides up to 6 analogue audio input paths. Each of these inputs is referenced to the internal DC reference, VMID. A DC blocking capacitor is required for each analogue input pin used in the target application. The choice of capacitor is determined by the filter that is formed between that capacitor and the impedance of the input pin. The circuit is illustrated in Figure 87.



$$Fc = \frac{1}{2\pi RC}$$

Fc = high pass 3dB cut-off frequency

Figure 87 Audio Input Path DC Blocking Capacitor

In accordance with the CS47L85 input pin resistance (see “Electrical Characteristics”), it is recommended that a 1µF capacitance for all input connections will give good results in most cases, with a 3dB cut-off frequency around 13Hz.

Ceramic capacitors are suitable, but care must be taken to ensure the desired capacitance is maintained at the AVDD operating voltage. Also, ceramic capacitors may show microphonic effects, where vibrations and mechanical conditions give rise to electrical signals. This is particularly problematic for microphone input paths where a large signal gain is required.

A single capacitor is required for a single-ended line or microphone input connection. For a differential input connection, a DC blocking capacitor is required on both input pins.

The external connections for single-ended and differential microphones, incorporating the CS47L85 microphone bias circuit, are shown later in the “Microphone Bias Circuit” section - see Figure 88.

DIGITAL MICROPHONE INPUT PATHS

The CS47L85 provides up to 8 digital microphone input paths; two channels of audio data can be multiplexed on each of the DMICDATn pins. Each of these stereo pairs is clocked using the respective DMICCLKn pin.

The external connections for digital microphones, incorporating the CS47L85 microphone bias circuit, are shown later in the “Microphone Bias Circuit” section - see Figure 90.

Ceramic decoupling capacitors for the digital microphones may be required - refer to the specific recommendations for the application microphone(s).

When two microphones are connected to a single DMICDAT pin, the microphones must be configured to ensure that the Left mic transmits a data bit when DMICCLK is high, and the Right mic transmits a data bit when DMICCLK is low. The CS47L85 samples the digital microphone data at the end of each DMICCLK phase. Each microphone must tri-state its data output when the other microphone is transmitting. Integrated pull-down resistors can be enabled on the DMICDAT pins if required.

The voltage reference for each digital microphone interface is selectable. It is important that the selected reference for the CS47L85 interface is compatible with the applicable configuration of the external microphone.

MICROPHONE BIAS CIRCUIT

The CS47L85 is designed to interface easily with up to 6 analogue or 8 digital microphones.

Each microphone requires a bias current (electret condenser microphones) or voltage supply (silicon microphones); these can be provided by the MICBIAS1, MICBIAS2 or MICBIAS3 regulators on the CS47L85.

Note that the MICVDD pin can also be used (instead of MICBIASn) as a reference or power supply for external microphones. The MICBIAS outputs are recommended, as these offer better noise performance and independent enable/disable control.

Analogue microphones may be connected in single-ended or differential configurations, as illustrated in Figure 88. The differential configuration provides better performance due to its rejection of common-mode noise; the single-ended method provides a reduction in external component count.

A bias resistor is required when using an electret condenser microphone (ECM). The bias resistor should be chosen according to the minimum operating impedance of the microphone and MICBIAS voltage so that the maximum bias current of the CS47L85 is not exceeded.

A 2.2kΩ bias resistor is recommended; this provides compatibility with a wide range of microphone components.

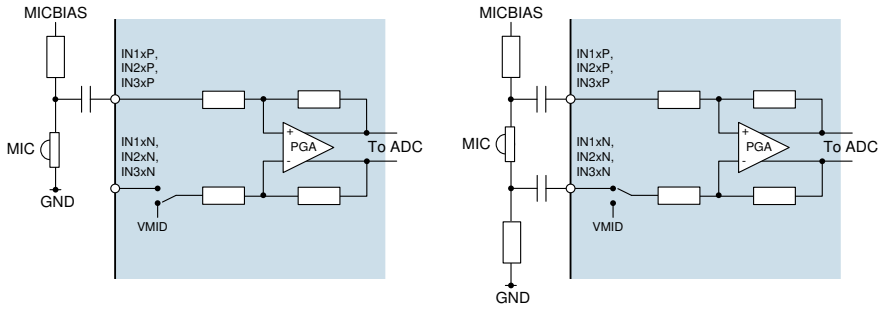


Figure 88 Single-Ended and Differential Analogue Microphone Connections

Analogue MEMS microphones can be connected to the CS47L85 as illustrated in Figure 89. In this configuration, the MICBIAS generators provide a low-noise supply for the microphones; a bias resistor is not required.

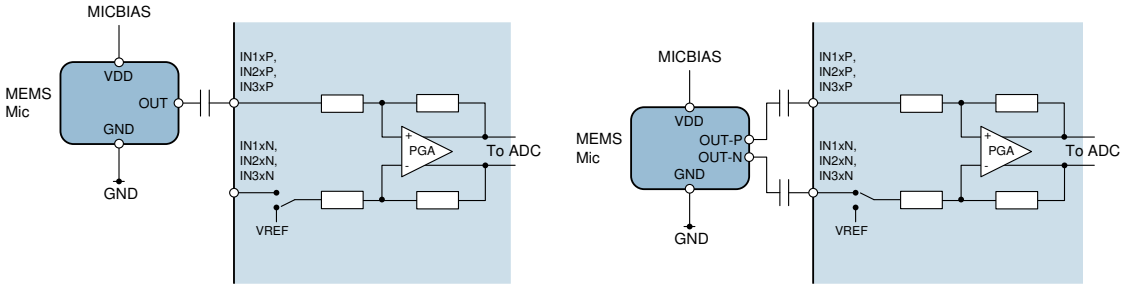


Figure 89 Single-Ended and Differential Analogue Microphone Connections

Digital microphone connection to the CS47L85 is illustrated in Figure 90.

Ceramic decoupling capacitors for the digital microphones may be required - refer to the specific recommendations for the application microphone(s).

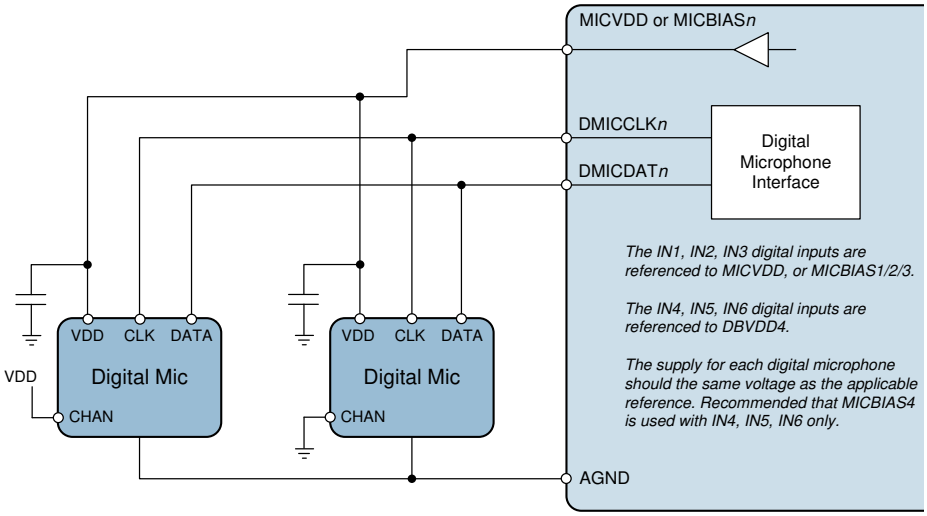


Figure 90 Digital Microphone Connection

The MICBIAS generators can each operate as a voltage regulator or in bypass mode. See “Charge Pumps, Regulators and Voltage Reference” for details of the MICBIAS generators.

In Regulator mode, the MICBIAS regulators are designed to operate without external decoupling capacitors. The regulators can be configured to support a capacitive load if required (e.g., for digital microphone supply decoupling). The compatible load conditions are detailed in the “Electrical Characteristics” section.

If the capacitive load on MICBIAS1, MICBIAS2 or MICBIAS3 exceeds the specified conditions for Regulator mode (e.g., due to a decoupling capacitor or long PCB trace), then the respective generator must be configured in Bypass mode.

The maximum output current for each MICBIAS*n* pin is noted in the “Electrical Characteristics”. This limit must be observed on each MICBIAS output, especially if more than one microphone is connected to a single MICBIAS pin. Note that the maximum output current differs between Regulator mode and Bypass mode. The MICBIAS output voltage can be adjusted using register control in Regulator mode.

HEADPHONE DRIVER OUTPUT PATH

The CS47L85 provides 3 stereo headphone output drivers. These outputs are all ground-referenced, allowing direct connection to the external load(s). There is no requirement for DC blocking capacitors.

In single-ended (default) configuration, the headphone outputs comprise 6 independently controlled output channels, for up to 3 stereo headphone or line outputs. In mono (BTL) mode, the headphone drivers support up to 3 differential outputs, suitable for a mono earpiece or hearing coil load.

The headphone outputs incorporate a common mode, or ground loop, feedback path which provides rejection of system-related ground noise. The feedback pins must be connected to ground for normal operation of the headphone outputs. A separate feedback path is provided for each of the stereo headphone outputs. The HPOUT1 feedback is supported on two pins - the applicable pin is selected using the ACCDET_SRC register bit.

The feedback pins should be connected to GND close to the respective headphone jack, as illustrated in Figure 91. In mono (differential) mode, the feedback pin(s) should be connected to the ground plane that is physically closest to the earpiece output PCB tracks.

It is recommended to ensure that the electrical characteristics of the PCB traces for each output pair are closely matched. This is particularly important to matching the two traces of a differential (BTL) output.

Typical headphone and earpiece connections are illustrated in Figure 91.

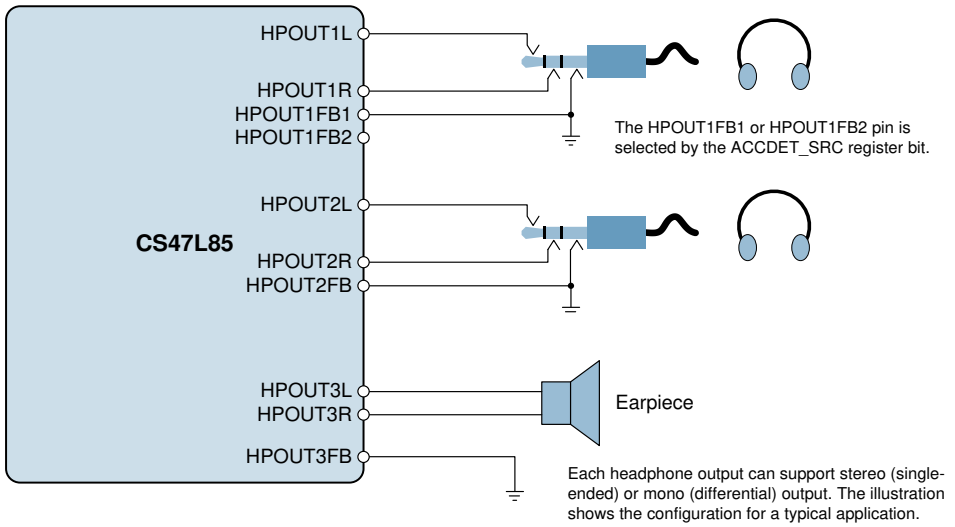


Figure 91 Headphone and Earpiece Connection

It is common for ESD diodes to be wired to pins that link to external connectors. This provides protection from potentially harmful ESD effects. In a typical application, ESD diodes would be recommended for the headphone paths (HPOUT1, HPOUT2, HPOUT3), when used as external headphone or line output.

The HPOUTn outputs are ground-referenced, and the respective voltages may swing between +1.8V and -1.8V. The ESD diode configuration must be carefully chosen.

The recommended ESD diode configuration for these ground-referenced outputs is illustrated in Figure 92. The 'back-to-back' arrangement is necessary in order to prevent clipping and distortion of the output signal.

Note that similar care is required when connecting the CS47L85 outputs to external circuits that provide input path ESD protection - the configuration on those input circuits must be correctly designed to accommodate ground-referenced signals.

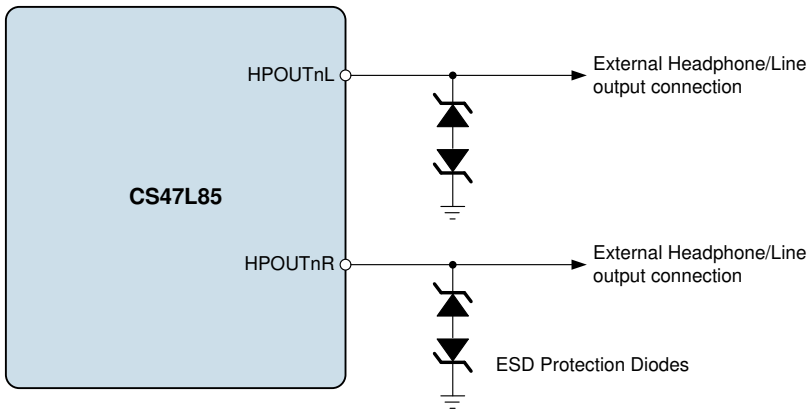


Figure 92 ESD Diode Configuration for External Output Connections

SPEAKER DRIVER OUTPUT PATH

The CS47L85 incorporates two Class D speaker drivers, offering high amplifier efficiency at large signal levels. As the Class D output is a pulse width modulated signal, the choice of speakers and tracking of signals is critical for ensuring good performance and reducing EMI in this mode.

The efficiency of the speaker drivers is affected by the series resistance between the CS47L85 and the speaker (e.g. PCB track loss and inductor ESR) as shown in Figure 93. This resistance should be as low as possible to maximise efficiency.

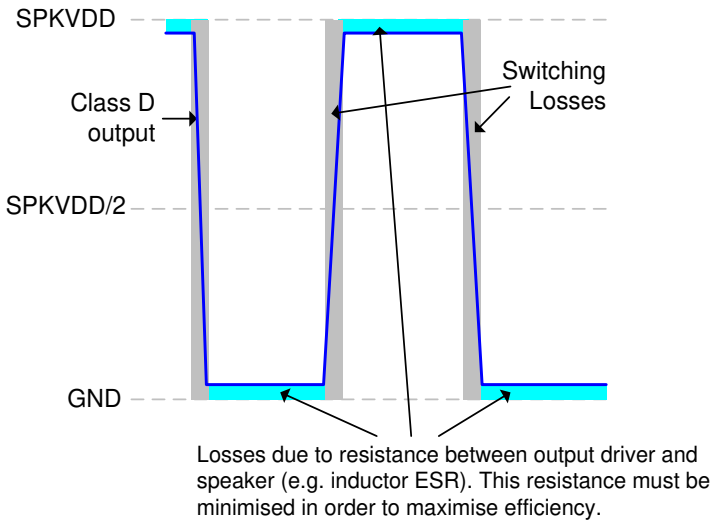


Figure 93 Speaker Connection Losses

The Class D output requires external filtering in order to recreate the audio signal. This may be implemented using a 2nd order LC or 1st order RC filter, or else may be achieved by using a loudspeaker whose internal inductance provides the required filter response. An LC or RC filter should be used if the loudspeaker characteristics are unknown or unsuitable, or if the length of the loudspeaker connection is likely to lead to EMI problems.

In applications where it is necessary to provide Class D filter components, a 2nd order LC filter is the recommended solution as it provides more attenuation at higher frequencies and minimises power dissipated in the filter when compared to a first order RC filter (lower ESR). This maximises both rejection of unwanted switching frequencies and overall speaker efficiency. A suitable implementation is illustrated in Figure 94.

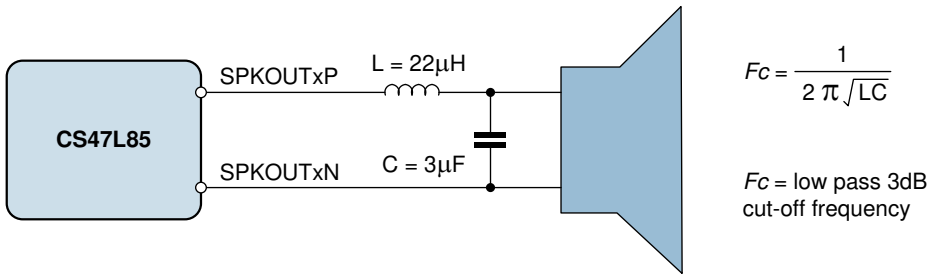


Figure 94 Class D Output Filter Components

A simple equivalent circuit of a loudspeaker consists of a serially connected resistor and inductor, as shown in Figure 95. This circuit provides a low pass filter for the speaker output. If the loudspeaker characteristics are suitable, then the loudspeaker itself can be used in place of the filter components described earlier. This is known as 'filterless' operation.

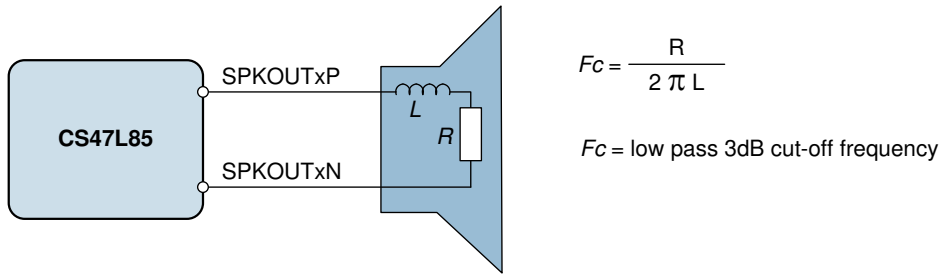


Figure 95 Speaker Equivalent Circuit for Filterless Operation

For filterless Class D operation, it is important to ensure that a speaker with suitable inductance is chosen. For example, if we know the speaker impedance is 8Ω and the desired cut-off frequency is 20kHz, then the optimum speaker inductance may be calculated as:

$$L = \frac{R}{2 \pi Fc} = \frac{8\Omega}{2 \pi * 20kHz} = 64\mu H$$

8Ω loudspeakers typically have an inductance in the range 20μH to 100μH, however, it should be noted that a loudspeaker inductance will not be constant across the relevant frequencies for Class D operation (up to and beyond the Class D switching frequency). Care should be taken to ensure that the cut-off frequency of the loudspeaker's filtering is low enough to suppress the high frequency energy of the Class D switching and, in so doing, to prevent speaker damage. The Class D outputs of the CS47L85 operate at much higher frequencies than is recommended for most speakers and it must be ensured that the cut-off frequency is low enough to protect the speaker.

The Class D speaker outputs are designed to support monitoring of external loudspeakers, giving real-time feedback for algorithms such as Cirrus Logic's Speaker Protection software. This enables maximum audio output to be achieved, whilst ensuring the loudspeakers are also fully protected from damage,

The external speaker connections, incorporating the output current monitoring requirements, are illustrated in Figure 96. Note that, if output current monitoring is not required on one or more speaker channels, then the respective ground connections should be tied directly to ground on the PCB.

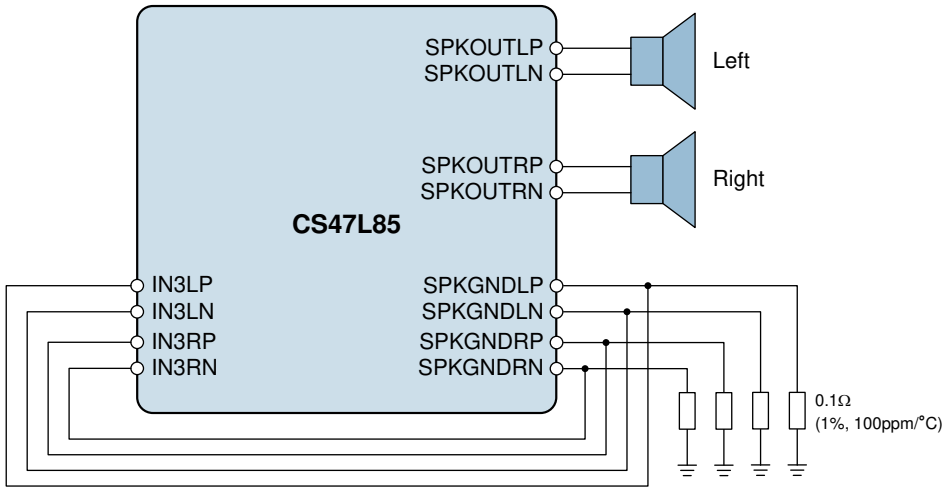


Figure 96 Speaker Output Current Monitoring Connections (Speaker Protection)

POWER SUPPLY / REFERENCE DECOUPLING

Electrical coupling exists particularly in digital logic systems where switching in one sub-system causes fluctuations on the power supply. This effect occurs because the inductance of the power supply acts in opposition to the changes in current flow that are caused by the logic switching. The resultant variations ('spikes') in the power supply voltage can cause malfunctions and unintentional behaviour in other components. A decoupling ('bypass') capacitor can be used as an energy storage component which will provide power to the decoupled circuit for the duration of these power supply variations, protecting it from malfunctions that could otherwise arise.

Coupling also occurs in a lower frequency form when ripple is present on the power supply rail caused by changes in the load current or by limitations of the power supply regulation method. In audio components such as the CS47L85, these variations can alter the performance of the signal path, leading to degradation in signal quality. A decoupling capacitor can be used to filter these effects, by presenting the ripple voltage with a low impedance path that does not affect the circuit to be decoupled.

These coupling effects are addressed by placing a capacitor between the supply rail and the corresponding ground reference. In the case of systems comprising multiple power supply rails, decoupling should be provided on each rail.

The recommended power supply decoupling capacitors for CS47L85 are detailed below in Table 136.

POWER SUPPLY	DECOUPLING CAPACITOR
LDOVDD, DBVDD1, DBVDD2, DBVDD3	0.1µF ceramic (see Note)
AVDD1, AVDD2	1.0µF ceramic
CPVDD	4.7µF ceramic
CPVDD2	4.7µF ceramic
MICVDD	4.7µF ceramic
DCVDD, FLLVDD	4 x 1.0µF ceramic - one close to each pin. Alternatively, a single 4.7µF ceramic.
SPKVDDL, SPKVDDR	4.7µF ceramic
VREFC	2.2µF ceramic

Table 136 Power Supply Decoupling Capacitors

Note: 0.1µF is required with 4.7µF a guide to the total required power rail capacitance.

All decoupling capacitors should be placed as close as possible to the CS47L85 device. The connection between AGND, the AVDD decoupling capacitor and the main system ground should be made at a single point as close as possible to the AGND balls of the CS47L85.

Due to the wide tolerance of many types of ceramic capacitors, care must be taken to ensure that the selected components provide the required capacitance across the required temperature and voltage ranges in the intended application. For most application the use of ceramic capacitors with capacitor dielectric X5R is recommended.

CHARGE PUMP COMPONENTS

The CS47L85 incorporates two Charge Pump circuits, identified as CP1 and CP2.

CP1 generates the CP1VOUTP and CP1VOUTN supply rails for the ground-referenced headphone drivers; CP2 generates the CP2VOUT supply rail for the microphone bias (MICBIAS) regulators.

Decoupling capacitors are required on each of the Charge Pump outputs. Two fly-back capacitors are required for CP1; a single fly-back capacitor is required for CP2.

The recommended Charge Pump capacitors for CS47L85 are detailed below in Table 137.

DESCRIPTION	CAPACITOR
CP1VOUT1P decoupling	Required capacitance is 2.0µF at 2V. Suitable component typically 4.7µF.
CP1VOUT1N decoupling	Required capacitance is 2.0µF at 2V. Suitable component typically 4.7µF.
CP1 fly-back 1 (connect between CP1C1A and CP1C1B)	Required capacitance is 1.0µF at 2V. Suitable component typically 2.2µF.
CP1VOUT2P decoupling	Required capacitance is 2.0µF at 2V. Suitable component typically 4.7µF.
CP1VOUT2N decoupling	Required capacitance is 2.0µF at 2V. Suitable component typically 4.7µF.
CP1 fly-back 2 (connect between CP1C2A and CP1C2B)	Required capacitance is 1.0µF at 2V. Suitable component typically 2.2µF.
CP2VOUT decoupling	Required capacitance is 1.0µF at 3.6V. Suitable component typically 4.7µF.
CP2 fly-back (connect between CP2CA and CP2CB)	Required capacitance is 220nF at 2V. Suitable component typically 470nF.

Table 137 Charge Pump External Capacitors

Ceramic capacitors are recommended for these Charge Pump requirements. Note that, due to the wide tolerance of many types of ceramic capacitors, care must be taken to ensure that the selected components provide the required capacitance across the required temperature and voltage ranges in the intended application. Ceramic capacitors with X5R dielectric are recommended.

The positioning of the Charge Pump capacitors is important, particularly the fly-back capacitors. These capacitors should be placed as close as possible to the CS47L85. The component choice and positioning of the CP1 components are more critical than those of CP2, due to the higher output power requirements of CP1.

EXTERNAL ACCESSORY DETECTION COMPONENTS

The external accessory detection circuit measures jack insertion using the JACKDET1 and JACKDET2 pins. The insertion switch status is detected using an internal pull-up resistor circuit on the respective pin. The logic thresholds associated with the each of the JACKDETn pins are the same, as noted in the “Electrical Characteristics” section. Note that an external resistor (e.g., 500kΩ) can be used to lower the effective jack detection thresholds; this provides support for different jack switch configurations.

Microphone detection and key-button press detection is supported using the MICDETn pins. The applicable pin should be connected to one of the MICBIASn outputs, via a 2.2kΩ bias resistor, as described in the “Microphone Bias Circuit” section. Note that, when using the External Accessory Detection function, the MICBIASn resistor must be 2.2kΩ +/-2%.

A recommended circuit configuration, including headphone output on HPOUT1 and microphone connections, is shown in Figure 97. See “Analogue Input Paths” for details of the DC-blocking microphone input capacitor selection.

The recommended external components and connections for microphone / push-button detection are illustrated in Figure 98.

Note that, when using the Microphone Detect circuit, it is recommended to use the IN1B or IN2B analogue microphone input paths, to ensure best immunity to electrical transients arising from the external accessory.

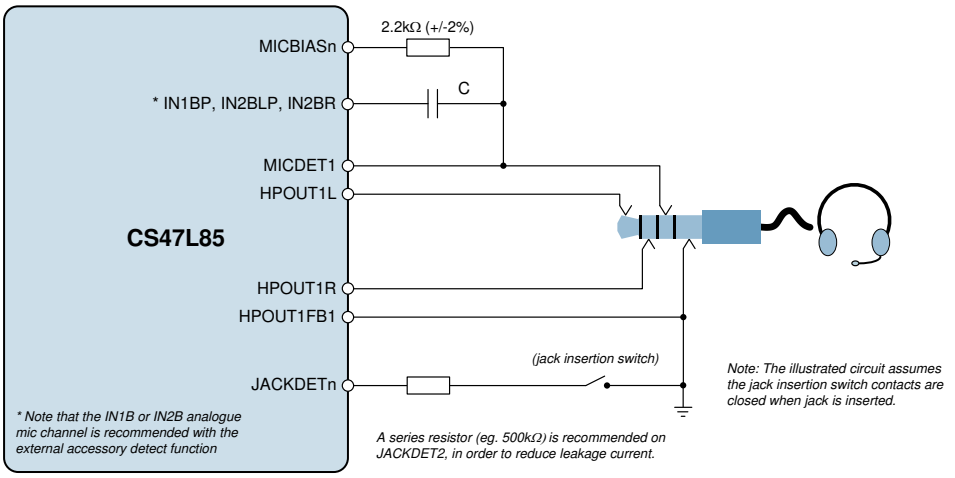


Figure 97 External Accessory Detection

The accessory detection circuit measures the impedance of an external load connected to one of the MICDET pins.

The microphone detection circuit uses MICVDD, MICBIAS1, MICBIAS2 or MICBIAS3 as a reference. The applicable source is configured using the MICD_BIAS_SRC register.

The CS47L85 can detect the presence of a typical microphone and up to 6 push-buttons, using the components shown in Figure 98. When the microphone detection circuit is enabled, then each of the push-buttons shown will cause a different bit within the MICD_LVL register to be set.

The microphone detect function is specifically designed to detect a video accessory (typical 75Ω) load if required. A measured external impedance of 75Ω will cause the MICD_LVL [3] bit to be set.

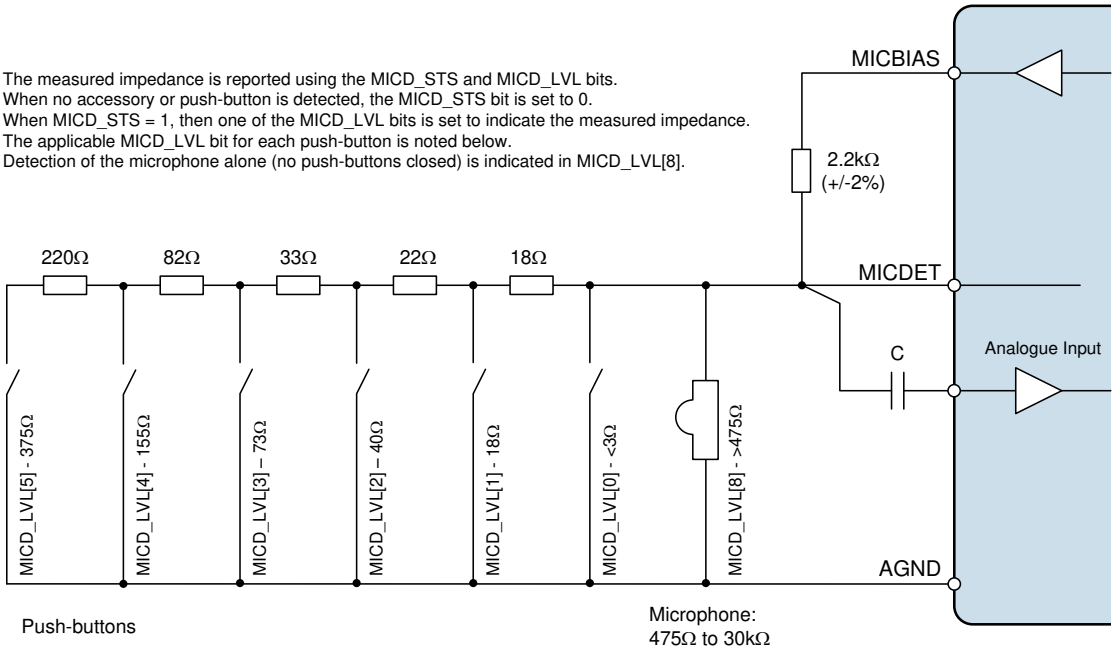
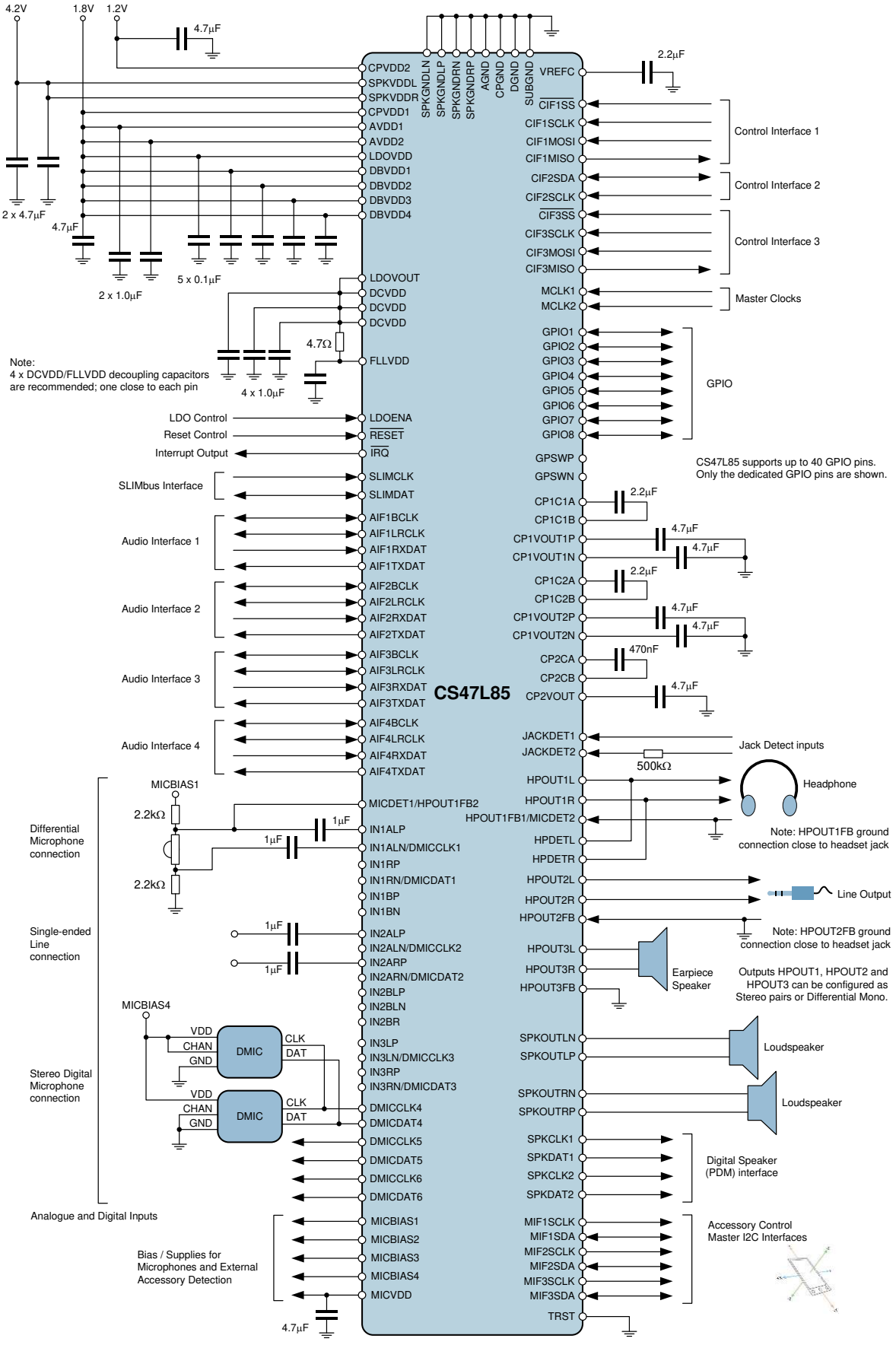


Figure 98 External Accessory Detect Connection

RECOMMENDED EXTERNAL COMPONENTS DIAGRAM



RESETS SUMMARY

The contents of Table 138 provide a summary of the CS47L85 registers and other programmable memory under different reset conditions. The associated events and conditions are listed below.

- A Power-On Reset occurs when AVDD or DBVDD1 is below its respective reset threshold. (Note that DCVDD is also required for initial start-up; subsequent interruption to DCVDD should only be permitted as part of a control sequence for entering Sleep mode.)
- A Hardware Reset occurs when the RESET input is asserted (logic 0).
- A Software Reset occurs when register R0 is written to.
- Sleep Mode is selected when LDO1 is disabled. Note that the AVDD, DBVDD1 and LDOVDD supplies must be present, and the LDOENA pin held low. (It is assumed that DCVDD is supplied by LDO1.)

	ALWAYS-ON REGISTERS	OTHER REGISTERS	CONTROL SEQUENCER MEMORY	DSP FIRMWARE MEMORY DSP1,2,3,4,5,7	DSP FIRMWARE MEMORY DSP6
Power-On Reset	Reset	Reset	Reset	Reset	Reset
Hardware Reset	Reset	Reset	Reset	Reset	Retained (see note)
Software Reset	Reset	Reset	Retained	Retained (see note)	Retained (see note)
Sleep Mode	Retained	Reset	Reset	Reset	Reset

Table 138 Memory Reset Summary

See “Low Power Sleep Configuration” for details of Sleep Mode, and the ‘Always-On’ registers.

Note that, to retain the DSP firmware memory contents during Hardware Reset or Software Reset, it must be ensured that DCVDD is held above its reset threshold. If DCVDD is powered from internal LDO, then it is recommended to assert the LDOENA pin before the Reset, in order to maintain the DCVDD supply.

OUTPUT SIGNAL DRIVE STRENGTH CONTROL

The CS47L85 supports configurable drive strength control for the digital output pins. This can be used to assist system-level integration and design considerations.

The drive strength control registers are described in Table 139. Note that, in the case of bi-directional pins (e.g., GPIOn), the drive strength control registers are only applicable when the pin is configured as an output.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (0008h) Ctrl_IF_CFG_1	8	CIF1MISO_DRV_STR	1	CIF1MISO output drive strength 0 = 4mA 1 = 8mA
R9 (0009h) Ctrl_IF_CFG_2	9	CIF2SDA_DRV_STR	1	CIF2SDA output drive strength 0 = 4mA 1 = 8mA
R10 (000Ah) Ctrl_IF_CFG_3	8	CIF3MISO_DRV_STR	1	CIF3MISO output drive strength 0 = 4mA 1 = 8mA
R1520 (05F0h) Slimbus_Pad_Ctrl	1	SLIMDAT_DRV_STR	0	SLIMDAT output drive strength 0 = 8mA 1 = 12mA
	0	SLIMCLK_DRV_STR	0	SLIMCLK output drive strength 0 = 2mA 1 = 4mA
R5889 (1701h) GPIO1_CTRL2	12	GP1_DRV_STR	1	GPIO1 output drive strength 0 = 4mA 1 = 8mA
R5891 (1703h) GPIO2_CTRL2	12	GP2_DRV_STR	1	GPIO2 output drive strength 0 = 4mA 1 = 8mA
R5893 (1705h) GPIO3_CTRL2	12	GP3_DRV_STR	1	GPIO3 output drive strength 0 = 4mA 1 = 8mA
R5895 (1707h) GPIO4_CTRL2	12	GP4_DRV_STR	1	GPIO4 output drive strength 0 = 4mA 1 = 8mA
R5897 (1709h) GPIO5_CTRL2	12	GP5_DRV_STR	1	GPIO5 output drive strength 0 = 4mA 1 = 8mA
R5899 (170Bh) GPIO6_CTRL2	12	GP6_DRV_STR	1	GPIO6 output drive strength 0 = 4mA 1 = 8mA
R5901 (170Dh) GPIO7_CTRL2	12	GP7_DRV_STR	1	GPIO7 output drive strength 0 = 4mA 1 = 8mA
R5903 (170Fh) GPIO8_CTRL2	12	GP8_DRV_STR	1	GPIO8 output drive strength 0 = 4mA 1 = 8mA

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5905 (1711h) GPIO9_CTRL2	12	GP9_DRV_STR	1	MIF1SCLK/GPIO9 output drive strength 0 = 4mA 1 = 8mA
R5907 (1713h) GPIO10_CTRL2	12	GP10_DRV_STR	1	MIF1SDA/GPIO10 output drive strength 0 = 4mA 1 = 8mA
R5909 (1715h) GPIO11_CTRL2	12	GP11_DRV_STR	1	MIF2SCLK/GPIO11 output drive strength 0 = 4mA 1 = 8mA
R5911 (1717h) GPIO12_CTRL2	12	GP12_DRV_STR	1	MIF2SDA/GPIO12 output drive strength 0 = 4mA 1 = 8mA
R5913 (1719h) GPIO13_CTRL2	12	GP13_DRV_STR	1	MIF3SCLK/GPIO13 output drive strength 0 = 4mA 1 = 8mA
R5915 (171Bh) GPIO14_CTRL2	12	GP14_DRV_STR	1	MIF3SDA/GPIO14 output drive strength 0 = 4mA 1 = 8mA
R5917 (171Dh) GPIO15_CTRL2	12	GP15_DRV_STR	1	AIF1TXDAT/GPIO15 output drive strength 0 = 4mA 1 = 8mA
R5919 (171Fh) GPIO16_CTRL2	12	GP16_DRV_STR	1	AIF1BCLK/GPIO16 output drive strength 0 = 4mA 1 = 8mA
R5921 (1721h) GPIO17_CTRL2	12	GP17_DRV_STR	1	AIF1RXDAT/GPIO17 output drive strength 0 = 4mA 1 = 8mA
R5923 (1723h) GPIO18_CTRL2	12	GP18_DRV_STR	1	AIF1LRCLK/GPIO18 output drive strength 0 = 4mA 1 = 8mA
R5925 (1725h) GPIO19_CTRL2	12	GP19_DRV_STR	1	AIF2TXDAT/GPIO19 output drive strength 0 = 4mA 1 = 8mA
R5927 (1727h) GPIO20_CTRL2	12	GP20_DRV_STR	1	AIF2BCLK/GPIO20 output drive strength 0 = 4mA 1 = 8mA
R5929 (1729h) GPIO21_CTRL2	12	GP21_DRV_STR	1	AIF2RXDAT/GPIO21 output drive strength 0 = 4mA 1 = 8mA
R5931 (172Bh) GPIO22_CTRL2	12	GP22_DRV_STR	1	AIF2LRCLK/GPIO22 output drive strength 0 = 4mA 1 = 8mA
R5933 (172Dh) GPIO23_CTRL2	12	GP23_DRV_STR	1	AIF3TXDAT/GPIO23 output drive strength 0 = 4mA 1 = 8mA

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5935 (172Fh) GPIO24_ CTRL2	12	GP24_DRV_STR	1	AIF3BCLK/GPIO24 output drive strength 0 = 4mA 1 = 8mA
R5937 (1731h) GPIO25_ CTRL2	12	GP25_DRV_STR	1	AIF3RXDAT/GPIO25 output drive strength 0 = 4mA 1 = 8mA
R5939 (1733h) GPIO26_ CTRL2	12	GP26_DRV_STR	1	AIF3LRCLK/GPIO26 output drive strength 0 = 4mA 1 = 8mA
R5941 (1735h) GPIO27_ CTRL2	12	GP27_DRV_STR	1	AIF4TXDAT/GPIO27 output drive strength 0 = 4mA 1 = 8mA
R5943 (1737h) GPIO28_ CTRL2	12	GP28_DRV_STR	1	AIF4BCLK/GPIO28 output drive strength 0 = 4mA 1 = 8mA
R5945 (1739h) GPIO29_ CTRL2	12	GP29_DRV_STR	1	AIF4RXDAT/GPIO29 output drive strength 0 = 4mA 1 = 8mA
R5947 (173Bh) GPIO30_ CTRL2	12	GP30_DRV_STR	1	AIF4LRCLK/GPIO30 output drive strength 0 = 4mA 1 = 8mA
R5949 (173Dh) GPIO31_ CTRL2	12	GP31_DRV_STR	1	DMICCLK4/GPIO31 output drive strength 0 = 4mA 1 = 8mA
R5951 (173Fh) GPIO32_ CTRL2	12	GP32_DRV_STR	1	DMICDAT4/GPIO32 output drive strength 0 = 4mA 1 = 8mA
R5953 (1741h) GPIO33_ CTRL2	12	GP33_DRV_STR	1	DMICCLK5/GPIO33 output drive strength 0 = 4mA 1 = 8mA
R5955 (1743h) GPIO34_ CTRL2	12	GP34_DRV_STR	1	DMICDAT5/GPIO34 output drive strength 0 = 4mA 1 = 8mA
R5957 (1745h) GPIO35_ CTRL2	12	GP35_DRV_STR	1	DMICCLK6/GPIO35 output drive strength 0 = 4mA 1 = 8mA
R5959 (1747h) GPIO36_ CTRL2	12	GP36_DRV_STR	1	DMICDAT6/GPIO36 output drive strength 0 = 4mA 1 = 8mA
R5961 (1749h) GPIO37_ CTRL2	12	GP37_DRV_STR	1	SPKCLK1/GPIO37 output drive strength 0 = 4mA 1 = 8mA
R5963 (174Bh) GPIO38_ CTRL2	12	GP38_DRV_STR	1	SPKCLK2/GPIO38 output drive strength 0 = 4mA 1 = 8mA

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5965 (174Dh) GPIO39_ CTRL2	12	GP39_DRV_STR	1	SPKDAT1/GPIO39 output drive strength 0 = 4mA 1 = 8mA
R5967 (174Fh) GPIO40_ CTRL2	12	GP40_DRV_STR	1	SPKDAT2/GPIO40 output drive strength 0 = 4mA 1 = 8mA

Table 139 Output Drive Strength and Slew Rate Control

DIGITAL AUDIO INTERFACE CLOCKING CONFIGURATIONS

The digital audio interfaces (AIF1, AIF2, AIF3, AIF4) can be configured in Master or Slave modes. In all applications, it is important that the system clocking configuration is correctly designed. Incorrect clock configurations will lead to audible clicks arising from dropped or repeated audio samples; this is caused by the inherent tolerances of multiple asynchronous system clocks.

To ensure reliable clocking of the audio interface functions, it is a requirement that the external interface clocks (e.g., BCLK, LRCLK) are derived from the same clock source as SYSCLK (or ASYNCCLK, where applicable).

In AIF Master mode, the external BCLK and LRCLK signals are generated by the CS47L85 and synchronisation of these signals with SYSCLK (or ASYNCCLK) is ensured. In this case, clocking of the AIF is typically derived from the MCLK1 or MCLK2 inputs, either directly or via one of the Frequency Locked Loop (FLL) circuits. It is also possible to use a different interface (AIFn or SLIMbus) to provide the reference clock to which the AIF Master can be synchronised.

In AIF Slave mode, the external BCLK and LRCLK signals are generated by another device, as inputs to the CS47L85. In this case, it must be ensured that the applicable system clock (SYSCLK or ASYNCCLK) is generated from a source that is synchronised to the external BCLK and LRCLK inputs.

In a typical Slave mode application, the BCLK input is selected as the clock reference, using the FLL to perform frequency shifting. It is also possible to use the MCLK1 or MCLK2 inputs, but only if the selected clock is synchronised externally to the BCLK and LRCLK inputs. The SLIMbus interface can also provide the clock reference, via one of the FLLs, provided that the BCLK and LRCLK signals are externally synchronised with the SLIMCLK input.

The valid AIF clocking configurations are listed in Table 140 for AIF Master and AIF Slave modes.

The applicable system clock (SYSCLK or ASYNCCLK) depends on the AIFn_RATE setting for the relevant digital audio interface; if AIFn_RATE < 1000, then SYSCLK is applicable; if AIFn_RATE ≥ 1000, then ASYNCCLK is applicable.

AIF MODE	CLOCKING CONFIGURATION
AIF Master Mode	SYSCLK_SRC (ASYNCCLK_SRC) selects MCLK1 or MCLK2 as SYSCLK (ASYNCCLK) source.
	SYSCLK_SRC (ASYNCCLK_SRC) selects FLLn as SYSCLK (ASYNCCLK) source; FLLn_REFCLK_SRC selects MCLK1 or MCLK2 as FLLn source.
	SYSCLK_SRC (ASYNCCLK_SRC) selects FLLn as SYSCLK (ASYNCCLK) source; FLLn_REFCLK_SRC selects a different interface (BCLK, LRCLK, SLIMCLK) as FLLn source.
AIF Slave Mode	SYSCLK_SRC (ASYNCCLK_SRC) selects FLLn as SYSCLK (ASYNCCLK) source; FLLn_REFCLK_SRC selects BCLK as FLLn source.
	SYSCLK_SRC (ASYNCCLK_SRC) selects MCLK1 or MCLK2 as SYSCLK (ASYNCCLK) source, provided MCLK is externally synchronised to the BCLK input.
	SYSCLK_SRC (ASYNCCLK_SRC) selects FLLn as SYSCLK (ASYNCCLK) source; FLLn_REFCLK_SRC selects MCLK1 or MCLK2 as FLLn source, provided MCLK is externally synchronised to the BCLK input.
	SYSCLK_SRC (ASYNCCLK_SRC) selects FLLn as SYSCLK (ASYNCCLK) source; FLLn_REFCLK_SRC selects a different interface (e.g., SLIMCLK) as FLLn source, provided the other interface is externally synchronised to the BCLK input.

Table 140 Audio Interface (AIF) Clocking Confgurations

In each case, the SYSCLK (ASYNCCLK) frequency must be a valid ratio to the LRCLK frequency; the supported clocking rates are defined by the SYSCLK_FREQ (ASYNC_CLK_FREQ) and SAMPLE_RATE_n (ASYNC_SAMPLE_RATE_n) registers.

The valid AIF clocking configurations are illustrated in Figure 99 to Figure 105 below. Note that, where MCLK1 is illustrated as the clock source, it is equally possible to select MCLK2 as the clock source. Similarly, in cases where FLL1 is illustrated, it is equally possible to select FLL2 or FLL3.

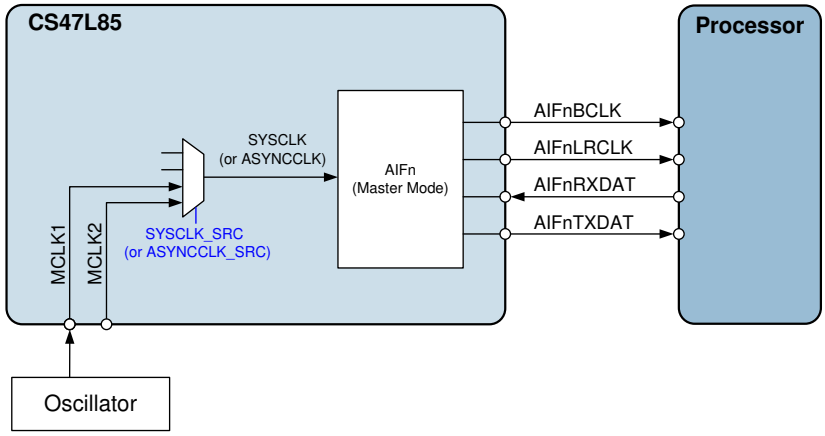


Figure 99 AIF Master Mode, using MCLK as Reference

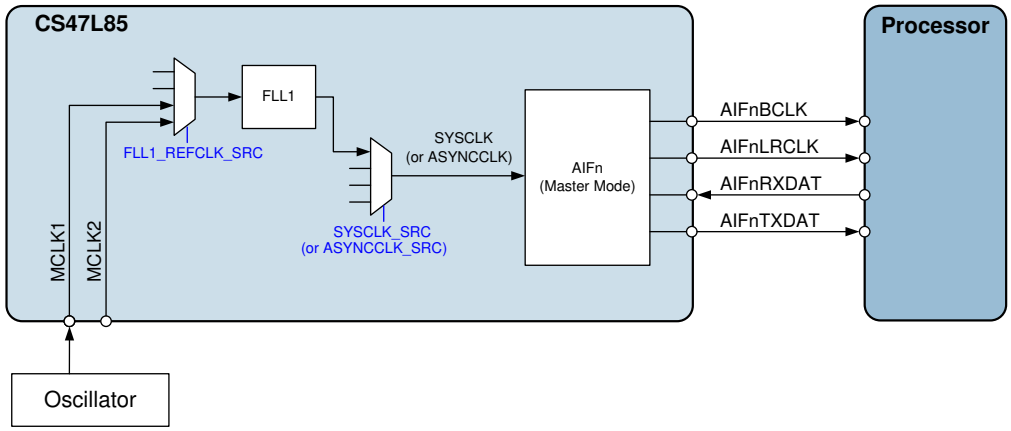


Figure 100 AIF Master Mode, using MCLK and FLL as Reference

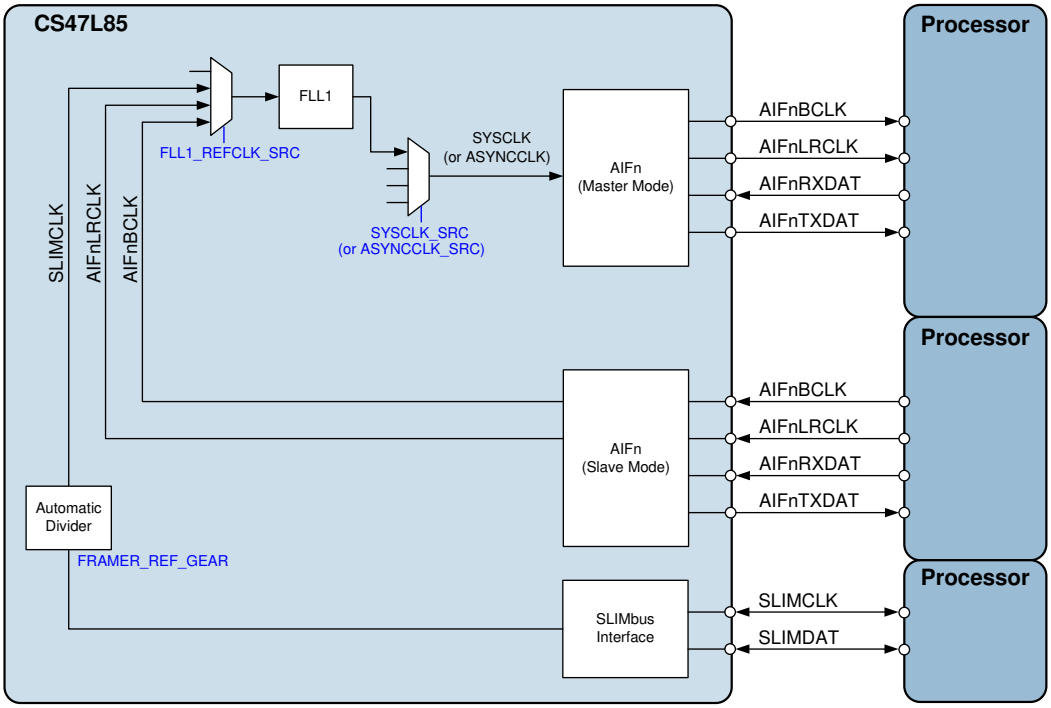


Figure 101 AIF Master Mode, using another Interface as Reference

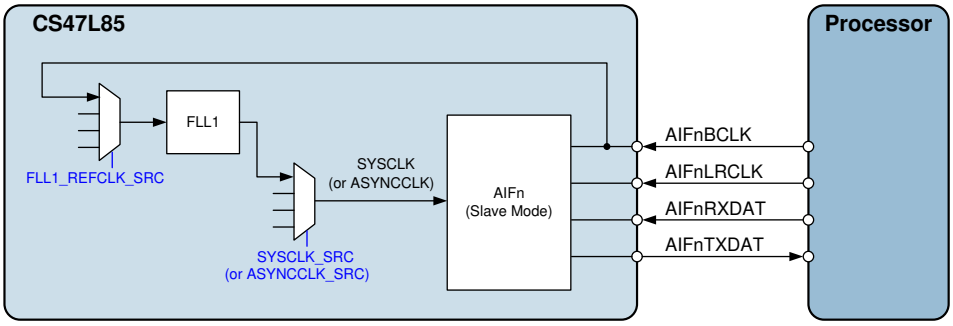


Figure 102 AIF Slave Mode, using BCLK and FLL as Reference

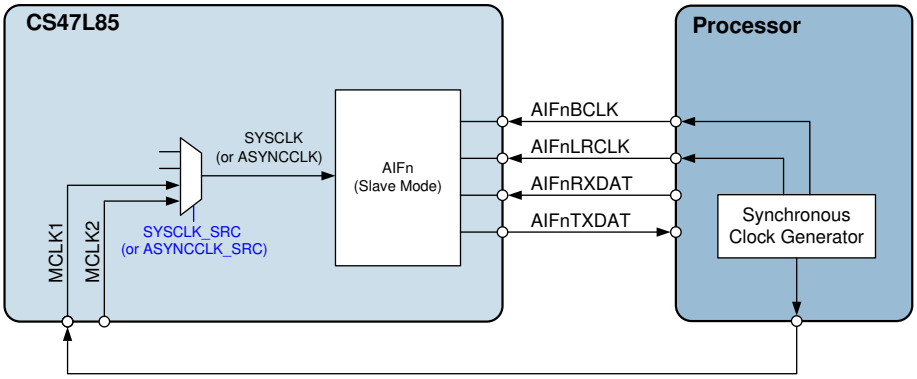


Figure 103 AIF Slave Mode, using MCLK as Reference

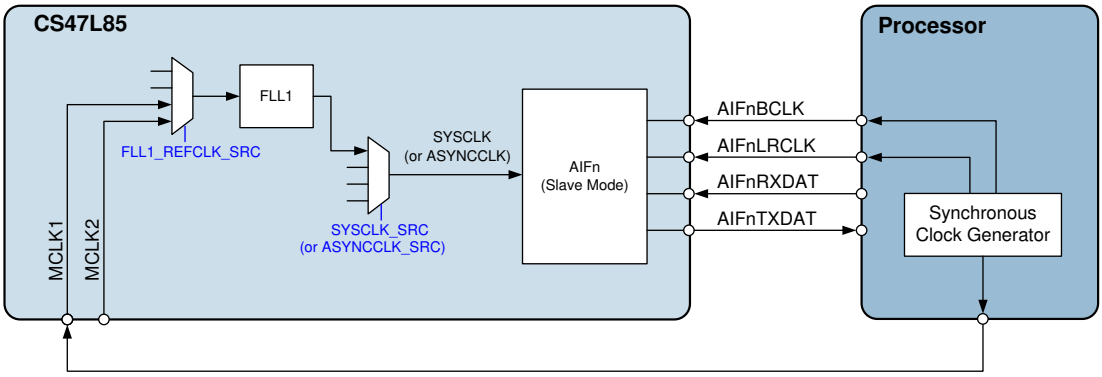


Figure 104 AIF Slave Mode, using MCLK and FLL as Reference

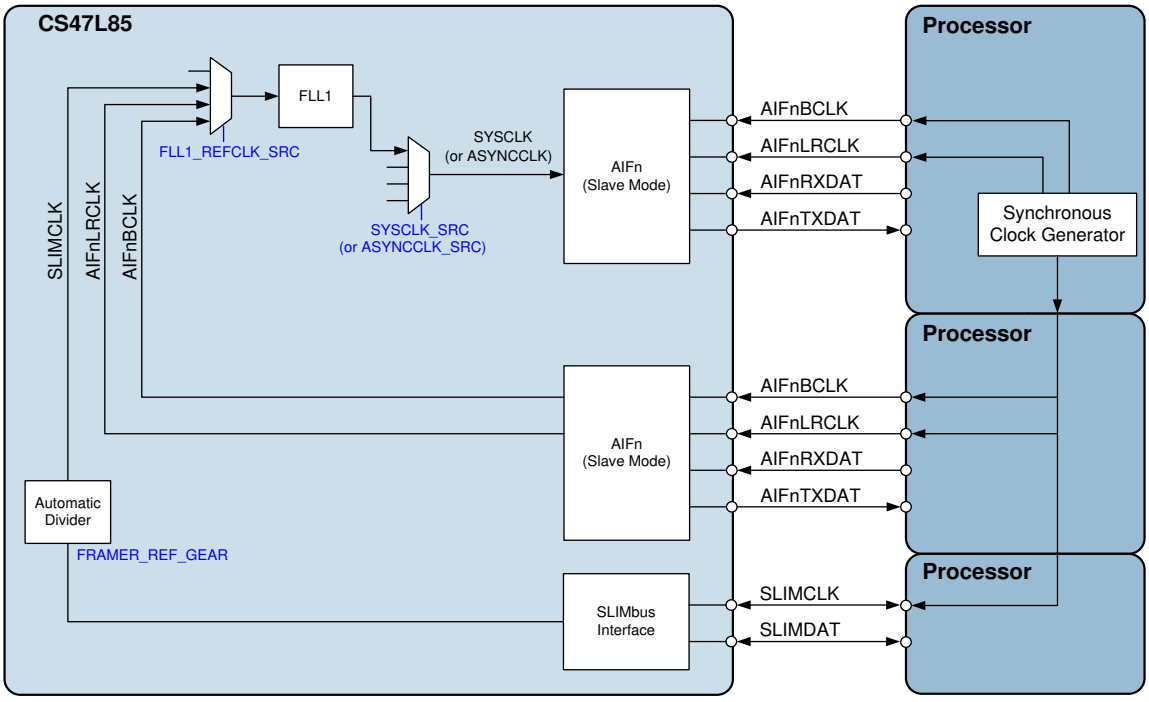


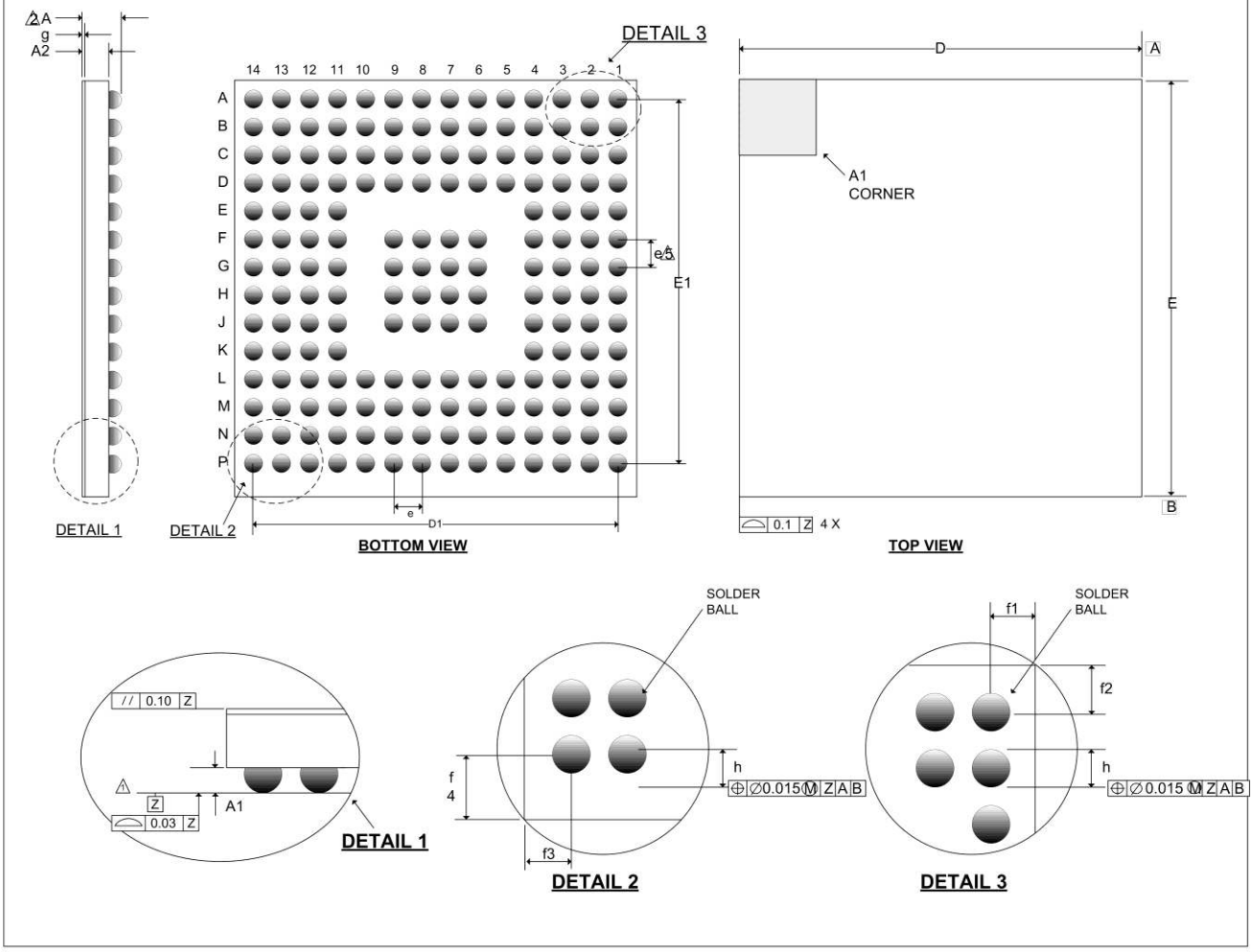
Figure 105 AIF Slave Mode, using another Interface as Reference

PCB LAYOUT CONSIDERATIONS

Poor PCB layout will degrade the performance and be a contributory factor in EMI, ground bounce and resistive voltage losses. All external components should be placed as close to the CS47L85 device as possible, with current loop areas kept as small as possible.

PACKAGE DIMENSIONS

A: 176 BALL W-CS PACKAGE 5.855 x 5.955 x 0.574 mm BODY, 0.40 mm BALL PITCH DM130.A



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.530	0.574	0.629	
A1	0.165	0.194	0.223	
A2	0.370	0.380	0.396	
D	5.800	5.855	5.880	
D1		5.20 BSC		
E	5.900	5.955	5.980	
E1		5.20 BSC		
e		0.40 BSC		5
f1		0.3275 BSC		
f2		0.2775 BSC		
f3		0.3275 BSC		
f4		0.4775 BSC		
g		0.022		
h	0.218	0.268	0.318	

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1'.
3. A1 CORNER IS IDENTIFIED BY INL/LASER MARK ON TOP PACKAGE.
4. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
5. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
7. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.

Revision History

Table 141 Revision History

Revision	Changes
1.0 SEP '14	• Initial version
1.1 DEC '14	• Thermal Characteristics added • Correction to PWMn_LVL description • Updates to DSP Clocking registers and controls • Added description of DSP DMA functions • Changes to Master Interface registers and operation • Updates to Timer Clocking registers and controls • Updates to SLIMbus register access description • Output Path Hi-Fi filter controls added • Recommended 500k JACKDET2 resistor connection
1.1 JAN '15	• SPI clock frequency spec updated • Recommend TRST is tied to DGND if JTAG function is not used • Noted SYSCLK_ENA and ASYNC_CLK_ENA must be set to 0 before the respective clock source is stopped • Noted 32kHz clock requirement for GPIO input de-bounce • Clocking required for FLL Interrupt • DSP_CLK_FREQ_RANGE defined (replaces DSP_CLK_FREQ) • CIF1MISO pull-down described • Signal Timing Requirements updated • DSP memory reset behaviour corrected • Electrical Characteristics updated • GPIO functions updated (added/removed) • Sleep Mode requirements (external DCVDD) added
2.0 MAY '15	• Converted to Cirrus document template • Sleep Mode requirements (external DCVDD) deleted • DBVDD operating range updated • Signal passband noted for each DMIC clock frequency • Clarification of voltage domains for DMIC operation • Register Map listing is referenced to a separate document • CPVDD2 absolute maximum rating updated • Noted DCVDD/FLLVDD must be tied together • Digital Mixer control requirements updated
4.0 MAY '15	• Updated to 'Production Data' status
4.1 JUL '15	• Clarification of SLIMbus requirements for different Transport Protocol (TP) options • FLL1_DIV6 system clocking option added • Correction to FLL Spread Spectrum control register (FLLn_SS_SEL) description • Noted constraints for using WSEQ_START to trigger the Control Sequencer • System clocking control requirements updated • Added comments describing bus-keeper start-up condition, and digital I/O in Sleep Mode
4.2 DEC '16	• Series resistor recommended on FLLVDD connection • Clarification of PDM input/output digital signal levels • Typical performance data added • DSPn_DMA_WORD_SEL description added • Master interface section updated to include clocking requirements • Output path noise gate threshold (NGATE_THR) updated • Headphone detect (HPDET) calculation and measurement time updated • FLL configuration and example settings updated

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.