



PJL9452A

100V N-Channel Enhancement Mode MOSFET

Voltage	100 V	Current	3.3 A
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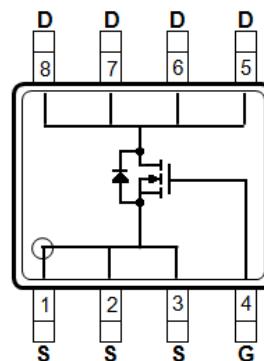
Features

- R_{DS(ON)}, V_{GS}@10V, I_D@3.3A<115mΩ
- R_{DS(ON)}, V_{GS}@4.5V, I_D@1.5A<120mΩ
- Advanced Trench Process Technology
- High density cell design for ultra low on-resistance
- Lead free in compliance with EU RoHS 2011/65/EU directive.
- Green molding compound as per IEC61249 Std.
(Halogen Free)

Mechanical Data

- Case: SOP-8 package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Marking: L9452A

SOP-8



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _{GS}	<u>±20</u>	V
Continuous Drain Current	I _D	3.3	A
		2.6	
Pulsed Drain Current ^(Note 1)	I _{DM}	13.2	A
Power Dissipation	P _D	2.5	W
		1.6	
Single Pulse Avalanche Energy ^(Note 5)	E _{AS}	3.2	mJ
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55~150	°C
Typical Thermal resistance - Junction to Ambient, t≤10s ^(Note 5)	R _{θJA}	50	°C/W



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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_D=250\text{\mu A}$	100	-	-	V
Gate Threshold Voltage	$\text{V}_{\text{GS(th)}}$	$\text{V}_{\text{DS}}=\text{V}_{\text{GS}}, \text{I}_D=250\text{\mu A}$	1.0	1.76	2.5	V
Drain-Source On-State Resistance	$\text{R}_{\text{DS(on)}}$	$\text{V}_{\text{GS}}=10\text{V}, \text{I}_D=3.3\text{A}$	-	92	115	$\text{m}\Omega$
		$\text{V}_{\text{GS}}=4.5\text{V}, \text{I}_D=1.5\text{A}$	-	95	120	
Zero Gate Voltage Drain Current	I_{DSS}	$\text{V}_{\text{DS}}=100\text{V}, \text{V}_{\text{GS}}=0\text{V}$	-	-	1.0	\mu A
Gate-Source Leakage Current	I_{GSS}	$\text{V}_{\text{GS}}=\pm 20\text{V}, \text{V}_{\text{DS}}=0\text{V}$	-	-	± 100	nA
Dynamic (Note 6)						
Total Gate Charge	Q_g	$\text{V}_{\text{DS}}=50\text{V}, \text{I}_D=2\text{A}$, $\text{V}_{\text{GS}}=10\text{V}$ (Note 1,2)	-	20	-	nC
Gate-Source Charge	Q_{gs}		-	3.2	-	
Gate-Drain Charge	Q_{gd}		-	3.6	-	
Input Capacitance	C_{iss}	$\text{V}_{\text{DS}}=25\text{V}, \text{V}_{\text{GS}}=0\text{V}$, $f=1.0\text{MHz}$	-	1413	-	pF
Output Capacitance	C_{oss}		-	60	-	
Reverse Transfer Capacitance	Crss		-	34	-	
Turn-On Delay Time	$\text{td}_{(\text{on})}$	$\text{V}_{\text{DD}}=50\text{V}, \text{I}_D=1\text{A}$, $\text{V}_{\text{GS}}=10\text{V}$, $R_{\text{G}}=3.3\Omega$ (Note 1,2)	-	18	-	ns
Turn-On Rise Time	tr		-	4.3	-	
Turn-Off Delay Time	$\text{td}_{(\text{off})}$		-	41	-	
Turn-Off Fall Time	tf		-	4.2	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_s	---	-	-	3.3	A
Diode Forward Voltage	V_{SD}	$\text{I}_s=1.0\text{A}, \text{V}_{\text{GS}}=0\text{V}$	-	0.73	1.0	V

NOTES :

1. Pulse width<300us, Duty cycle<2%
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature $T_J(\text{MAX})=150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$.
4. The maximum current rating is package limited.
5. The test condition is $L=0.1\text{mH}$, $\text{I}_{\text{AS}}=8\text{A}$, $\text{V}_{\text{DD}}=25\text{V}$, $\text{V}_{\text{GS}}=10\text{V}$
6. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
7. Guaranteed by design, not subject to production testing.



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TYPICAL CHARACTERISTIC CURVES

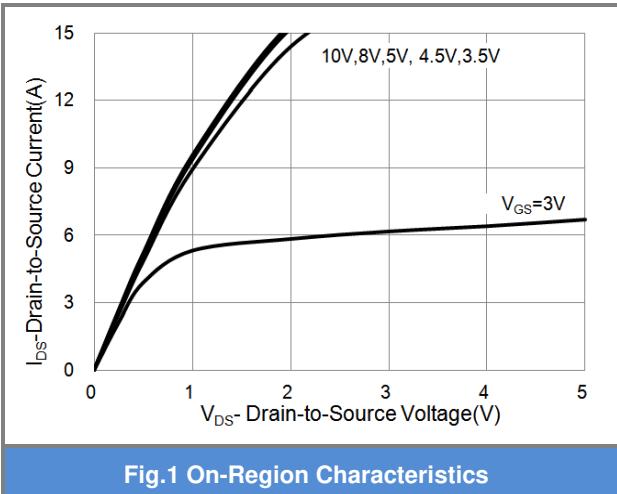


Fig.1 On-Region Characteristics

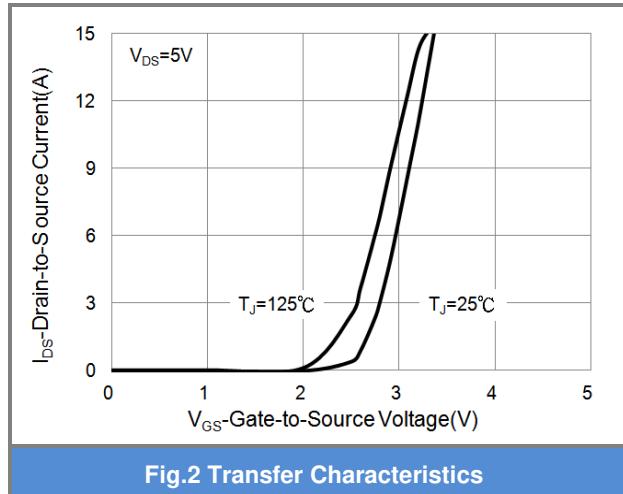


Fig.2 Transfer Characteristics

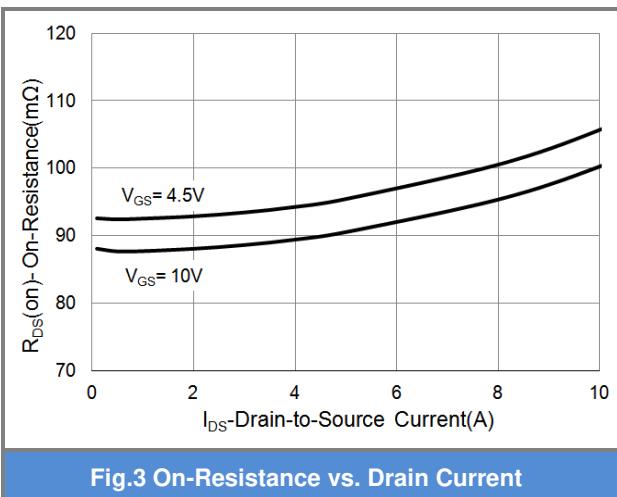


Fig.3 On-Resistance vs. Drain Current

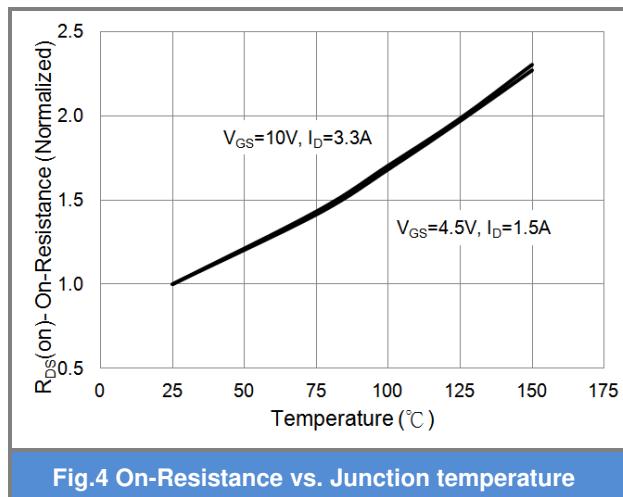


Fig.4 On-Resistance vs. Junction temperature

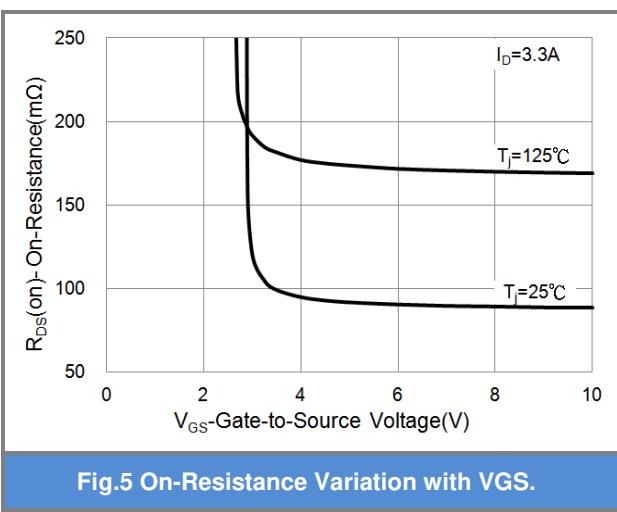


Fig.5 On-Resistance Variation with VGS.

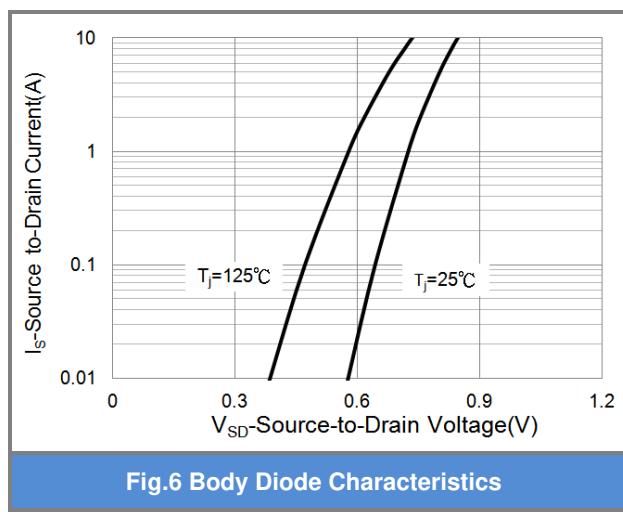
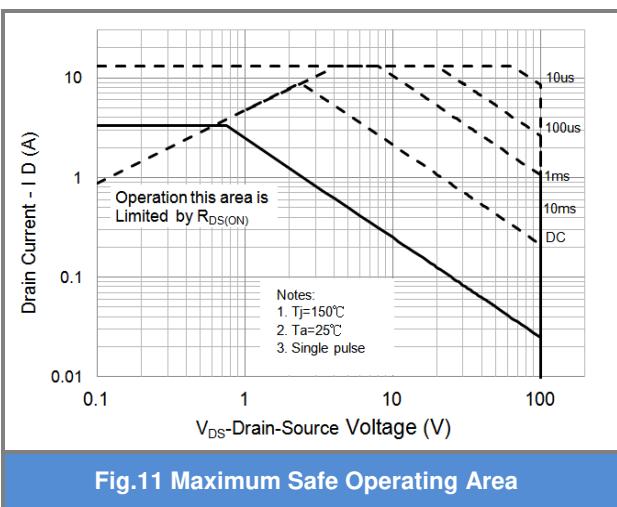
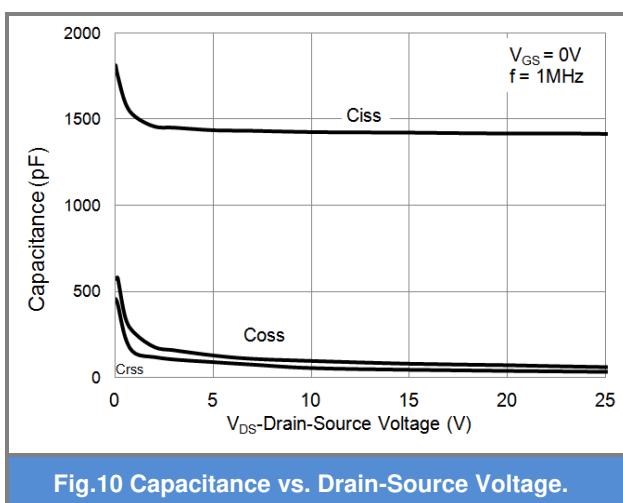
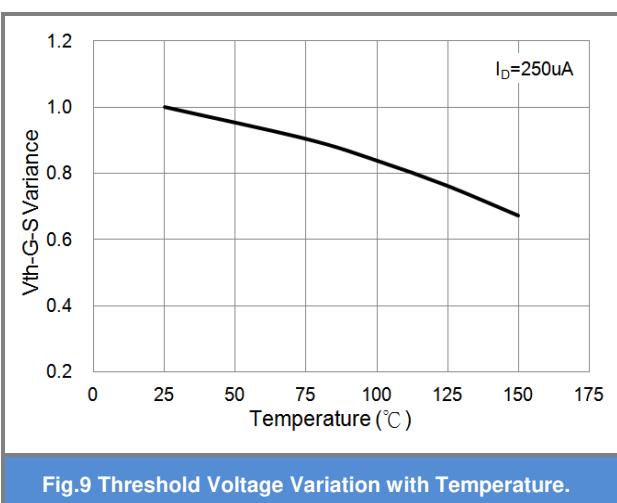
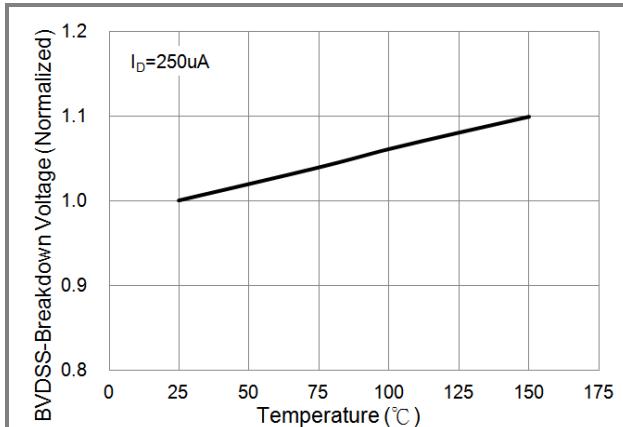
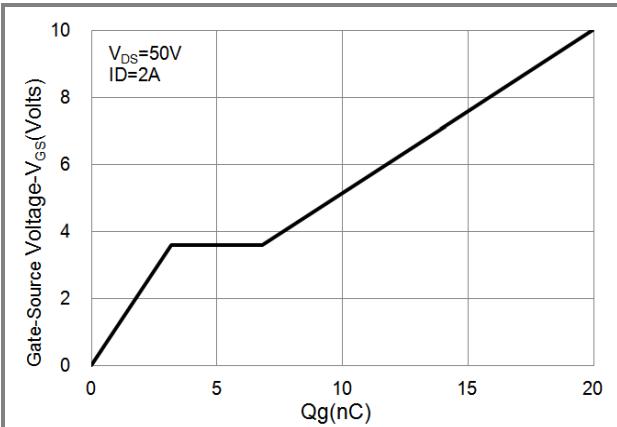


Fig.6 Body Diode Characteristics



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TYPICAL CHARACTERISTIC CURVES





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TYPICAL CHARACTERISTIC CURVES

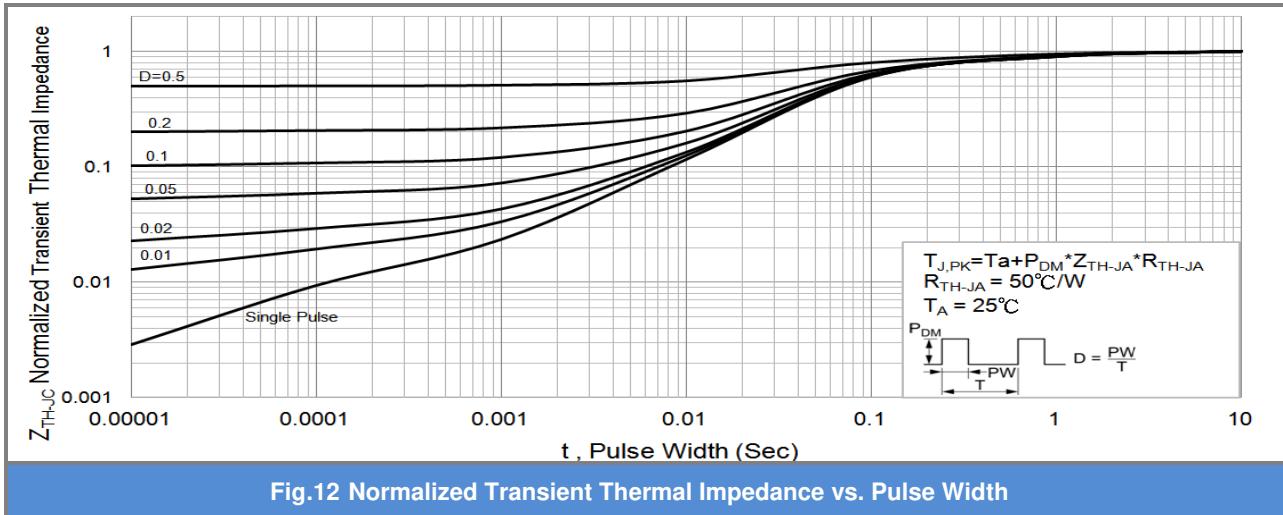


Fig.12 Normalized Transient Thermal Impedance vs. Pulse Width

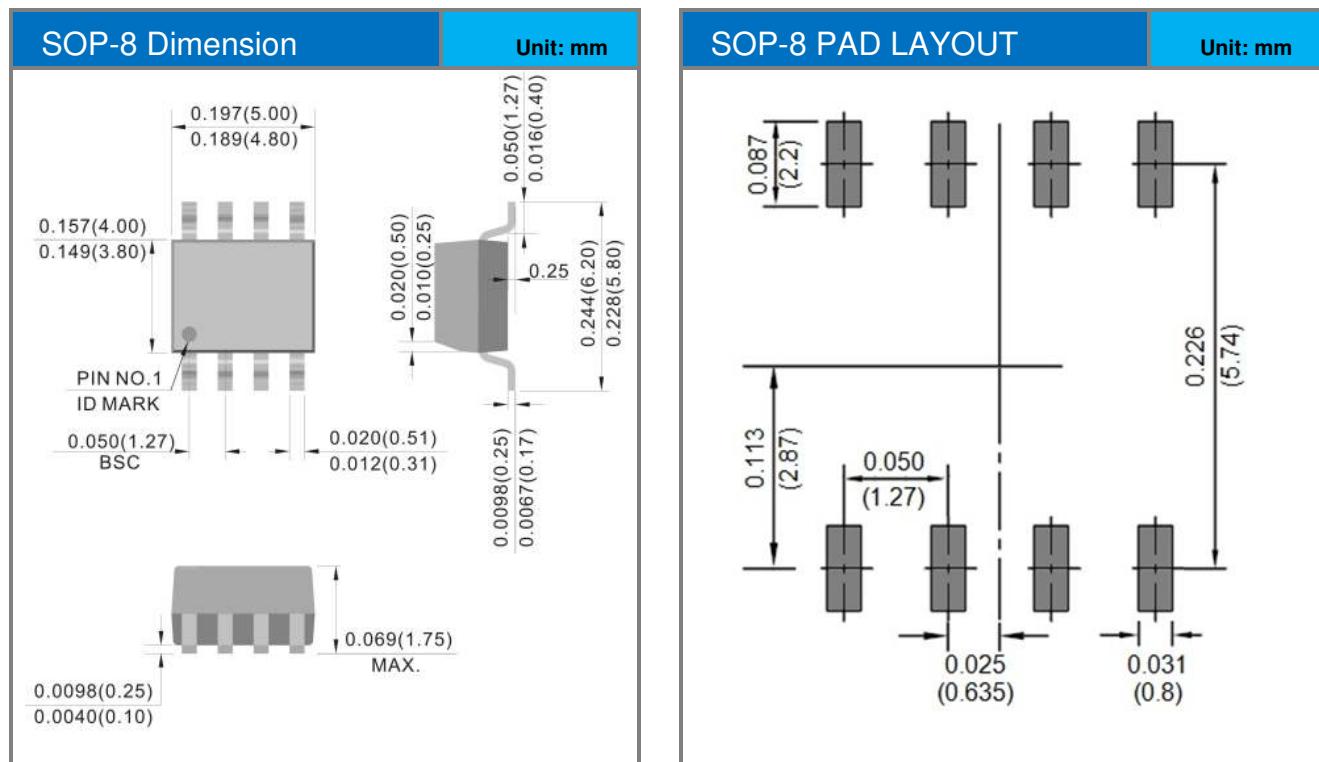


PJL9452A

PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing type	Marking	Version
PJL9452A_R2_00001	SOP-8	2.5K pcs / 13" reel	L9452A	Halogen free

Packaging Information & Mounting Pad Layout





PJL9452A

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