HARRIS SEMICONDUCTOR

HSP43220

December 1996

Decimating Digital Filter

Features

- Single Chip Narrow Band Filter with up to 96dB Attenuation
- DC to 33MHz Clock Rate
- 16-Bit 2's Complement Input
- 20-Bit Coefficients in FIR
- 24-Bit Extended Precision Output
- Programmable Decimation up to a Maximum of 16,384
- Standard 16-Bit Microprocessor Interface
- Filter Design Software Available DECI•MATE™
- Up to 512 Taps

Applications

- Very Narrow Band Filters
- Zoom Spectral Analysis
- Channelized Receivers
- Large Sample Rate Converter

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HSP43220VC-15	0 to 70	100 Ld MQFP	Q100.14x20
HSP43220VC-25	0 to 70	100 Ld MQFP	Q100.14x20
HSP43220VC-33	0 to 70	100 Ld MQFP	Q100.14x20
HSP43220JC-15	0 to 70	84 Ld PLCC	N84.1.15
HSP43220JC-25	0 to 0	84 Ld PLCC	N84.1.15
HSP43220JC-33	0 to 70	84 Ld PLCC	N84.1.15
HSP43220GC-15	0 to 70	84 Ld CPGA	G84.A
HSP43220GC-25	0 to 70	84 Ld CPGA	G84.A
HSP43220GC-33	0 to 70	84 Ld CPGA	G84.A
HSP43220GI-15	-40 to 85	84 Ld CPGA	G84.A
HSP43220GI-25	-40 to 85	84 Ld CPGA	G84.A
HSP43220GI-33	-40 to 85	84 Ld CPGA	G84.A
Deci•Mate™ Software Development Tool (This software tool may be downloaded from our Internet site: http://www.semi.harris.com)			

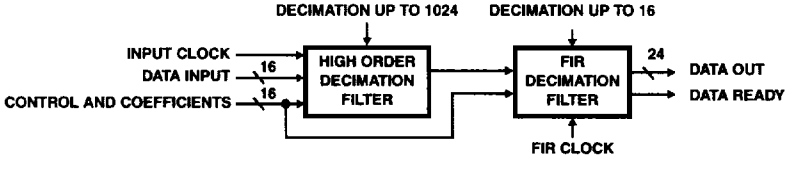
Description

The HSP43220 Decimating Digital Filter is a linear phase low pass decimation filter which is optimized for filtering narrow band signals in a broad spectrum of a signal processing applications. The HSP43220 offers a single chip solution to signal processing applications which have historically required several boards of ICs. This reduction in component count results in faster development times as well as reduction of hardware costs.

The HSP43220 is implemented as a two stage filter structure. As seen in the block diagram, the first stage is a high order decimation filter (HDF) which utilizes an efficient sample rate reduction technique to obtain decimation up to 1024 through a coarse low-pass filtering process. The HDF provides up to 96dB aliasing rejection in the signal pass band. The second stage consists of a finite impulse response (FIR) decimation filter structured as a transversal FIR filter with up to 512 symmetric taps which can implement filters with sharp transition regions. The FIR can perform further decimation by up to 16 if required while preserving the 96dB aliasing attenuation obtained by the HDF. The combined total decimation capability is 16,384.

The HSP43220 accepts 16-bit parallel data in 2's complement format at sampling rates up to 33 MSPS. It provides a 16-bit microprocessor compatible interface to simplify the task of programming and three-state outputs to allow the connection of several ICs to a common bus. The HSP43220 also provides the capability to bypass either the HDF or the FIR for additional flexibility.

Block Diagram



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CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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