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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

Character Display Module

Part Number

C204ALBVKS16WN55RWS

Overview

UWVD: 20x4(98x60), UWVD, Black background, White Edge lit, Bottom view, Wide temp, Transmissive (negative), 5V LCD, 5V LED, Controller=RW1063, RoHS Compliant

1. Features

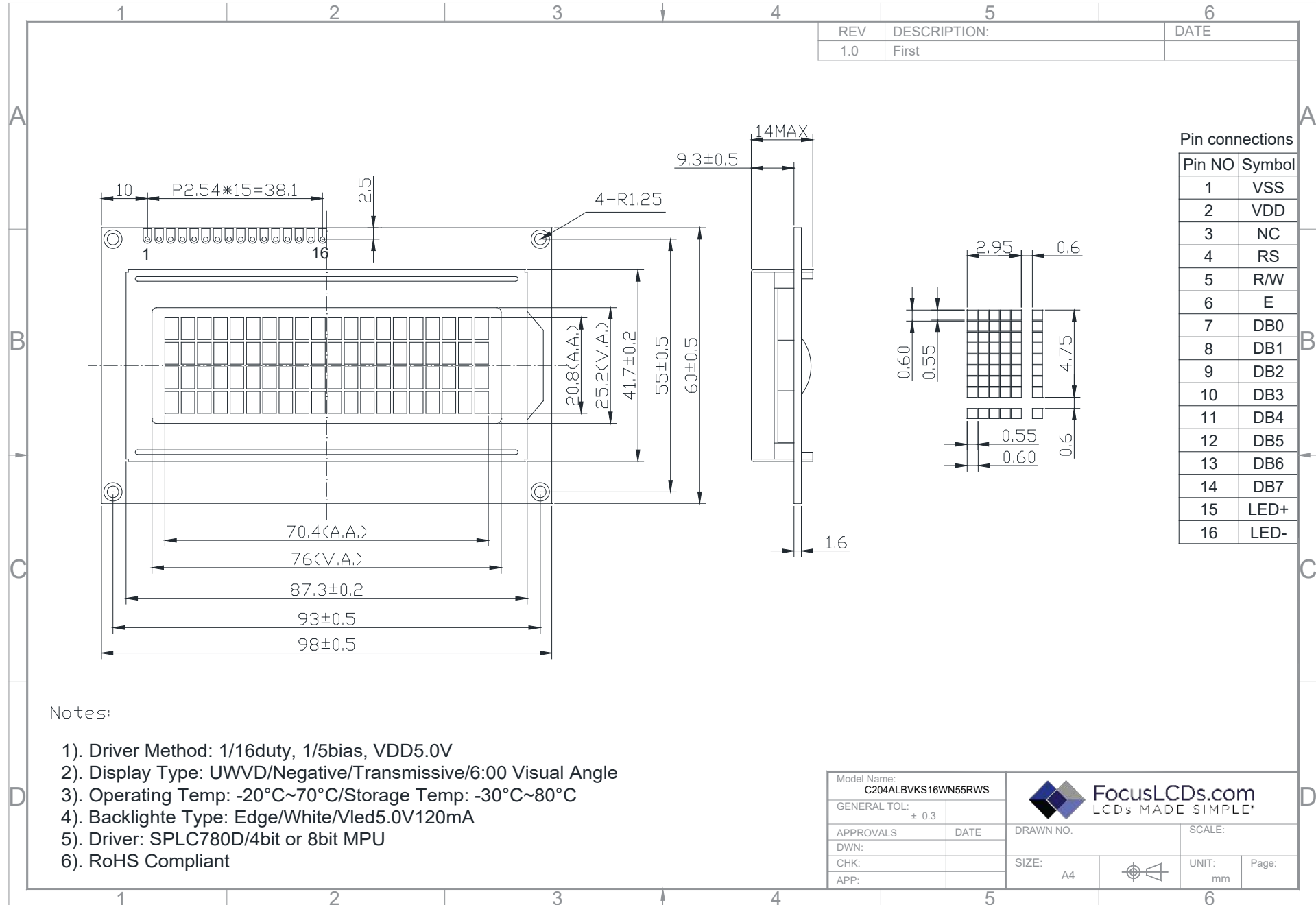
1. 5x7 dots with cursor
2. 16characters *2lines display
3. 4-bit or 8-bit MPU interfaces
4. Built-in controller (SPLC780D or equivalent)
5. Display Mode & Backlight Variations
6. ROHS Compliant

LCD type	<input type="checkbox"/> TN		<input checked="" type="checkbox"/> UWWD	
	<input type="checkbox"/> FSTN		<input type="checkbox"/> FSTN Negative	
	<input type="checkbox"/> STN Yellow Green	<input type="checkbox"/> STN Gray		STN Blue Negative
View direction	<input checked="" type="checkbox"/> 6 O'clock		<input type="checkbox"/> 12 O'clock	
Rear Polarizer	<input type="checkbox"/> Reflective		<input type="checkbox"/> Transflective	<input checked="" type="checkbox"/> Transmissive
Backlight Type	<input type="checkbox"/> LED Array		<input type="checkbox"/> EL	
	<input checked="" type="checkbox"/> LED Edge		<input type="checkbox"/> CCFL	
Backlight Color	<input checked="" type="checkbox"/> White		<input type="checkbox"/> Internal Power	
	<input type="checkbox"/> Blue	<input type="checkbox"/> Amber		<input type="checkbox"/> Yellow-Green
Temperature Range	<input type="checkbox"/> Normal		<input checked="" type="checkbox"/> Wide	<input type="checkbox"/> Super Wide
DC to DC circuit	<input type="checkbox"/> Build-in		<input checked="" type="checkbox"/> Not Build-in	
Touch screen	<input type="checkbox"/> With		<input checked="" type="checkbox"/> Without	
Font type	<input checked="" type="checkbox"/> English-Japanese		<input type="checkbox"/> English-Europen	<input type="checkbox"/> English-Russian
			<input type="checkbox"/> Other	

2. MECHANICAL SPECIFICATIONS

Module size	98.0mm(L)*60.0mm(W)* Max14(H)mm
Viewing area	76mm(L)*25.2mm(W)
Character size	2.95mm(L)*4.75mm(W)
Character pitch	3.55mm(L)*5.35mm(W)
Weight	Approx.

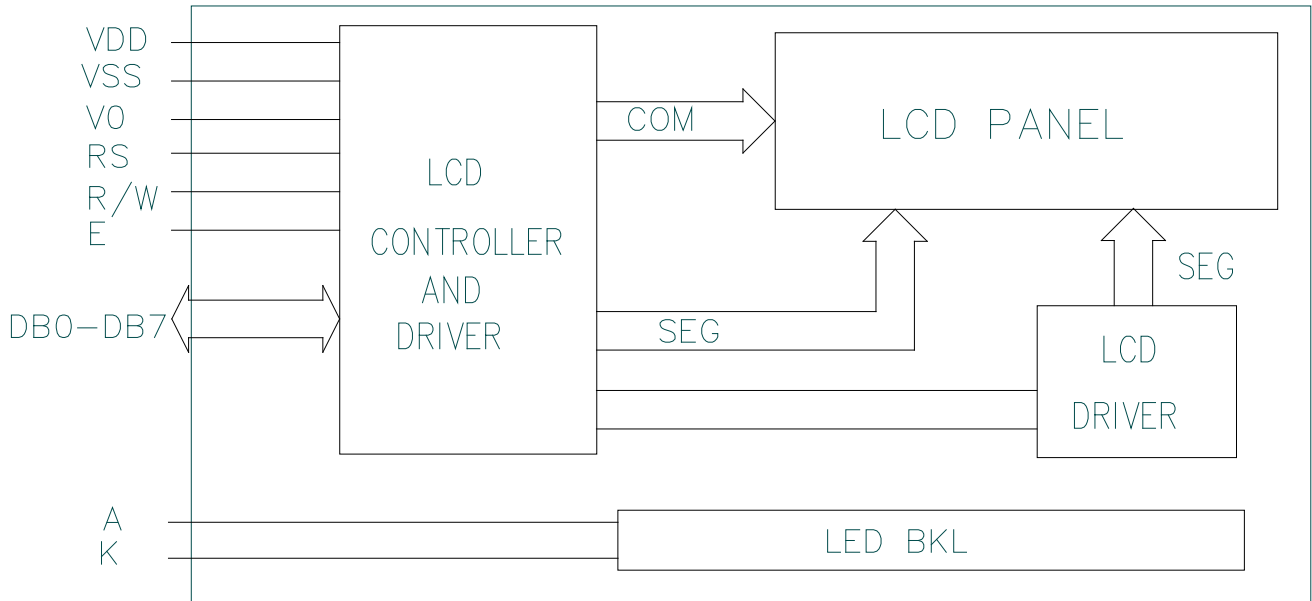
3. Outline dimension



4. Absolute maximum ratings

Item	Symbol	Standard			Unit
Power voltage	$V_{DD}-V_{SS}$	0	-	7.0	V
Input voltage	V_{IN}	VSS	-	VDD	
Operating temperature range	V_{OP}	-20	-	70	°C
Storage temperature range	V_{ST}	-30	-	80	

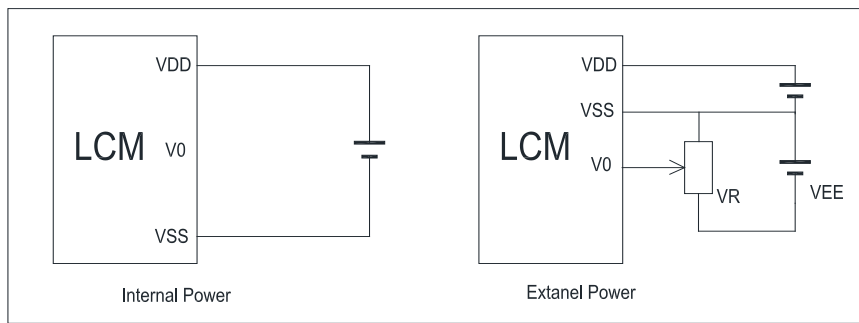
5. Block diagram



6. Interface pin description

Pin no.	Symbol	External connection	Function
1	Vss	Power supply	Signal ground for LCM
2	V _{DD}		Power supply for logic for LCM
3	NC		Don't connect
4	RS	MPU	Register select signal
5	R/W	MPU	Read/write select signal
6	E	MPU	Operation (data read/write) enable signal
7~10	DB0~DB3	MPU	Four low order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCM. These four are not used during 4-bit operation.
11~14	DB4~DB7	MPU	Four high order bi-directional three-state data bus lines. Used for data transfer between the MPU
15	LED+	LED BKL power supply	Power supply for BKL
16	LED-		Power supply for BKL

7. Contrast adjust



$V_{DD}-V_0$: LCD Driving voltage
 VR: 10k~20k

8. Optical characteristics

UWVD type display module ($T_a=25^\circ\text{C}$, $V_{DD}=5.0\text{V}$)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle	Horizontal	Θ_{x+}	$T_a=25^\circ\text{C}$	60	70	-	deg
		Θ_{x-}		60	70	-	
	Vertical	Φ_{y+}		40	50	-	
		Φ_{y-}		60	70	-	
Contrast ratio		Cr		2	5	-	-
Response time	rise	T_r		-	150	250	ms
Response time	fall	T_f		-	200	300	

9. Electrical characteristics

DC characteristics

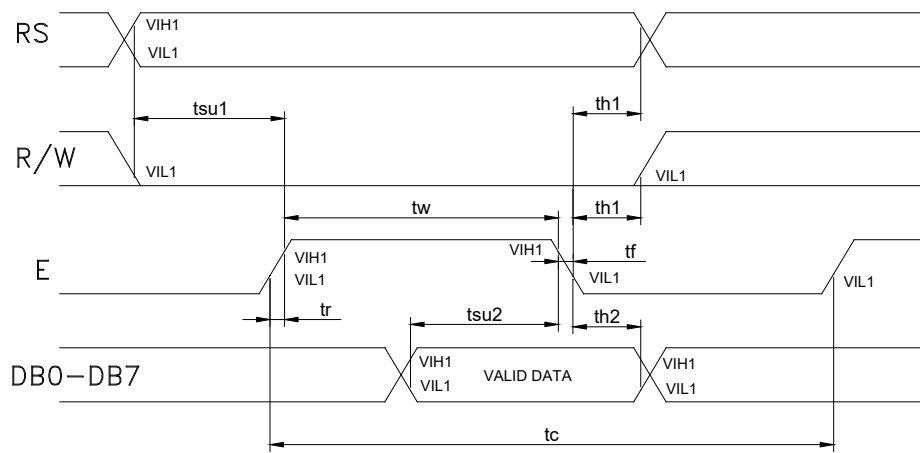
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage for LCD	$V_{DD}-V_0$	$T_a=25^\circ\text{C}$	6.8	7.0	7.2	V
Input voltage	V_{DD}		4.7	5.0	5.3	
Supply current	I_{DD}	$T_a=25^\circ\text{C}$, $V_{DD}=5.0\text{V}$	-	1.5	2.0	mA
Input leakage current	I_{LKG}		-	-	1.0	μA
“H” level input voltage	V_{IH}		2.2	-	V_{DD}	V
“L” level input voltage	V_{IL}	Twice initial value or less	0	-	0.6	
“H” level output voltage	V_{OH}	LOH=-0.25mA	2.4	-	-	
“L” level output voltage	V_{OL}	LOH=1.6mA	-	-	0.4	
Backlight supply voltage	V_F		-	5.0	5.3	
Backlight supply current	I_{LED}	$V_F=5.0\text{V}$ R=16.5 OHM	-	100	120	

10. Timing Characteristics

Write cycle (Ta=25°C, VDD=5.0V)

Parameter	Symbol	Test pin	Min.	Typ.	Max.	Unit
Enable cycle time	t_c	E	500	-	-	ns
Enable pulse width	t_w		300	-	-	
Enable rise/fall time	t_r, t_f		-	-	25	
RS; R/W setup time	t_{su1}	RS; R/W RS; R/W	100	-	-	
RS; R/W address hold time	t_{h1}		10	-	-	
Read data output delay	t_{su2}	DB0~DB7	60	-	-	
Read data hold time	t_{h2}		10	-	-	

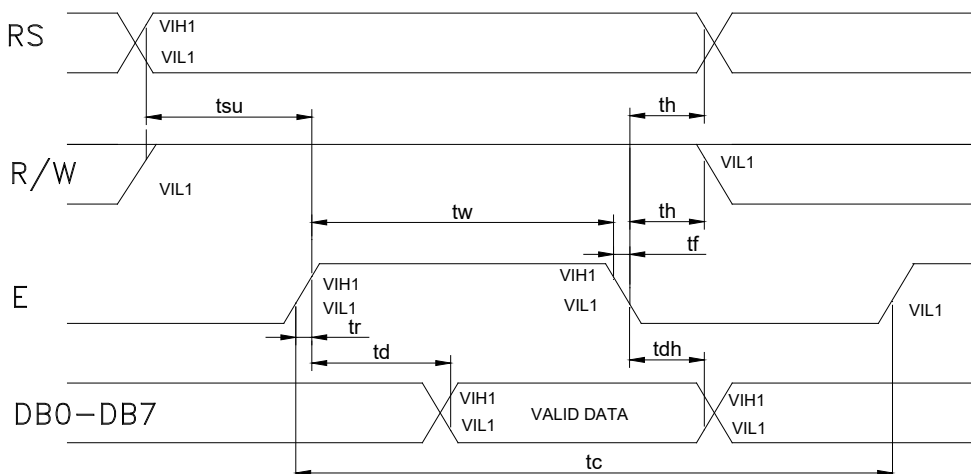
Write mode timing diagram



Read cycle (Ta=25°C, VDD=5.0V)

Parameter	Symbol	Test pin	Min.	Typ.	Max.	Unit
Enable cycle time	t_c	E	500	-	-	ns
Enable pulse width	t_w		300	-	-	
Enable rise/fall time	t_r, t_f		-	-	25	
RS; R/W setup time	t_{su}	RS; R/W RS; R/W	100	-	-	
RS; R/W address hold time	t_h		10	-	-	
Read data output delay	t_d	DB0~DB7	60	-	90	
Read data hold time	t_{dh}		20	-	-	

Read mode timing diagram



11. Instruction description

11.1 Outline

To overcome the speed difference between the internal clock of SPLC780D and the MPU clock, SPLC780D performs internal operations by storing control formations to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus (Refer to Table7).

Instructions can be divided largely into four groups:

- 1) SPLC780D function set instructions (set display methods, set data length, etc.)
- 2) Address set instructions to internal RAM
- 3) Data transfer instructions with internal RAM
- 4) Others

The address of the internal RAM is automatically increased or decreased by 1.

Note: during internal operation, busy flag (DB7) is read "High".

Busy flag check must be preceded by the next instruction.

11.2 Instruction Table

Instruction	Instruction code										Description	Execution time (fosc=270 KHZ)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRA and set DDRAM address to "00H" from AC	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" From AC and return cursor to Its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction And blinking of entire display	39us
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and Blinking of cursor (B) on/off Control bit.	
Cursor or Display shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display Shift control bit, and the Direction, without changing of DDRAM data.	39us
Function set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-Bit/4-bit), numbers of display Line (N: =2-line/1-line) and, Display font type (F: 5x11/5x8)	39us
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address Counter.	39us
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address Counter.	39us
Read busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal Operation or not can be known By reading BF. The contents of Address counter can also be read.	0us
Write data to Address	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43us
Read data From RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43us

NOTE:

When an MPU program with checking the busy flag (DB7) is made, it must be necessary 1/2fosc is necessary for executing the next instruction by the falling edge of the "E" signal after the busy flag (DB7) goes to "Low".

11.3 Contents

1) Clear display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter).

Return cursor to the original status, namely, bring the cursor to the left edge on the first line of the display. Make the entry mode increment (I/D="High").

2) Return home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

Return home is cursor return home instruction.

Set DDRAM address to "00H" into the address counter.

Return cursor to its original site and return display to its original status, if shifted.

Contents of DDRAM does not change.

3) Entry mode set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.

I/D: increment / decrement of DDRAM address (cursor or blink)

When I/D="high", cursor/blink moves to right and DDRAM address is increased by 1.

When I/D="Low", cursor/blink moves to left and DDRAM address is increased by 1.

*CGRAM operates the same way as DDRAM, when reading from or writing to CGRAM.

SH: shift of entire display

When DDRAM read (CGRAM read/write) operation or SH="Low", shifting of entire display is not performed. If SH="High" and DDRAM write operation, shift of entire display is performed according to I/D value. (I/D="high". shift left, I/D="Low". Shift right).

4) Display ON/OFF control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF control bit

When D="High", entire display is turned on.

When D="Low", display is turned off, but display data remains in DDRAM.

C: cursor ON/OFF control bit

When D="High", cursor is turned on.

When D="Low", cursor is disappeared in current display, but I/D register preserves its data.

B: Cursor blink ON/OFF control bit

When B="High", cursor blink is on, which performs alternately between all the "High" data and display characters at the cursor position.

When B="Low", blink is off.

5) Cursor or display shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shifting of right/left cursor position or display without writing or reading of display data.

This instruction is used to correct or search display data.

During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line.

Note that display shift is performed simultaneously in all the lines.

When display data is shifted repeatedly, each line is shifted individually.

When display shift is performed, the contents of the address counter are not changed.

Shift patterns according to S/C and R/L bits

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

6) Function set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

DL: Interface data length control bit

When DL="High", it means 8-bit bus mode with MPU.

When DL="Low", it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.

When 4-bit bus mode, it needs to transfer 4-bit data twice.

N: Display line number control bit

When N="Low", 1-line display mode is set.

When N="High", 2-line display mode is set.

F: Display line number control bit

When F="Low", 5x8 dots format display mode is set.

When F="High", 5x11 dots format display mode.

7) Set CGRAM address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.

The instruction makes CGRAM data available from MPU.

8) Set DDRAM address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU.

When 1-line display mode (N=LOW), DDRAM address is from "00H" to "4FH". In 2-line display mode (N=High), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

9) Read busy flag & address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether SPLC780D is in internal operation or not.

If the resultant BF is "High", internal operation is in progress and should wait BF is to be LOW, which by then the next instruction can be performed. In this instruction you can also read the value of the address counter.

10) Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction (DDRAM address set, CGRAM address set).

RAM set instruction can also determine the AC direction to RAM.

After write operation. The address is automatically increased/decreased by 1, according to the entry mode.

11) Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, the data that has been read first is invalid, as the direction of AC is not yet determined. If RAM data is read several times without RAM address instructions set before, read operation, the correct RAM data can be obtained from the second. But the first data would be incorrect, as there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction, it also transfers RAM data to output data register.

After read operation, address counter is automatically increased/decreased by 1 according to the entry mode.

After CGRAM read operation, display shift may not be executed correctly.

NOTE: In case of RAM write operation, AC is increased/decreased by 1 as in read operation.

At this time, AC indicates next address position, but only the previous data can be read by the read instruction.

12. Display character address code:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

13. Standard character pattern

Lower 4 Bits	Upper 4 Bits																			
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111				
xxxx0000	CG RAM (1)			0	a	P	`	P				-	夕	ミ	α	P				
xxxx0001	(2)		!	1	A	Q	a	q			。	ア	チ	△	ä	q				
xxxx0010	(3)		"	2	B	R	b	r			「	イ	ツ	×	ß	θ				
xxxx0011	(4)		#	3	C	S	c	s			」	ウ	テ	モ	ε	∞				
xxxx0100	(5)		\$	4	D	T	d	t			、	エ	ト	ト	μ	Ω				
xxxx0101	(6)		%	5	E	U	e	u			・	オ	ナ	1	€	Ü				
xxxx0110	(7)		&	6	F	V	f	v			ヲ	カ	ニ	ヨ	ρ	Σ				
xxxx0111	(8)		'	7	G	W	g	w			ア	キ	ヌ	ラ	g	π				
xxxx1000	(1)		(8	H	X	h	x			イ	ク	ネ	リ	♪	⊗				
xxxx1001	(2))	9	I	Y	i	y			ウ	ケ	ル	ル	'	γ				
xxxx1010	(3)		*	:	J	Z	j	z			エ	コ	ハ	レ	j	≠				
xxxx1011	(4)		+	;	K	[k	(オ	サ	ヒ	ロ	*	π				
xxxx1100	(5)		,	<	L	¥	l	l			カ	シ	フ	ワ	φ	π				
xxxx1101	(6)		-	=	M]	m)			ユ	ス	ハ	ン	も	÷				
xxxx1110	(7)		.	>	N	^	n	+			ヨ	セ	ホ	°	ñ					
xxxx1111	(8)		/	?	O	_	o	+			ッ	ソ	マ	°	ö	■				