DS3170DK
DS3/E3 Single-Chip Transceiver Design Kit

www.maxim-ic.com

GENERAL DESCRIPTION

The DS3170DK is a fully integrated design kit for the DS3170 DS3/E3 single-chip transceiver (SCT). This design kit contains all the necessary circuitry to evaluate the DS3170 in all modes of operation. The design kit also includes an on-board microprocessor to run real-time code for further part evaluation.

DESIGN KIT CONTENTS

DS3170DK Board
Download:
- ChipView Software
- DS3170DK.DEF Definition File
- DS3170DK Data Sheet

ORDERING INFORMATION

PART	DESCRIPTION
DS3170DK	Design Kit for the DS3170 DS3/E3 Single-Chip Transceiver

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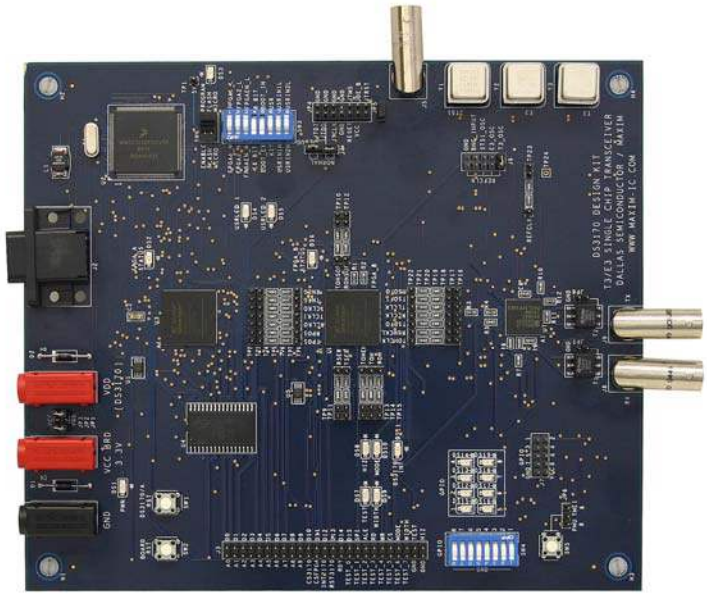
FEATURES

- Expedites New Designs by Eliminating First-Pass Prototyping
- Demonstrates Key Functions of the DS3170 DS3/E3 Single-Chip Transceiver (SCT)
- Includes DS3170 Single-Chip Transceiver (SCT), Transformers, 75Ω BNC, and Termination Passives
- Interfaces with Any PC with an RS-232 Serial Interface
- High Level Windows®-Based Software Provides Visual Access to All Registers
- Software Controlled (Register) Mapped Configuration Switches Facilitate Real-Time Clock and Signal Routing
- Precision Test Points for All Clocks and Signals
- On-Board DS3 and E3 Crystal Oscillators for Stable Clock Generation
- Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDS



REV: 091205

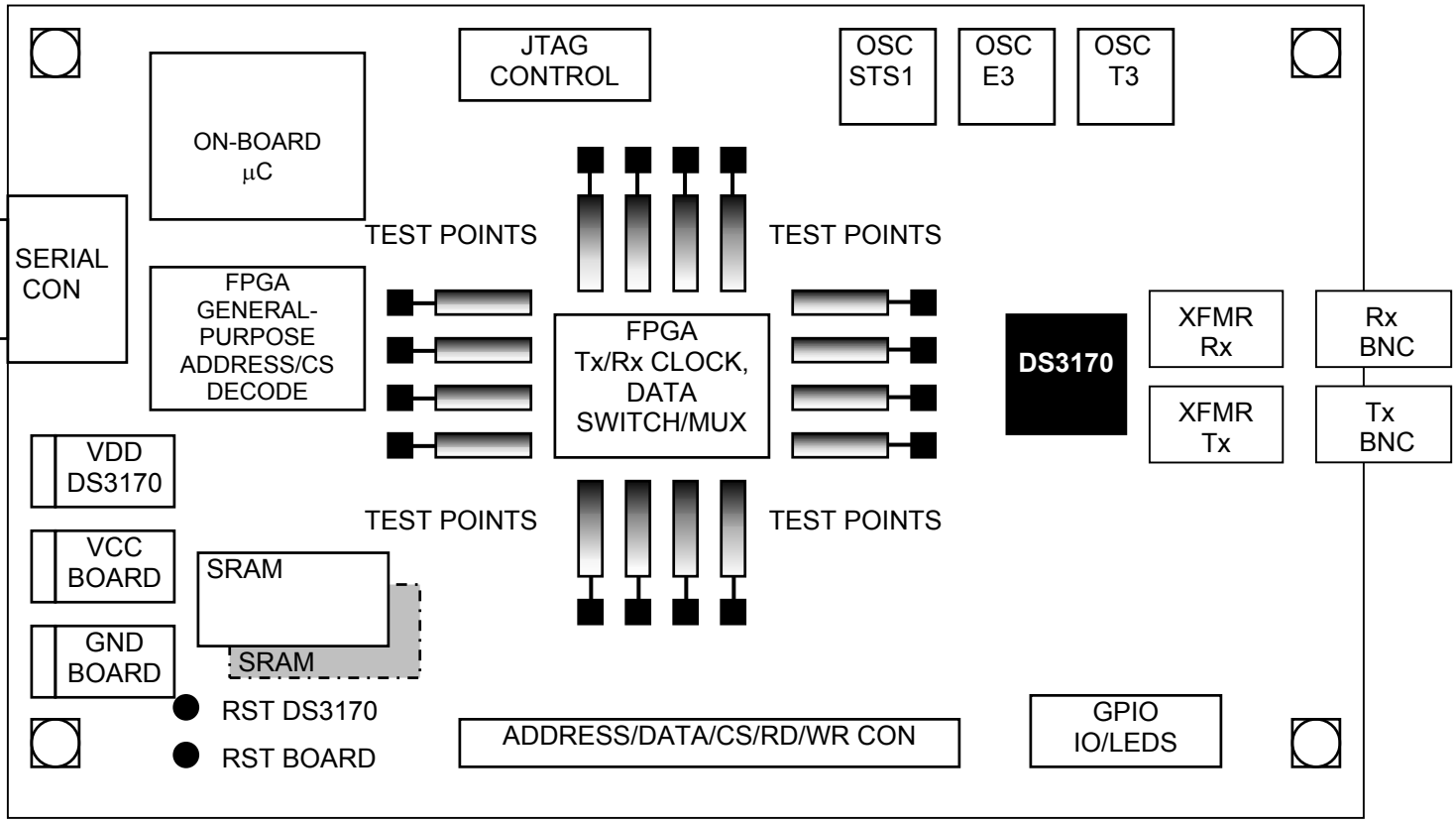
COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART NUMBER
C1, C4, C5, C10, C14, C15, C18, C19, C21, C24, C25–C32, C36-C38, C39–C44, C47–C49, C50, C52–C56, C59–C61, C66, C68, C70, C73, C74	44	0.1μF 20%, 16V X7R ceramic capacitors (0603)	AVX	0603YC104MAT
C2, C3, C16, C17, C20, C22, C23, C33, C34, C51, C57, C69, C75	13	1μF 10%, 16V ceramic capacitors (1206)	Panasonic	ECJ-3YB1C105K
C6, C62, C65	3	0.001μF 10%, 50V ceramic capacitors (0603)	Panasonic	ECJ-1VB1H102K
C7, C8, C9, C11, C35, C58, C76	7	68μF 20%, 16V tantalum capacitors (D case)	Panasonic	ECS-T1CD686R
C12, C13	2	10pF 5%, 50V ceramic capacitors (tall case)	Phycomp	1206CG100J9B200
C45, C46	2	10,000pF 10%, 16V ceramic capacitors (0603)	Panasonic	ECJ-1VB1C103K
C63, C64, C67	3	0.01μF 10%, 50V X7R ceramic capacitors (0603)	AVX	06035C103KAT
C71, C72	2	56,000pF 10%, 16V ceramic capacitors (0603)	Panasonic	ECJ-1VB1C563K
D1, D2	2	1A 50V general-purpose silicon diodes	General Semiconductor	1N4001
DS1, DS2, DS6–DS10	7	LED, green, SMD	Panasonic	LN1351C
DS3, DS4, DS5, DS11–DS19	12	LED, red, SMD	Panasonic	LN1251C
J1, PWR_CONNBAN1	2	Banana plug sockets (horizontal, black)	Mouser Electronics	164-6218
J2	1	DB9 right-angle connector (long case)	AMP	747459-1
J3	1	50-pin, dual-row, vertical terminal strip	Samtec	TSW-125-07-T-D
J4	1	100-mils 4-position jumper	Samtec	NA
J5	1	50Ω BNC connector (5-pin right-angle header)	Trompeter	CBJR220
J6, J7	2	Terminal strip, 10-pin, dual row, vertical	Samtec	NA
J8, J9	2	75Ω BNC connectors (5-pin right-angle)	Trompeter	UCBJR220
JP1, JP2, JP3, JP5, JP7, JP8	6	2-pin headers, 0.100” centerline (vertical)	Samtec	TSW-102-07-T-S
JP4	1	14-pin connector (dual row, vertical)	Samtec	NA
JP6	1	100-mils 3-position jumper	Samtec	NA
L1	1	1.0μH 20% 2-pin surface-mount inductor	Coiltronics	UP1B-1R0
PWR_CONNBAN2	1	Banana plug socket (horizontal, red)	Mouser Electronics	164-6219

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART NUMBER
R1–R4, R12, R42, R43, R54–R56, R59, R63, R68, R69, R70, R73, R74, R83, R93, R107	20	150Ω 1%, 1/16W resistors (0603)	Panasonic	ERJ-3EKF1500V
R5–R8, R10, R15, R51, R57, R62, R71, R81, R85, R92, R94, R95, R100, R101, R103–R106, R109	22	33Ω 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ330V
R9, R11, R16, R22, R30, R32, R38, R46, R60, R61, R64, R65, R72, R77–R80, R89, R90, R91, R96	22	330Ω 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ331V
R13	1	1.0MΩ 5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ105V
R14, R17–R21, R23–R29, R31, R33–R37, R39, R40, R41, R44, R45, R47, R48, R49, R52, R53, R58, R67, R75, R76, R82, R86, R87, R98, R99, R102, R108, R110	41	10kΩ 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ103V
R50	1	1.0kΩ 5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ102V
R66, R88, R97	3	0Ω 1%, 1/16W resistors (0603)	AVX	CJ10-000F
R84	1	51.1Ω 1%, 1/16W resistor (0603)	Panasonic	ERJ-3EKF51R1V
SW1, SW2, SW5	3	4-pin single-pole switch MOM	Panasonic	EVQPAE04M
SW3, SW4	2	8-position switch, 16-pin DIP, low profile	AMP	435668-7
SW6	1	Slide switch (DPDT) 6-pin through-hole	Tyco	SSA22
T1, T2	2	1:2 XFMR T3/E3/STS-1 (industrial)	Pulse	T3012
TP1–TP24	24	Test points, compensated, 3pF, 953Ω, 3 plated holes	NA	KIT1
U1, U5	2	8-pin power-μMAX (1.8V or Adj)	Maxim	MAX1792EUA18
U2	1	M-CORE 32-bit microcontroller	Motorola	MMC2107
U3, U6	2	Spartan-IIE 200K gate, 1.8V FPGA, 256 PIN BGA	Xilinx	XC2S200E-6FT256C
U4, U11	2	128K x 8 SRAM	Cypress	CY62128V
U7	1	DS3/E3 SCT 100-pin CSBGA (11mm x 11mm)	Dallas Semiconductor	DS3170
U8	1	3.3V RS-232 20-pin SO	Maxim	MAX3233EEWP
U9, U14, U16–U20, U23	8	High-speed buffer	Fairchild	NC7SZ86

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART NUMBER
U10, U12	2	2Mb flash-based configuration memory	Xilinx	XCF02SV020C
U13	1	Quad 2-input NAND gate 14-pin SO	Toshiba	TC74HC00AFN
U15, U21, U24	3	Hex inverter, SO	Toshiba	TC74HC04AFN
U22	1	SOT switch debouncer	Maxim	MAX6816
X1	1	8.0MHz low-profile crystal	Dove Electronic	EC1-8.000M
Y1	1	3.3V 51.840MHz oscillator, crystal clock	SaRonix	NTH089AA3-51.840
Y2	1	3.3V 34.368MHz oscillator, crystal clock	SaRonix	NTH089AA3-34.368
Y3	1	3.3V 44.736MHz oscillator, crystal clock	SaRonix	NTH089AA3-44.736

BOARD FLOORPLAN



BASIC OPERATION

This design kit relies upon several supporting files, which are available for downloading on our website at www.maxim-ic.com/telecom. See the DS3170DK QuickView page for files.

The support files are used with an evaluation program called ChipView with is available for download at www.maxim-ic.com/telecom.

HARDWARE CONFIGURATION

Quick Start (Hardware Settings)

- For single power-supply operation, short jumpers JP1-JP3. This connects VDD of the DS3170 to the board VCC.
- Ensure that *PROGRAM FLASH MICRO* is selected (SW6). DS3 should not be on.
- Connect reference clock. See Table 1.
- DIP switches (SW3) can be in either the ON or OFF position depending on the desired configuration. See Table 6..
- Connect serial cable from DS3170DK (J2) to PC.
- Supply 3.3V to the banana-plug receptacles marked GND and VCC_3.3V.

Reference Clock Configuration

The reference clock for the DS3170 (SCT) can be configured a number of ways depending on the application's need. This is done by shorting the REFCLK signal on J6 to the signal inputs, which are also connected to J6.

Table 1: Reference Clock Configuration

REFERENCE CLOCK	DESCRIPTION
GND	Short pins J6.1 and J6.2 together. Open all other pins on J6.
BNC Input	Short pins J6.3 and J6.4 together. Open all other pins on J6.
STS1 OSC	Short pins J6.5 and J6.6 together. Open all other pins on J6.
E3 OSC	Short pins J6.7 and J6.8 together. Open all other pins on J6.
T3 OSC	Short pins J6.9 and J6.10 together. Open all other pins on J6.

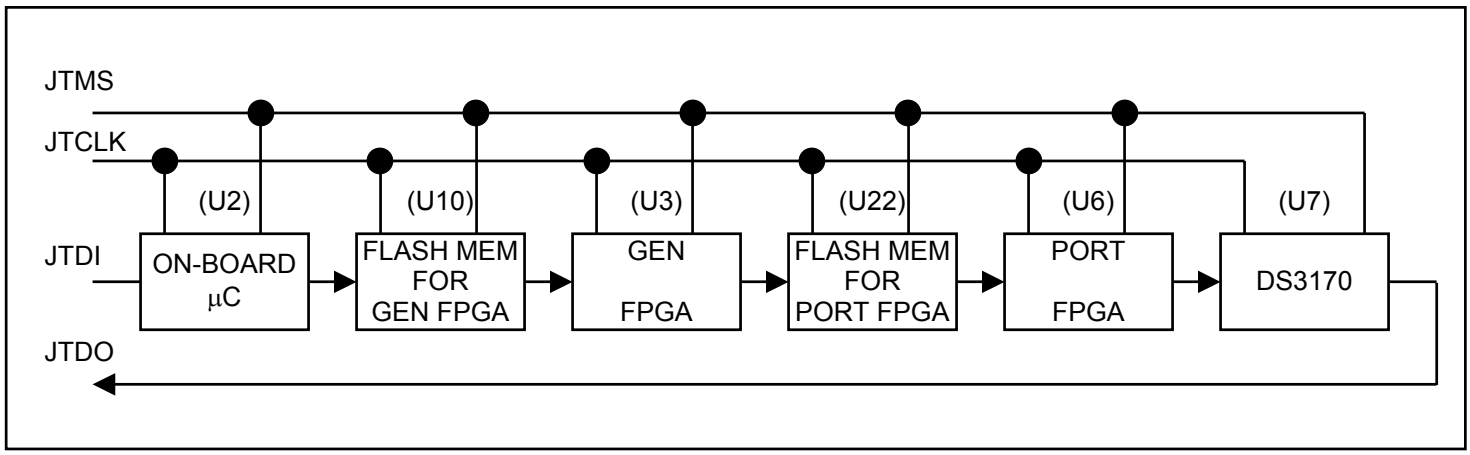
JTAG Configuration

The JTAG chain is controlled by the following connectors: J4, JP4, and JP5. Depending on the function, such as programming the internal microcontroller flash or performing boundary scan operations, the three connectors can be configured to accomplish the desired task. For information on programming the internal flash of the microcontroller, refer to the microcontroller user manual and board schematic.

For most purposes, having the complete JTAG chain is sufficient. Figure 1 shows the complete chain as well as what order the devices will appear during boundary scan. To set up this configuration, perform the following:

- Connect JTDI to JP4.1
- Connect JTDO to JP4.3
- Connect JTMS to JP4.10
- Connect JCLK to JP4.5
- Connect J4.1 to J4.2
- Connect J4.3 to J4.4
- Connect JP5.1 to JP5.2

Figure 1. JTAG Chain



Address/Data BUS Connector

The DS3170DK has a connector (J3) to monitor all local bus activity for the design kit. All the signals can be captured with a high-impedance probe and displayed on an oscilloscope or logic analyzer. **Note:** If FPGA_ENABLE (SW3.3) is logic 0, the on-board microcontroller will no longer drive any data onto the local bus. Therefore, the user can now connect the local bus of the DS3170 into another system without making any modifications to the hardware. See Table 2 for specific pin information for connector J3.

Table 2. Address/Data Connector

PIN NUM	PIN NAME	DESCRIPTION		PIN NUM	PIN NAME	DESCRIPTION
1	A0	Local Address Bit 0		2	D0	Local Data Bit 0
3	A1	Local Address Bit 1		4	D1	Local Data Bit 1
5	A2	Local Address Bit 2		6	D2	Local Data Bit 2
7	A3	Local Address Bit 3		8	D3	Local Data Bit 3
9	A4	Local Address Bit 4		10	D4	Local Data Bit 4
11	A5	Local Address Bit 5		12	D5	Local Data Bit 5
13	A6	Local Address Bit 6		14	D6	Local Data Bit 6
15	A7	Local Address Bit 7		16	D7	Local Data Bit 7
17	A8	Local Address Bit 8		18	D8	Local Data Bit 8
19	A9	Local Address Bit 9		20	D9	Local Data Bit 9
21	CS3170	Chip Select DS3170		22	D10	Local Data Bit 10
23	CSFPGA	Chip Select Port FPGA		24	D11	Local Data Bit 11
25	INT3170	INT PIN DS3170		26	D12	Local Data Bit 12
27	RST3170	RST PIN DS3170		28	D13	Local Data Bit 13
29	RDY	Ready Handshake DS3170		30	D14	Local Data Bit 14
31	TEST0	Generic I/O Bit 0		32	D15	Local Data Bit 15
33	TEST1	Generic I/O Bit 1		34	SPI	DS3170 Serial/Parallel Bus Mode
35	TEST2	Generic I/O Bit 2		36	ALE	Address Latch Enable
37	TEST3	Generic I/O Bit 3		38	RD_DS	Read (Intel)/Data Strobe (MOT)
39	TEST4	Generic I/O Bit 4		40	WR_W/R	Write (Intel)/Write_READ (MOT)
41	TEST5	Generic I/O Bit 5		42	CS_OUT	Programmable CS_OUT Pin
43	TEST6	Generic I/O Bit 6		44	MODE	Mot/Intel Mode
45	TEST7	Generic I/O Bit 7		46	WIDTH	Data Bus Width
47	GND	GND		48	TEST	Test Enable (Active Low)
49	GND	GND		50	HIZ	High Impedance (Active Low)

High Impedance and Compensated Test Points

The test points for all the clock and data lines are unique for this board such that each test point listed in Table 3 have a relative high-impedance pin and a compensated pin. The compensated pin is part of a (20:1) voltage divider that when used with the standard 50Ω load of an oscilloscope provides a very clean signal. If you are making critical timing and or slew rate measurements, the compensated test points are very useful. Figure 2 shows the relationship between the high-impedance and compensated test point pins.

Figure 2. Test Point Logical and Physical View

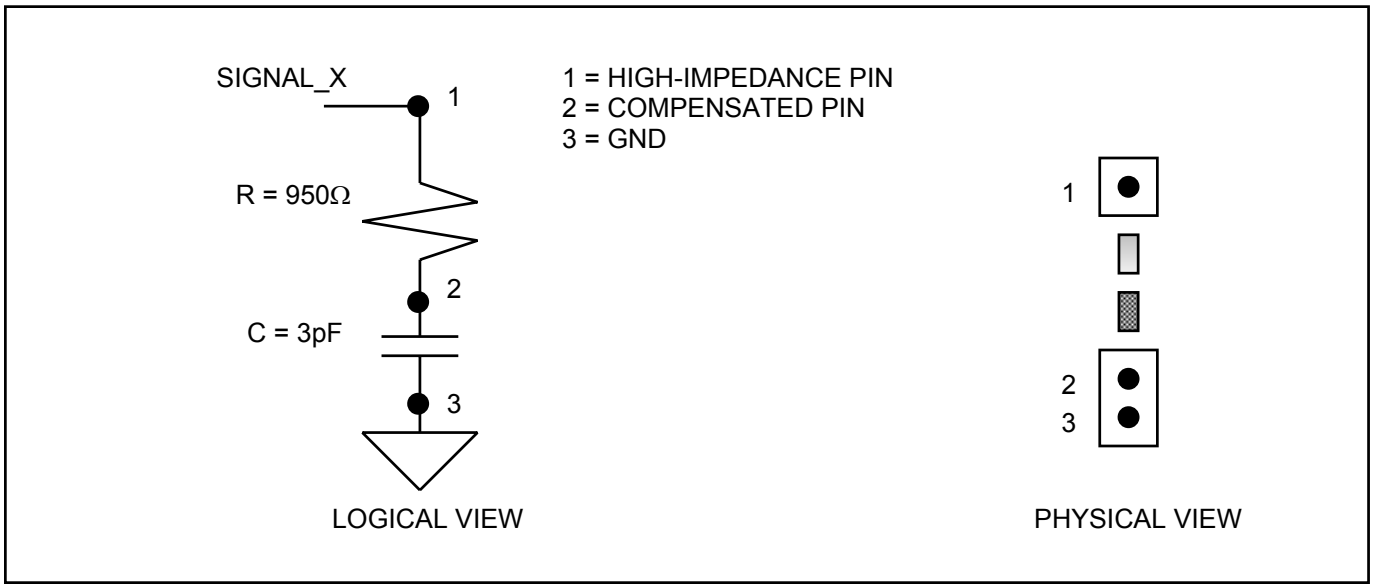


Table 3. Test Points

REF DES	SIGNAL NAME		REF DES	SIGNAL NAME
TP5	TCLKI		TP7	TNEG
TP6	TCLKO		TP8	RNEG
TP4	RCLKO		TP2	TPOS
TP20	TLCLK		TP3	RPOS
TP19	RLCLK		TP11	TSER
TP10	TOHSOF		TP9	RSER
TP12	ROHSOF		TP13	TOHEN
TP16	TOHCLK		TP14	TOH
TP17	ROHCLK		TP15	ROH
TP19	TSOFO		TP23	REFCLK
TP22	RSOFO		TP21	TSOFI

General Purpose Input/Output for DS3170

The DS3170 SCT has an 8-bit port that can be bit configured as either general-purpose I/O or specific alarms, a TEMI input, or PMU input. Refer to the DS3170 data sheet for specific questions about the operation of the DS3170 GPIO port.

Each GPIO pin has two types of inputs and an LED for easy identification of the pin's state. The first input type for the GPIO port is an 8-bit switch (SW4). Each pin on SW4 corresponds to the bit in the GPIO. When the switch is in the "On" position, the pin for the switch is grounded and provides logic 0 to the port. When the switch is in the "Off" position, the pin for the switch floats to VDD and provides logic 1 to the port.

The second input type for the GPIO port is a straight 10-pin header (J7). This can be simply a monitoring pin for the GPIO port or used as input stimulus. **Note:** If you plan to drive a bit to a value other than GND, the GPIO bit in SW4 must be in the "Off" position. See the DS3170DK schematic for questions on the connection of the GPIO port.

Table 4 provides a description of pin out of SW4 and J7.

Table 4. GPIO Header and Switch Pinout

PIN NUMBER		PIN NAME
SW4.1	J7.1	GPIO Bit 1
SW4.2	J7.2	GPIO Bit 2
SW4.3	J7.3	GPIO Bit 3
SW4.4	J7.4	GPIO Bit 4
SW4.5	J7.5	GPIO Bit 5
SW4.6	J7.6	GPIO Bit 6
SW4.7	J7.7	GPIO Bit 7
SW4.8	J7.8	GPIO Bit 8

TEMI and PMU Inputs

GPIO Bit 6 and GPIO Bit 8 can be configured to be the TEMI and PMU inputs respectively. A pushbutton (SW5) and 3-position jumper (JP6) are available to provide a glitch-free input to either of these inputs. **Note:** When using the pushbutton (SW5) and 3-position jumper (JP6) as an input to the GPIO pins, you must have the appropriate switch in SW4 in the "Off" position.

Table 5. TEMI and PMU Configuration

SIGNAL NAME	SETUP PROCEDURE
TEMI	Set SW4.6 to the "Off" position
	Short (Jumper) JP6.3 and JP2
PMU	Set SW4.8 to the "Off" position
	Short (Jumper) JP6.1 and JP2

User Input Switch (SW3)

SW3 is an 8-pin DIP switch that controls the function of the on-board microcontroller and the two on-board FPGAs, and offers a number of generic inputs for user programs.

Table 6. User Input Switch Pinout

PIN	NAME	FUNCTION
1	FPGA INPUT 1	Generic Input-Only Pin to the General-Purpose FPGA. Value of pin is copied to general-purpose register XXXXXXXX. Can be used for user programs. This pin has no effect if FPGA ENABLE is logic 0.
2	FPGA INPUT 2	Generic Input-Only Pin to the General-Purpose FPGA. Value of pin is copied to general-purpose register XXXXXXXX. Can be used for user programs. This pin has no effect if FPGA ENABLE is logic 0.
3	FPGA ENABLE	Input-Only Pin to the General-Purpose FPGA (U3). When this pin is logic 1 (SW3.3 is OFF), the FPGA is enabled and will transfer data from the DS3170 and FPGA as directed from the on-board microcontroller. When this pin is logic 0 (SW3.3 is ON), the FPGA is disabled. All inputs and outputs to the DS3170 and port FPGA are tri-stated. **Note:** This pin does not cause a hardware enable for the PORT FGPA.
4	DATA BUS SELECT	Input-Only Pin to the General-Purpose FPGA (U3). When this pin is logic 1 (SW3.4 is OFF), the DS3170 and the port FPGA are set up such that they use the 16-bit bus from the on-board microcontroller. When this pin is logic 0 (SW3.4 is ON), the DS3170 and the port FPGA are set up such that they use the 8-bit bus from the on-board microcontroller. This pin has no effect if FPGA ENABLE is logic 0.
5	BOOT SEL	Input-Only Pin to the On-Board Microcontroller. When this pin is logic 1 (SW3.5 is OFF), the on-board microcontroller loads the firmware from an external source rather than the internal flash bank. When this pin is logic 0 (SW3.5 is ON), the microcontroller loads the firmware from the internal flash bank. If you choose to load code from an external source, refer to the user manual for the on-board microcontroller (U2) to ensure that all the timing and data are correct to run this program. This option should only be used by the advanced user.
6	KIT	Input-Only Pin to the On-Board Microcontroller. Not implemented with the firmware shipped from Dallas Semiconductor. This pin can be used by a user program.
7	USER INPUT 1	Input/Output Pin to the General-Purpose FPGA (U3). This pin has an LED (DS4) to track the value of this signal. This pin has no effect if FPGA ENABLE is logic 0. **Note:** If you choose to use this as an output, USER INPUT 1 (SW3.7) must be in the off position.
8	USER INPUT 2	Input/Output Pin to the General-Purpose FPGA (U3). This pin has an LED (DS5) to track the value of this signal. This pin has no effect if FPGA ENABLE is logic 0. **Note:** If you choose to use this as an output, USER INPUT 1 (SW3.8) must be in the off position.

SOFTWARE CONFIGURATION

Quick Start (Software—ChipView)

- Perform steps in the Quick Start (Hardware Settings).
- Load ChipView software.
- Select COM port.
- Select Register View.
- From the Programs menu, launch the host application named ChipView.EXE. If the default installation options were used, click the Start button on the Windows toolbar and select Programs → ChipView → ChipView.
- Load the DS3170DK.DEF file.
- Make sure that all the register settings are correct for the proper function desired for the DS3170DK.
- Refer to the DS3170 data sheet for all questions pertaining to device functionality.

MEMORY MAP

The on-board microcontroller is configured to start the user address space at 0x81000000. All offsets given in Table 7 are relative to the beginning of the user address space. All device registers can be easily modified using ChipView.EXE host-based user-interface software.

Table 7. Relative Address Map

REF DES	DEVICE	OFFSET
U3	General-purpose FPGA	0x0000
U6	FPGA Tx/Rx clock, data switch/mux	0x1000
U7	DS3170 DS3/E3 single-chip transceiver	0x2000

Table 8. General-Purpose Memory Map

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0x00	BRDID	Read Only	Board ID
0x02	DSIDH	Read Only	Dallas Extended ID Upper Nibble
0x03	DSIDM	Read Only	Dallas Extended ID Middle Nibble
0x04	DSIDL	Read Only	Dallas Extended ID Lower Nibble
0x05	BRDREV	Read Only	Board Rev
0x06	ASMREV	Read Only	Assembly Rev
0x07	FPGAREV	Read Only	FPGA Firmware Rev
0x08	CTRL1	Control	Control Reg #1

ID REGISTERS

BID: BOARD ID (Offset=0X0000)

BID is read only with a value of 0xD.

XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset=0X0002)

XBIDH is read only with a value of 0x00.

XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset=0X0003)

XBIDM is read only with a value of 0x07.

XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset=0X0004)

XBIDL is read only with a value of 0x00.

BREV: BOARD FAB REVISION (Offset=0X0005)

BREV is read only and displays the current fab revision.

AREV: BOARD ASSEMBLY REVISION (Offset=0X0006)

AREV is read only and displays the current assembly revision.

PREV: PLD REVISION (Offset=0X0007)

PREV is read only and displays the current PLD firmware revision.

CONTROL REGISTERS

Register Name: **CTRL1**
Register Description: **Control Register 1**
Register Offset: **0x0008**

Bit #	7	6	5	4	3	2	1	0
Name	SPI_CPOL	SPI_CPHA	SPI_SWAP	SPI	HIZ	WIDTH	MOT	MUX
Default	0	0	0	0	1	0	0	0

Bit 7: SPI_CPOL: This bit controls the SPI Interface Clock Polarity pin, which is muxed with the D7 pin on the DS3170. Bit 7 is only active when bit 4 (SPI) is a logic 1. Refer to the DS3170 data sheet for pin operation.

Bit 6: SPI_CPHA: This bit controls the SPI Interface Clock Phase pin, which is muxed with the D6 pin on the DS3170. Bit 6 is only active when Bit 4 (SPI) is a logic 1. Refer to the DS3170 data sheet for pin operation.

Bit 5: SPI_SWAP: This bit controls the SPI Interface Bit Order Swap pin, which is muxed with the D5 pin on the DS3170. Bit 5 is only active when Bit 4 (SPI) is a logic 1. Refer to the DS3170 data sheet for pin operation.

Bit 4: SPI: This bit controls the SPI Bus Mode bit.
0 = parallel bus mode
1 = SPI bus mode

Bit 3: HIZ: This bit controls the high-impedance test-enable bit (active low). This signal puts all the digial outputs and bidirectional outputs to a high-impedance state when pulled low and also when the JTRST is pulled low. For nomal operation, keep it as a logic 1.

Bit 2: WIDTH: This bit controls the databus width pin for parallel bus mode.
0 = 8-bit parallel mode
1 = 16-bit parallel mode

Bit 1: MOT: This bit controls the MODE pin for the DS3170.
0 = RD/WR strobe mode (Intel)
1 = DS strobe mode (Motorola)

Bit 0: MUX: This bit determines if the ALE pin on the DS3170 is in mux mode or nonmux mode (constantly high).
0 = nonmux mode
1 = mux mode

Register Name: **CTRL2**
Register Description: **Control Register 2–Line IO**
Register Offset: **0x0009**

Bit #	7	6	5	4	3	2	1	0
Name	RNEG3	RNEG2	RNEG1	RNEG0	RPOS3	RPOS2	RPOS1	RPOS0
Default	0	0	0	0	1	0	0	0

Bits 7 to 4: RNEGx: These bits control the source of the RNEG signal.

Bits 3 to 0: RPOSx: These bits control the source of the RPOS signal.

RPOSx	DESCRIPTION
0x00	HI-Z
0x01	TPOS
0x02	T3 OSC
0x03	E3 OSC
0x04	STS1 OSC
0x05	BNC_INPUT
0x06	Logic 0
0x07	Logic 1
0x08–0xFF	HI-Z

RNEGx	DESCRIPTION
0X00	HI-Z
0X01	TNEG
0X02	T3 OSC
0X03	E3 OSC
0X04	STS1 OSC
0X05	BNC_INPUT
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

Register Name: **CTRL3**
Register Description: **Control Register 3–Line RCLK**
Register Offset: **0x000A**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	RLCLK3	RLCLK2	RLCLK1	RLCLK0
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: These bits are unused.

Bits 3 to 0: RLCLKx: These bits control the source of the RLCLK signal.

RLCLKx	DESCRIPTION
0X00	HI-Z
0X01	TLCLK
0X02	T3 OSC
0X03	E3 OSC
0X04	STS1 OSC
0X05	BNC_INPUT
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

Register Name: **CTRL4**
Register Description: **Control Register 4 Overhead Interface**
Register Offset: **0x000B**

Bit #	7	6	5	4	3	2	1	0
Name	TOHEN3	TOHEN2	TOHEN1	TOHEN0	TOH3	TOH2	TOH1	TOH0
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: TOHENx: These bits control the source of the TOHEN signal.

Bits 3 to 0: TOHx: These bits control the source of the TOH signal.

TOHENx	DESCRIPTION
0X00	HI-Z
0X01	TOHSOF
0X02	ROHSOF
0X03	Not used
0X04	Not used
0X05	Not used
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

TOHx	DESCRIPTION
0X00	HI-Z
0X01	ROH
0X02	Not used
0X03	Not used
0X04	Not used
0X05	Not used
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

Register Name: **CTRL5**
Register Description: **Control Register 5 Serial Data Overhead Interface**
Register Offset: **0x000C**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	TSER3	TSER2	TSER1	TSER0
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: These bits are unused.

Bits 3 to 0: TSERx: These bits control the source of the TSER signal.

TSERx	DESCRIPTION
0X00	HI-Z
0X01	RSER
0X02	Not Used
0X03	Not Used
0X04	Not Used
0X05	Not Used
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

Register Name: **CTRL6**
Register Description: **Control Register 6 Serial Data Overhead Interface**
Register Offset: **0x000D**

Bit #	7	6	5	4	3	2	1	0
Name	TSOFI3	TSOFI2	TSOFI1	TSOFI0	TCLKI3	TCLKI2	TCLKI1	TCLKI0
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: TSOFIx: These bits control the source of the TSOFI signal.

Bits 3 to 0: TCLKIx: These bits control the source of the TCLKI signal.

TSOFIx	DESCRIPTION
0X00	HI-Z
0X01	TSOFO
0X02	RSOFO
0X03	Not Used
0X04	Not Used
0X05	Not Used
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

TCLKIx	DESCRIPTION
0X00	HI-Z
0X01	TCLKO
0X02	RCLKO
0X03	Not Used
0X04	Not Used
0X05	Not Used
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

DS3170 INFORMATION

For more information about the DS3170, refer to the DS3170 data sheet available on our website at www.maxim-ic.com/DS3170. Software downloads are also available for this design kit.

DS3170DK INFORMATION

For more information about the DS3170DK including software downloads, consult the DS3170DK data sheet available on our website at www.maxim-ic.com/DS3170DK.

TECHNICAL SUPPORT

For additional technical support, e-mail your questions to telecom.support@dalsemi.com.

SCHEMATICS

The DS3170DK schematics are featured in the following 23 pages.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

DS3170 DESIGN KIT

CREATED BY
DALLAS SEMICONDUCTOR
JUNE 26, 2004

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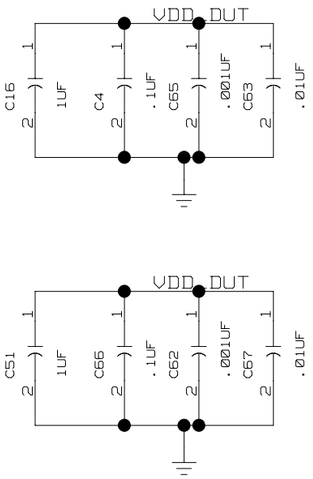
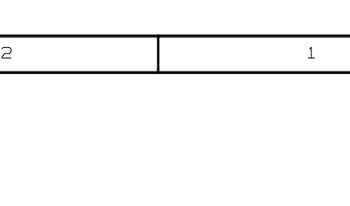
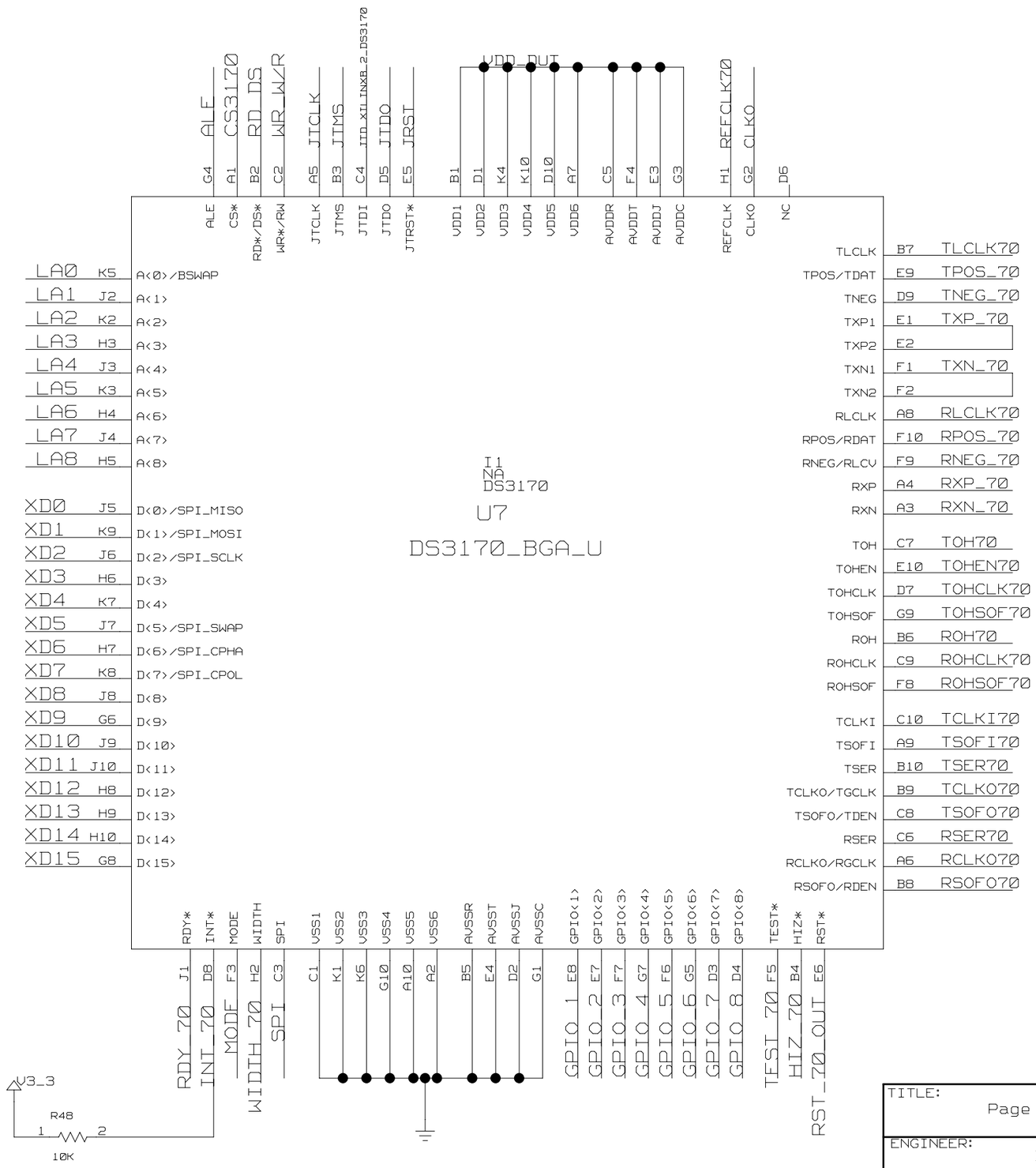
TITLE: Page 1. COVER PAGE	DATE:
ENGINEER: DALLAS SEMICONDUCTOR	PAGE: 1

DS3170
100 PIN BGA







Fri Mar 18 13:46:03 2005

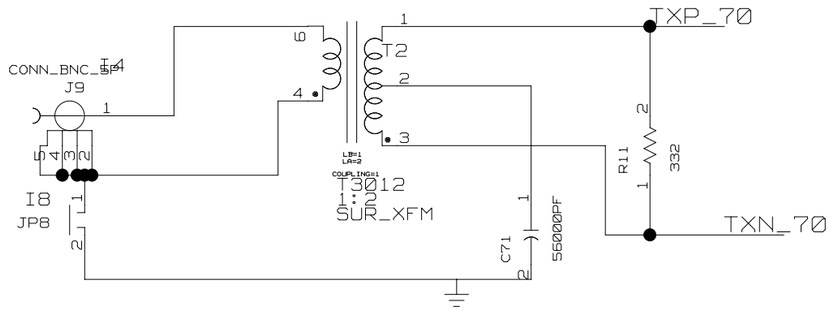
TITLE: Page 2. DS3170 BGA	DATE:
ENGINEER: DALLAS SEMICONDUCTOR	PAGE: 2

DS3170

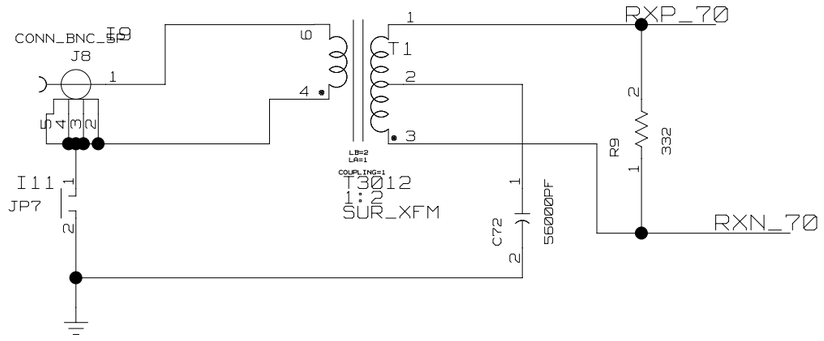
100 PIN BGA

LIU INTERFACE

TRANSMIT



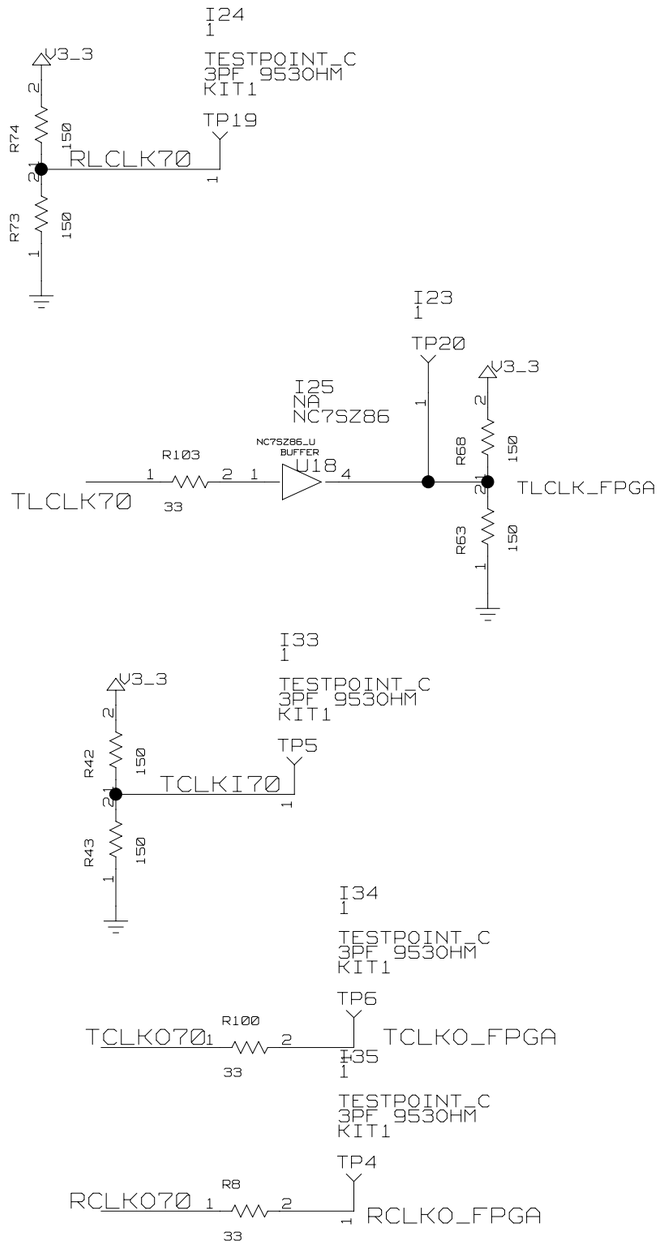
RECEIVE



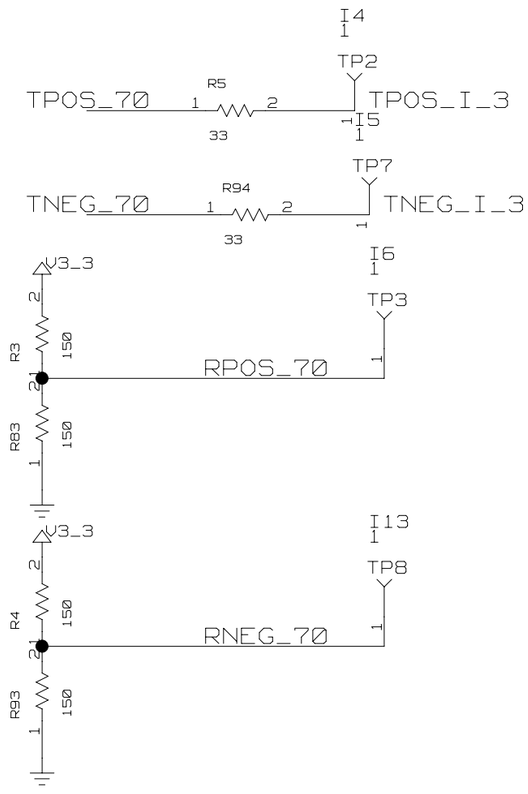
Fri Mar 18 13:46:04 2005

TITLE: Page 3. LIU INTERFACE	DATE:
ENGINEER: DALLAS SEMICONDUCTOR	PAGE: 3

TCLK/RCLK TERMINATION



TELECOM DATA IO
TPOS/TNEG/RPOS/RNEG

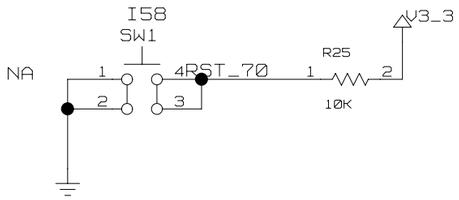


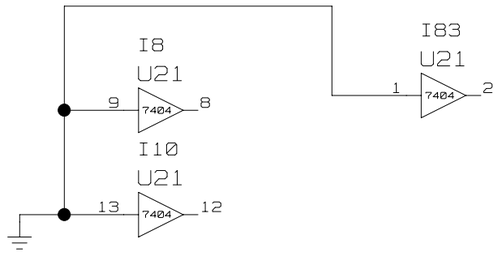
Fri Mar 18 13:46:04 2005

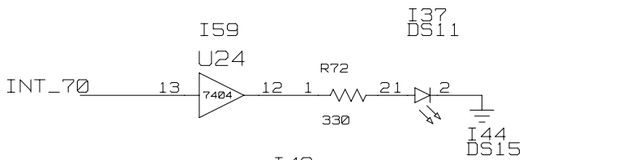
TITLE: Page 4. TCLK/RCLK/TELECOM DATA	DATE:
ENGINEER: DALLAS SEMICONDUCTOR	PAGE: 4

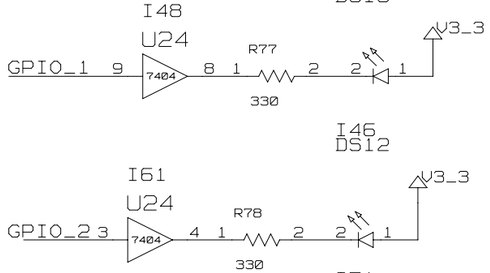
RESET

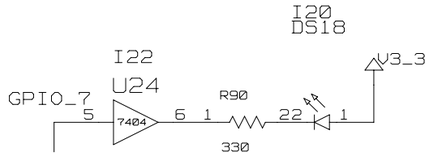
DS3170

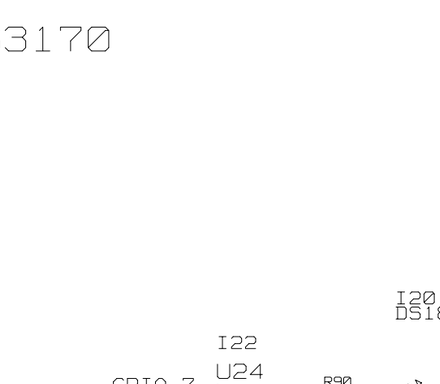






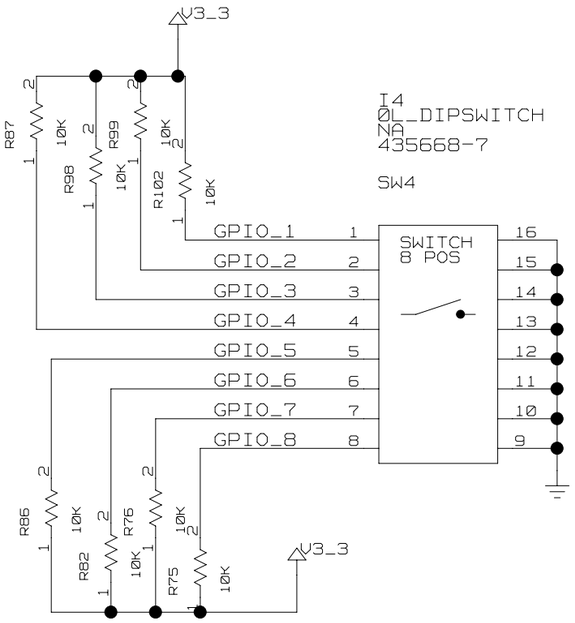


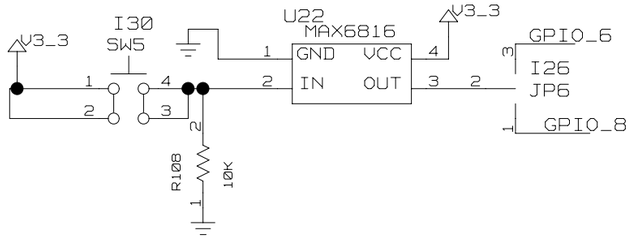




GPIO

DS3170



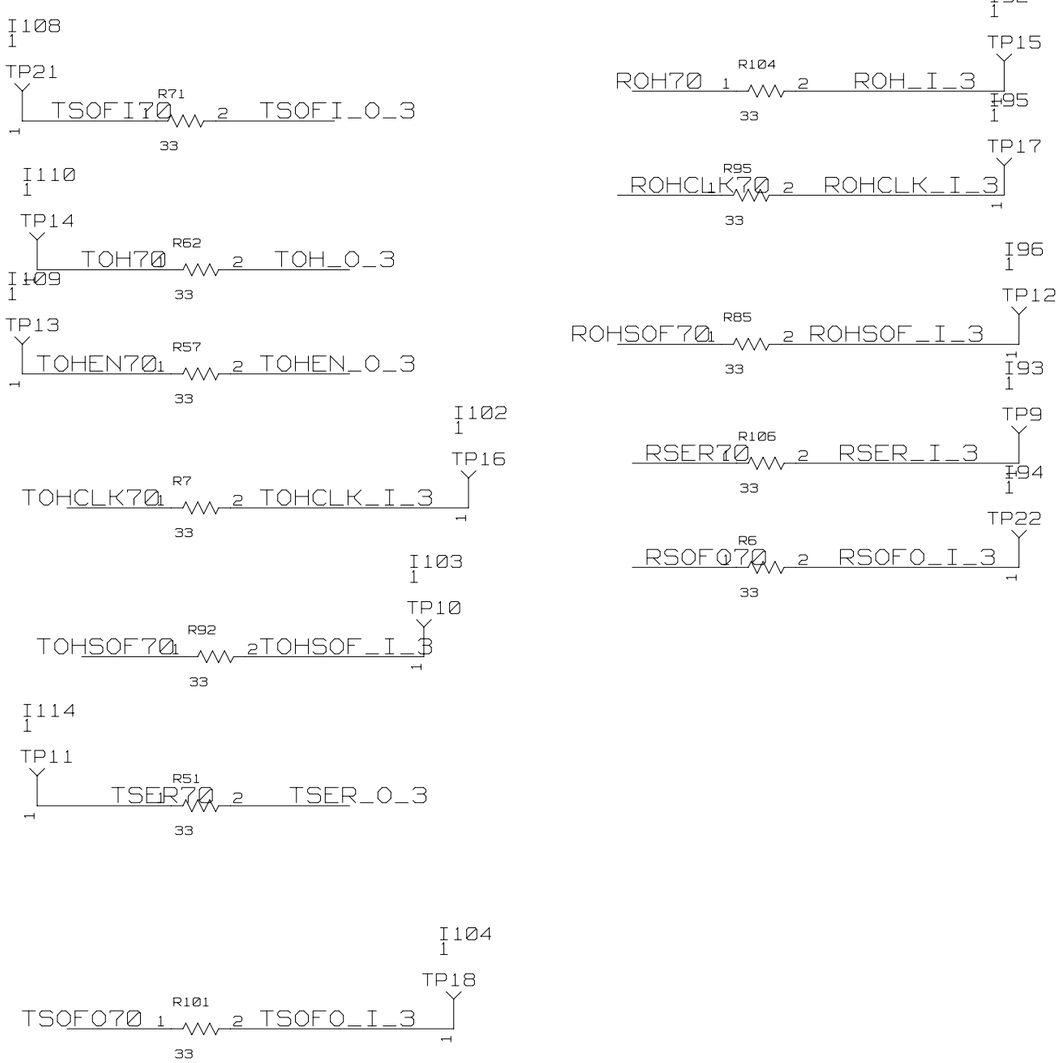


Fri Mar 18 13:46:04 2005

TITLE: Page 5. DS3170 RESET / GPIO	DATE:
ENGINEER: DALLAS SEMICONDUCTOR	PAGE: 5

DS3170

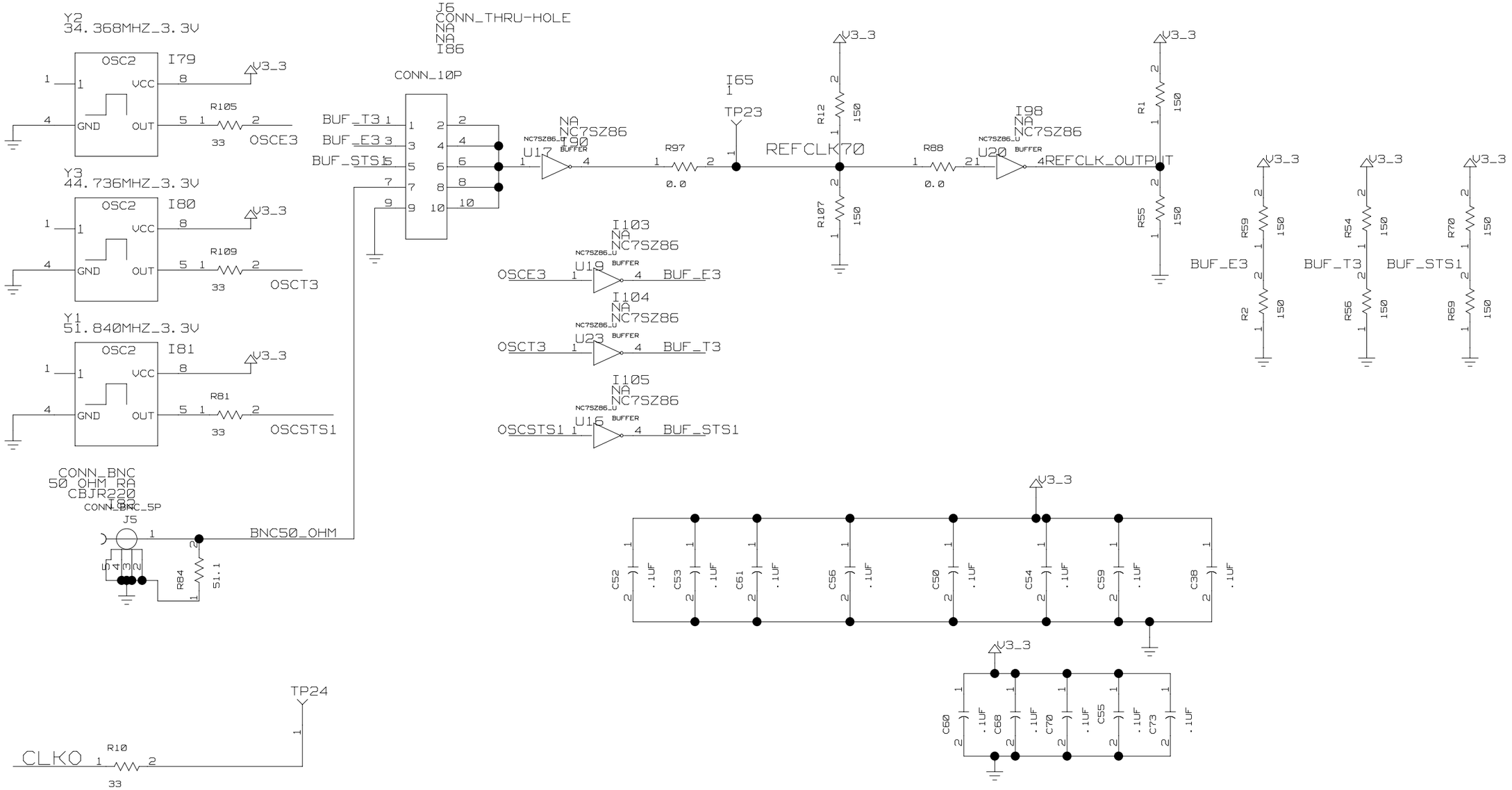
MISC TELECOM TERM



Fri Mar 18 13:46:05 2005

TITLE: Page 6. MISC TELECOM SIGNALS	DATE:
ENGINEER: DALLAS SEMICONDUCTOR	PAGE: 6

REFERENCE CLOCK



Fri Mar 18 13:46:05 2005

TITLE: Page 7. REF OSC	DATE:
ENGINEER: DALLAS SEMICONDUCTOR	PAGE: 7

FPGA PORT (DS3170)

I15
MAX1792
NA
MAX1792EUA18

U5
MAX1792

V3_3
V1_8_C

IN, IN, RST, SHDN
OUT, OUT, SET, GND

C40 .1UF
C48 .1UF
C43 .1UF
C49 .1UF
C42 .1UF

C45 10000PF
C44 .1UF
C47 .1UF
C46 10000PF

I6
XILINX_PLD
200K
XC2S200E-6FT256C

XC2SE_FT256_U

SPARTAN IIE

VCCINT1 C14
VCCINT2 D4
VCCINT3 D13
VCCINT4 E5
VCCINT5 E12
VCCINT6 M5
VCCINT7 M12
VCCINT8 N4
VCCINT9 N13
VCCINT10 P3
VCCINT11 P14
VCCINT12 C3

VCC1 E8
VCC2 F7
VCC3 F8
VCC4 E9
VCC5 F9
VCC6 F10
VCC7 G11
VCC8 H11
VCC9 H12
VCC10 J11
VCC11 J12
VCC12 K11
VCC13 L9
VCC14 L10
VCC15 M9
VCC16 L7
VCC17 L8
VCC18 M8
VCC19 J5
VCC20 J6
VCC21 K6
VCC22 G6
VCC23 H5
VCC24 H6

GND1 A1
GND2 A16
GND3 B2
GND4 B15
GND5 F6
GND6 F11
GND7 G7
GND8 G8
GND9 G9
GND10 G10
GND11 H7
GND12 H8
GND13 H9
GND14 H10
GND15 J7
GND16 J8
GND17 J9
GND18 J10
GND19 K7
GND20 K8
GND21 K9
GND22 K10
GND23 L6
GND24 L11
GND25 R2
GND26 R15
GND27 T1
GND28 T15

TMS B1 JTMS
TDI C15 JTD_FLASHB_2_XILINXB
TCK A2 JTCLK
TDO B14 JTD_XILINXB_2_DS3170
PROGRAM* R16 PROGRAM_B
CCLK A15 CCLK_B
DONE T15 DONE_B
M0 T2
M1 R1
M2 R3

I25
TSSOP
2MBIT
XCF02SV020C

U12
XILINX_XCF01S

CFG_DIN_B 1 D0
2 DNC1
CCLK_B 3 CLK
JTD_XILINXA_2_FLASHB 4 TDI
JTMS 5 TMS
JTCLK 6 TCK
PROGRAM_B 7 CF*
RESET_B 8 OE/RST*
9 DNC2
DONE_B 10 CE*

VCCJ 20
VCCO 19
VCCINT 18
TDO 17 JTD_FLASHB_2_XILINXB
DNC3 16
DNC4 15
DNC5 14
CEO* 13
DNC6 12
GND 11

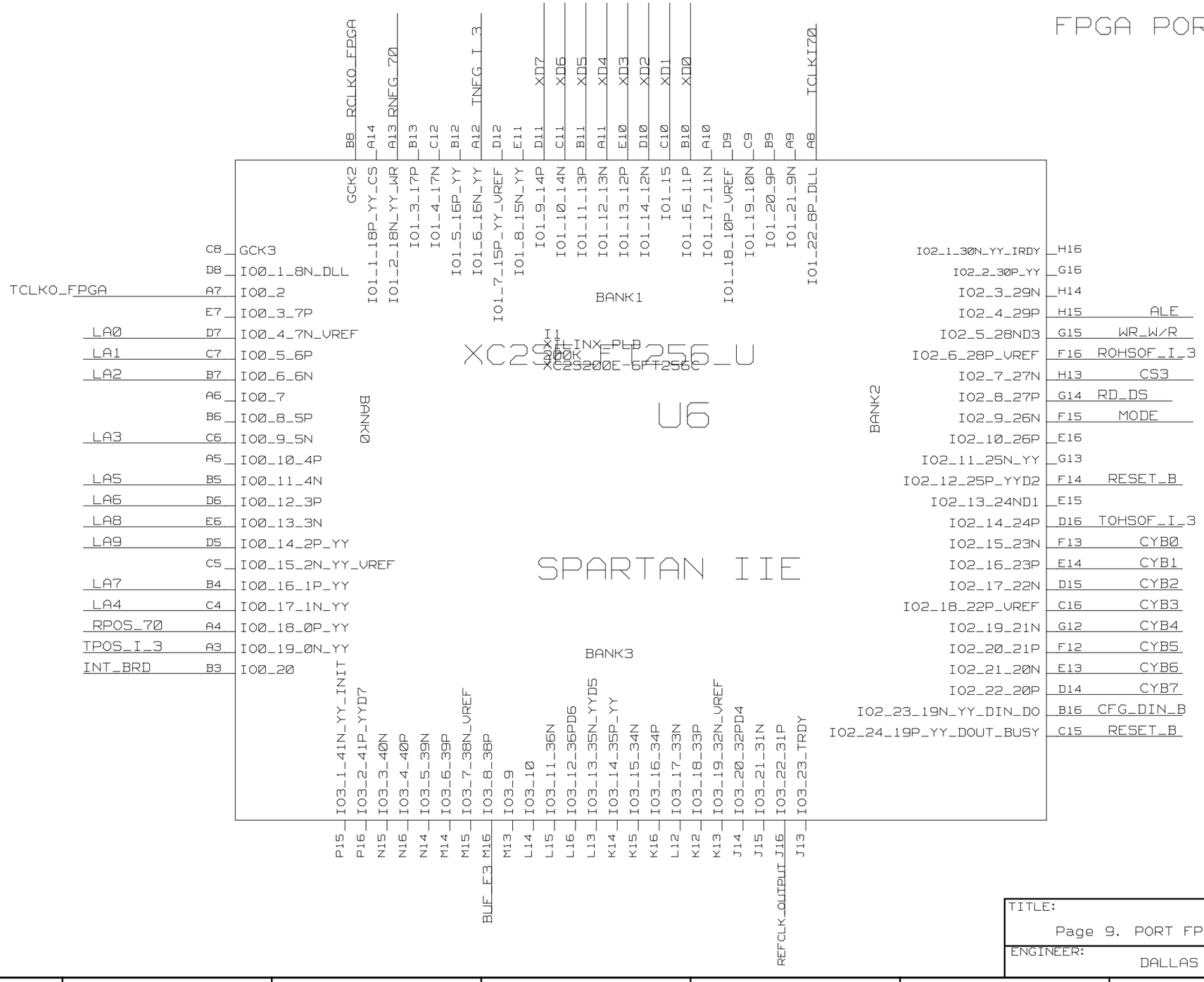
I2
NZ
NC7SZ86
U14
INVERTER
DONE_B

I8
DS6
R46
330

Fri Mar 18 13:46:05 2005

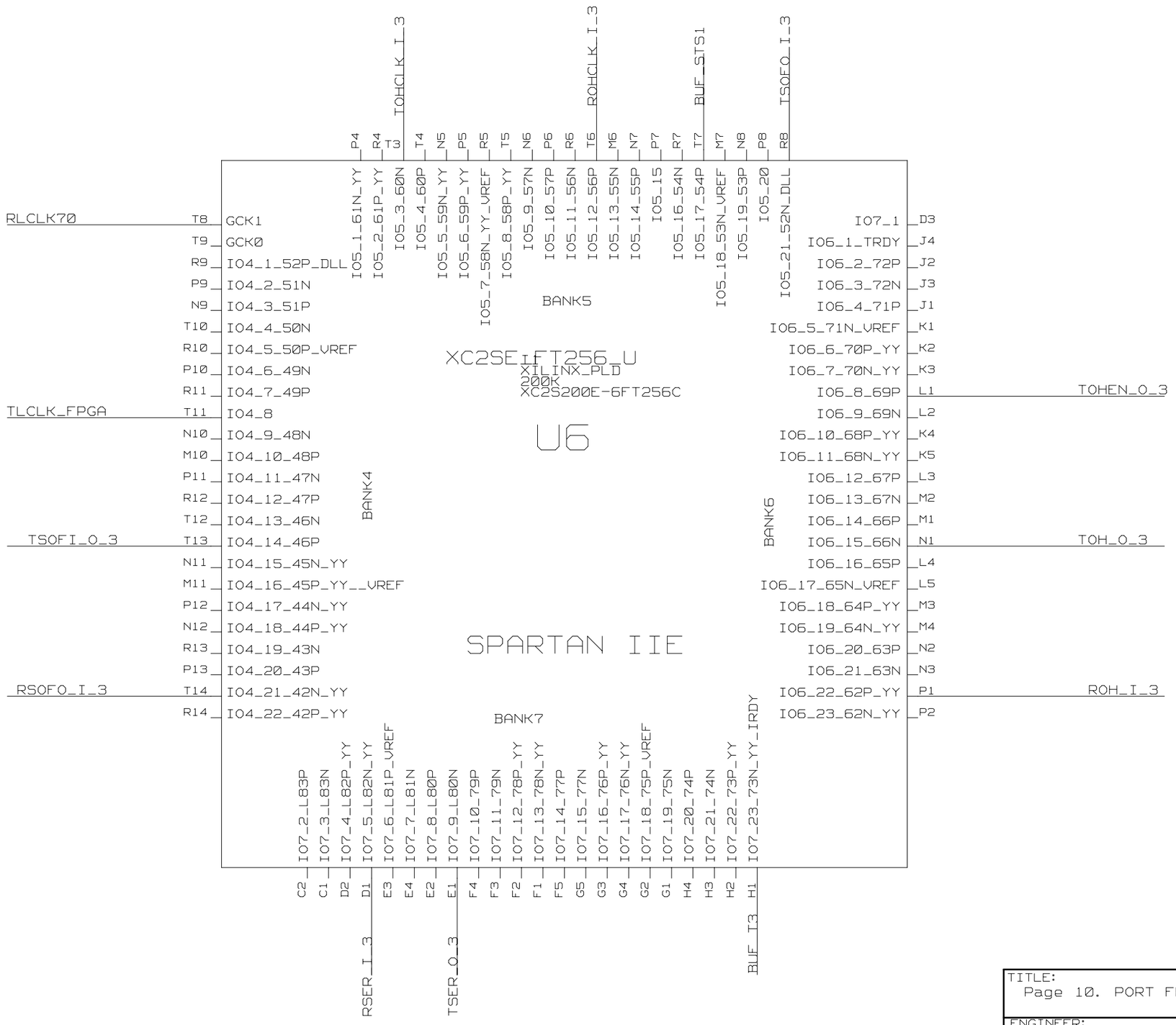
TITLE: Page 8. PORT FPGA CONTROL / FLASH	DATE:
ENGINEER: DALLAS SEMICONDUCTOR	PAGE: 8

FPGA PORT (DS3170)



Fri Mar 18 13:46:05 2005

TITLE: Page 9. PORT FPGA BLOCK1	DATE:
ENGINEER: DALLAS SEMICONDUCTOR	PAGE: 9

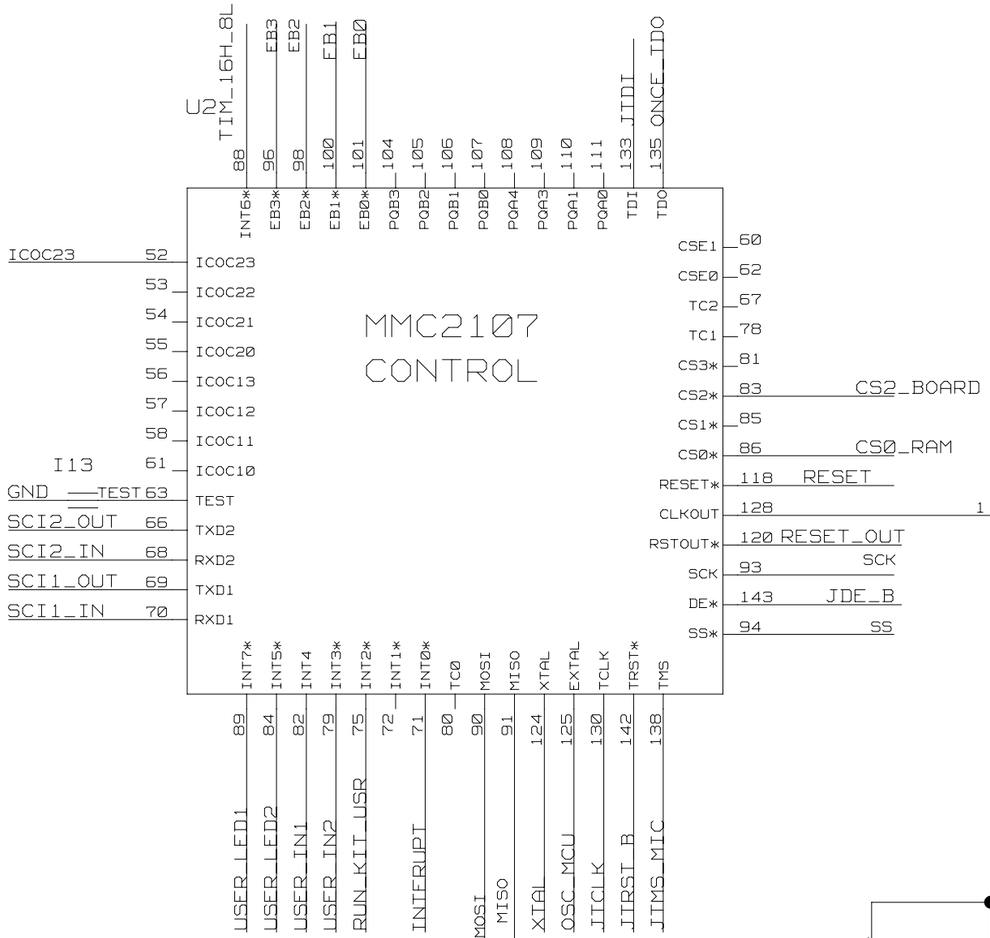


Fri Mar 18 13:46:06 2005

TITLE: Page 10. PORT FPGA BLOCK2	DATE:
ENGINEER: DALLAS SEMICONDUCTOR	PAGE: 10

I14
144PIN_TQFP
NA
MMC2107

U2
TIM_16H_8L



I13
GND
SCI2_OUT
SCI2_IN
SCI1_OUT
SCI1_IN

USER_LED1
USER_LED2
USER_IN1
USER_IN2
RUN_KIT_USR
INTERRUPT
MOSI
MISO
XTAL
OSC_MCU
JTCLK
JTRST_B
JTMS_MIC

CS2_BOARD
CS0_RAM
RESET
RESET_OUT
SCK
JDE_B
SS

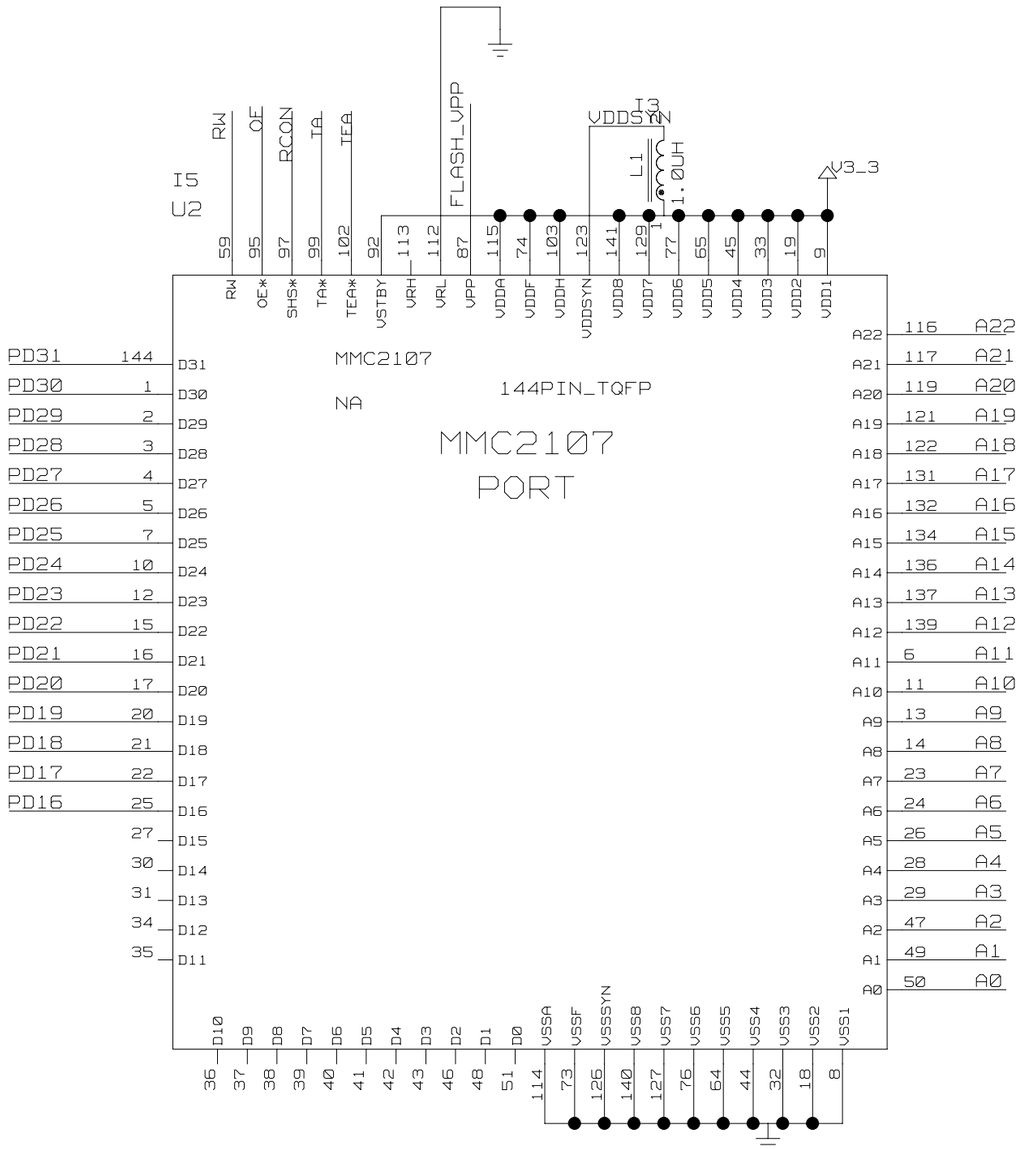
R15
33
2 CLKOUT

OSC_MCU
AXIAL_TH
8.0MHZ
EC1-8.000M
X1
I2
R13
1.0M
C12
10PF
C13
10PF
XTAL
I4
VSSSSYN

V3_3
C24
0.1UF
C15
0.1UF
C29
0.1UF
C14
0.1UF

Fri Mar 18 13:46:06 2005

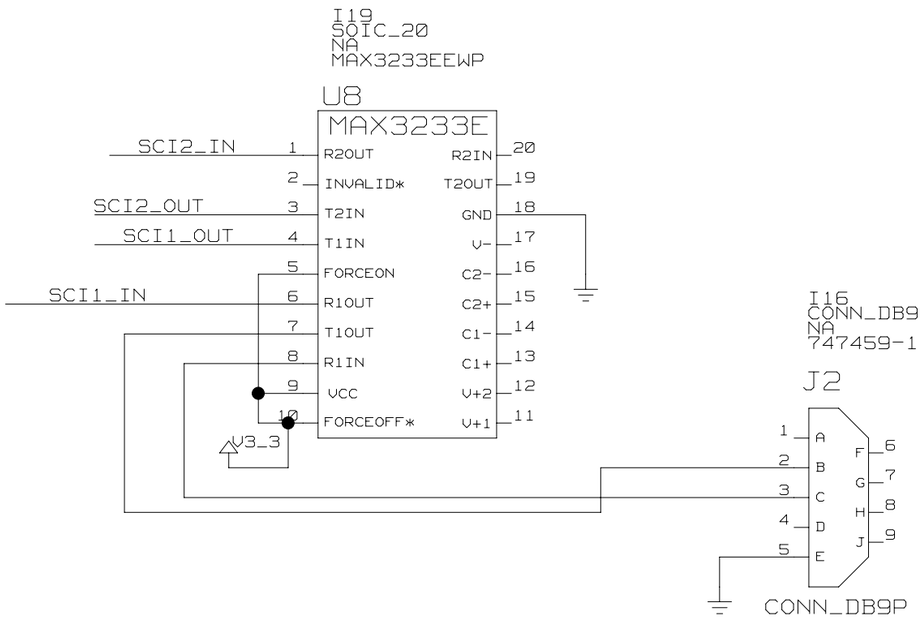
TITLE: Page 11. MICROCONTROLLER BLOCK1	DATE:
ENGINEER: DALLAS SEMICONDUCTOR	PAGE: 11



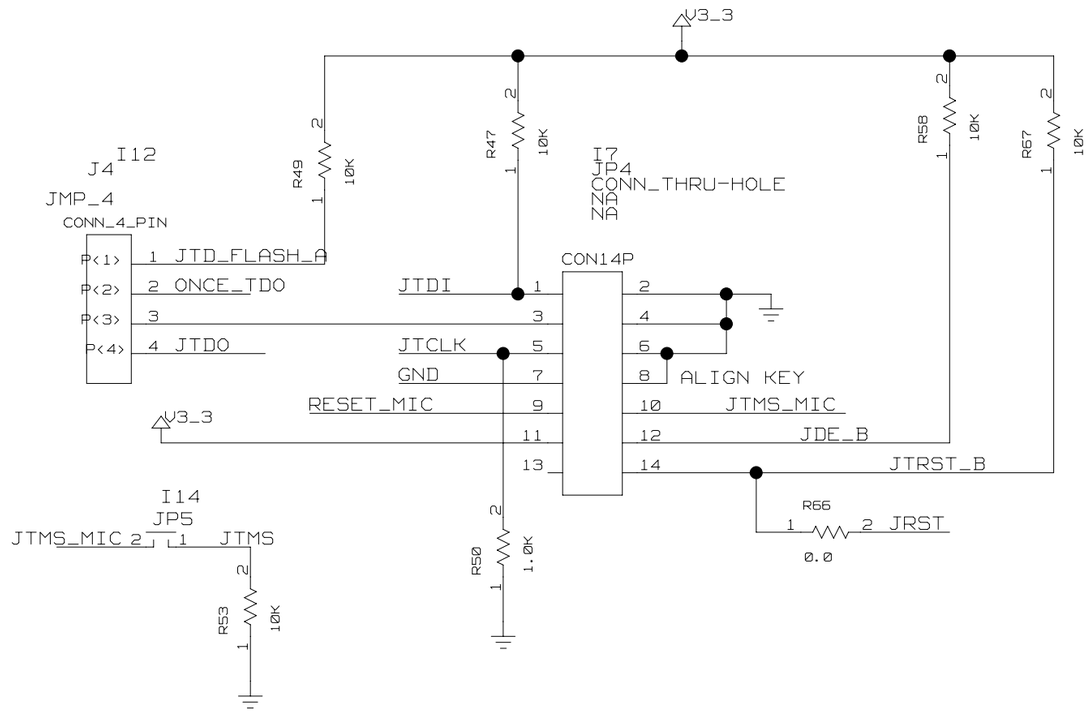
Fri Mar 18 13:46:06 2005

TITLE: Page 12. MICROCONTROLLER BLOCK2	DATE:
ENGINEER: DALLAS SEMICONDUCTOR	PAGE: 12

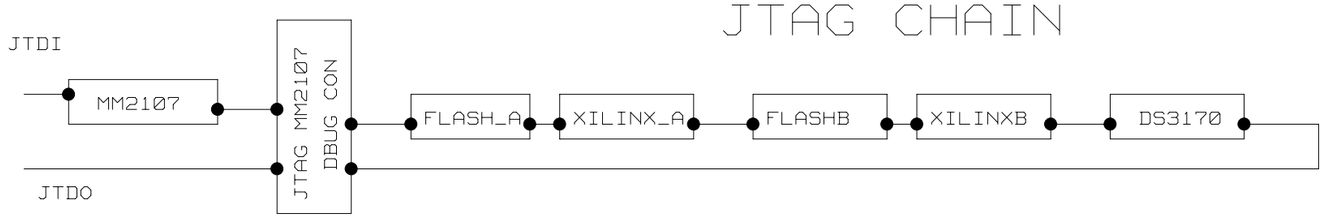
SERIAL INTERFACE



JTAG CON



JTAG CHAIN



Fri Mar 18 13:46:06 2005

TITLE: Page 13. SERIAL/JTAG CONN	DATE:
ENGINEER: DALLAS SEMICONDUCTOR	PAGE: 13

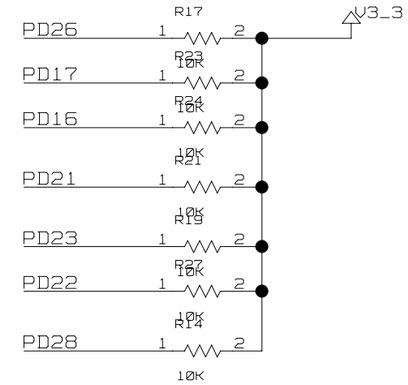
RESET CONFIGURATION

MASTER MODE

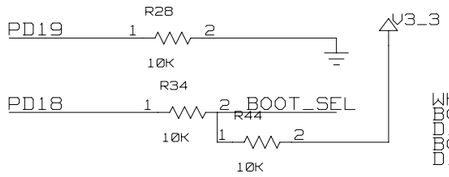
FULL DRIVE

XTAL W/ PLL

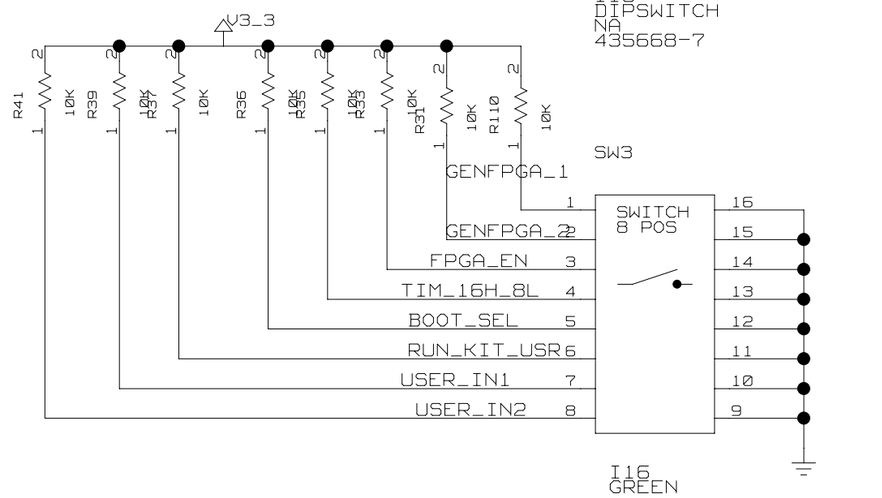
INTERNAL
FLASH ENABLE

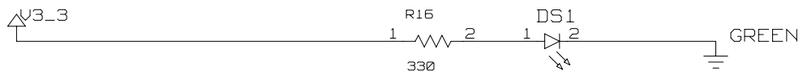


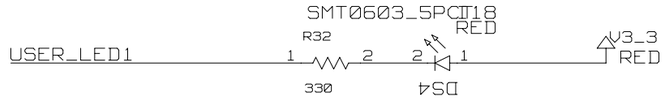
BOOT
INTERN/EXTERN

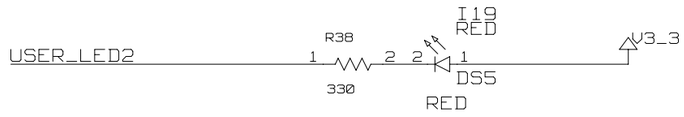


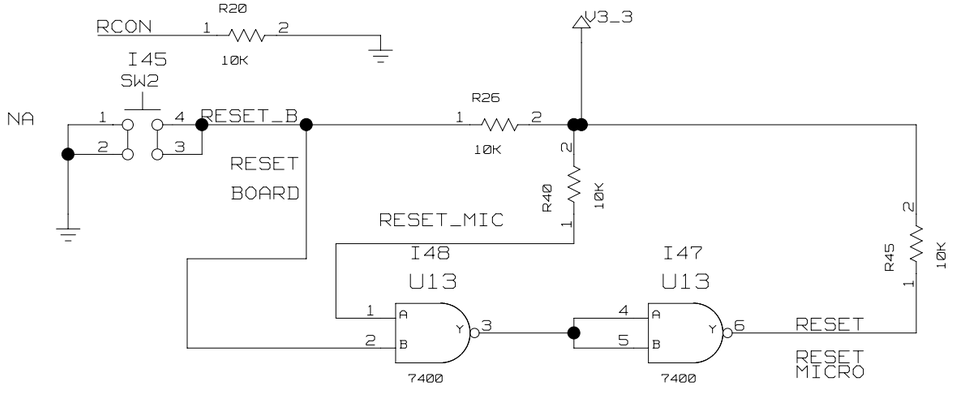
WHEN SET FOR
BOOT INTERNAL
D18 HAS A 10K LOAD TO GND
BOOT EXT
D18 HAS A 10.5K LOAD TO V3V

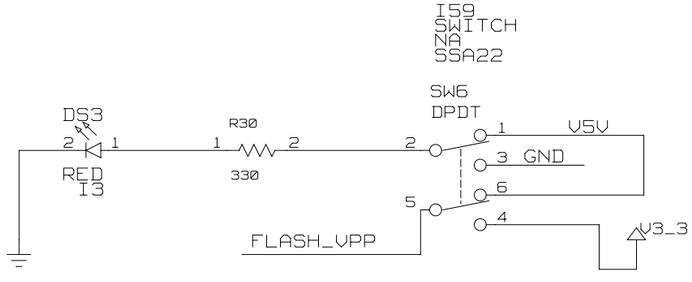


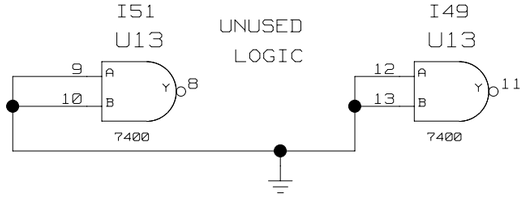


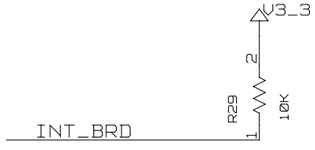












Fri Mar 18 13:46:07 2005

TITLE: Page 14. MISC USER INPUTS	DATE:
ENGINEER: DALLAS SEMICONDUCTOR	PAGE: 14

XILINX A/ FLASH A

I17
MAX1792
NA
MAX1792EUA18

U1
MAX1792

V3_3
V1_8_A

XC2SE_FT256_U

I9
XILINX_PLD
200K
XC2S200E-6FT256C

SPARTAN IIE

I24
TSSOP
2MBIT
XCF02SV020C

U10
XILINX_XCF01S

I5
NA
NC7SZ86

U9
NC7SZ86_U
INVERTER

DS2

TMS	B1	JTMS
TDI	C13	JTD_FLASHA_2_XILINXA
TCK	A2	JTCLK
TDO	B14	JTD_XILINXA_2_FLASHB
PROGRAM*	R16	PROGRAM_A
CCLK	A15	CCLK_A
DONE	T15	DONE_A
M0	T2	
M1	R1	
M2	R3	

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TITLE: Page 15. GP FPGA CONTROL / FLASH	DATE:
ENGINEER: DALLAS SEMICONDUCTOR	PAGE: 15

LOCAL SWAPPED

DATA BUS

LSB

B8 GCK2
A14 IO1_1_18P_YY_CS
A13 IO1_2_18N_YY_WR
B13 IO1_3_17P
C12 IO1_4_17N
B12 INTERUPT
A12 XD15
D12 XD14
E11 XD13
D11 XD12
C11 XD11
B11 XD10
A11 XD9
E10 XD8
D10 XD7
C10 XD6
B10 XD5
A10 XD4
D9 XD3
C9 XD2
B9 XD1
A9 XD0
A8

C8 GCK3
D8 IO0_1_8N_DLL
A7 IO0_2
E7 IO0_3_7P
D7 IO0_4_7N_VREF
C7 IO0_5_6P
B7 IO0_6_6N
A6 IO0_7
B6 IO0_8_5P
C6 IO0_9_5N
A5 IO0_10_4P
B5 IO0_11_4N
D6 IO0_12_3P
E6 IO0_13_3N
D5 IO0_14_2P_YY
C5 IO0_15_2N_YY_VREF
B4 IO0_16_1P_YY
C4 IO0_17_1N_YY
A4 IO0_18_0P_YY
A3 IO0_19_0N_YY
B3 IO0_20

10K R18

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17

ADDRESS BUS FROM MICRO

BANK1

BANK0

I4

XILINX PLD

XC2S200_FT256_U

XC2S200E-6FT256C

U3

SPARTAN IIE

BANK2

H16 IO2_1_30N_YY_IRDY
G16 IO2_2_30P_YY
H14 IO2_3_29N
H15 IO2_4_29P
G15 IO2_5_28ND3
F16 IO2_6_28P_VREF
H13 IO2_7_27N
G14 IO2_8_27P
F15 IO2_9_26N
E16 IO2_10_26P
G13 IO2_11_25N_YY
F14 IO2_12_25P_YYD2
E15 IO2_13_24ND1
D16 IO2_14_24P
F13 IO2_15_23N
E14 IO2_16_23P
D15 IO2_17_22N
C16 IO2_18_22P_VREF
G12 IO2_19_21N
F12 IO2_20_21P
E13 IO2_21_20N
D14 IO2_22_20P
B16 IO2_23_19N_YY_DIN_DO
C15 IO2_24_19P_YY_DOUT_BUSY

IC0C23

EB0 EB1 EB2 EB3 INT_BRD INT_70 RD_DS TA TEA OE WR_W/R RW CS2_BOARD BOOT_SEL ALE MODE WIDTH_70 TEST_70 HIZ_70 RST_70_OUT RST_70 CFG_DIN_A RESET_B

R52 10K

BANK3

P15 RESET_OUT
P16 IO3_1_41N_YY_INIT
N15 IO3_2_41P_YYD7
N16 IO3_3_40N
N14 IO3_4_40P
M14 IO3_5_39N
M15 IO3_6_39P
M16 IO3_7_38N_VREF
M13 IO3_8_38P
L14 IO3_9
L15 IO3_10
L16 IO3_11_36N
L13 IO3_12_36PD6
K14 IO3_13_35N_YYD5
K15 IO3_14_35P_YY
K16 IO3_15_34N
L12 IO3_16_34P
K12 IO3_17_33N
K13 IO3_18_33P
J14 IO3_19_32N_VREF
J15 IO3_20_32PD4
J16 IO3_21_31N
J13 IO3_22_31P
IO3_23_TRDY

A18 A19 A20 A21 A22 PD16 PD17 PD18 PD19 PD20 PD21 PD22 PD23 PD24 PD25 PD26 PD27 PD28 PD29 PD30 PD31

ADDRESS BUS FROM MICRO

DATA BUS FROM MICRO

LSB

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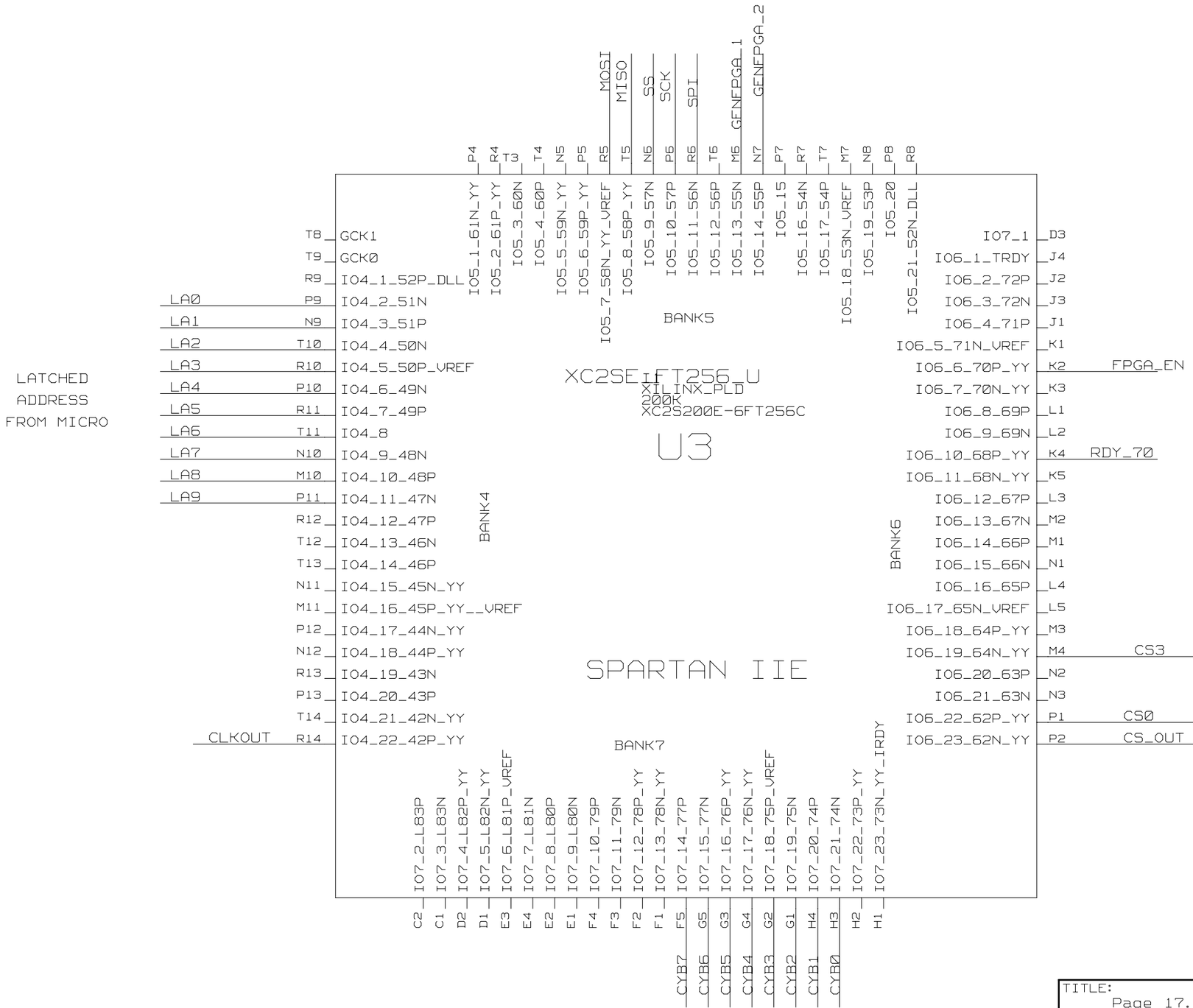
TITLE: Page 16. GP FPGA BLOCK1	DATE:
ENGINEER: DALLAS SEMICONDUCTOR	PAGE: 16


XC2SE_FT256_U
XILINX_PLD
200K
XC2S200E-6FT256C
U3
SPARTAN IIE
BANK5
BANK4
BANK6
BANK7
LATCHED
ADDRESS
FROM MICRO
CLKOUT
FPGA_EN
RDY_70
CS3
CS0
CS_OUT
GCK1
GCK0
IO4_1_52P_DLL
IO4_2_51N
IO4_3_51P
IO4_4_50N
IO4_5_50P_VREF
IO4_6_49N
IO4_7_49P
IO4_8
IO4_9_48N
IO4_10_48P
IO4_11_47N
IO4_12_47P
IO4_13_46N
IO4_14_46P
IO4_15_45N_YY
IO4_16_45P_YY__VREF
IO4_17_44N_YY
IO4_18_44P_YY
IO4_19_43N
IO4_20_43P
IO4_21_42N_YY
IO4_22_42P_YY
IO5_1_61N_YY
IO5_2_61P_YY
IO5_3_60N
IO5_4_60P
IO5_5_59N_YY
IO5_6_59P_YY
IO5_7_58N_YY_VREF
IO5_8_58P_YY
IO5_9_57N
IO5_10_57P
IO5_11_56N
IO5_12_56P
IO5_13_55N
IO5_14_55P
IO5_15
IO5_16_54N
IO5_17_54P
IO5_18_53N_VREF
IO5_19_53P
IO5_20
IO5_21_52N_DLL
IO6_1_TRDY
IO6_2_72P
IO6_3_72N
IO6_4_71P
IO6_5_71N_VREF
IO6_6_70P_YY
IO6_7_70N_YY
IO6_8_69P
IO6_9_69N
IO6_10_68P_YY
IO6_11_68N_YY
IO6_12_67P
IO6_13_67N
IO6_14_66P
IO6_15_66N
IO6_16_65P
IO6_17_65N_VREF
IO6_18_64P_YY
IO6_19_64N_YY
IO6_20_63P
IO6_21_63N
IO6_22_62P_YY
IO6_23_62N_YY
IO7_1
IO7_2_L83P
IO7_3_L83N
IO7_4_L82P_YY
IO7_5_L82N_YY
IO7_6_L81P_VREF
IO7_7_L81N
IO7_8_L80P
IO7_9_L80N
IO7_10_79P
IO7_11_79N
IO7_12_78P_YY
IO7_13_78N_YY
IO7_14_77P
IO7_15_77N
IO7_16_76P_YY
IO7_17_76N_YY
IO7_18_75P_VREF
IO7_19_75N
IO7_20_74P
IO7_21_74N
IO7_22_73P_YY
IO7_23_73N_YY_IRDY
MOSI
MISO
SS
SCK
SPI
GENFPGA_1
GENFPGA_2
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TITLE:
Page 17. GP FPGA BLOCK2
DATE:
ENGINEER:
DALLAS SEMICONDUCTOR
PAGE:
17

MISC HEADERS

I18
J3
0L_THROUGH HOLE
NA
TSW-125-07-T-D

LA0	1	1	2	2	XD0
LA1	3	3	4	4	XD1
LA2	5	5	6	6	XD2
LA3	7	7	8	8	XD3
LA4	9	9	10	10	XD4
LA5	11	11	12	12	XD5
LA6	13	13	14	14	XD6
LA7	15	15	16	16	XD7
LA8	17	17	18	18	XD8
LA9	19	19	20	20	XD9
CS3170	21	21	22	22	XD10
CS3	23	23	24	24	XD11
INT_70	25	25	26	26	XD12
RST_70_OUT	27	27	28	28	XD13
RDY_70	29	29	30	30	XD14
CYB0	31	31	32	32	XD15
CYB1	33	33	34	34	SPI
CYB2	35	35	36	36	ALE
CYB3	37	37	38	38	RD_DS
CYB4	39	39	40	40	WR_W/R
CYB5	41	41	42	42	CS_OUT
CYB6	43	43	44	44	MODE
CYB7	45	45	46	46	WIDTH_70
GND	47	47	48	48	TEST_70
GND	49	49	50	50	HIZ_70

I8
CS3170 — CS0

V3_3
I10
DS10
R65
I12
DS9
330
I1
U15
7404
MODE
I3
R64
330
WIDTH_70
I13
DS7
R60
330
I2
TEST_70
I14
DS8
R61
330
I4
HIZ_70
I16
I17

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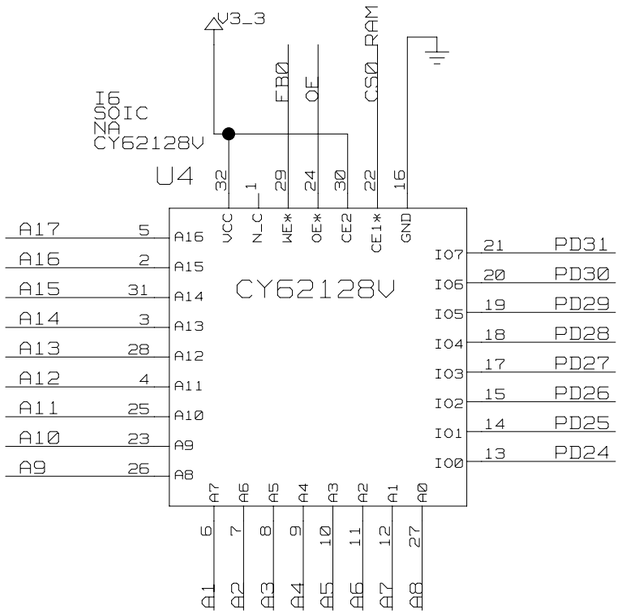
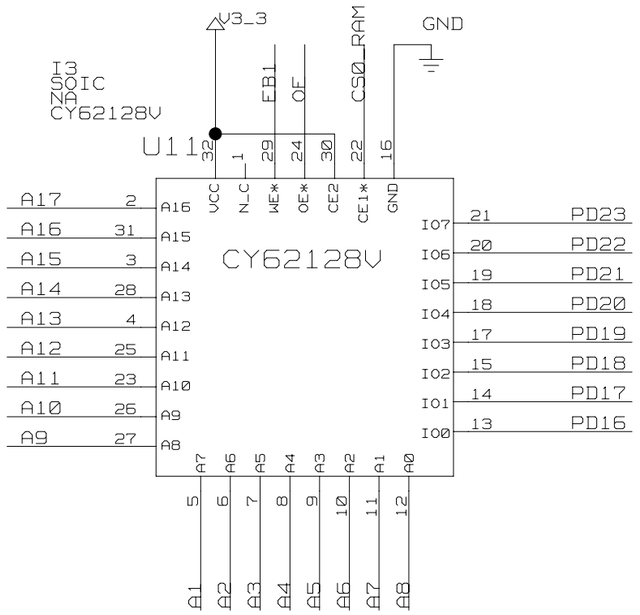
TITLE: Page 18. ADDRESS/DATA HEADERS	DATE:
ENGINEER: DALLAS SEMICONDUCTOR	PAGE: 18





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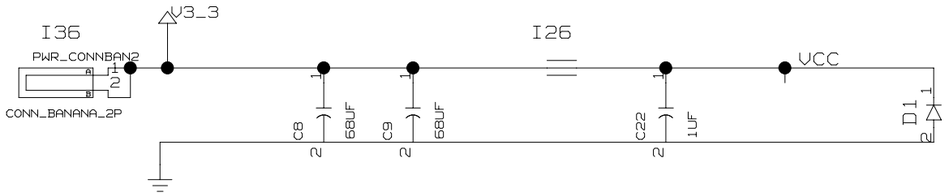
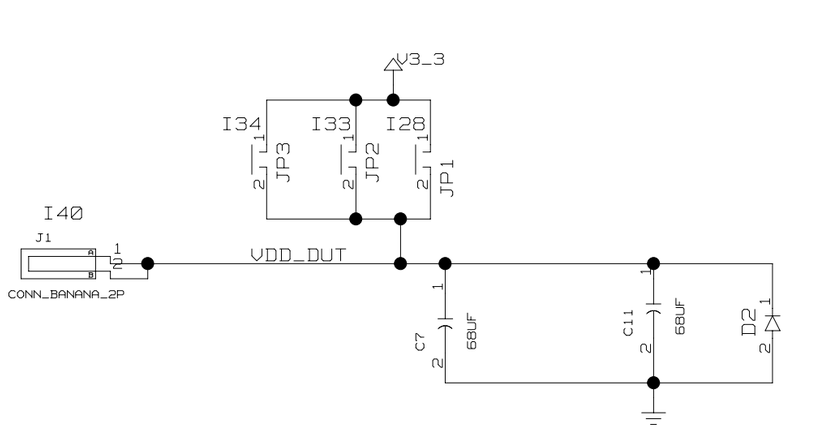
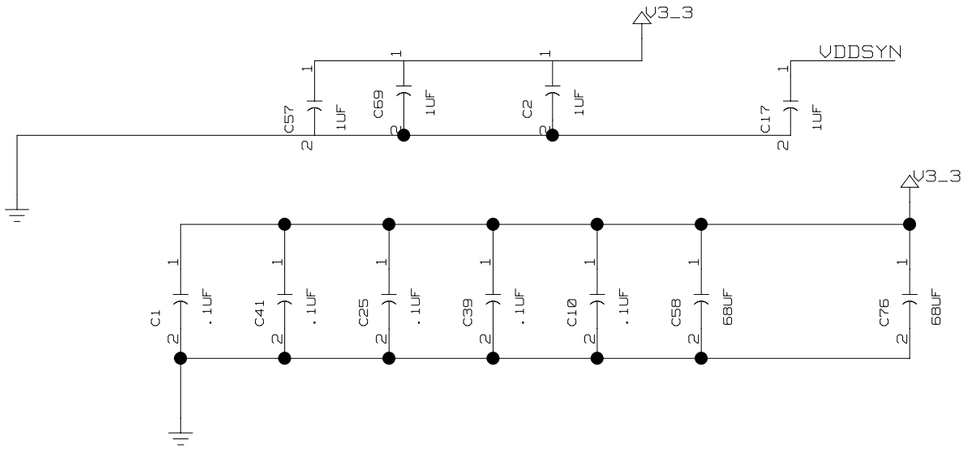
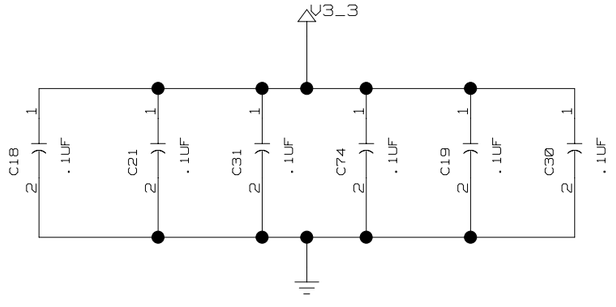
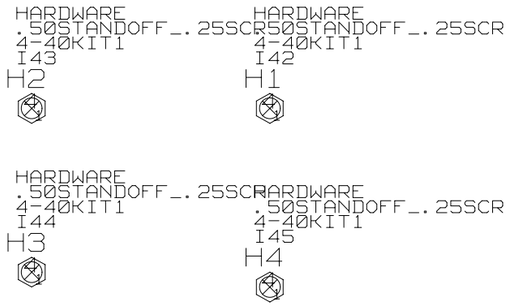
TITLE: Page 19. MICROCONTROLOR SRAM	DATE:
ENGINEER:	PAGE: 19











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TITLE: Page 20. POWER CONN	DATE:
ENGINEER: DALLAS SEMICONDUCTOR	PAGE: 20

DESIGN NOTES:

1. 1/20/05 DESIGN / LAYOUT COMPLETED AND ARCHIEVED

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TITLE: Page 21. NOTES	DATE:
ENGINEER: DALLAS SEMICONDUCTOR	PAGE: 21

*** Signal Cross-Reference for the entire design ***

A0	12A4<> 16C7<>
A1	12A4<> 16C7<> 19A3<> 19A7<>
A2	12A4<> 16C7<> 19A3<> 19A7<>
A3	12A4<> 16C7<> 19A3<> 19A7<>
A4	12A4<> 16C7<> 19A3<> 19A6<>
A5	12A4<> 16C7<> 19A3<> 19A6<>
A6	12A4<> 16B7<> 19A3<> 19A6<>
A7	12B4<> 16B7<> 19A3<> 19A6<>
A8	12B4<> 16B7<> 19A3<> 19A6<>
A9	12B4<> 16B7<> 19B4<> 19B7<>
A10	12B4<> 16B7<> 19B4<> 19B7<>
A11	12B4<> 16B7<> 19B4<> 19B7<>
A12	12B4<> 16B7<> 19B4<> 19B7<>
A13	12B4<> 16B7<> 19B4<> 19B7<>
A14	12B4<> 16B7<> 19B4<> 19B7<>
A15	12B4<> 16B7<> 19B4<> 19B7<>
A16	12B4<> 16B7<> 19B4<> 19B7<>
A17	12B4<> 16B7<> 19B4<> 19B7<>
A18	12B4<> 16A6<>
A19	12C4<> 16A6<>
A20	12C4<> 16A6<>
A21	12C4<> 16A6<>
A22	12C4<> 16A6<>
ALE	9C2<> 16B2<> 18B6<> 2D6<
BNC50_OHM	7B7<>
BOOT_SEL	14C3<> 16B2<> 14B6<
BUF_E3	7C5<> 7C6<> 9A5<> 7C2<
BUF_ST51	7B5<> 7C6<> 10D4<> 7C1<
BUF_T3	7C5<> 7C6<> 10A4<> 7C2<
CCLK_A	15A8<> 15B1<
CCLK_B	8A8<> 8B1<
CFG_DIN_A	15A8<> 16A2<>
CFG_DIN_B	8A8<> 9A2<>
CLKO	2D4> 7A8<
CLKOUT	17A7<> 11B4<
CS0	17A2<> 18C4>
CS0_RAM	11B5<> 19C3<> 19C6<>
CS2_BOARD	11B5<> 16B2<>
CS3	9C2<> 17B2<> 18B8<>
CS3170	18B8<> 2D6< 18C5<
CS_OUT	17A2<> 18B6<>
CYB0	9B2<> 17A4<> 18B8<>
CYB1	9B2<> 17A4<> 18B8<>
CYB2	9B2<> 17A4<> 18B8<>
CYB3	9B2<> 17A4<> 18B8<>
CYB4	9B2<> 17A4<> 18B8<>
CYB5	9A2<> 17A5<> 18B8<>
CYB6	9A2<> 17A5<> 18A8<>
CYB7	9A2<> 17A5<> 18A8<>
DONE_A	15A2<> 15A8<> 15B1<
DONE_B	8A2<> 8A8<> 8B2<
EB0	11C7<> 16C2<> 19C7<>
EB1	11C7<> 16C2<> 19C3<>
EB2	11C7<> 16C2<>
EB3	11C7<> 16C2<>
FLASH_VPP	14A3<> 12D5<
FPGA_EN	14D3<> 17C3<>
GENFPGA_1	14D3<> 17D4<>
GENFPGA_2	14D3<> 17D4<>
GPIO_1	2A4<> 5A6<> 5C2<> 5C8<
GPIO_2	2A4<> 5A5<> 5C2<> 5B8<
GPIO_3	2A4<> 5A6<> 5B2<> 5B8<
GPIO_4	2A4<> 5A5<> 5B2<> 5A8<
GPIO_5	2A4<> 5A6<> 5B2<> 5A8<
GPIO_6	2A4<> 5A2<> 5A5<> 5B2<> 5A8<
GPIO_7	2A4<> 5A6<> 5B2<> 5C6<
GPIO_8	2A4<> 5A2<> 5A5<> 5B2<> 5B6<
HIZ_70	16B2<> 18A6<> 2A3< 18B2<
ICOC23	11C8<> 16C2<>
INTERUPT	11A7<> 16D6<>
INT_70	2A6<> 16C2<> 18B8<> 5C8<
INT_BRD	9A7<> 16C2<> 14A6<
JDE_B	11B5<> 13C2<>
JRST	2D5< 13B1<
JTCLK	8A8<> 11A6<> 13C3<> 15A8<> 2D5< 8C2< 15B1<
JTDI	11C6<> 13C3<>
JTDO	2D5<> 13C4<
JTD_FLASHA_2_XILINXA	15A6<> 15C1<
JTD_FLASHB_2_XILINXB	8A6<> 8C2<
JTD_FLASH_A	15A8<> 13C4<
JTD_XILINXA_2_FLASHB	8A8<> 15B1>
JTD_XILINXB_2_DS3170	8B2> 2D5<
JTMS	8A8<> 8C2<> 13B4<> 15A8<> 15C1<> 2D5<
JTMS_MIC	11A6<> 13B4<> 13C2<>
JTRST_B	11A6<> 13B2<>
LA0	9C7<> 17C7<> 18C8<> 2C7<
LA1	9C7<> 17C7<> 18C8<> 2C7<
LA2	9C7<> 17C7<> 18C8<> 2C7<
LA3	9B7<> 17C7<> 18C8<> 2C7<
LA4	9B7<> 17C7<> 18C8<> 2C7<
LA5	9B7<> 17C7<> 18C8<> 2C7<
LA6	9B7<> 17C7<> 18C8<> 2C7<
LA7	9B7<> 17B7<> 18C8<> 2C7<
LA8	9B7<> 17B7<> 18C8<> 2C7<
LA9	9B7<> 17B7<> 18B8<>
MISO	11A6<> 17D5<>
MODE	9B2<> 16B2<> 18A6<> 2A6< 18B3<
MOSI	11A6<> 17D5<>
OE	12D6<> 16B2<> 19C3<> 19C6<>
ONCE_TDO	11C6<> 13C4<
OSCE3	7C6<> 7C7<
OSCSTS1	7B6<> 7B6<
OSCT3	7C6<> 7C7<
OSC_MCU	11A6<> 11C2<
PD16	12A7<> 16A5<> 19B2<> 14D7<
PD17	12B7<> 16A5<> 19B2<> 14D7<
PD18	12B7<> 16A5<> 19B2<> 14B7<
PD19	12B7<> 16A5<> 19B2<> 14C7<
PD20	12B7<> 16A5<> 19B2<>
PD21	12B7<> 16A5<> 19B2<> 14C7<
PD22	12B7<> 16A5<> 19B2<> 14C7<
PD23	12B7<> 16A5<> 19B2<> 14C7<
PD24	12B7<> 16A5<> 19B5<>
PD25	12B7<> 16A5<> 19B5<>
PD26	12B7<> 16A4<> 19B5<> 14D7<
PD27	12B7<> 16A4<> 19B5<>
PD28	12B7<> 16A4<> 19B5<> 14C7<
PD29	12C7<> 16A4<> 19B5<>
PD30	12C7<> 16A4<> 19B5<>
PD31	12C7<> 16A4<> 19B5<>
PROGRAM_A	15A8<> 15B1<
PROGRAM_B	8A8<> 8B1<
RCLKO70	2A2> 4A7<
RCLKO_FPGA	4A6<> 9D6<
RCON	12D6<> 14B8<
RDY_70	2A6<> 17B3<> 18B8<>
RD_DS	9B2<> 16C2<> 18B6<> 2D6<
REFCLK70	7C4<> 2D4<
REFCLK_OUTPUT	7C3<> 9A4<>
RESET	11B5<> 14A5<>
RESET_B	8A8<> 9A2<> 9B2<> 14B7<> 15A8<> 16A2<>
RESET_MIC	13C3<> 14A7<
RESET_OUT	11B5<> 16A6<>
RLCLK70	4C7<> 2C2< 10C8<
RNEG_70	4A3<> 9D6<> 2C2<
ROH70	2B2> 6C5<
ROHCLK70	2B2> 6C5<
ROHCLK_I_3	6C4<> 10D5<>
ROHSOF70	2B2> 6C5<
ROHSOF_I_3	6C4<> 9C2<>
ROH_I_3	6C4<> 10B2<>
RPOS_70	4B3<> 9B7<> 2C2<
RSER70	2A2> 6B5<
RSER_I_3	6B4<> 10A6<>
RSOFO70	2A2> 6B5<
RSOFO_I_3	6B4<> 10B8<>
RST_70	5D8<> 16A2<>
RST_70_OUT	16B2<> 18B8<> 2A3<
RUN_KIT_USR	11A7<> 14C3<>
RW	12D6<> 16B2<>
RXN_70	2C2< 3A4<
RXP_70	2C2< 3A4<
SCI1_IN	11B8<> 13C8>
SCI1_OUT	11B8<> 13C8<
SCI2_IN	11B8<> 13C8>
SCI2_OUT	11B8<> 13C8<
SCK	11B5<> 17D5<>
SPI	17D5<> 18B6<> 2A6<
SS	11B5<> 17D5<>
TA	12D6<> 16C2<>
TCLKI70	4B7<> 9D4<> 2B2<
TCLKO70	2B2> 4A7<
TCLKO_FPGA	4A6<> 9C7<>
TEA	12D6<> 16B2<>
TEST	11B8<>
TEST_70	16B2<> 18A6<> 2A3< 18B2<
TIM_16H_8L	11C7<> 14C3<>
TLCLK70	2C2> 4C7<
TLCLK_FPGA	4B6<> 10C8<>
TNEG_70	2C2> 4B4<
TNEG_I_3	4B3<> 9D6<>
TOH70	6C7<> 2B2<
TOHCLK70	2B2> 6B7<
TOHCLK_I_3	6B6<> 10D6<>
TOHEN70	6C7<> 2B2<
TOHEN_O_3	10C2<> 6C6<
TOHSOF70	2B2> 6B7<
TOHSOF_I_3	6B6<> 9B2<>
TOH_O_3	10B2<> 6C6<
TPOS_70	2C2> 4C4<
TPOS_I_3	4C3<> 9A7<>
TSER70	6A7<> 2B2<
TSER_O_3	10A6<> 6A6<
TSOFI70	6C7<> 2B2<
TSOFI_O_3	10B8<> 6C6<
TSOFO70	2A2> 6A7<
TSOFO_I_3	6A6<> 10D4<>
TXN_70	2C3> 3C4<
TXP_70	2C3> 3C4<
USER_IN1	11A7<> 14C3<>
USER_IN2	11A7<> 14C3<>
USER_LED1	11A7<> 14B3<
USER_LED2	11A7<> 14B3<
V1_8_A	15D6<> 15D4<
V1_8_C	8D7<> 8D4<
V5V	14A2<> 20D5<>
VDDSYN	12C5<> 20C2<
VDD_DUT	20B7<> 2B2< 2B8< 2C8< 2D5<
VSSSSYN	11C2<
WIDTH_70	16B2<> 18A6<> 2A6< 18B2<
WR_W/R	9C2<> 16B2<> 18B6<> 2D6<
XD0	2C7<> 9D5<> 16D4<> 18C6<>
XD1	2B7<> 9D5<> 16D4<> 18C6<>
XD2	2B7<> 9D5<> 16D4<> 18C6<>
XD3	2B7<> 9D5<> 16D4<> 18C6<>
XD4	2B7<> 9D5<> 16D4<> 18C6<>
XD5	2B7<> 9D5<> 16D5<> 18C6<>
XD6	2B7<> 9D5<> 16D5<> 18C6<>
XD7	2B7<> 9D5<> 16D5<> 18C6<>
XD8	2B7<> 16D5<> 18C6<>
XD9	2B7<> 16D5<> 18B6<>
XD10	2B7<> 16D5<> 18B6<>
XD11	2B7<> 16D5<> 18B6<>
XD12	2B7<> 16D5<> 18B6<>
XD13	2A7<> 16D5<> 18B6<>
XD14	2A7<> 16D5<> 18B6<>
XD15	2A7<> 16D6<> 18B6<>
XTAL	11A6<> 11C2<

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*** Part Cross-Reference for the entire design ***

C1	CAP1	20B4
C2	CAP1	20C3
C3	CAP1	15C8
C4	CAP1	2C8
C5	CAP1	2B2
C6	CAP1	2B1
C7	CAP1	20B7
C8	CAP1	20C7
C9	CAP1	20C6
C10	CAP1	20B3
C11	CAP1	20B6
C12	CAP	11C4
C13	CAP	11C3
C14	CAP1	11A4
C15	CAP1	11A5
C16	CAP1	2C8
C17	CAP1	20C2
C18	CAP1	20A4
C19	CAP1	20A3
C20	CAP1	15D6
C21	CAP1	20A4
C22	CAP1	20C6
C23	CAP1	15D7
C24	CAP1	11A5
C25	CAP1	20B4
C26	CAP1	15A6
C27	CAP1	15A6
C28	CAP1	15A6
C29	CAP1	11A4
C30	CAP1	20A3
C31	CAP1	20A4
C32	CAP1	15A7
C33	CAP1	15D6
C34	CAP1	15D6
C35	CAP	20D4
C36	CAP1	20D5
C37	CAP1	20D5
C38	CAP1	7B2
C39	CAP1	20B3
C40	CAP1	8C8
C41	CAP1	20B4
C42	CAP1	8D6
C43	CAP1	8D6
C44	CAP1	8B8
C45	CAP1	8B8
C46	CAP1	8B7
C47	CAP1	8B7
C48	CAP1	8D7
C49	CAP1	8D6
C50	CAP1	7B3
C51	CAP1	2B8
C52	CAP1	7B5
C53	CAP1	7B5
C54	CAP1	7B3
C55	CAP1	7A3
C56	CAP1	7B4
C57	CAP1	20C4
C58	CAP1	20B3
C59	CAP1	7B3
C60	CAP1	7A3
C61	CAP1	7B4
C62	CAP1	2B8
C63	CAP1	2C7
C64	CAP1	2B1
C65	CAP1	2C8
C66	CAP1	2B8
C67	CAP1	2B7
C68	CAP1	7A3
C69	CAP1	20C4
C70	CAP1	7A3
C71	CAP1	3B5
C72	CAP1	3A5
C73	CAP1	7A2
C74	CAP1	20A3
C75	CAP1	2B2
C76	CAP1	20B2
D1	DIODE	20C5
D2	DIODE	20B5
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DS2	LED	15A1
DS3	LED	14A3
DS4	LED	14B2
DS5	LED	14B2
DS6	LED	8A1
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DS8	LED	18B5
DS9	LED	18B4
DS10	LED	18B5
DS11	LED	5C7
DS12	LED	5B7
DS13	LED	5B7
DS14	LED	5B7
DS15	LED	5C7
DS16	LED	5A7
DS17	LED	5A7
DS18	LED	5C5
DS19	LED	5B5
H1	4_40_HDWR_U	20D2
H2	4_40_HDWR_U	20D3
H3	4_40_HDWR_U	20C3
H4	4_40_HDWR_U	20C2
J1	CONN_BANANA_2P	20B8
J2	CONN_DB9P	13B6
J3	CONN_50P2	18D7
J4	CONN_4_PIN	13C4
J5	CONN_BNC_5P	7B7
J6	CONN_10P	7D6
J7	CONN_10P	5A5
J8	CONN_BNC_5P	3A6
J9	CONN_BNC_5P	3C6
JP1	JMP	20B6
JP2	JMP	20B7
JP3	JMP	20B7
JP4	CON14P	13C3
JP5	JMP	13B4
JP6	JMP3	5A2
JP7	JMP	3A6
JP8	JMP	3C6
L1	COIL_2P	12C5
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PWR_CONNBAN2	CONN_BANANA_2P	20C8
R1	RES1	7D2
R2	RES1	7C2
R3	RES1	4B4
R4	RES1	4A4
R5	RES1	4C3
R6	RES1	6B4
R7	RES1	6B6
R8	RES1	4A7
R9	RES1	3A4
R10	RES1	7A7
R11	RES1	3C4
R12	RES1	7C4
R13	RES1	11C2
R14	RES1	14C6
R15	RES1	11B5
R16	RES1	14C2
R17	RES1	14D6
R18	RES1	16C7
R19	RES1	14C6
R20	RES1	14B7
R21	RES1	14C6
R22	RES1	15A1
R23	RES1	14D6
R24	RES1	14D6
R25	RES1	5D7
R26	RES1	14B6
R27	RES1	14C6
R28	RES1	14C6
R29	RES1	14A5
R30	RES1	14A3
R31	RES1	14D3
R32	RES1	14B2
R33	RES1	14D3
R34	RES1	14B6
R35	RES1	14D3
R36	RES1	14D3
R37	RES1	14D4
R38	RES1	14B2
R39	RES1	14D4
R40	RES1	14A6
R41	RES1	14D4
R42	RES1	4B7
R43	RES1	4A7
R44	RES1	14B6
R45	RES1	14A5
R46	RES1	8A2
R47	RES1	13C3
R48	RES1	2A7
R49	RES1	13C3
R50	RES1	13B3
R51	RES1	6A6
R52	RES1	16C1
R53	RES1	13B4
R54	RES1	7C1
R55	RES1	7C2
R56	RES1	7C1
R57	RES1	6C6
R58	RES1	13C1
R59	RES1	7C2
R60	RES1	18B4
R61	RES1	18B4
R62	RES1	6C6
R63	RES1	4B6
R64	RES1	18B4
R65	RES1	18B4
R66	RES1	13B2
R67	RES1	13C1
R68	RES1	4C6
R69	RES1	7C1
R70	RES1	7C1
R71	RES1	6C6
R72	RES1	5C7
R73	RES1	4C7
R74	RES1	4C7
R75	RES1	5B2
R76	RES1	5B2
R77	RES1	5C7
R78	RES1	5B7
R79	RES1	5B7
R80	RES1	5A7
R81	RES1	7B7
R82	RES1	5B2
R83	RES1	4B4
R84	RES1	7B7
R85	RES1	6C5
R86	RES1	5B3
R87	RES1	5C3
R88	RES1	7C4
R89	RES1	5B5
R90	RES1	5C5
R91	RES1	5A7
R92	RES1	6B6
R93	RES1	4A4
R94	RES1	4C3
R95	RES1	6C5
R96	RES1	5A7
R97	RES1	7C5
R98	RES1	5C2
R99	RES1	5C2
R100	RES1	4A7
R101	RES1	6A6
R102	RES1	5C2
R103	RES1	4C7
R104	RES1	6C4
R105	RES1	7D7
R106	RES1	6B4
R107	RES1	7C4
R108	RES1	5A4
R109	RES1	7C7
R110	RES1	14D2
SW1	PUSHBUTTON	5D8
SW2	PUSHBUTTON	14B8
SW3	SWITCH_8POS	14D2
SW4	SWITCH_8POS	5C1
SW5	PUSHBUTTON	5A4
SW6	SWITCH_DPDT_SLIDE_6P	14A2
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T2	TRANSFORMER_PULSE	3C5
TP1	TESTPOINT1	20D4
TP2	TESTPOINT1	4C3
TP3	TESTPOINT1	4B3
TP4	TESTPOINT1	4A6
TP5	TESTPOINT1	4B7
TP6	TESTPOINT1	4A6
TP7	TESTPOINT1	4C3
TP8	TESTPOINT1	4A3
TP9	TESTPOINT1	6B4
TP10	TESTPOINT1	6B6
TP11	TESTPOINT1	6A7
TP12	TESTPOINT1	6C4
TP13	TESTPOINT1	6C7
TP14	TESTPOINT1	6C7
TP15	TESTPOINT1	6D4
TP16	TESTPOINT1	6B5
TP17	TESTPOINT1	6C4
TP18	TESTPOINT1	6A6
TP19	TESTPOINT1	4D7
TP20	TESTPOINT1	4C6
TP21	TESTPOINT1	6C7
TP22	TESTPOINT1	6B4
TP23	TESTPOINT1	7D5
TP24	TESTPOINT1	7A7
U1	MAX1792	15D8
U2	MMC2107	11C7 12C6
U3	XC2SE_FT256_U	15C4 16C5 17B5
U4	CY62128V	19B7
U5	MAX1792	8D8
U6	XC2SE_FT256_U	8C4 9B5 10C5
U7	DS3170_BGA_U	2C5
U8	MAX3233E	13C7
U9	NC7SZ86_U	15A2
U10	XILINX_XCF01S	15B7
U11	CY62128V	19B4
U12	XILINX_XCF01S	8A7
U13	74_00	14A6 14A7 14A8
U14	NC7SZ86_U	8A2
U15	74_04	18A4 18B3 18C3
U16	NC7SZ86_U	7B5
U17	NC7SZ86_U	7C5
U18	NC7SZ86_U	4C7
U19	NC7SZ86_U	7C5
U20	NC7SZ86_U	7C3
U21	74_04	5A7 5B8 5D2 5D3
U22	MAX6816	5A3
U23	NC7SZ86_U	7C5
U24	74_04	5A7 5B5 5B8 5C5 5C8
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Y2	OSC2	7D8
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