

TPS65167EVM-277

The TPS65167EVM-277 evaluation module operates from a 8-V to 14-V input rail and provides the three bias-supply voltages and two logic-supply voltages that are required for television and monitor TFT-LCD panels. The TPS65167EVM-277 has one boost converter with an integrated low-side FET, one negative charge-pump controller requiring external Schottky diodes, and one fully integrated positive charge pump for TFT-LCD bias supply. External passive components to support the boost converter include disconnect transistor, rectifying diode, inductors and capacitors. External components for the charge pumps include capacitors. One nonsynchronous buck converter with external Schottky diode and LDO controller requiring external pass transistor make up the two logic supplies.

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1 Introduction

This section contains background information for the TPS65167EVM-277 evaluation module (EVM).

1.1 Specification

Table 1 provides a summary of the TPS65167EVM-277 performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1. Performance Specification Summary

Specification	Voltage Range (V)			Current Range (mA)		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
VIN	6	12	14		1500	
Vs	14.7	15	15.3			1000
VGL	-5.15	-5	-4.85			50
VGH	23.0	23.8 ⁽¹⁾	24.5			50
Vlogic		3.3				2500
Vaux		1.8				500

⁽¹⁾ Assumes that SUP = Vs.

1.2 Modifications

The primary goal of this EVM is to facilitate user evaluation of the TPS65167 in a power-supply application for a typical large TFT display. To facilitate user customization of the EVM, the board was designed with devices having 0805 or larger footprints. A production-optimized implementation would likely occupy less total board space.

1.2.1 Customizing Power Supply

The user can change each rail's regulated output voltage by changing the appropriate feedback resistors per the device data sheet ([SLVS760](#)). The user is responsible for not exceeding each output's maximum voltage specifications. In addition, alternate capacitors, inductors and/or diodes can be used. When using alternate capacitors, ensure that at least the minimum recommended capacitance per the data sheet is used, and that the capacitor voltage rating is appropriate for the application. The switching converters are designed to be used with ceramic output capacitors. Using nonceramic output capacitors with significantly large equivalent series resistances (ESR) can result in larger output ripple or unstable operation of the inductive switching converters. Each charge pump's flying and output capacitors must be ceramic capacitors. When selecting an alternate inductor, use the data-sheet design equations to ensure that an appropriate inductance value is selected, and that the inductor current rating is appropriate for the desired output current. Using an inductor with larger dc resistance results in lower efficiency. When using alternate diodes, ensure that the diode is rated for both the expected peak current and expected power per the data-sheet design equations.

The user can change the delay time between Vin and EN signal with C30. When Vin exceeds the undervoltage lockout threshold, the Vlogic and Vaux start up, and C30 begins to charge after delay to EN goes high and boost converter Vs starts. If EN is connected to REGOUT, then there is no delay.

Using capacitor C22 on GDLY pin 25, the delay time between Vs reaching normal value and VGH going active with CTRL = high can be adjusted also.

1.2.2 Input to Output Isolation

The nonsynchronous boost converter has a path from input to output, VIN to Vs, through external switching diode D3. Transistor Q2 acts as an isolation switch for this path once the device is turned off.

2 Setup and Test Results

This section explains the input, output, and jumper connections of the TPS65167EVM-277. It also describes how to set up test equipment for evaluating the EVM and provides test results.

2.1 Connections and Jumpers

The DEFAULT jumper settings are required for the EVM to operate within the specifications of [Table 1](#).

Table 2. Default Jumper Settings

Jumper	Default Setting
JP1 – LDO INPUT	VLOGIC
JP2 – HVS	GND
JP3 – EN	REGOUT
JP4 – CTRL	REGOUT

J1-VAUX/GND:	Output voltage for LDO and ground return connection
J2-VIN/GND:	Input power supply and ground connection, Vin range 6 V to 14 V
J3-VLOGIC/GND:	Output voltage for 3.3-V buck converter and ground return connection
J4-VGL/GND:	Output voltage for negative charge pump and ground return connection
J5-VGH/GND:	Output connection for the internal high-voltage switch and ground return connection
J6-POUT/GND:	Output voltage of the positive charge pump, internally connected to the high-voltage switch and ground return
J7-Vs/GND:	Output connection for the main boost converter and ground return connection
J8-TEMP/GND:	Output of internal temperature sensor voltage is proportional to the chip temperature and ground return
JP2-HVS:	When the HVS pin is connected to VIN, high-voltage stress test is enabled (Vs goes high, and VGH goes to a fixed 30 V). When the HVS pin is connected to GND, the high-voltage stress test is disabled.
JP3-EN:	When connected to GND, unit is OFF; when connected to REGOUT, unit turns on with no delay between Vin and Vs. When connected to C30 position, unit turns on with a delay between Vin and Vs set by C30.
JP4-CTRL:	Gate voltage shaping function; connect to REGOUT if not used.

2.2 Recommended Test Setup

Before turning on the power supply, ensure that jumpers JP2--JP4 are in their default positions.

Connect a power supply rated at 3 A or more to provide 6 V to 14 V to J2. Do not exceed 14 V on J2. In order to avoid voltage drop through the input power supply line, connect heavy gauge, twisted-pair wire to J2. The output voltages can be monitored by voltmeters and/or an oscilloscope with standard high-impedance voltage probes.

The output voltages reach their respective regulation voltages per [Table 1](#) after the appropriate soft-start times and relative delays. Resistive or electronic loads can be attached to output J1 for Vaux, J3 for Vlogic, and J7 for Vs. Only resistive loads can be attached to outputs J4 for VGL and J5 for VGH. Exceeding an output load specified in [Table 1](#) results in the output voltage falling out of regulation.

2.3 Test Results

Test results using the TPS65167EVM-277 are shown in [Figure 1](#).

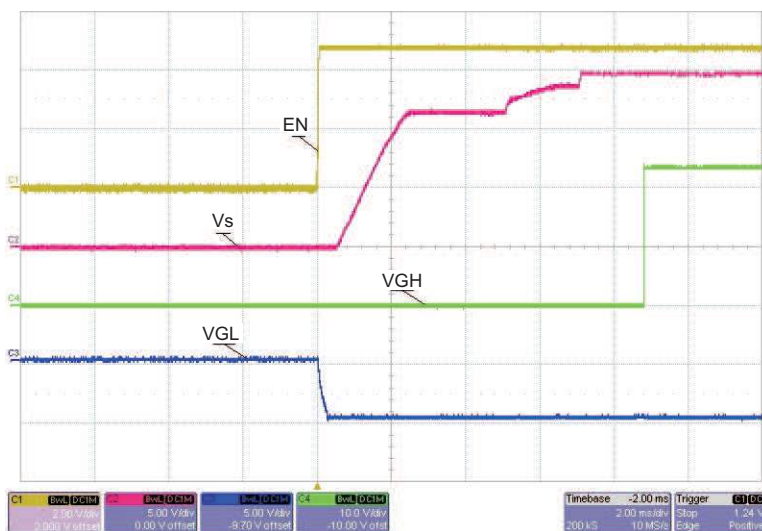


Figure 1. Start-up Waveform

3 Board Layout

This section provides board layout recommendations as well as illustrations of the EVM board layers.

3.1 Board Layout Recommendations

For information regarding PC board layout, see the TPS65167 data sheet ([SLVS760](#)).

3.2 Board Layers

The following illustrations show the top assembly and top and bottom layers of the TPS65167EVM-277.

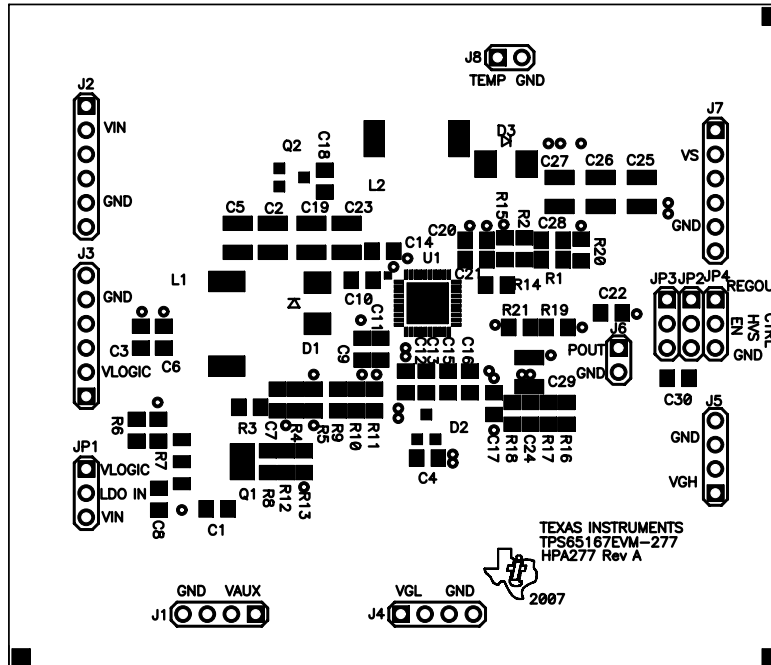


Figure 2. Top Assembly

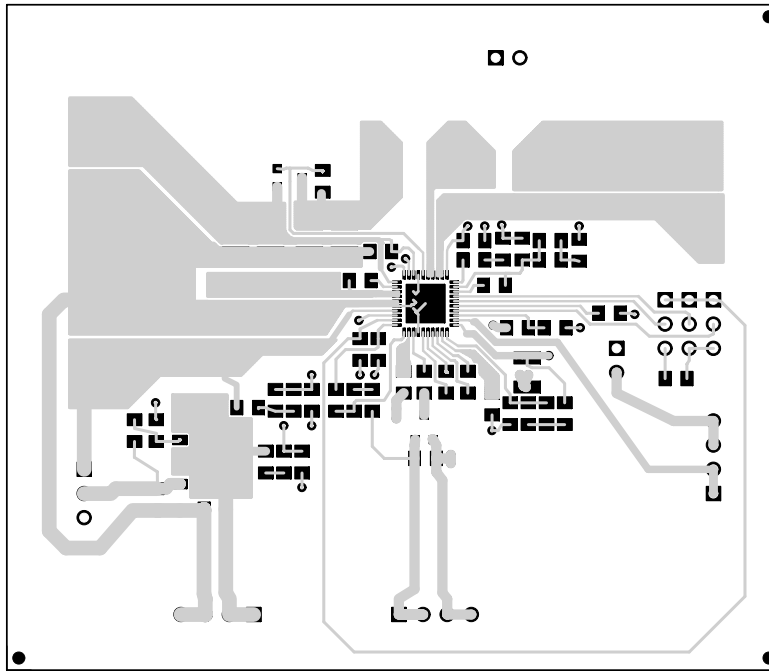


Figure 3. Top Layer

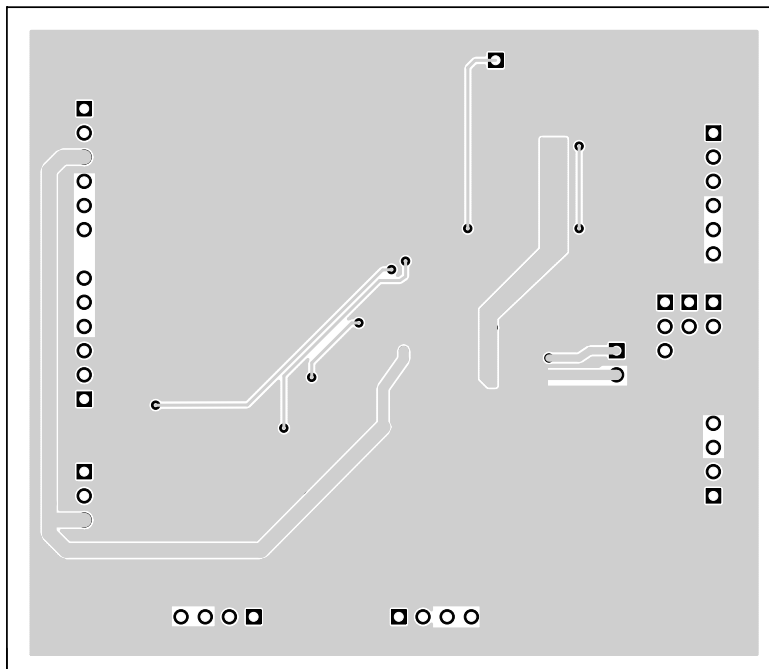


Figure 4. Bottom Layer

Table 3. Bill of Materials

Count	ReDes	Description	Size	Part Number	MFR
1	C1	Capacitor, Ceramic, 10 μ F, 10V, X5R, 10%	0805	GRM21BR61A106KE19L	Murata
1	C10	Capacitor, Ceramic, 0.1 μ F, 25V, X7R, 10%	0805	C2012X7R1E104K	TDK
1	C11	Capacitor, Ceramic, 0.22 μ F, 50V, X5R, 10%	0805	UMK212BJ224KG-T	Taiyo Yuden
5	C12–C16	Capacitor, Ceramic, 0.47 μ F, 25V, X5R, 10%	0805	TMK212BJ474KD-T	Taiyo Yuden
2	C18, C20	Capacitor, Ceramic, 1000 pF, 50V, X7R, 10%	0805	C2012X7R1H102K	TDK
6	C2, C5, C19, C25–C27	Capacitor, Ceramic, 22 μ F, 25V, X5R, 10%	1210	GRM32ER61E226KE15L	Murata
2	C21, C30	Capacitor, Ceramic, 0.022 μ F, 50V, X7R, 10%	0805	GRM216R71H223KA01D	Murata
1	C22	Capacitor, Ceramic, 0.01 μ F, 50V, X7R, 10%	0805	C2012X7R1H103K	TDK
0	C23	Capacitor, Ceramic Open	1210		
1	C24	Capacitor, Ceramic, 100 pF, 50V, C0G, 5%	0805	C2012C0G1H101J	TDK
1	C28	Capacitor, Ceramic, 47 pF, 50V, C0G, 5%	0805	ECJ-2VC1H470J	Panasonic
1	C29	Capacitor, Ceramic, 1.0 μ F, 50V, X7R, 10%	1210	C3225X7R1H105K	TDK
2	C3, C6	Capacitor, Ceramic, 22 μ F, 6.3V, X5R, 10%	0805	JMK212BJ226KG-T	Murata
1	C4	Capacitor, Ceramic, 2.2 μ F, 10V, X5R, 10%	0805	C2012X5R1A225K/0.85	TDK
1	C7	Capacitor, Ceramic, 470 pF, 50V, C0G, 5%	0805	GRM2165C1H471JA01D	Murata
3	C8, C9, C17	Capacitor, Ceramic, 1.0 μ F, 25V, X5R, 10%	0805	C2012X5R1E105K	TDK
2	D1, D3	Diode, Schottky Rectifier, 2A, 20 V	DO-214AA	SL22	Vishay
1	D2	Diode, Dual Schottky, 200 mA, 30V	SOT23	BAT54S	Zetex
3	J1, J4, J5	Header, Male 4 pin, 100 mil spacing, (36-pin strip)	0.100 \times 4	PTC36SAAN	Sullins
3	J2, J3, J7	Header, Male 6 pin, 100 mil spacing, (36-pin strip)	0.100 \times 6	PTC36SAAN	Sullins
2	J6, J8	Header, Male 2 pin, 100 mil spacing, (36-pin strip)	0.100 \times 2	PTC36SAAN	Sullins
4	JP1–JP4	Header, 3 pin, 100 mil spacing, (36-pin strip)	0.100 \times 3	PTC36SAAN	Sullins
2	L1, L2	Inductor, 10 μ H, 3.6 A, 35 m Ω	0.394 \times 0.394	744066100	Würth Elektronik
1	Q1	Transistor, PNP, 60V, 800 mA, 1000 mW	SOT-223	PZT2907A	Fairchild
1	Q2	MOSFET, Pch, –30 V, 4 A, 53 m Ω	SOT23	Si2343DS	Vishay
1	R1	Resistor, Chip, 365 k Ω , 1/10W, 1%	0805	Std	Std
1	R10	Resistor, Chip, 178 k Ω , 1/10W, 1%	0805	Std	Std
1	R12	Resistor, Chip, 4.75 k Ω , 1/10W, 1%	0805	Std	Std
1	R13	Resistor, Chip, 15.0 k Ω , 1/10W, 1%	0805	Std	Std
1	R14	Resistor, Chip, 82.5 k Ω , 1/10W, 1%	0805	Std	Std
1	R17	Resistor, Chip, 301 k Ω , 1/10W, 1%	0805	Std	Std
1	R18	Resistor, Chip, 16.2 k Ω , 1/10W, 1%	0805	Std	Std
2	R19, R21	Resistor, Chip, 10.0 k Ω , 1/10W, 1%	0805	Std	Std
1	R2	Resistor, Chip, 30.1 k Ω , 1/10W, 1%	0805	Std	Std
7	R3, R7, R8, R11, R15, R16, R20	Resistor, Chip, 0 Ω , 1/10W, 5%	0805	Std	Std
1	R4	Resistor, Chip, 2.00 k Ω , 1/10W, 1%	0805	Std	Std
1	R5	Resistor, Chip, 1.21 k Ω , 1/10W, 1%	0805	Std	Std
1	R6	Resistor, Chip, 1.00 k Ω , 1/10W, 1%	0805	Std	Std
1	R9	Resistor, Chip, 43.2 k Ω , 1/10W, 1%	0805	Std	Std
1	U1	IC, Compact LCD Bias Supply TV, Monitor TFT LCD panels	QFN-40	TPS65167RHAR	TI
1	—	PCB, 3.2 In \times 2.8 In \times 0.062 In		HPA277	Any
4	—	Shunt, 100 mil, Black	0.100	929950-00	3M

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 4.5 V to 5.5 V and the output voltage range of 14.7 V to 15.3 V (Vs).

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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