19-5952; Rev 1; 3/12

EVALUATION KIT AVAILABLE

MAX14972

Dual SuperSpeed USB 3.0 Equalizer/Redriver

General Description

The MAX14972 dual SuperSpeed USB 3.0 equalizer/redriver utilizes programmable input equalization and output deemphasis to reduce deterministic jitter and restore signal loss caused by circuit-board or signal-cable losses, and allows optimal placement of key SuperSpeed USB 3.0 components and longer circuit-board traces or cables. The device features advanced power management with receiver detection and explicit support for USB 3.0 low-frequency periodic signals (LFPS).

The device is available in a small, 24-pin (4.0mm x 4.0mm) TQFN package with flow-through traces for optimal layout and minimal space requirements. The device is specified over the 0°C to +70°C commercial operating temperature range.

Applications

USB Ports

USB Hubs

Notebook Computers

Desktop Computers

Docking Stations

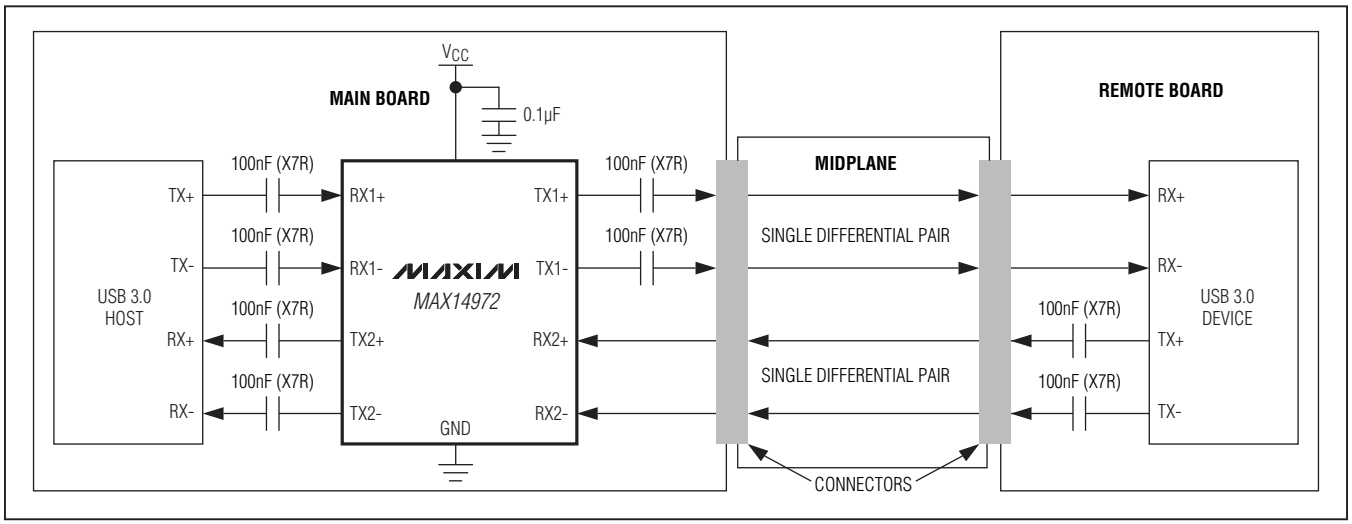
Industrial USB Switching

Ordering Information appears at end of data sheet.

Benefits and Features

- **Innovative Design Eliminates Need for Costly External Components**
  - **Single +3.3V Supply Operation**
- **Advanced Power Management for Maximum Efficiency**
  - **1mW (typ) in Standby State**
  - **23mW (typ) in Receiver Detect State**
  - **82.5mW (typ) in Dynamic Power-Down State**
  - **304mW (typ) in Active State**
- **High Level of Integration for Performance**
  - **Very Low Latency with 250ps (typ) Propagation Delay**
  - **10dB (typ) Input/Output Return Loss Up to 2.5GHz**
  - **Three-Level Programmable Input Equalization**
  - **Six-Level Programmable Output Deemphasis**
  - **Explicit LFPS Support with Frequency Shaping**
  - **SuperSpeed USB 3.0-Compliant Receiver Detection**
  - **Low-Voltage (1.8V) Compatible Controls**
  - **Excellent Jitter and Loss Compensation Capability > 40in of 4mil Microstrip**
- **Ideal for Space-Sensitive Applications**
  - **On-Chip 50Ω Input/Output Terminations**
  - **24-Pin, 4.0mm x 4.0mm TQFN Packaging**
  - **±8kV HBM ESD Protection on All Pins**
  - **Pin-to-Pin Compatible with TI SN65LVPE502 and TI SN65LVPE502CP**

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)

V_{CC} ..... -0.3V to +4.0V
All Other Pins (Note 1) ..... -0.3V to (V_{CC} + 0.3V)
Continuous Current RX_+, RX_-, TX_+, TX_-..... ±30mA
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 27.8mW/°C above +70°C) 2222.2mW

Operating Temperature Range ..... 0°C to +70°C
Junction Temperature Range ..... -40°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: All I/O pins are clamped by internal diodes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

TQFN

Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 36°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....3°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, C_C = 100nF coupling capacitor on each output, R_L = 50Ω and C_L = 1pF on each output, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC PERFORMANCE						
Power-Supply Range	V_{CC}		3.0	3.3	3.6	V
Operating Supply Current	I_{CC}	ENRXD = 1, data rate = 5.0Gbps, D10.2 pattern, DE_ = V_{CC}, OS_ = GND		92	125	mA
		ENRXD = 1, CM = 0, no output termination		7	10	
		Dynamic power-down mode, ENRXD = 1, CM = 0, with output termination, no input signal		25	32	
Standby Supply Current	I_{STBY}	ENRXD = 0			500	µA
Differential Input Impedance	$Z_{RX-DC-DIFF}$	DC	72		120	Ω
Differential Output Impedance	$Z_{TX-DC-DIFF}$	DC	72		120	Ω
Single-Ended High Input Impedance	$Z_{RX-SE-HIGH}$	No output termination, CM = 0 (Note 3)	25	50		kΩ
Common-Mode Input Impedance	$Z_{RX-DC-CM}$	(Note 3)	18		30	Ω
Common-Mode Output Impedance	$Z_{TX-DC-CM}$	(Note 4)	18		30	Ω
Common-Mode Input Voltage	$V_{RX-DC-CM}$	(Note 3)		0		V
Common-Mode Output Voltage	$V_{TX-DC-CM}$	(Note 3)		2.75		V
Active LFPS Common-Mode Delta	$\Delta V_{LFPS-CM}$	Active LFPS squelched and not squelched			50	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, C_C = 100nF coupling capacitor on each output, R_L = 50Ω and C_L = 1pF on each output, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC PERFORMANCE (Note 5)						
Redriver-Operation Differential Input Signal Range	$V_{RX-DIFF-PP}$	USB 3.0 data	150		1200	mV_{P-P}
LFPS Detect Threshold	$V_{LFPS-DIFF-PP}$	USB 3.0 data	100		300	mV
Differential Input Return Loss	$RL_{RX-DIFF}$	50MHz ≤ f < 1250MHz	16	18		dB
		1250MHz ≤ f < 2500MHz	8	12		
Differential Output Return Loss	$RL_{TX-DIFF}$	50MHz ≤ f < 1250MHz	13	16		dB
		1250MHz ≤ f < 2500MHz	8	10		
Common-Mode Input Return Loss	RL_{RX-CM}	50MHz ≤ f < 2500MHz	11	13		dB
Common-Mode Output Return Loss	RL_{TX-CM}	50MHz ≤ f < 2500MHz	11	13		dB
Differential Output Amplitude (Transition Bit), Figure 1	$V_{TX-DIFF-TB-PP}$	OS_ = 0, DE_ = 0		1120		mV_{P-P}
		OS_ = 0, DE_ = N.C.		940		
		OS_ = 0, DE_ = 1		1210		
		OS_ = 1 or N.C., DE_ = 0		1180		
		OS_ = 1 or N.C., DE_ = N.C.		1010		
		OS_ = 1 or N.C., DE_ = 1		1270		
Differential Output Amplitude (Nontransition Bit), Figure 1	$V_{TX-DIFF-NTB-PP}$	DE_ = N.C.		640		mV_{P-P}
		DE_ = 0		840		
		DE_ = 1		940		
LFPS Idle Differential Output Voltage	$V_{LFPS-IDLE-DIFF-PP}$	Highpass filter to remove DC offset			30	mV
Voltage Change to Allow Receiver Detect	V_{DETECT}	Positive voltage to sense receiver termination			500	mV
Deterministic Jitter	$t_{TX-DJ-DD}$	K28.5 pattern, data rate = 5.0Gbps, EQ_ = not connected			12	ps_{P-P}
Random Jitter	$t_{TX-RJ-DD}$	K28.5 pattern, data rate = 5.0Gbps, EQ_ = not connected			1	ps_{RMS}
Rise/Fall Time	$t_{TX-RISE-FALL}$	(Note 6)	40			ps
Differential Propagation Delay	t_{PD}	Propagation delay input to output at 50%		250		ps
LFPS Idle Entry Delay	$t_{IDLE-ENTRY}$	USB 3.0 LFPS pattern, active state		4	6	ns
LFPS Idle Exit Delay	$t_{IDLE-EXIT}$	USB 3.0 LFPS pattern, active state		4	6	ns
		USB 3.0 LFPS pattern, dynamic power-down state		15.6	22.5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, C_C = 100nF coupling capacitor on each output, R_L = 50Ω and C_L = 1pF on each output, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL LOGIC						
Input Logic-High	V_{IH}	ENRXD, CM, EQ_, OS_, and DE_	1.5			V
Input Logic-Low	V_{IL}	ENRXD, CM, EQ_, OS_, and DE_			0.5	V
Input Logic Hysteresis	V_{HYST}	ENRXD, CM, EQ_, OS_, and DE_		0.075		V
ESD PROTECTION						
HBM ESD Protection		Human Body Model		±8		kV

Note 3: Measured with respect to ground.
Note 4: Measured with respect to V_{CC}.
Note 5: Guaranteed by design, unless otherwise noted.
Note 6: Rise and fall times are measured using 20% and 80% levels.

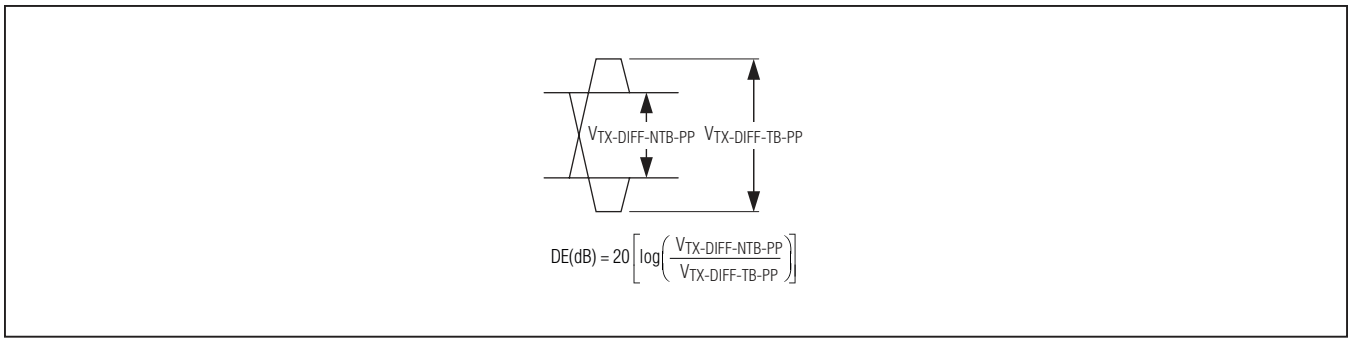


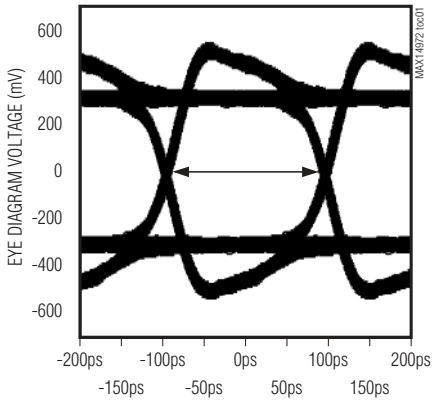
Figure 1. Illustration of Output Deemphasis

Dual SuperSpeed USB 3.0 Equalizer/Redriver

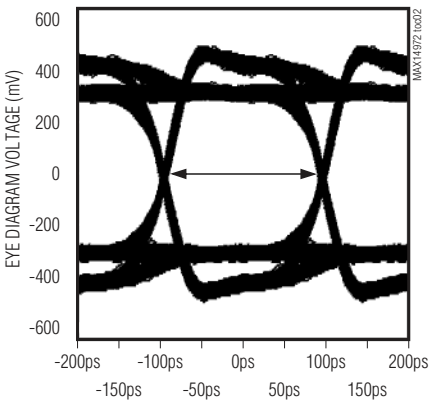
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, EQ_ = N.C., using 5Gbps ±K28.5 pattern, unless otherwise noted.)

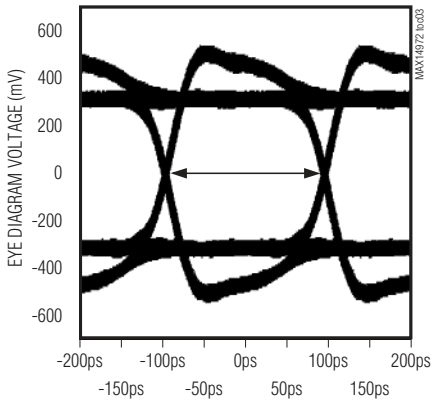
DE_ = N.C, OS_ = N.C or 1,
$V_{RX-DIFF-PP}$ = 150mV_{P-P}



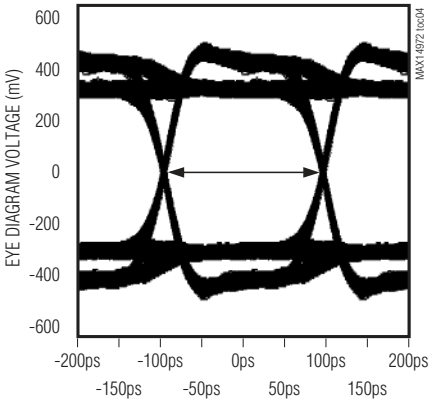
DE_ = N.C, OS_ = 0,
$V_{RX-DIFF-PP}$ = 150mV_{P-P}



DE_ = N.C, OS_ = N.C or 1,
$V_{RX-DIFF-PP}$ = 1200mV_{P-P}



DE_ = N.C, OS_ = 0,
$V_{RX-DIFF-PP}$ = 1200mV_{P-P}

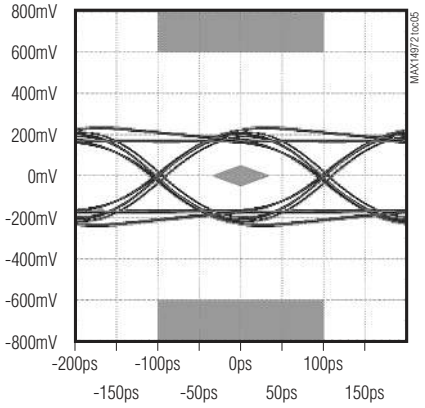


Dual SuperSpeed USB 3.0 Equalizer/Redriver

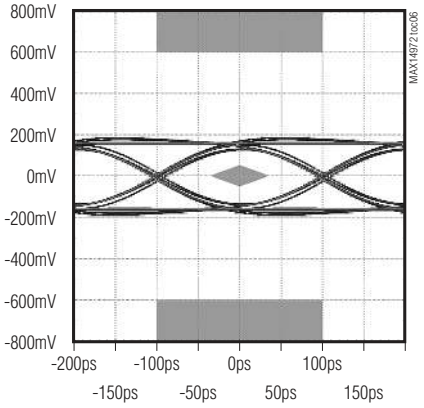
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, EQ_ = N.C., using 5Gbps ±K28.5 pattern, unless otherwise noted.)

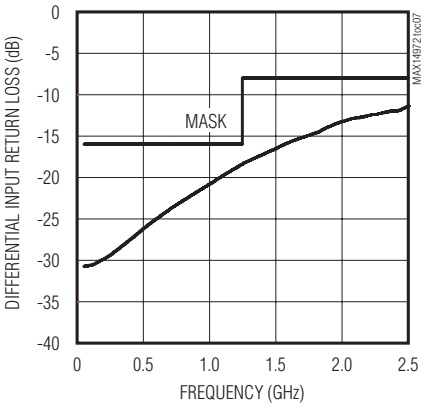
DE_ = N.C, OS_ = 1,
$V_{RX-DIFF-PP}$ = 150mV_{P-P}
USB 3.0 HOST COMPLIANCE FILTER



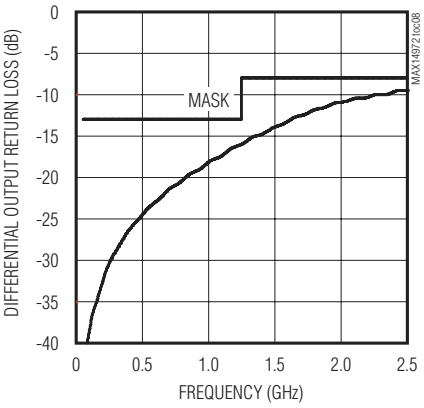
DE_ = N.C, OS_ = 1,
$V_{RX-DIFF-PP}$ = 150mV_{P-P}
USB 3.0 DEVICE COMPLIANCE FILTER



DIFFERENTIAL INPUT RETURN LOSS vs. FREQUENCY

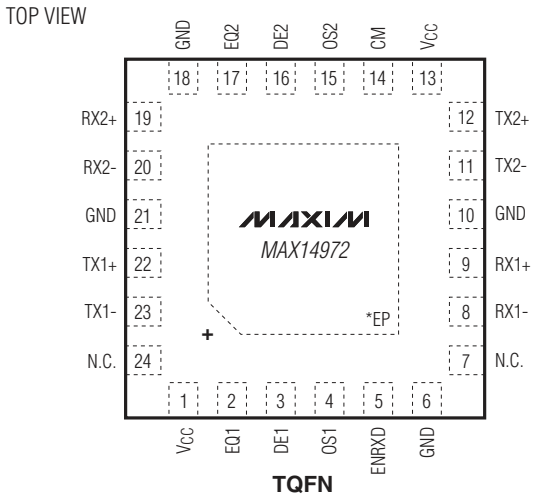


DIFFERENTIAL OUTPUT RETURN LOSS vs. FREQUENCY



Dual SuperSpeed USB 3.0 Equalizer/Redriver

Pin Configuration



*CONNECT EXPOSED PAD (EP) TO GND.

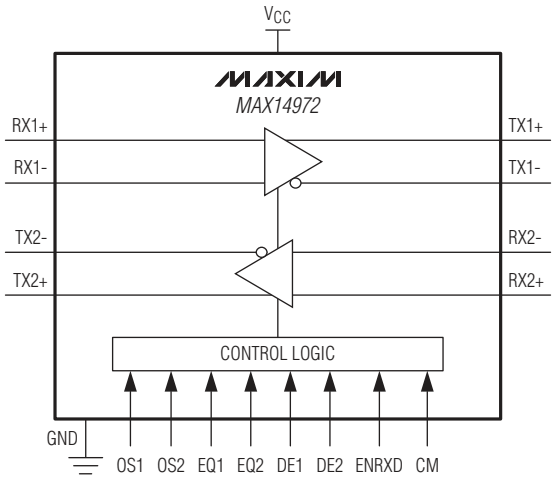
Pin Description

PIN	NAME	FUNCTION
1, 13	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with 0.1µF and 2.2µF low-ESR capacitors in parallel as close as possible to the device.
2	EQ1	Three-State Input Equalization Control, Channel 1. Leave EQ1 unconnected for default state.
3	DE1	Three-State Transition Bit and Nontransition Bit Output Amplitude Control, Channel 1. Connect DE1 to V_{CC} for default state.
4	OS1	Two-State Transition-Bit Output Amplitude Control, Channel 1. Connect OS1 to GND for default state.
5	ENRXD	Active-High Enable. Drive ENRXD high or leave unconnected for normal operation. Drive ENRXD low to enter standby state. ENRXD has a 400kΩ (typ) pullup resistor to V_{CC}.
6, 10, 18, 21	GND	Ground
7, 24	N.C.	No Connection. Not internally connected.
8	RX1-	Inverting Input, Channel 1. AC-couple RX1- with a low-ESR 100nF capacitor.
9	RX1+	Noninverting Input, Channel 1. AC-couple RX1+ with a low-ESR 100nF capacitor.
11	TX2-	Inverting Output, Channel 2. AC-couple TX2- with a low-ESR 100nF capacitor.
12	TX2+	Noninverting Output, Channel 2. AC-couple TX2+ with a low-ESR 100nF capacitor.
14	CM	Active-High Compliance Mode Control. Drive CM high to force active state. Drive CM low or leave unconnected for normal operation. CM has a 400kΩ (typ) pulldown resistor to GND.

Pin Description (continued)

PIN	NAME	FUNCTION
15	OS2	Two-State Transition-Bit Output Amplitude Control, Channel 2. Connect OS2 to GND for default state.
16	DE2	Three-State Transition Bit and Nontransition Bit Output Amplitude Control, Channel 2. Connect DE2 to V_{CC} for default state.
17	EQ2	Three-State Input Equalization Control, Channel 2. Leave EQ2 unconnected for default state.
19	RX2+	Noninverting Input, Channel 2. AC-couple RX2+ with a low-ESR 100nF capacitor.
20	RX2-	Inverting Input, Channel 2. AC-couple RX2- with a low-ESR 100nF capacitor.
22	TX1+	Noninverting Output, Channel 1. AC-couple TX1+ with a low-ESR 100nF capacitor.
23	TX1-	Inverting Output, Channel 1. AC-couple TX1- with a low-ESR 100nF capacitor.
—	EP	Exposed Pad. Internally connected to GND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

Functional Diagram



Detailed Description

The MAX14972 features two identical drivers to support a complete single SuperSpeed USB 3.0 link. Programmable equalization and deemphasis on each channel allows for optimal board placement of SuperSpeed transceivers and enables flexibility of front, rear, and side SuperSpeed ports. The device features advanced power management with receiver detection and support for USB 3.0 low-frequency periodic signals (LFPS).

Programmable Input Equalization

Input equalization for channel 1 is controlled by EQ1, while input equalization for channel 2 is controlled by EQ2. Each of the two pins, EQ1 and EQ2, has three equalization settings, which offer flexible compensation for varied input circuit-board trace, connector, or cable losses (Table 1). The EQ_ three-state inputs interpret voltages below V_{IH} and higher than V_{IL} as high impedance. Set EQ_ to 1V, for example, or leave unconnected if the impedance state is required.

Programmable Output Deemphasis

Channel 1 output transition bit amplitude is controlled by the OS1 and DE1 pins, and the nontransition bit amplitude is controlled only by the DE1 pin. Channel 2 output transition bit amplitude is controlled by the OS2 and DE2 pins, and the nontransition bit amplitude is controlled only by the DE2 pin. There are six possible output deemphasis states for each of the two channels, which offer flexibility to compensate for varied losses in the output circuit-board traces, connectors, or cables runs (Table 2, Table 3, and Table 4.) The DE_ three-state input interprets voltages below V_{IH} and higher than V_{IL} as high impedance. Set DE_ to 1V, for example, or leave unconnected if a high-impedance state is required.

LFPS Support

The device explicitly supports USB 3.0 LFPS by detecting an idle state at the input and squelching the corresponding output to prevent unwanted noise from being redriven. When the differential input LFPS signal falls below the $100mV_{P-P}$ threshold, the device squelches the output. When a differential LFPS signal above $300mV_{P-P}$ (typ) is present at the input, the device turns on the corresponding output and redrives the signal. The device features an LFPS idle entry time of 4ns (typ) and exit time of 4ns (typ) in the active state.

Advanced Power Management

Standby State

Drive ENRXD low to place the device into a low-power standby state. In standby, the inputs are in a common-mode high-impedance state and the device consumes less than 1mW (typ) of power. The entry time to standby is 2µs (typ), and the exit time is 50µs (typ).

Table 1. Typical Input Equalization

EQ_	EQUALIZATION (dB)
N.C.*	0
0	6
1	10

*Not connected.

Table 2. Typical Output Transition Bit Amplitude (Refer to the *Electrical Characteristics* Table)

OS_	AMPLITUDE (mV_{P-P})
N.C.*, 1	1010 to 1270
0	940 to 1210

*Not connected.

Table 3. Typical Output Nontransition Bit Amplitude

DE_	AMPLITUDE (mV_{P-P})
N.C*	640
0	840
1	940

*Not connected.

Table 4. Typical Output Deemphasis

CONTROL LOGIC	OS_ = 0	OS_ = 1, N.C.*
DE_ = 0	-2.5dB	-3.0dB
DE_ = N.C.	-3.3dB	-3.9dB
DE_ = 1	-2.2dB	-2.7dB

*Not connected.

Receiver Detection

The device features independent receiver detection on each channel. Upon initial power-up, if ENRXD is high, receiver detection initializes. If the device is in a powered-up state, the receiver detection is initiated on the rising edge of ENRXD. During receiver detection, the part remains in low-power mode 23mW (typ) and the outputs and inputs are in a common-mode high-impedance state. The receiver detection repeats every 12ms (typ) until the receiver is detected. The receiver must be detected on both channels to exit the receiver detection state.

Dynamic Power-Down

The device enters dynamic power-down state when a receiver has been detected and no signal is present at the input. The device exits this state when a signal is detected at the input. The device consumes less than 82.5mW (typ) power in dynamic power-down state. The device enters dynamic power-down after 30µs idle detection. If no signal is detected for more than 12ms (typ), the part enters receiver detection state.

Active State

The device automatically enters active state after a receiver is detected and an input signal is present. The part can be forced into the active state by setting CM = 1 as shown in Table 5. The device consumes less than 304mW (typ) of power in this state.

USB 3.0 Compliance Mode

The MAX14972 features a USB 3.0 compliance mode that forces the device to remain in the active state. The device redrives signals to test the transmitter for voltage and timing specifications compliance as required by USB 3.0 specifications. Drive ENRXD high or leave unconnected, and CM high to activate USB 3.0 compliance mode. Drive ENRXD high or leave unconnected, and CM low or leave unconnected for normal operation (Table 5). Receiver detection and dynamic power-down are disabled in compliance mode (CM = 1), while the part remains in the active state with functional LFPS support.

Table 5. Digital Control Truth Table

ENRXD	CM	DESCRIPTION
0	0	Power-Down
0	1	Power-Down
1 or N.C.*	0 or N.C.*	Normal Operation
1 or N.C.*	1	Compliance Mode (Active)

*Not connected.

Applications Information

Layout

Circuit-board layout and design can significantly affect the performance of the device. Use good high-frequency design techniques, including minimizing ground inductance and using controlled-impedance transmission lines on data signals. Power-supply decoupling capacitors must be placed as close as possible to V_{CC}. Always connect V_{CC} to a power plane.

Exposed-Pad Package

The exposed pad, 24-pin TQFN package incorporates features that provide a very low thermal resistance path for heat removal from the IC. The exposed pad on the device must be soldered to the PCB ground plane for proper electrical and thermal performance. For more information on exposed-pad packages, refer to Application Note 862: *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

Power-Supply Sequencing

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all devices. Always apply GND then V_{CC} before applying signals, especially if the signal is not current limited.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14972CTG+	0°C to +70°C	24 TQFN-EP*

+*Denotes a lead(Pb)-free/RoHS-compliant package.*

**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T2444+3	21-0139	90-0021

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/11	Initial release	—
1	3/12	Updated *Electrical Characteristics* table	14