



NX138AKS

60 V, dual N-channel Trench MOSFET

15 June 2016

Product data sheet

1. General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection

3. Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

4. Quick reference data

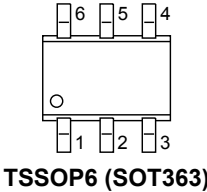
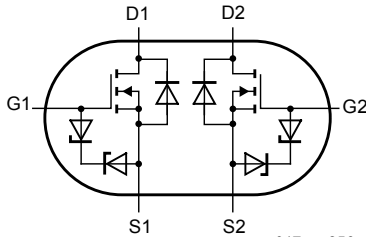
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	60	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	170	mA
Static characteristics (per transistor)						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 170\text{ mA}; T_j = 25\text{ °C}$	-	3	4.5	Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm^2 .

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>TSSOP6 (SOT363)</p>	 <p>017aaa256</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NX138AKS	TSSOP6	plastic surface-mounted package; 6 leads	SOT363

7. Marking

Table 4. Marking codes

Type number	Marking code
NX138AKS	F8%

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	60	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	170	mA
		$V_{GS} = 10\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	110	mA
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C};$ single pulse; $t_p \leq 10\text{ }\mu\text{s}$		-	680	mA
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	265	mW
			[1]	-	325	mW
		$T_{sp} = 25\text{ °C}$		-	1.33	W
Per device						
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
Source-drain diode						
I_S	source current	$T_{amb} = 25\text{ °C}$	[1]	-	170	mA

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm².

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

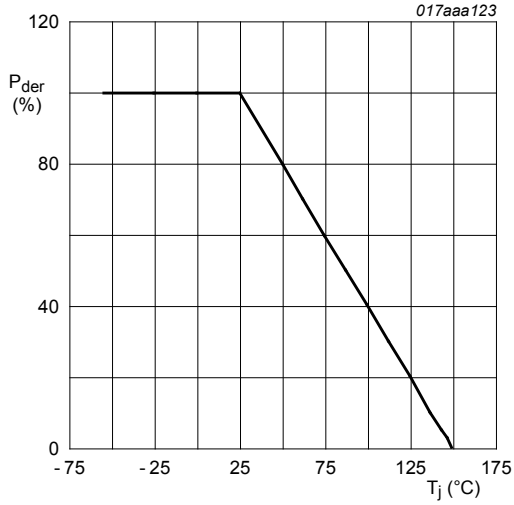


Fig. 1. MOSFET transistor: Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

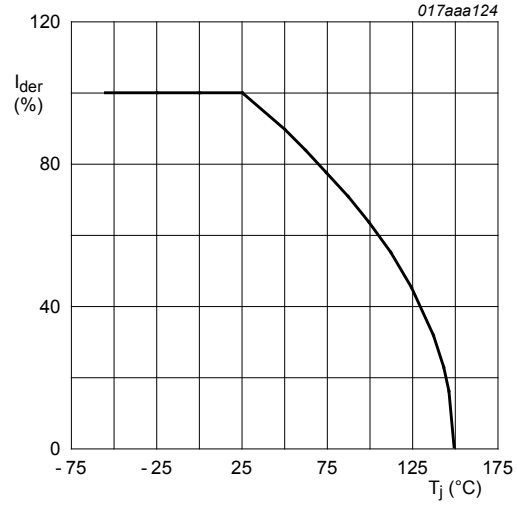
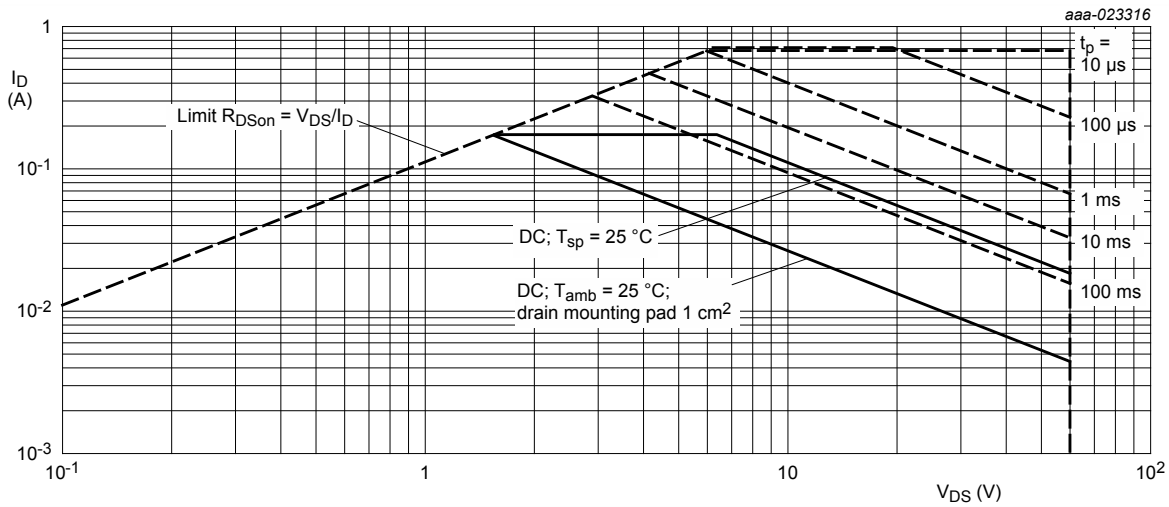


Fig. 2. MOSFET transistor: Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$



I_{DM} = single pulse

Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

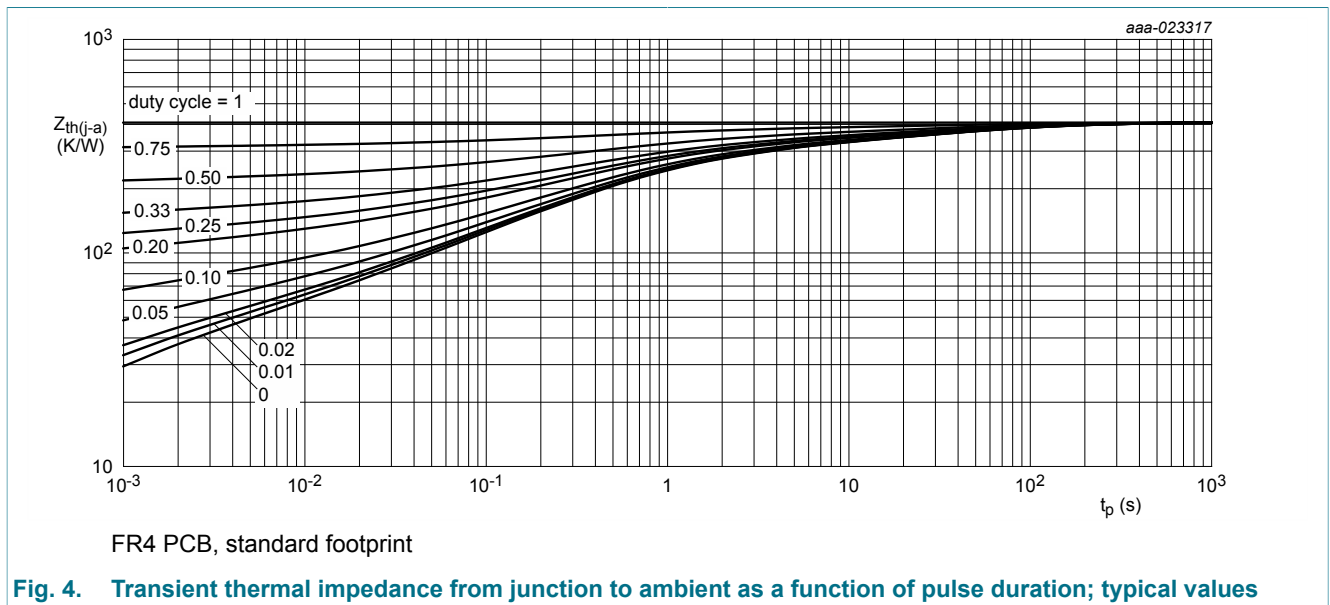
9. Thermal characteristics

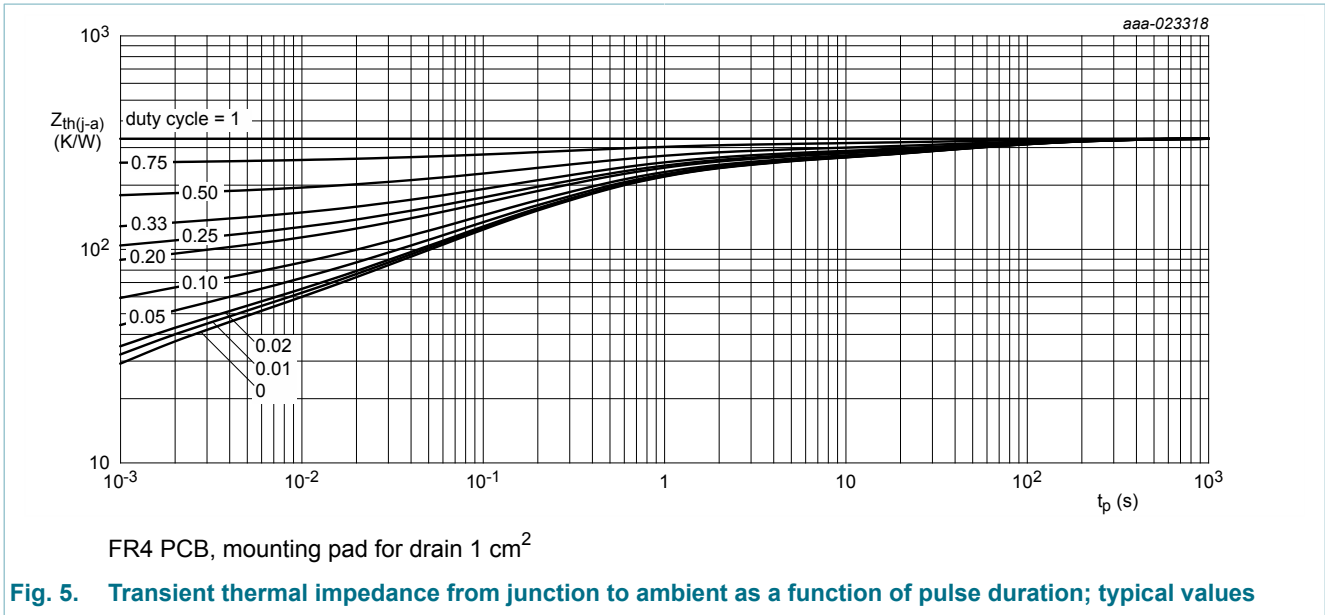
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	500	560	K/W
			[2]	-	450	480	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	100	115	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².

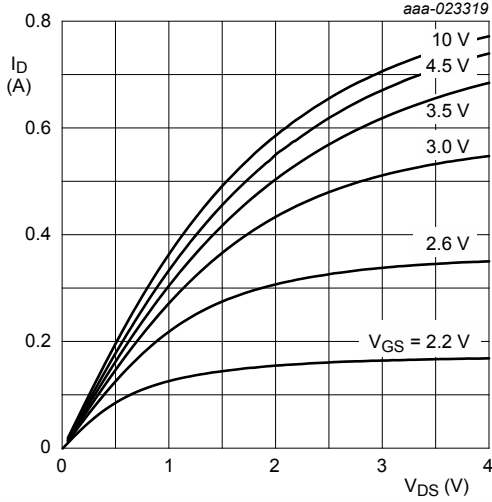




10. Characteristics

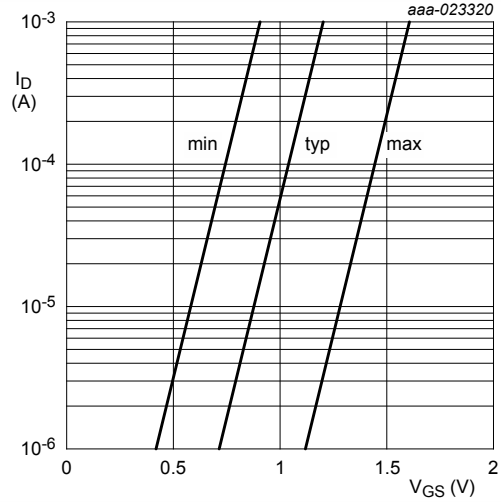
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics (per transistor)						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	60	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu\text{A}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	0.8	1.1	1.5	V
I_{DSS}	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	2	μA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-2	μA
		$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	0.5	μA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-0.5	μA
		$V_{GS} = 5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 170 \text{ mA}; T_j = 25 \text{ }^\circ\text{C}$	-	3	4.5	Ω
		$V_{GS} = 10 \text{ V}; I_D = 170 \text{ mA}; T_j = 150 \text{ }^\circ\text{C}$	-	6	9	Ω
		$V_{GS} = 5 \text{ V}; I_D = 150 \text{ mA}; T_j = 25 \text{ }^\circ\text{C}$	-	3.7	5.2	Ω
		$V_{GS} = 4 \text{ V}; I_D = 130 \text{ mA}; T_j = 25 \text{ }^\circ\text{C}$	-	4	6.3	Ω
		$V_{GS} = 2.5 \text{ V}; I_D = 100 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	5	10	Ω
g_{fs}	forward transconductance	$V_{DS} = 10 \text{ V}; I_D = 170 \text{ mA}; T_j = 25 \text{ }^\circ\text{C}$	-	3.5	-	S
Dynamic characteristics (per transistor)						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 30 \text{ V}; I_D = 170 \text{ mA}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.9	1.4	nC
Q_{GS}	gate-source charge		-	0.1	-	nC
Q_{GD}	gate-drain charge		-	0.2	-	nC
C_{iss}	input capacitance	$V_{DS} = 30 \text{ V}; f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	15	20	pF
C_{oss}	output capacitance		-	2.3	-	pF
C_{rss}	reverse transfer capacitance		-	1.5	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; I_D = 170 \text{ mA}; V_{GS} = 10 \text{ V}; R_{G(ext)} = 75 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	8	12	ns
t_r	rise time		-	10	-	ns
$t_{d(off)}$	turn-off delay time		-	8	20	ns
t_f	fall time		-	5	-	ns
Source-drain diode (per transistor)						
V_{SD}	source-drain voltage	$I_S = 170 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.8	1.2	V



$T_j = 25\text{ }^\circ\text{C}$

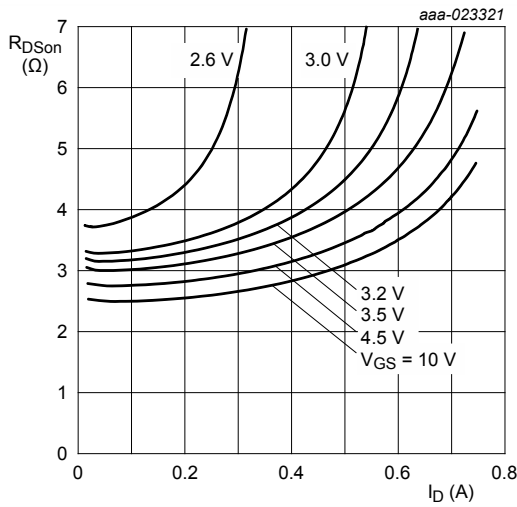
Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values



$V_{DS} = 5\text{ V}$

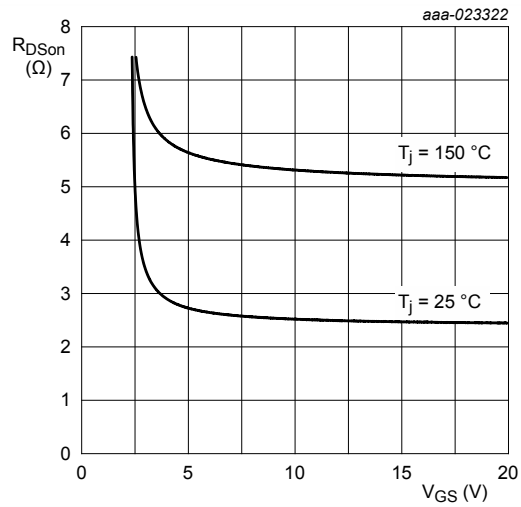
$T_j = 25\text{ }^\circ\text{C}$

Fig. 7. Sub-threshold drain current as a function of gate-source voltage



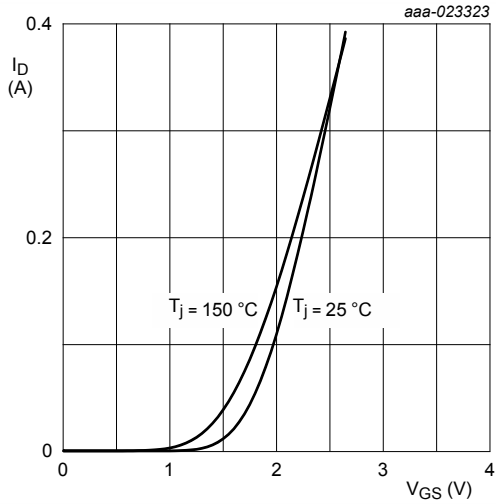
$T_j = 25\text{ }^\circ\text{C}$

Fig. 8. Drain-source on-state resistance as a function of drain current; typical values



$I_D = 0.2\text{ A}$

Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



$$V_{DS} > I_D \times R_{DSon}$$

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

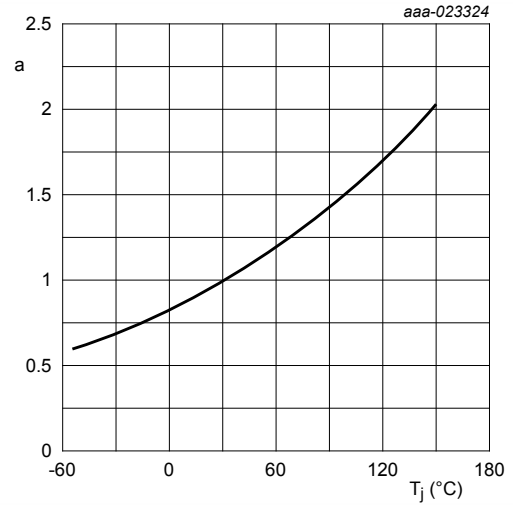
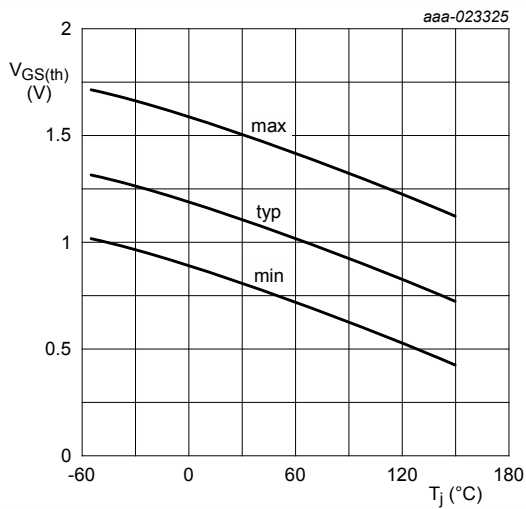


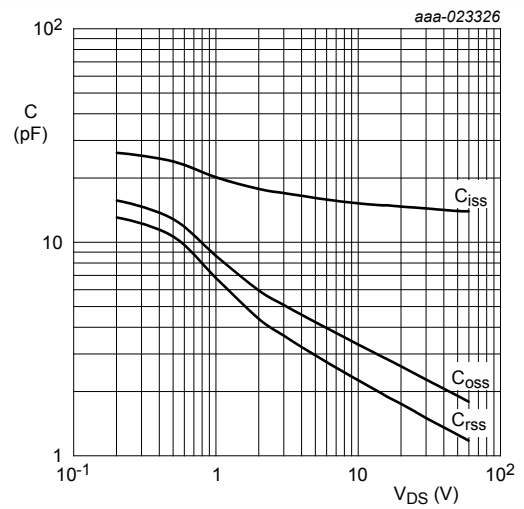
Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25\text{ }^\circ\text{C})}}$$



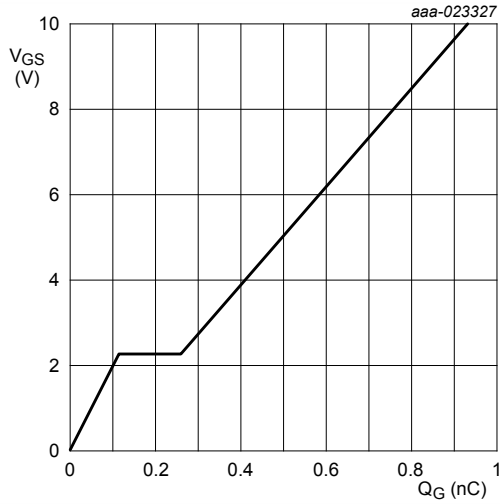
$$I_D = 250\ \mu\text{A}; V_{DS} = V_{GS}$$

Fig. 12. Gate-source threshold voltage as a function of junction temperature



$$f = 1\ \text{MHz}; V_{GS} = 0\ \text{V}$$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = 30$ V; $I_D = 0.9$ A

Fig. 14. Gate-source voltage as a function of gate charge; typical values

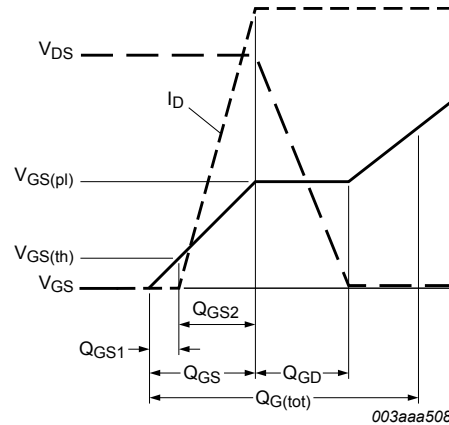
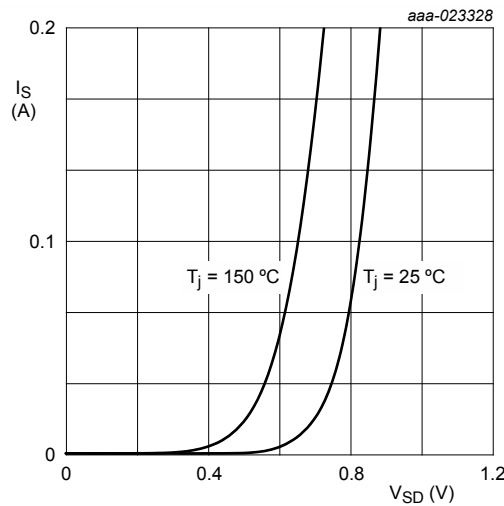


Fig. 15. MOSFET transistor: Gate charge waveform definitions



$V_{GS} = 0$ V

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

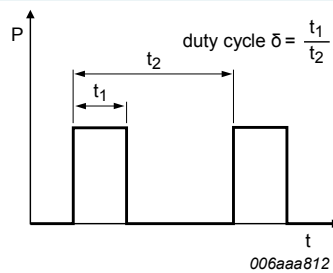


Fig. 17. Duty cycle definition

12. Package outline

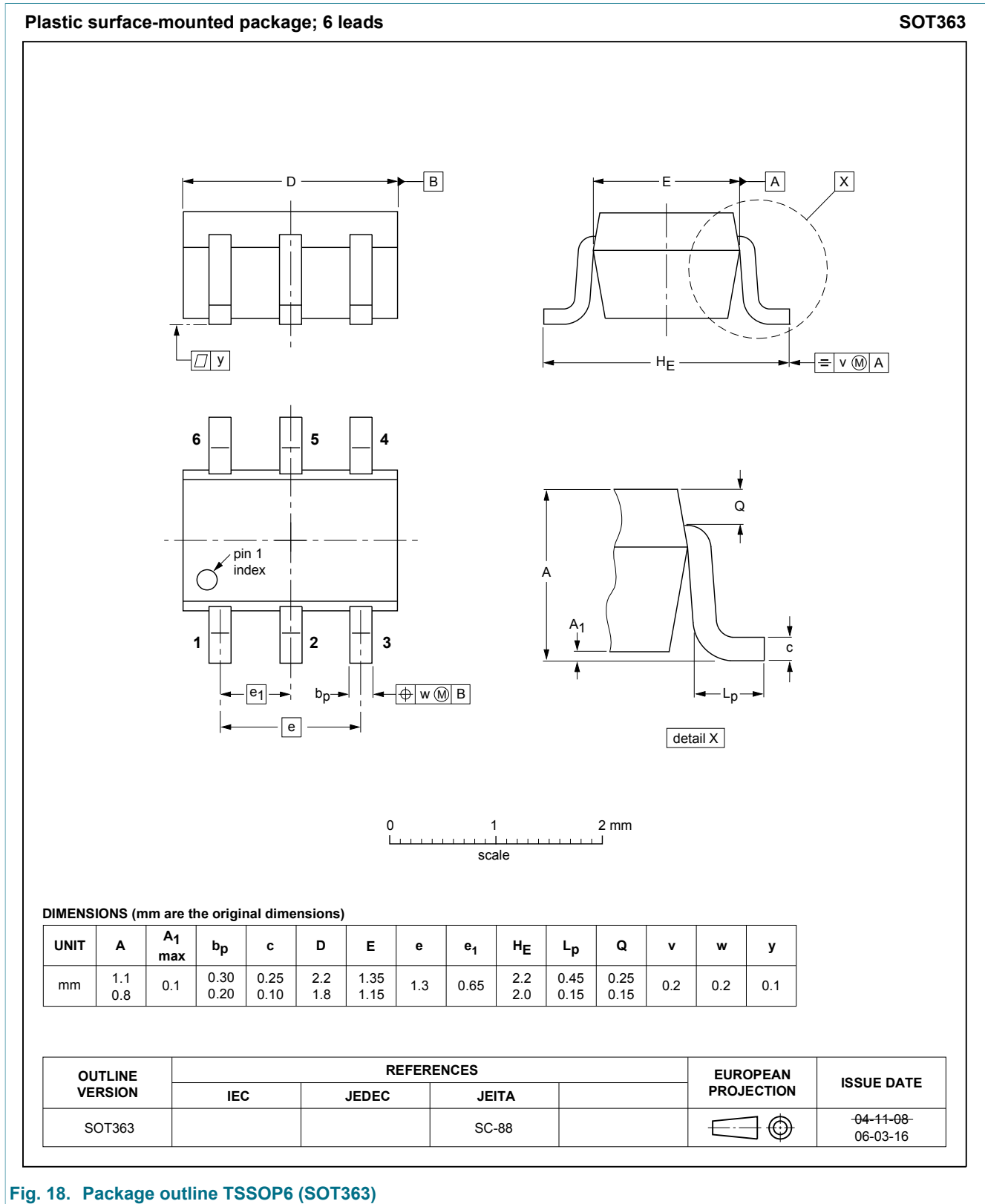


Fig. 18. Package outline TSSOP6 (SOT363)

13. Soldering

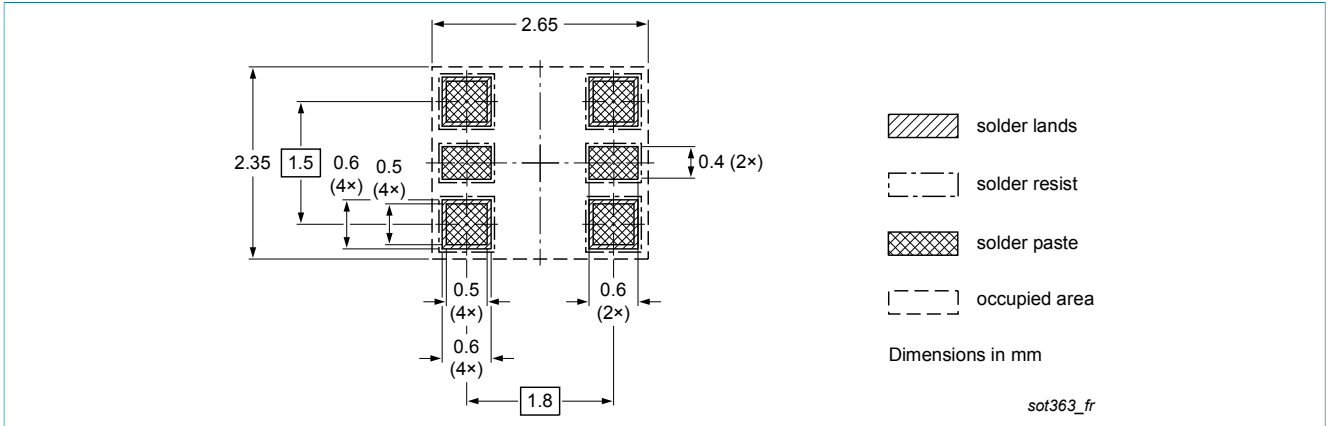


Fig. 19. Reflow soldering footprint for TSSOP6 (SOT363)

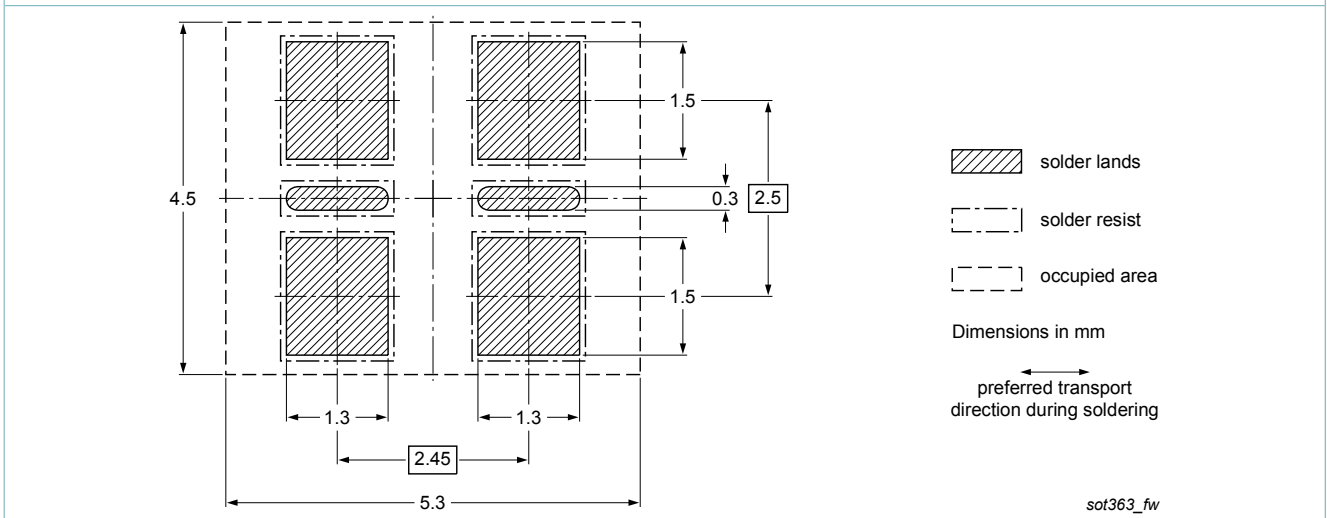


Fig. 20. Wave soldering footprint for TSSOP6 (SOT363)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
NX138AKS v.1	20160615	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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