# 4.25-Gbps Transimpedance Amplifier With AGC and RSSI

## FEATURES

- **2.8-GHz Bandwidth**
- **3.2-kΩ Differential Transimpedance**
- **Automatic Gain Control (AGC)**
- **8.8-pA/√Hz Typical Input Referred Noise**
- **2-mA$_{p-p}$ Maximum Input Current**
- **Received Signal Strength Indication (RSSI)**
- **CML Data Outputs With On-Chip 50-Ω Back-Termination**
- **On-Chip Supply Filter Capacitor**
- **Single 3.3-V Supply**
- **Die Size: 0,78 × 1,18 mm**

## APPLICATIONS

- **SONET/SDH Transmission Systems at OC24 and OC48**
- **4.25-Gbps, 2.125-Gbps, and 1.0625-Gbps Fiber-Channel Receivers**
- **Gigabit Ethernet Receivers**
- **PIN Preamplifier-Receivers**

## DESCRIPTION

The ONET4291TA is a high-speed transimpedance amplifier used in optical receivers with data rates up to 4.25 Gbps.

It features a low input referred noise, 2.8-GHz bandwidth, automatic gain control (AGC), 3.2-kΩ transimpedance, and received signal strength indication (RSSI).

The ONET4291TA is available in die form and is optimized for use in a TO can.

The ONET4291TA requires a single 3.3-V supply, and its power-efficient design typically dissipates less than 56 mW. The device is characterized for operation from –40°C to 85°C ambient temperature.

**AVAILABLE OPTIONS**

| $T_A$ | DIE |
|---|---|
| –40°C to 85°C | ONET4291TAY |

## BLOCK DIAGRAM

The ONET4291TA is a high-performance, 4.25-Gbps transimpedance amplifier consisting of the signal path, supply filter, a control block for dc input current cancellation, automatic gain control (AGC), received signal strength indication (RSSI), and a band-gap voltage reference and bias current generation block.

The signal path comprises a transimpedance amplifier stage, a voltage amplifier, and a CML output buffer.

The on-chip filter circuit provides filtered $V_{CC}$ for the photodiode and for the transimpedance amplifier. The dc input current cancellation and AGC use internal low-pass filters to cancel the dc current on the input and to adjust the transimpedance amplifier gain. Furthermore, circuitry to monitor the received signal strength is provided.

A simplified block diagram of the ONET4291TA is shown in Figure 1.

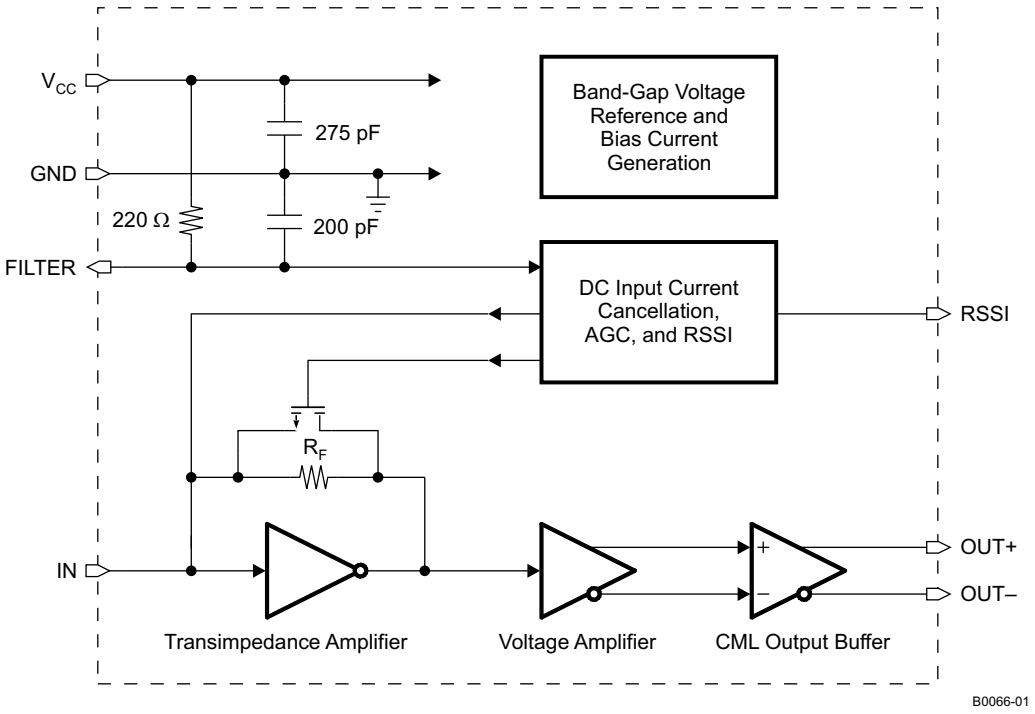



**Figure 1. Simplified Block Diagram of the ONET4291TA**

## SIGNAL PATH

The first stage of the signal path is a transimpedance amplifier that takes the photodiode current and converts it into a voltage signal.

If the input signal current exceeds a certain value, the transimpedance gain is reduced by means of AGC circuitry.

The second stage is a voltage amplifier that provides additional gain and converts its single-ended input voltage into a differential data signal.

The third signal-path stage is the output buffer, which provides CML outputs with on-chip, 50-Ω back-termination to $V_{CC}$.

## FILTER CIRCUITRY

The filter pin provides filtered $V_{CC}$ for the photodiode bias. The on-chip, low-pass filter for the photodiode $V_{CC}$ is implemented using a filter resistor of 220 Ω and an internal 200-pF capacitor. The corresponding corner frequency is below 4 MHz.

The supply voltage for the whole amplifier is filtered by means of an on-chip, 275-pF capacitor as well, thus avoiding the necessity to use an external supply-filter capacitor.

## DC INPUT CURRENT CANCELLATION, AGC, AND RSSI

The voltage drop across the internal photodiode supply-filter resistor is monitored by means of a dc input current cancellation, AGC, and RSSI control circuit block.

If the dc input current exceeds a certain level, it is partially cancelled by means of a controlled current source. This measure keeps the transimpedance amplifier stage within sufficient operating point limits for optimum performance. Furthermore, disabling the dc input cancellation at low input currents leads to superior noise performance.

The AGC circuitry lowers the effective transimpedance feedback resistor $R_F$ by means of a MOSFET device acting as a controlled shunt. This prevents the transimpedance amplifier from being overdriven at high input currents, which leads to improved jitter behavior within the complete input-current dynamic range. Because the voltage drop across the supply-filter resistor is sensed and used by the AGC circuit, the photodiode must be connected to a FILTER pad for the AGC to function correctly.

Finally, this circuit block senses the current through the filter resistor and generates a mirrored current, which is proportional to the input signal strength. The mirrored current is available at the RSSI output and must be sunk to ground (GND) using an external resistor. The RSSI gain can be adjusted by choosing the external resistor; however, for proper operation, ensure that the voltage at the RSSI pad never exceeds $V_{CC}$ – 0.65 V.

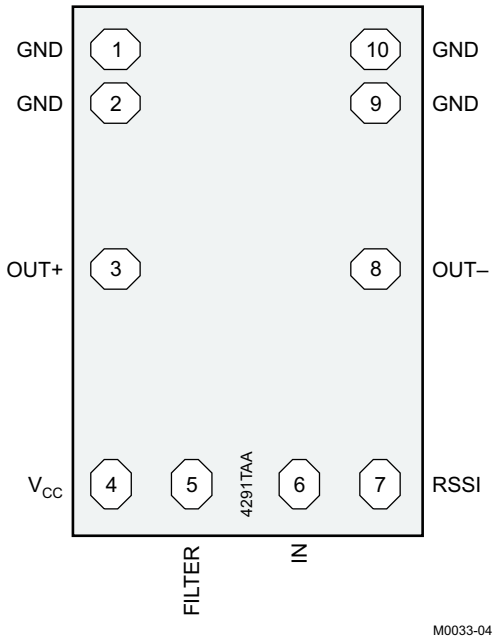
## BAND-GAP VOLTAGE AND BIAS GENERATION

The ONET4291TA transimpedance amplifier is supplied by a single, 3.3-V supply voltage connected to the $V_{CC}$ pad. This voltage is referred to GND.

On-chip band-gap voltage circuitry generates a supply-voltage-independent reference from which all other internally required voltages and bias currents are derived.

## BOND PAD ASSIGNMENT

The ONET4291TA is available as a bare die. The locations of the bond pads are shown in the following figure.




### BOND PAD DESCRIPTION

| PAD | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| FILTER | 5 | Analog | Bias voltage for photodiode (cathode). This pads connects through an internal 220-Ω resistor to $V_{CC}$ and a 200-pF filter capacitor to ground (GND). The FILTER pad(s) must be connected to the photodiode for the AGC to function. |
| GND | 1, 2, 9, 10 | Supply | Circuit ground. All GND pads are connected on die. Bonding all pads is optional; however, for optimum performance a good ground connection is mandatory. |
| IN | 6 | Analog input | Data input to TIA (photodiode anode) |
| OUT+ | 3 | Analog output | Non-inverted data output. On-chip 50-Ω back-terminated to $V_{CC}$. |
| OUT– | 8 | Analog output | Inverted data output. On-chip 50-Ω back-terminated to $V_{CC}$. |
| RSSI | 7 | Analog output | Analog output current proportional to the input data amplitude. Indicates the strength of the received signal (RSSI). Must be sunk through an external resistor to ground (GND). The RSSI gain can be adjusted by choosing the external resistor; however, for proper operation, ensure that the voltage at the RSSI pad never exceeds $V_{CC}$ – 0.65 V. If the RSSI feature is not used, this pad must be bonded to ground (GND) to ensure proper operation. |
| $V_{CC}$ | 4 | Supply | 3.3-V, +10%/–12% supply voltage |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

| | | |
|---|---|---|
| $V_{CC}$ | Supply voltage (2) | –0.3 V to 4 V |
| $V_{FILTER}$, $V_{OUT+}$, $V_{OUT–}$, $V_{RSSI}$ | Voltage at FILTER, OUT+, OUT–, RSSI (2) | –0.3 V to 4 V |
| $I_{IN}$ | Current into IN | –0.7 mA to 2.5 mA |
| $I_{FILTER}$ | Current into FILTER | – 8 mA to 8 mA |
| $I_{OUT+}$, $I_{OUT–}$ | Continuous current at outputs | – 8 mA to 8 mA |
| ESD | ESD rating at all pins except IN (3) | 1.5 kV (HBM) |
| | ESD rating at IN (3) | 300 V (HBM) |
| $T_{J,max}$ | Maximum junction temperature | 125°C |
| $T_{stg}$ | Storage temperature range | –65°C to 85°C |
| $T_A$ | Operating free-air temperature range | –40°C to 85°C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) For optimum high-frequency performance, the input pin has reduced ESD protection.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 2.9 | 3.3 | 3.6 | V |
| $T_A$ | Operating free-air temperature | –40 | | 85 | °C |
| $L_{FILTER}$, $L_{IN}$ | Wire-bond inductor at pins FILTER and IN | | | 0.8 | nH |
| $C_{PD}$ | Photodiode capacitance | | 0.2 | | pF |

## DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted). Typical values are at $V_{CC}$ = 3.3 V and $T_A$ = 25°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.9 | 3.3 | 3.6 | V |
| $I_{VCC}$ | Supply current | Average photodiode current $I_{PD}$ = 0 mA | 11 | 17 | 25 | mA |
| $V_{IN}$ | Input bias voltage | | | 0.85 | 1.05 | V |
| $R_{OUT}$ | Output resistance | Single-ended to $V_{CC}$ | 40 | 50 | 60 | Ω |
| $R_{FILTER}$ | Photodiode filter resistance | | | 220 | | Ω |

## AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted). Typical values are at $V_{CC}$ = 3.3 V and $T_A$ = 25°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $i_{IN-OVL}$ | AC input overload current | | 2 | | | $mA_{p-p}$ |
| $A_{RSSI}$ | RSSI gain | Resistive load to GND (1) | 0.95 | 1 | 1.05 | A/A |
| | RSSI output offset current (no light) | | | 15 | 30 | µA |
| $Z_{21}$ | Small-signal transimpedance | Differential output; input current $i_{IN}$ = 50 $\mu A_{p-p}$ | 2300 | 3200 | 3900 | Ω |
| $f_{H,3dB}$ | Small-signal bandwidth | $i_{IN}$ = 50 $\mu A_{p-p}$ (2) | 2.2 | 2.8 | | GHz |
| $f_{L,3dB}$ | Low-frequency, –3-dB bandwidth | – 3 dB, input current $i_{IN}$ < 50 $\mu A_{p-p}$ | | 40 | 70 | kHz |
| $f_{H,3dB,RSSI}$ | RSSI bandwidth | | | 3.5 | | MHz |
| $i_{N-IN}$ | Input referred RMS noise | 50 kHz–4 GHz (3) | | 465 | 590 | nA |
| | Input referred noise current density | | | 8.8 | | pA/√Hz |
| DJ | Deterministic jitter | $i_{IN}$ = 50 $\mu A_{p-p}$ (K28.5 pattern) (4) | | 10 | 23 | $ps_{p-p}$ |
| | | $i_{IN}$ = 100 $\mu A_{p-p}$ (K28.5 pattern) (4) | | 10 | 30 | |
| | | $i_{IN}$ = 1 $mA_{p-p}$ (K28.5 pattern) | | 8 | 28 | |
| | | $i_{IN}$ = 2 $mA_{p-p}$ (K28.5 pattern) | | 13 | 42 | |
| $V_{OUT,D,MAX}$ | Maximum differential output voltage | Input current $i_{IN}$ = 1 $mA_{p-p}$ | 140 | 200 | 310 | $mV_{p-p}$ |

(1) The RSSI output is a current output, which requires a resistive load to ground (GND). The voltage gain can be adjusted for the intended application by choosing the external resistor. However, for proper operation of the ONET4291TA, ensure that the voltage at RSSI never exceeds $V_{CC}$ – 0.65 V.

(2) The minimum small-signal bandwidth is specified over process corners, temperature, and supply voltage variation. The assumed photodiode capacitance is 0.2 pF. The bond-wire inductance is 0.8 nH. The small-signal bandwidth strongly depends on environmental parasitics. Careful attention to layout parasitics and external components is necessary to achieve optimal performance.

(3) Input referred RMS noise is (RMS output noise)/(gain @ 100 MHz). The maximum input referred noise is specified over process corners, temperature, and supply voltage variation.

(4) At small input currents a significant portion of the deterministic jitter (DJ) is caused by duty-cycle distortion (DCD) due to residual offset in the output signal. Because the TIA is not limiting, the DCD portion of the DJ is removed by the following limiting amplifier. The given maximum values include DCD as well as six-sigma margin.

## TYPICAL CHARACTERISTICS

Typical operating condition is at $V_{CC}$ = 3.3 V and $T_A$ = 25°C.

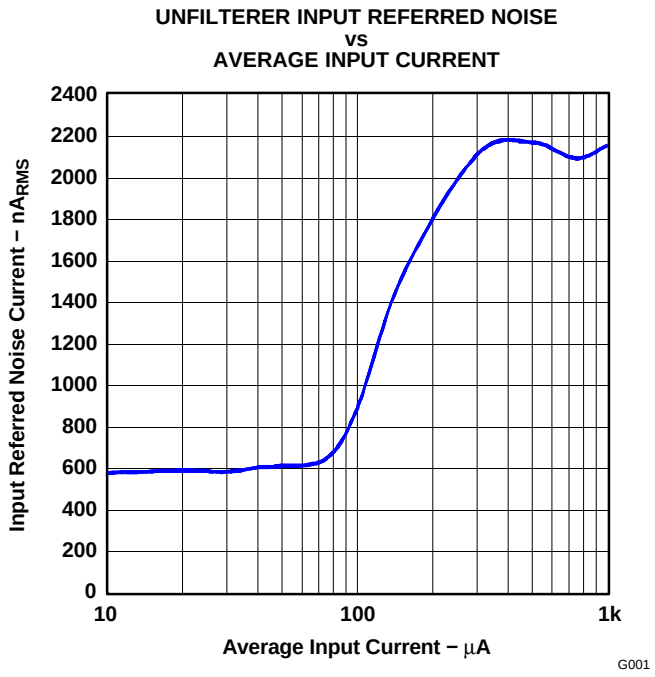



Figure 2.

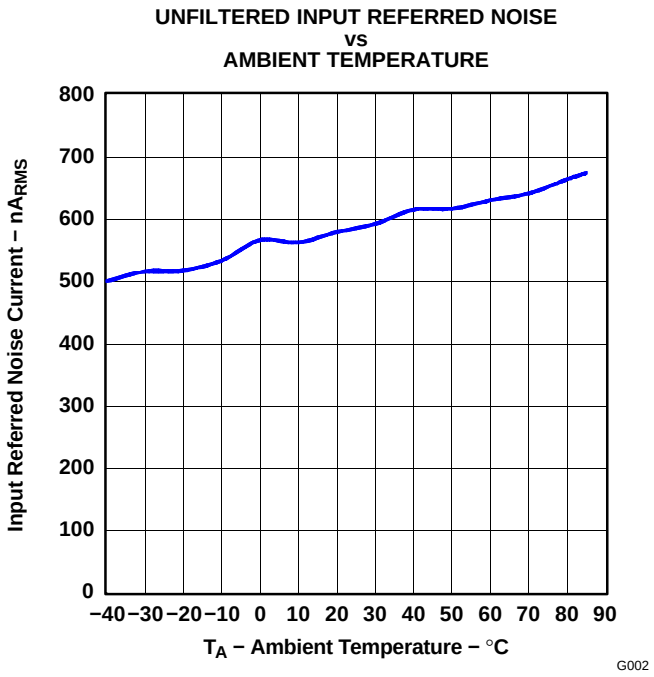



Figure 3.

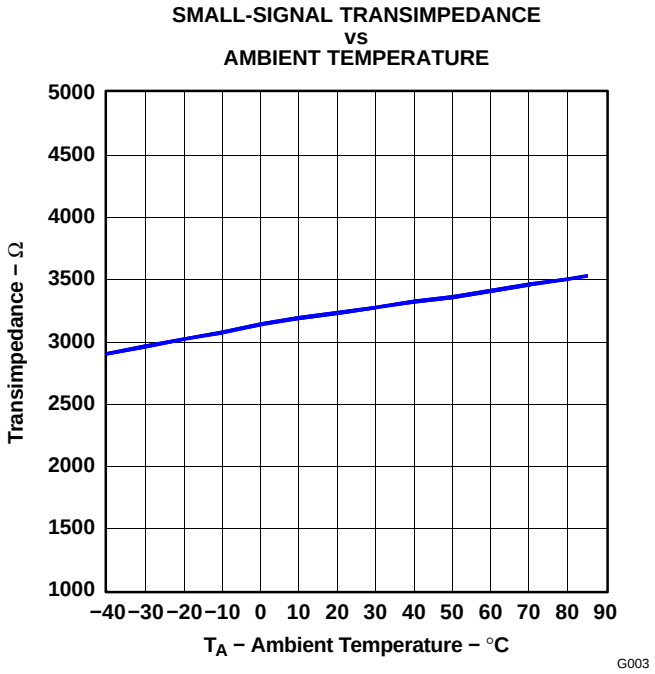



Figure 4.

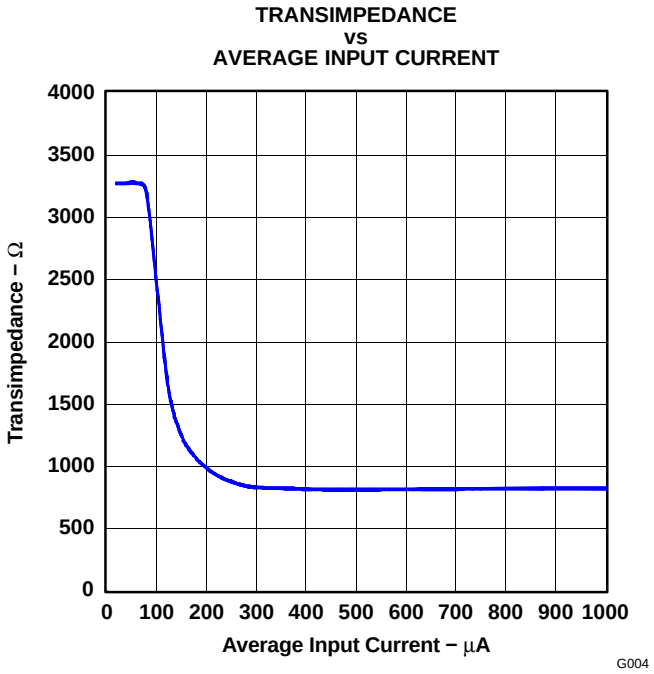



Figure 5.

## TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC}$ = 3.3 V and $T_A$ = 25°C.

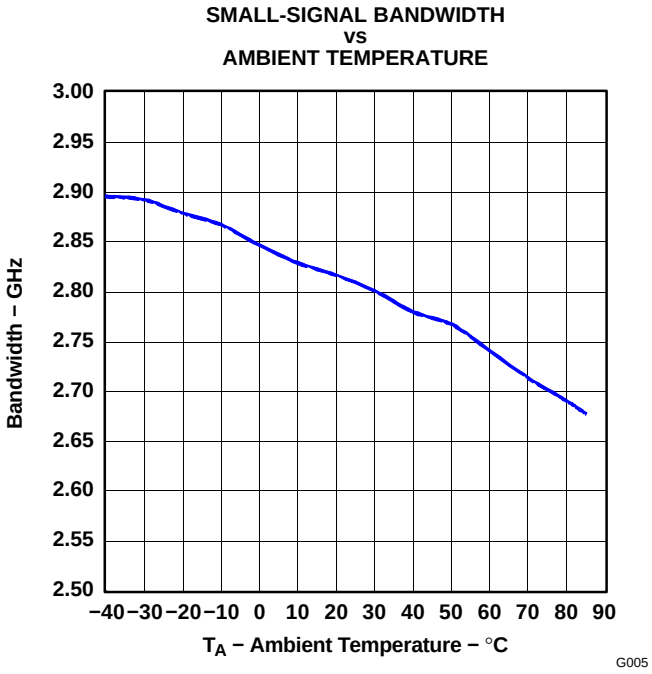



Figure 6.

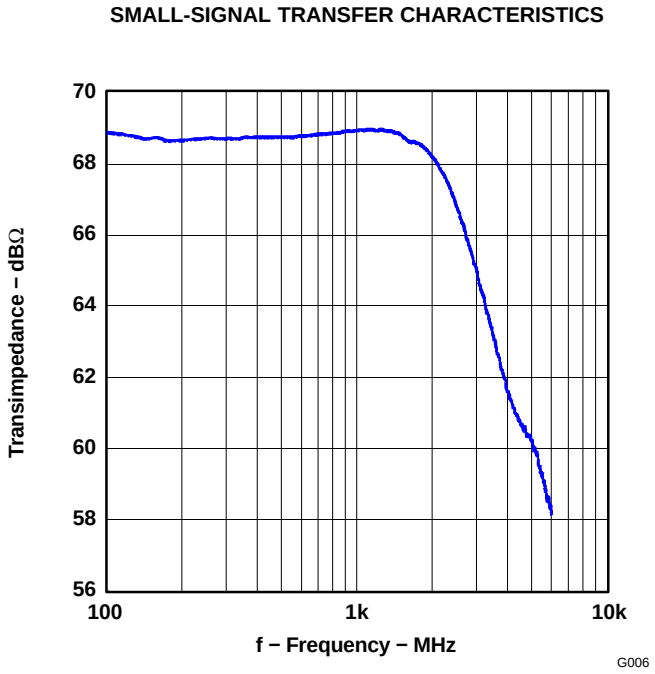



Figure 7.

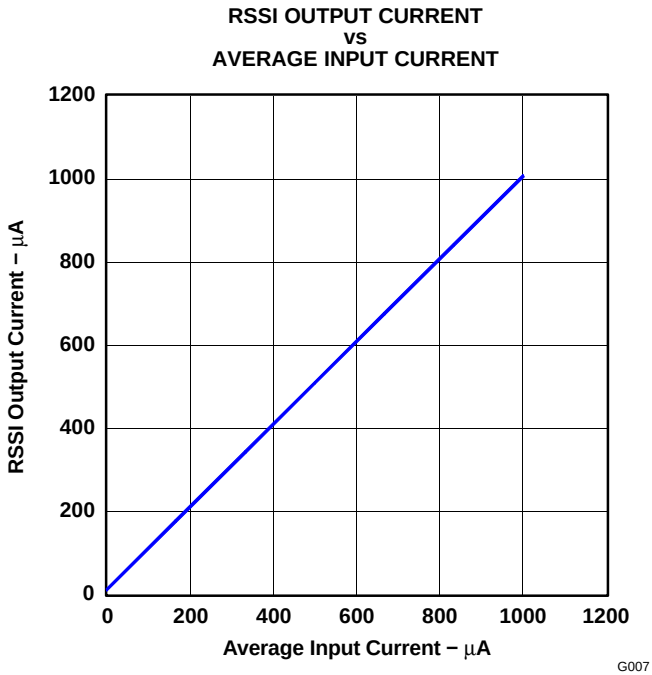



Figure 8.

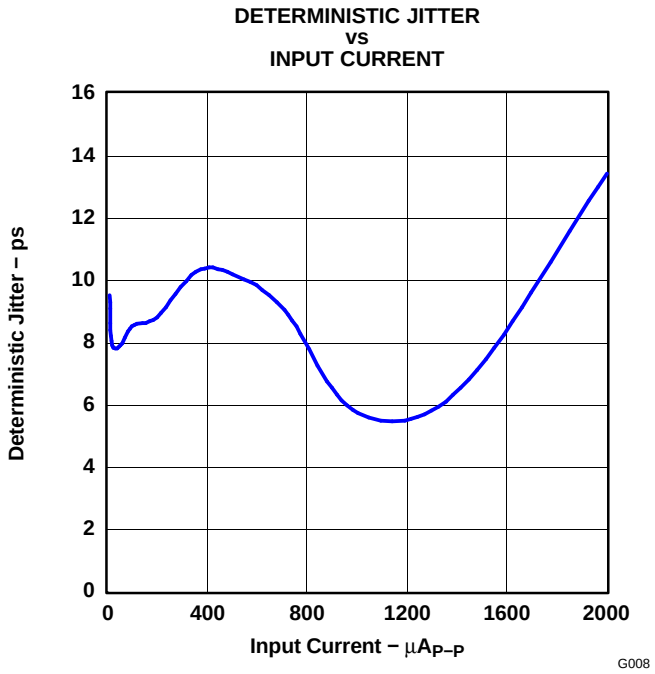



Figure 9.

## TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC}$ = 3.3 V and $T_A$ = 25°C.

**OUTPUT EYE DIAGRAM AT 4.25 Gbps AND 10-$\mu A_{p-p}$ INPUT CURRENT**

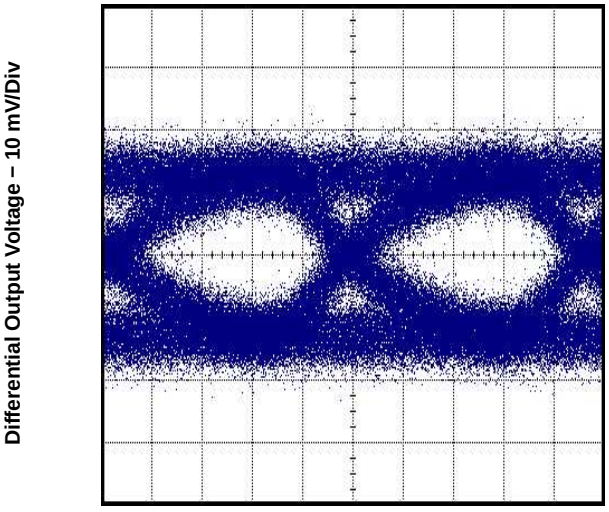



**Figure 10.**

**OUTPUT EYE DIAGRAM AT 4.25 Gbps AND 20-$\mu A_{p-p}$ INPUT CURRENT**

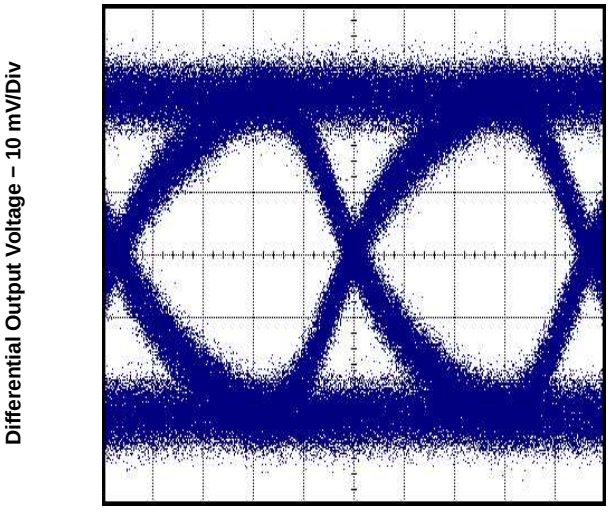



**Figure 11.**

**OUTPUT EYE DIAGRAM AT 4.25 Gbps AND 100-$\mu A_{p-p}$ INPUT CURRENT**

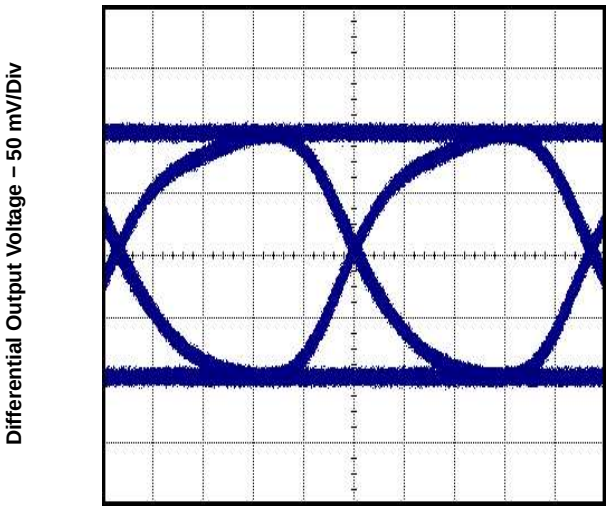



**Figure 12.**

**OUTPUT EYE DIAGRAM AT 4.25 Gbps AND 1-$mA_{p-p}$ INPUT CURRENT**

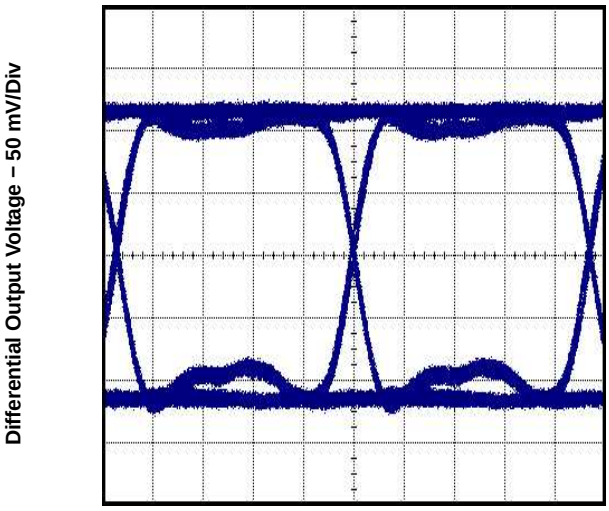



**Figure 13.**

## TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC}$ = 3.3 V and $T_A$ = 25°C.

**OUTPUT EYE DIAGRAM AT 4.25 Gbps AND 2-m$A_{p-p}$ INPUT CURRENT**

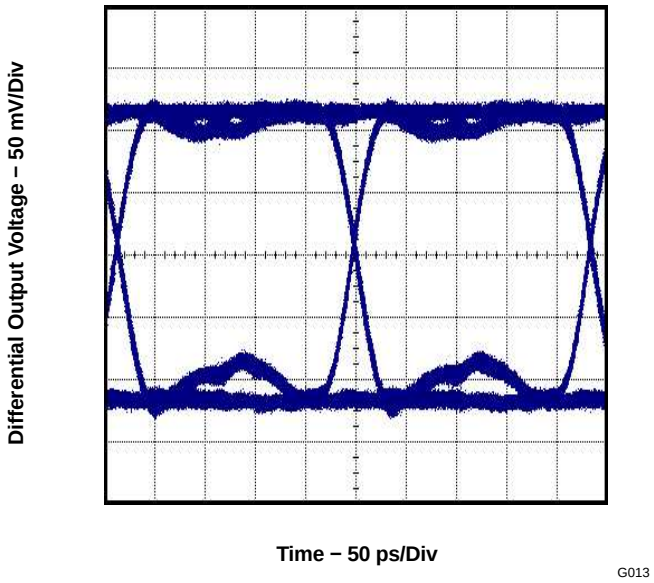



**Figure 14.**

## APPLICATION INFORMATION

Figure 15 shows an application circuit for an ONET4291TA being used in a typical fiber-optic receiver. The ONET4291TA converts the electrical current generated by the PIN photodiode into a differential output voltage. The FILTER input provides a dc bias voltage for the PIN that is low-pass filtered by the combination of the internal 220-Ω resistor and 200-pF capacitor. Because the voltage drop across the 220-Ω resistor is sensed and used by the AGC circuit, the photodiode must be connected to a FILTER pad for the AGC to function correctly.

The RSSI output is used to mirror the photodiode average current and must be connected via a resistor to GND. The voltage gain can be adjusted for the intended application by choosing the external resistor. However, for proper operation of the ONET4291TA, ensure that the voltage at RSSI never exceeds $V_{CC}$ – 0.65 V. If the RSSI output is not used, it must be grounded.

The OUT+ and OUT– pads are internally terminated by 50-Ω pullup resistors to $V_{CC}$. The outputs must be ac-coupled (e.g., using C1 = C2 = 0.1 μF) to the succeeding device. An additional capacitor, $C_{NBW}$, which is differentially connected between the two output pins OUT+ and OUT–, can be used to limit the noise bandwidth and thus optimize the noise performance.

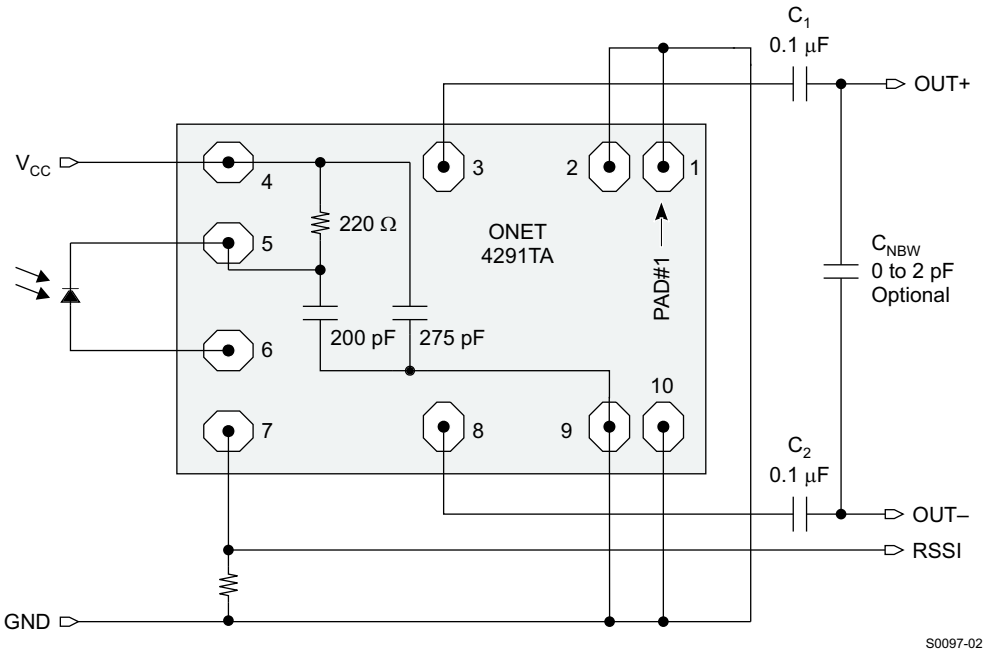



**Figure 15. Basic Application Circuit**

## ASSEMBLY RECOMMENDATIONS

When packaging the ONET4291TA, careful attention to parasitics and external components is necessary to achieve optimal performance. Recommendations that optimize performance include:

1. Minimize total capacitance on the IN pad by using a low-capacitance photodiode and paying attention to stray capacitances. Place the photodiode close to the ONET4291TA die to minimize the bond wire length and thus the parasitic inductance.
2. Use identical termination and symmetrical transmission lines at the ac-coupled differential output pins OUT+ and OUT–. A differential capacitor $C_{NBW}$ can be used to limit the noise bandwidth.
3. Use short bond-wire connections for the supply terminals $V_{CC}$ and GND. Supply-voltage filtering is provided on-chip. Filtering can be improved by using an additional external capacitor.

## CHIP DIMENSIONS AND PAD LOCATIONS

Overall chip dimensions and depiction of the bond-pad locations are given in Figure 16. Layout of the chip componentry is shown in Figure 17.

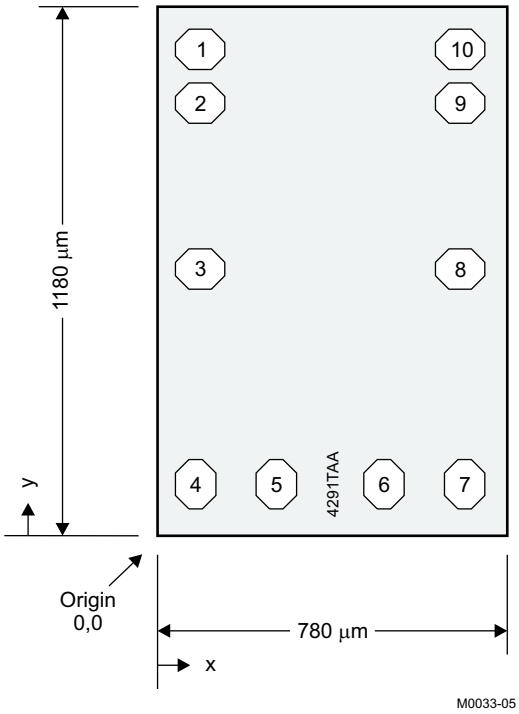



**Figure 16. Chip Dimensions and Pad Locations**

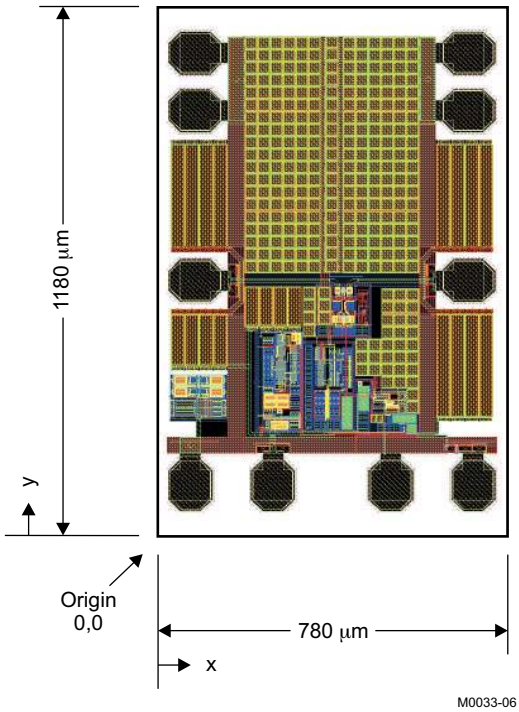



**Figure 17. Chip Layout**

**Pad Locations and Descriptions for the ONET4291TA**

| PAD | COORDINATES | | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| | x (μm) | y (μm) | | | |
| 1 | 100 | 1063 | GND | Supply | Circuit ground |
| 2 | 100 | 938 | GND | Supply | Circuit ground |
| 3 | 100 | 570 | OUT+ | Analog output | Non-inverted data output |
| 4 | 90 | 127 | $V_{CC}$ | Supply | 3.3-V supply voltage |
| 5 | 265 | 127 | FILTER | Analog | Bias voltage for photodiode |
| 6 | 515 | 127 | IN | Analog input | Data input to TIA |
| 7 | 690 | 127 | RSSI | Analog output | RSSI output signal |
| 8 | 680 | 570 | OUT– | Analog output | Inverted data output |
| 9 | 680 | 938 | GND | Supply | Circuit ground |
| 10 | 680 | 1063 | GND | Supply | Circuit ground |

## DIE INFORMATION

Die size: 1180 μm × 780 μm
Die thickness: 8 mils (203 μm)
Pad metallization: 99.5% Al, 0.5% Cu
Pad size: octagonal pads 120 μm × 100 μm
Passivation composition: 6000-Å silicon nitride
Backside contact: none
Die ID: 4291TAA

## TO46 LAYOUT EXAMPLES

Examples for layouts (top view) in 5-pin and 4-pin TO46 headers are given in Figure 18 and Figure 19, respectively.

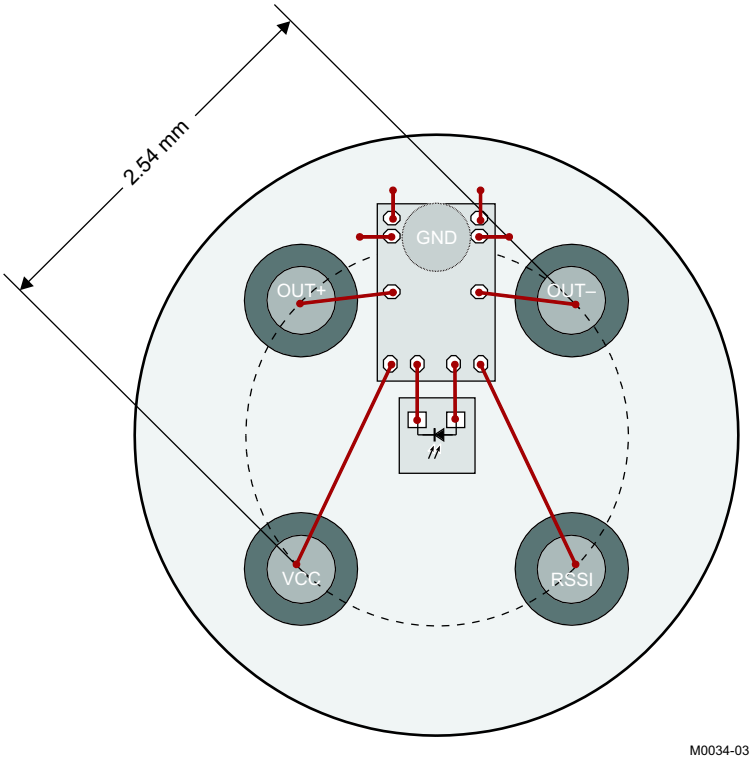



**Figure 18. TO46 5-Pin Layout Example Using the ONET4291TA**

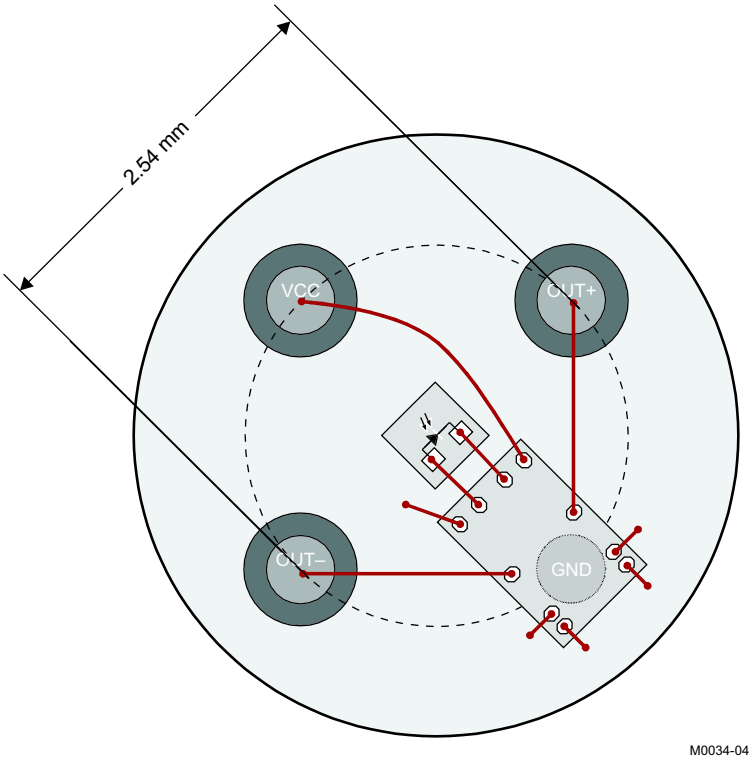



**Figure 19. TO46 4-Pin Layout Example Using the ONET4291TA**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ONET4291TAY | ACTIVE | DIESALE | Y | 0 | 1 | TBD | Call TI | Call TI | -40 to 85 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## IMPORTANT NOTICE AND DISCLAIMER

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