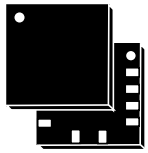
LIS2DS12

MEMS digital output motion sensor: ultra-low-power, high-performance 3-axis "pico" accelerometer

Datasheet - production data



LGA-12 (2.0x2.0x0.86 mm)

Features

- Supply voltage, 1.62 V to 1.98 V
- Independent IOs supply (1.8 V) and supply voltage compatible
- Ultra-low power consumption
- ±2*g*/±4*g*/±8*g*/±16*g* full scale
- High-speed I^2C/SPI digital output interface
- Low noise
- 16-bit data output
- Embedded temperature sensor
- Self-test
- 256-level FIFO
- 10000 *g* high shock survivability
- ECOPACK®, RoHS and “Green” compliant

Applications

- Motion-activated functions and user interfaces
- Gesture recognition and gaming
- Pedometer, step detector and step counters
- Display orientation
- Sensor hub function
- Tilt function
- Tap/double-tap recognition
- 6D/4D orientation
- Free-fall detection
- Smartpower saving for handheld devices
- Impact recognition and logging

Description

The LIS2DS12 is an ultra-low-power, high-performance three-axis linear accelerometer belonging to the “pico” family which leverages on the robust and mature manufacturing processes already used for the production of micromachined accelerometers.

The LIS2DS12 has user-selectable full scales of ±2*g*/±4*g*/±8*g*/±16*g* and is capable of measuring accelerations with output data rates from 1 Hz to 6400 Hz.

The LIS2DS12 has an integrated 256-level first-in, first-out (FIFO) buffer allowing the user to store data in order to limit intervention by the host processor.

The embedded self-test capability allows the user to check the functioning of the sensor in the final application.

The LIS2DS12 has a dedicated internal engine architecture in order to process internally motion and acceleration detection including free-fall, wakeup, single and double-tap detection, activity-inactivity, portrait and landscape detection, step counter and step detection along with significant motion detection.

The LIS2DS12 is available in a small thin plastic land grid array package (LGA) and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Order codes	Temperature range [°C]	Package	Packaging
LIS2DS12	-40 to +85	LGA-12	Tray
LIS2DS12TR	-40 to +85	LGA-12	Tape and reel

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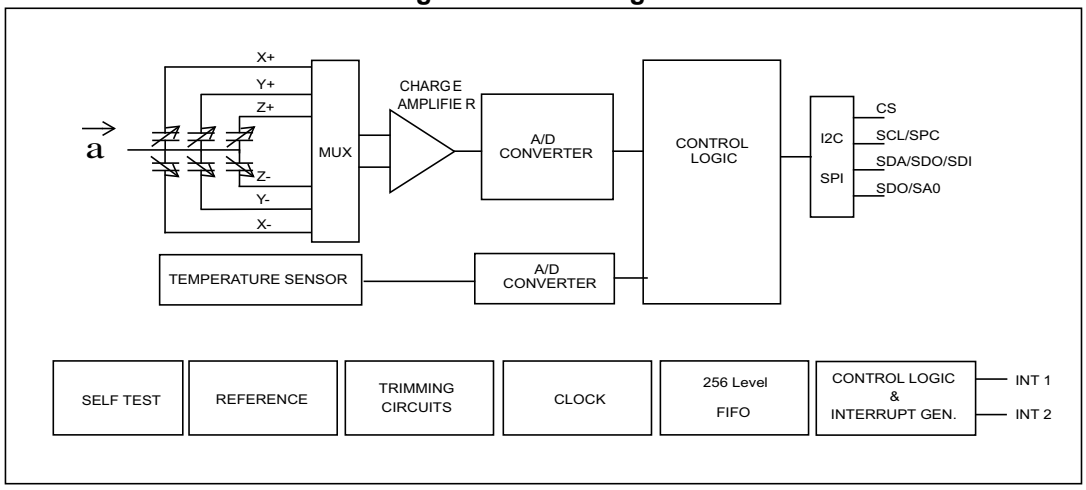
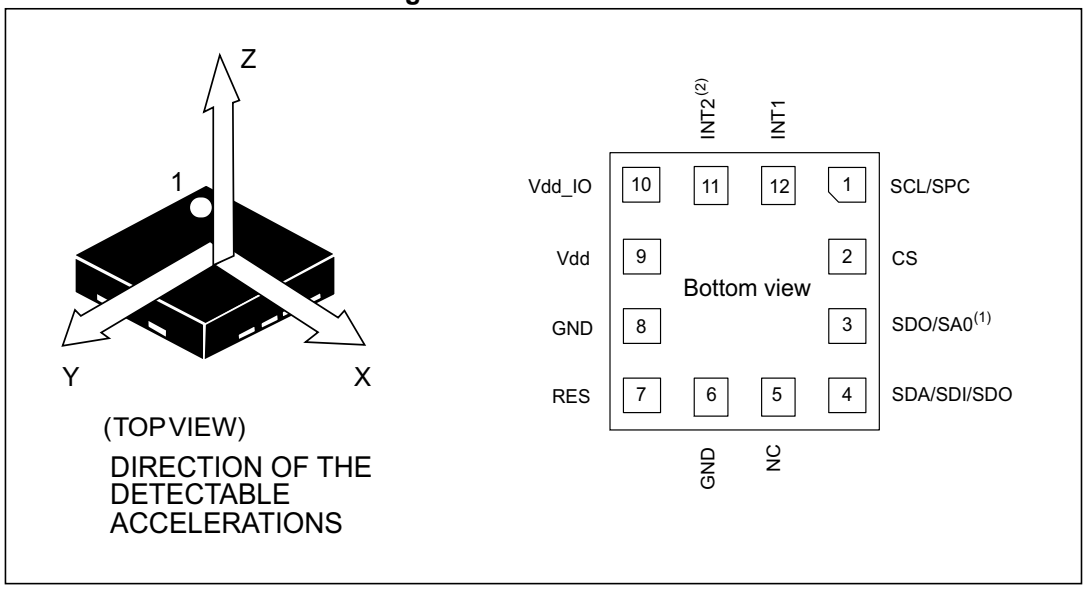
1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections



1. When the sensor hub is used, this pin is the I^2C data master line (MSDA).
2. When sensor hub is used, this pin is the I^2C clock master line (MSCL).

Table 2. Pin description

Pin#	Name	Function
1	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
2(1)	CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
3(2)	SDO SA0	SPI serial data output (SDO) I^2C less significant bit of the device address (SA0)
4	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	NC	Internally not connected. Can be tied to Vdd, Vdd_IO or GND.
6	GND	0 V supply
7	RES	Connect to GND
8	GND	0 V supply
9	Vdd	Power supply
10	Vdd_IO	Power supply for I/O pins
11(3)	INT2	Interrupt pin 2
12	INT1	Interrupt pin 1

1. CS has an active pull-up and can be left unconnected
2. When the sensor hub is used, this pin is the I^2C data master line (MSDA), is internally set to 0 and can be internally pulled up through the TUD_EN bit of *FUNC_CTRL (3Fh)*.
3. When sensor hub is used, this pin is the I^2C clock master line (MSCL) and can be internally pulled up through the TUD_EN bit of *FUNC_CTRL (3Fh)*.

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

Table 3. Mechanical characteristics @ Vdd = 1.8 V, T = 25 °C unless otherwise noted (1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
FS	Measurement range			±2		*g*
				±4		
				±8		
				±16		
So	Sensitivity 16-bit(3)	@ FS ±2 *g*		0.061		mg/digit
		@ FS ±4 *g*		0.122		
		@ FS ±8 *g*		0.244		
		@ FS ±16 *g*		0.488		
An	Noise density - high-performance mode (HR or HF mode)(4)	@ FS ±2 *g*		120		µg/√Hz
		@ FS ±4 *g*		150		
		@ FS ±8 *g*		200		
		@ FS ±16 *g*		300		
RMS	RMS noise - low-power mode(5)	@ FS ±2 *g*		6.3		mg(RMS)
		@ FS ±4 *g*		8.2		
		@ FS ±8 *g*		11		
		@ FS ±16 *g*		17		
Off, board	Zero-*g* offset on soldered board(6)			±30		mg
TCO	Zero-*g* offset change vs. temperature			±0.2		mg/°C
TCS	Sensitivity change vs. temperature			0.01		%/°C
ST	Self-test positive difference(7)		70		1500	mg

1. The product is factory calibrated at 1.8 V. The operational power supply range is from 1.62 V to 1.98 V.
2. Typical specifications are not guaranteed.
3. Sensitivity calculated at 16-bit.
4. Noise density is the same for all ODR.
5. RMS noise is the same for all ODR.
6. Offset can be eliminated by enabling the slope filter.
7. “Self-test positive difference” is defined as: OUTPUT[mg]$_{(CTRL3\ ST2,\ ST1\ bits=01)}$ - OUTPUT[mg]$_{(CTRL3\ ST2,\ ST1\ bits=00)}$ in steady state.

2.2 Electrical characteristics

Table 4. Electrical characteristics @ Vdd = 1.8 V, T = 25 °C unless otherwise noted (1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
Vdd	Supply voltage		1.62	1.8	1.98	V
Vdd_IO	I/O pins supply voltage(3)		1.62		Vdd+0.1	V
IddHR	Current consumption in high-resolution mode	@ ODR range 12.5 Hz - 6400 Hz, 12-14 bit		150		µA
IddLP	Current consumption in low-power mode	ODR 100 Hz		12.5		µA
		ODR 50 Hz		8		
		ODR 12.5 Hz		4		
		ODR 1 Hz		2.5		
Idd_PD	Current consumption in power-down			0.7		µA
V_{IH}	Digital high-level input voltage		0.8*Vdd_IO			V
V_{IL}	Digital low-level input voltage				0.2*Vdd_IO	V
V_{OH}	Digital high-level output voltage	I_{OH} = 4 mA(4)	VDD_IO - 0.2 V			
V_{OL}	Digital low-level output voltage	I_{OL} = 4 mA(4)			0.2 V	

1. The product is factory calibrated at 1.8 V. The operational power supply range is from 1.62 V to 1.98 V.
2. Typical specifications are not guaranteed.
3. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses. In this condition the measurement chain is powered off.
4. 4 mA is the maximum driving capability, ie. the maximum DC current that can be sourced/sunk by the digital pad in order to guarantee the correct digital output voltage levels V_{OH} and V_{OL}.

2.3 Temperature sensor characteristics

@ Vdd =1.8 V, T=25 °C unless otherwise noted

Table 5. Temperature sensor characteristics

Symbol	Parameter	Min.	Typ.(1)	Max.	Unit
Top	Operating temperature range	-40		+85	°C
Toff	Temperature offset(2)	-15		+15	°C
TSDr	Temperature sensor output change vs. temperature		1		LSB/°C(3)
TODR	Temperature refresh rate		12.5		Hz

1. Typical specifications are not guaranteed.
2. The output of the temperature sensor is 0 LSB (typ.) at 25 °C.
3. 8-bit resolution.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

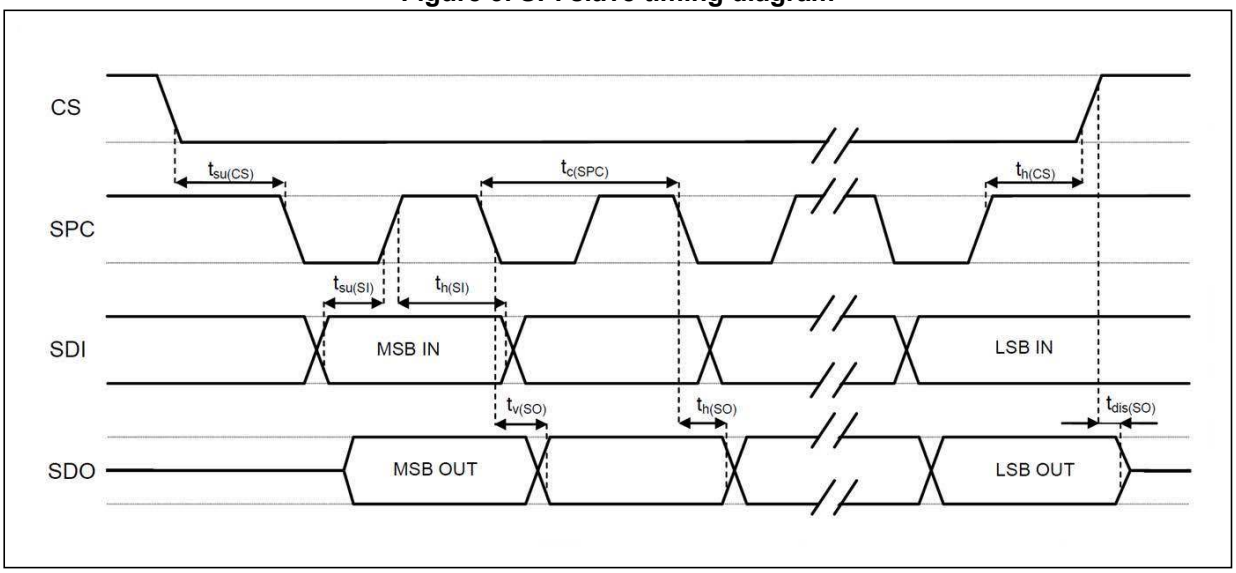
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

1. 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 I²C - inter-IC control interface

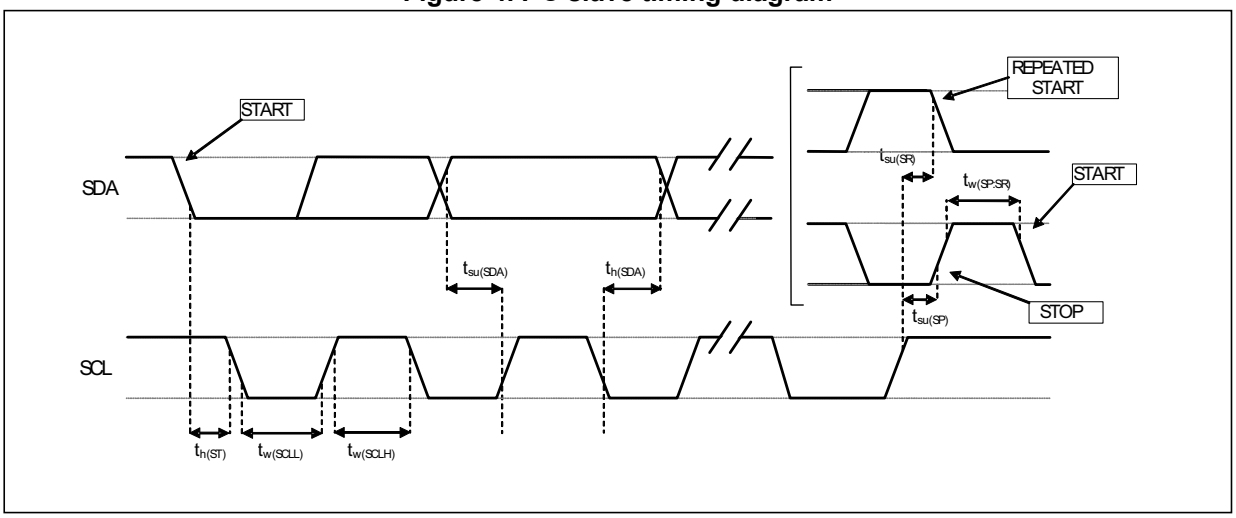
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0.01	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

Table 8. I^2C high-speed mode specifications at 1 MHz and 3.4 MHz

	Symbol	Parameter	Min	Max	Unit
Fast mode plus(1)	f_{SCL}	SCL clock frequency	0	1	MHz
	$t_{HD;STA}$	Hold time (repeated) START condition	260	-	ns
	t_{LOW}	Low period of the SCL clock	500	-	
	t_{HIGH}	High period of the SCL clock	260	-	
	$t_{SU;STA}$	Setup time for a repeated START condition	260	-	
	$t_{HD;DAT}$	Data hold time	0	-	
	$t_{SU;DAT}$	Data setup time	50	-	
	t_{rDA}	Rise time of SDA signal	-	120	
	t_{fDA}	Fall time of SDA signal	-	120	
	t_{rCL}	Rise time of SCL signal	20*Vdd/5.5	120	
	t_{fCL}	Fall time of SCL signal	20*Vdd/5.5	120	
	$t_{SU;STO}$	Setup time for STOP condition	260	-	
	C_b	Capacitive load for each bus line	-	550	pF
	$t_{VD;DAT}$	Data valid time	-	450	ns
	$t_{VD;ACK}$	Data valid acknowledge time	-	450	
	V_{nL}	Noise margin at low level	0.1Vdd	-	V
	V_{nH}	Noise margin at high level	0.2Vdd	-	
	t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0	50	ns
High-speed mode(1)	f_{SCLH}	SCLH clock frequency	0	3.4	MHz
	$t_{SU;STA}$	Setup time for a repeated START condition	160	-	ns
	$t_{HD;STA}$	Hold time (repeated) START condition	160	-	
	t_{LOW}	Low period of the SCLH clock	160	-	
	t_{HIGH}	High period of the SCLH clock	60	-	
	$t_{SU;DAT}$	Data setup time	10	-	
	$t_{HD;DAT}$	Data hold time	0	70	
	t_{rCL}	Rise time of SCLH signal	10	40	
	t_{rCL1}	Rise time of SCLH signal after a repeated START condition and after an acknowledge bit	10	80	
	t_{fCL}	Fall time of SCLH signal	10	40	
	t_{rDA}	Rise time of SDAH signal	10	80	
	t_{fDA}	Fall time of SDAH signal	10	80	
	$t_{SU;STO}$	Setup time for STOP condition	160	-	
	C_b	Capacitive load for each bus line	-	100	pF
	V_{nH}	Noise margin at high level	0.2Vdd	-	V
	t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0	10	ns

1. Data based on characterization, not tested in production

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 9. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 2.2	V
Vdd_IO	I/O pins supply voltage	-0.3 to 2.2	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 1.8 V)	3000 for 0.5 ms	*g*
		10000 for 0.2 ms	*g*
A_{UNP}	Acceleration (any axis, unpowered)	3000 for 0.5 ms	*g*
		10000 for 0.2 ms	*g*
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 2.2 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

2.6 Terminology

2.6.1 Zero-*g* offset

Zero-*g* offset describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on the X-axis and 0 *g* on the Y-axis whereas the Z-axis will measure 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from ideal value in this case is called Zero-*g* offset. Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-*g* offset change vs. temperature".

2.6.2 Sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

2.6.3 Self-test

The self-test allows checking the sensor functionality without moving it. The self-test function is off when the self-test bits (ST) are programmed to '00'. When the self-test bits are changed, an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs will exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified in *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

2.7 Sensing element

A proprietary process is used to create a surface micromachined accelerometer. The technology allows processing suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. In order to be compatible with the traditional packaging techniques, a cap is placed on top of the sensing element to avoid blocking the moving parts during the molding phase of the plastic encapsulation. When an acceleration is applied to the sensor the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the capacitor.

At steady-state the nominal value of the capacitors are a few pF and when an acceleration is applied, the maximum variation of the capacitive load is in the fF range.

2.8 IC interface

The complete measurement chain is composed of a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage using an analog-to-digital converter.

The acceleration data may be accessed through an I^2C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LIS2DS12 features a data-ready signal which indicates when a new set of measured acceleration data is available, thus simplifying data synchronization in the digital system that uses the device.

3 Factory calibration

The IC interface is factory-calibrated for sensitivity (So) and Zero-*g* offset.

The trim values are stored inside the device in nonvolatile memory. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during active operation. This allows using the device without further calibration.

4 Application hints

Figure 5. LIS2DS12 electrical connections in standard configuration (top view)

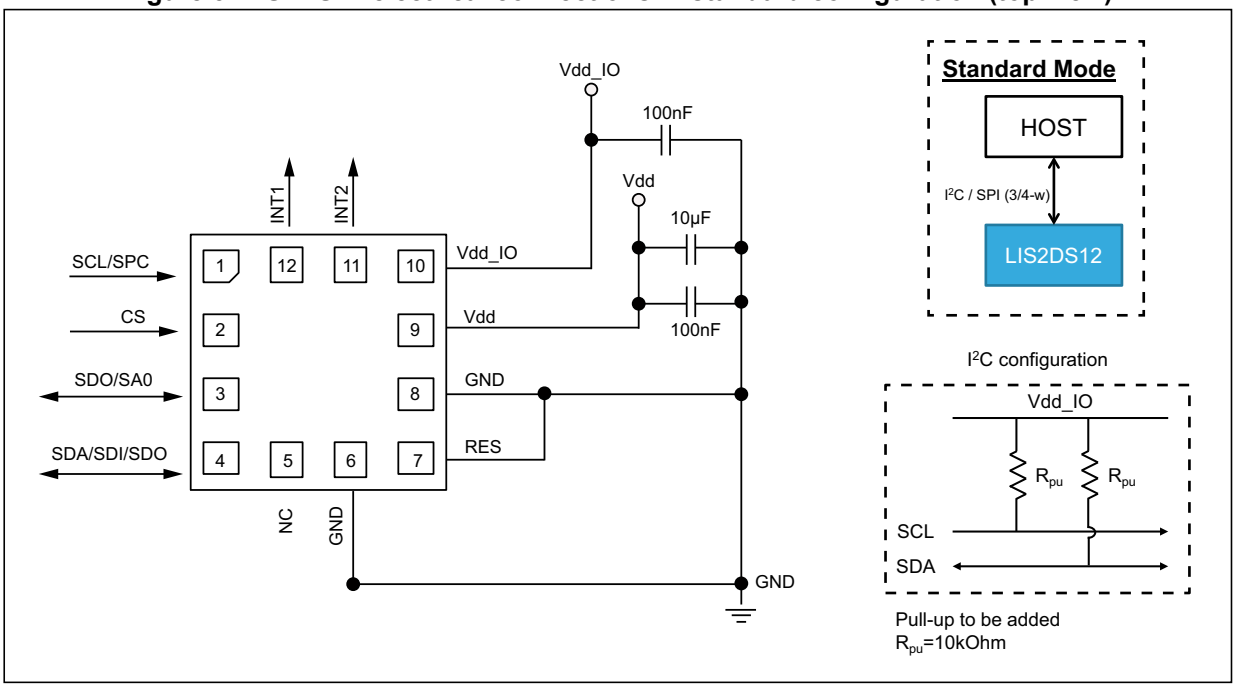
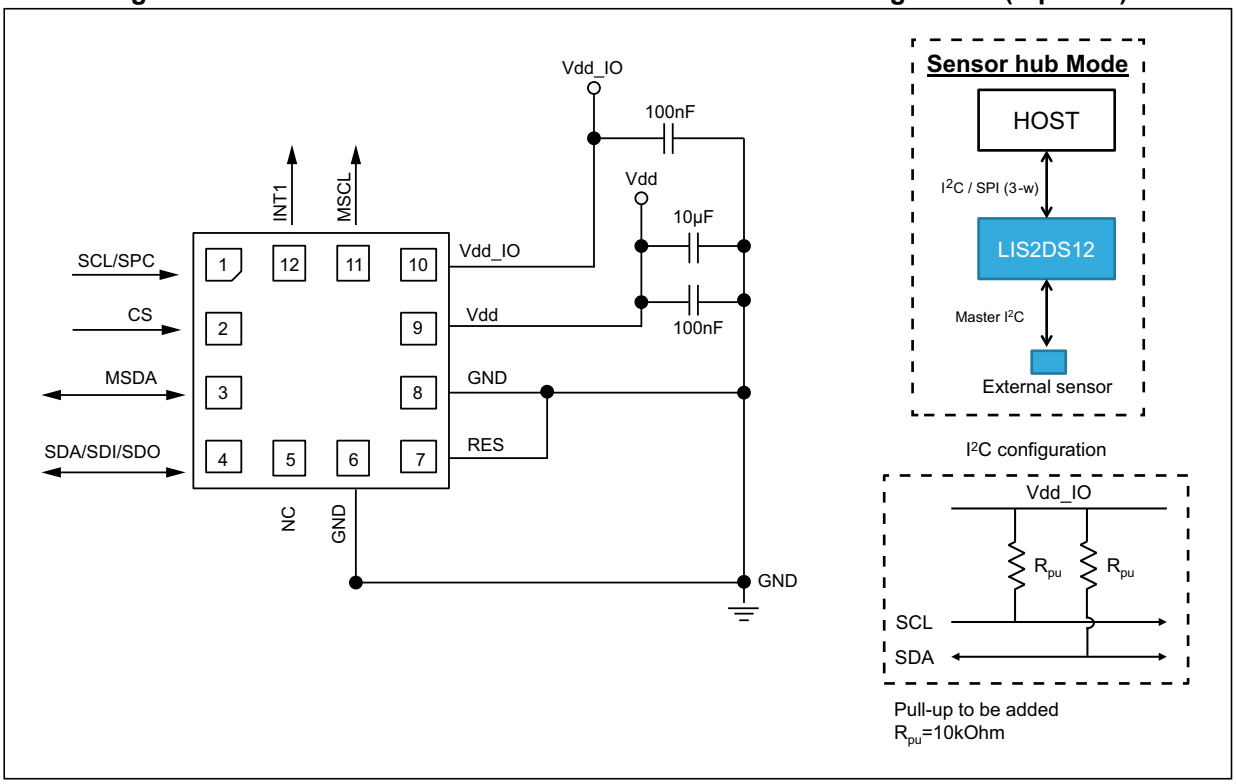


Figure 6. LIS2DS12 electrical connections in sensor hub configuration (top view)



The device core is supplied through the Vdd line while the I/O pads are supplied through the Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to pin 9 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 5* and *Figure 6*). It is possible to remove Vdd while maintaining Vdd_IO without blocking the communication bus, in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data are selectable and accessible through the I^2C or SPI interfaces. When using the I^2C, CS must be tied high (i.e. connected to Vdd_IO).

The functions, the threshold and the timing of the two interrupt pins (INT1 and INT2) can be completely programmed by the user through the I^2C/SPI interface.

Table 10. Internal pin status

Pin #	Name	Function	Pin status
1	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)	Default: input without pull-up
2	CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled 0: SPI communication mode / I^2C disabled)	Default: input with internal pull-up
3	SDO SA0	Serial data output (SDO) I^2C less significant bit of the device address (SA0)	Default: input without internal pull-up
4	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)	Default: (SDA) input without pull-up
5	NC	Internally not connected. Can be tied to Vdd, Vdd_IO or GND.	
6	GND	0 V supply	
7	RES	Connect to GND	
8	GND	0 V supply	
9	Vdd	Power supply	
10	Vdd_IO	Power supply for I/O pins	
11	INT2	Interrupt pin 2	Default: push-pull output forced to Gnd
12	INT1	Interrupt pin 1	Default: push-pull output forced to Gnd

5 Digital main blocks

5.1 Power modes

The LIS2DS12 provides two different power modes: high-resolution (including high-frequency mode) and low-power modes.

The tables below summarize the selection of the different operating modes as well as the low-pass filter and current consumption.

Table 11. Operating modes

CTRL1(ODR[3:1])	CTRL1(HF_ODR)	ODR selection [Hz]	Mode
Low-power mode			
0000	-	-	PD
1000	-	1	LP
1001	-	12.5	
1010	-	25	
1011	-	50	
1100	-	100	
1101	-	200	
1110	-	400	
1111	-	800	
High-resolution mode			
0001	-	12.5	HR
0010	-	25	
0011	-	50	
0100	-	100	
0101	0	200	
0110	0	400	
0111	0	800	
0101	1	1600	HF
0110	1	3200	
0111	1	6400	

Table 12. Low-pass filter in low-power, high-resolution and high-frequency modes

ODR [Hz]	LPF cutoff [Hz]
Low-power mode	
800	3200
400	
200	
100	
50	
25	
12.5	
1	
High-resolution mode	
800	355
400	177
200	88
100	44
50	22
25	11
12.5	5.5
High-frequency mode	
6400	2840
3200	1420
1600	710

Table 13. Current consumption of operating modes

ODR (Hz)	Typical current consumption in high-resolution/high-frequency mode [µA]	Typical current consumption in low-power mode [µA]
1	-	2.5
12.5	150	4
25		5.5
50		8
100		12.5
200		22
400		41
800		80
1600		-
3200		-
6400		-

5.2 Activity/Inactivity function

The Activity/Inactivity recognition function allows reducing the power consumption of the system in order to develop new smart applications.

When the Activity/Inactivity recognition function is activated, the LIS2DS12 is able to automatically go to 12.5 Hz sampling rate and to wake up as soon as the interrupt event has been detected, increasing the output data rate and bandwidth.

With this feature the system may be efficiently switched from low-power mode to full performance depending on user-selectable positioning and acceleration events, thus ensuring power saving and flexibility.

The Activity/Inactivity recognition function is activated by writing the desired threshold in the *WAKE_UP_THS (33h)* register. The high-pass filter is automatically enabled.

If the device is in Sleep (Inactivity) mode, when at least one of the axes exceeds the threshold in the *WAKE_UP_THS (33h)* the device goes into Sleep-to-Wake (as Wake-Up).

Activity/Inactivity threshold and duration can be configured in the control registers:

WAKE_UP_THS (33h)

WAKE_UP_DUR (34h)

5.3 Data stabilization time vs. ODR setting

The data stabilization time required when an ODR change is applied in order to have valid usable data depends on the ODR selected and device setting.

The table below provides the number of samples to be discarded in order to obtain valid usable data.

Table 14. Number of samples to be discarded

ODR [Hz]	HF	HR	LP
6400	6	-	-
3200	2	-	-
1600	1	-	-
800	-	1	0
400	-	1	0
200	-	1	0
100	-	1	0
50	-	0	0
25	-	0	0
12.5	-	0	0
1	-	-	0

5.4 FIFO

The LIS2DS12 embeds 256 slots of 14-bit data FIFO for each of the three output channels, X, Y and Z of the acceleration module. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

The internal FIFO allows collecting 256 samples (14-bit size data) for each axis or storing the output of the module computation up to 768 samples (14-bit size data).

When the FIFO mode is other than Bypass, reading the output registers (28h to 2Dh) returns the oldest FIFO sample set. In order to minimize communication between the master and slave, the address read may be automatically incremented by the device by setting the IF_ADD_INC bit of *CTRL2 (21h)* to '1'; the device rolls back to 0x28 when register 0x2D is reached.

This buffer can work according to the following 5 different modes:

- Bypass mode
- FIFO mode
- Continuous-to-FIFO
- Bypass-to-Continuous
- Continuous

Each mode is selected by the FIFO_MODE bits in the *FIFO_CTRL (25h)* register.

Programmable FIFO threshold status, FIFO overrun events and the number of unread samples stored are available in the *FIFO_SRC (2Fh)* and *FIFO_SAMPLES (30h)* registers and can be set to generate dedicated interrupts on the INT1 and INT2 pins using the *CTRL4 (23h)* and *CTRL5 (24h)* registers.

FIFO_SRC (2Fh) (FIFO_FTH) goes to '1' when the number of unread samples *FIFO_SRC (2Fh)* and *FIFO_SAMPLES (30h)* (Diff[8:0]) is greater than or equal to FTH [7:0] in *FIFO_THS (2Eh)*.

If FTH [7:0] is equal to '0', *FIFO_SRC (2Fh)* (FIFO_FTH) goes to '0'.

FIFO_SRC (2Fh) (FIFO_OVRN) is equal to '1' if a FIFO slot is overwritten.

FIFO_SRC (2Fh) and *FIFO_SAMPLES (30h)* (Diff[8:0]) contain stored data levels of unread samples. When Diff[8:0] is equal to '000000000', FIFO is empty. When Diff[8:0] is equal to '100000000', FIFO is full and the unread samples are 256.

When the FIFO threshold status flag is '0'-logic, FIFO filling is lower than the threshold level and when '1'-logic, FIFO filling is equal to or higher than the threshold level.

5.4.1 Bypass mode

In Bypass mode (*FIFO_CTRL (25h)* (FMODE [2:0])= 000), the FIFO is not operational, no data is collected in FIFO memory, and it remains empty with the only actual sample available in the output registers.

Bypass mode is also used to reset the FIFO when in FIFO mode.

For each channel only the first address is used. When new data is available, the old data is overwritten.

5.4.2 FIFO mode

In FIFO mode (*FIFO_CTRL (25h)* (FMODE [2:0])= 001) data from the X, Y and Z channels are stored in the FIFO until it is full, when 256 unread samples are stored in memory, data collecting is stopped.

To reset the FIFO content, Bypass mode should be written in the *FIFO_CTRL (25h)* register, setting the FMODE [2:0] bits to '000'. After this reset command, it is possible to restart FIFO mode, writing the value '001' in *FIFO_CTRL (25h)* (FMODE [2:0]).

The FIFO buffer can memorize 256 slots of X, Y and Z data.

5.4.3 Continuous mode

Continuous mode (*FIFO_CTRL (25h)* (FMODE[2:0] = 110) provides a continuous FIFO update: when 256 unread samples are stored in memory, as new data arrives the oldest data is discarded and overwritten by the newer.

A FIFO threshold flag *FIFO_CTRL (25h)* (FIFO_FTH) is asserted when the number of unread samples in FIFO is greater than or equal to *FIFO_THS (2Eh)* (FTH[7:0]).

It is possible to route *FIFO_CTRL (25h)*(FTH) to the INT1 pin by writing the INT1_FTH bit to '1' in register *CTRL4 (23h)* or to the INT2 pin by writing the INT2_FTH bit to '1' in register *CTRL5 (24h)*.

If an overrun occurs, the oldest sample in FIFO is overwritten and the FIFO_OVR flag in *FIFO_SRC (2Fh)* is asserted.

In order to empty the FIFO before it is full, it is also possible to pull from FIFO the number of unread samples available in *FIFO_SRC (2Fh)* and *FIFO_SAMPLES (30h)* (Diff[8:0]).

5.4.4 Continuous-to-FIFO mode

In Continuous-to-FIFO mode *FIFO_CTRL (25h)* (FMODE [2:0] = 011), FIFO operates in Continuous mode and FIFO mode starts upon an internal trigger event. When the FIFO is full, data collecting is stopped.

Figure 7. Continuous-to-FIFO mode

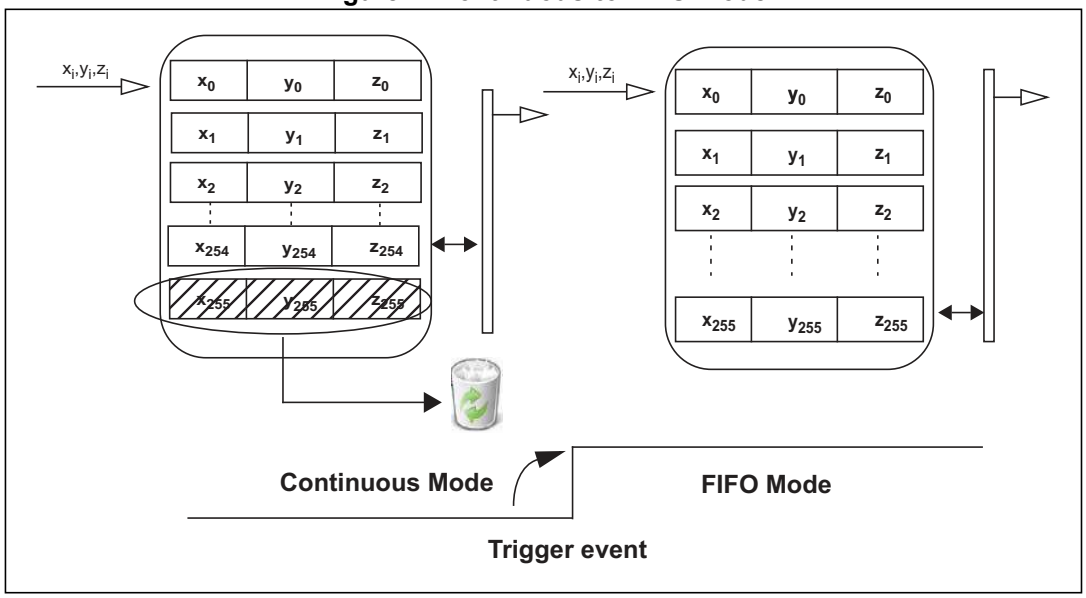
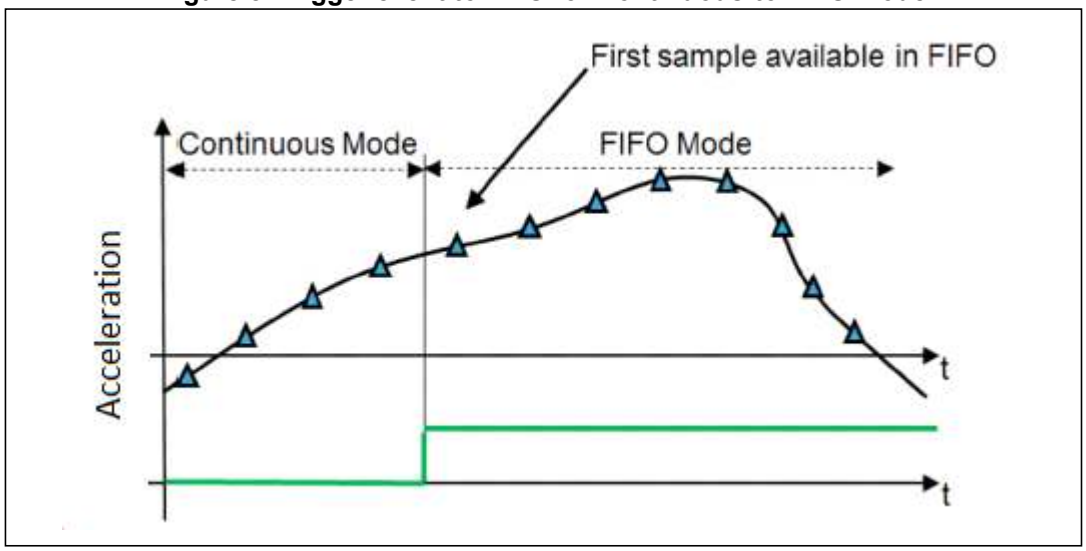


Figure 8. Trigger event to FIFO for Continuous-to-FIFO mode



5.4.5 Bypass-to-Continuous mode

In Bypass-to-Continuous mode (*FIFO_CTRL (25h)*(FMODE[2:0] = '100'), data measurement storage inside FIFO starts in Continuous mode upon an internal trigger event, then the sample that follows the trigger is available in FIFO.

Figure 9. Bypass-to-Continuous mode

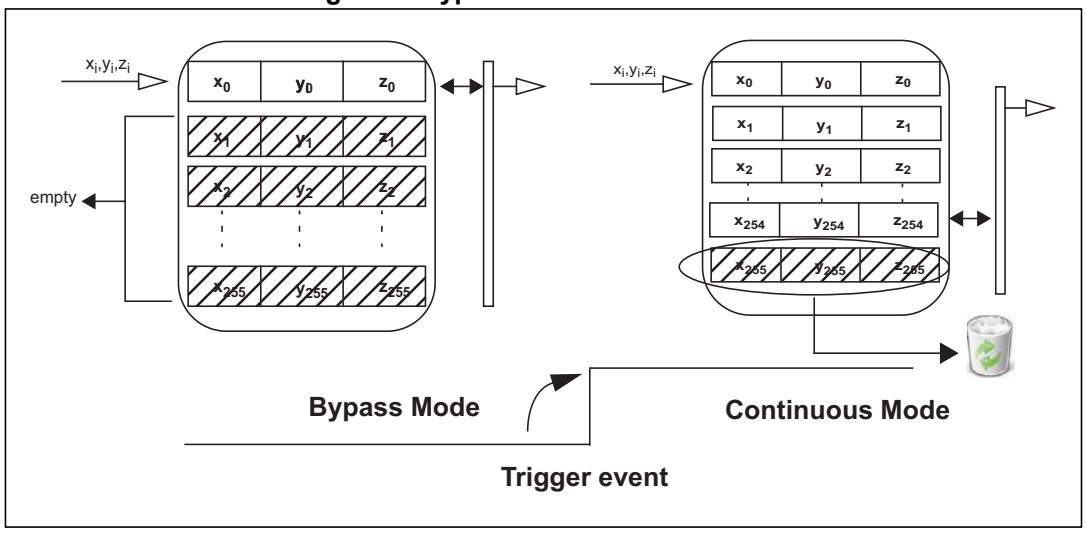
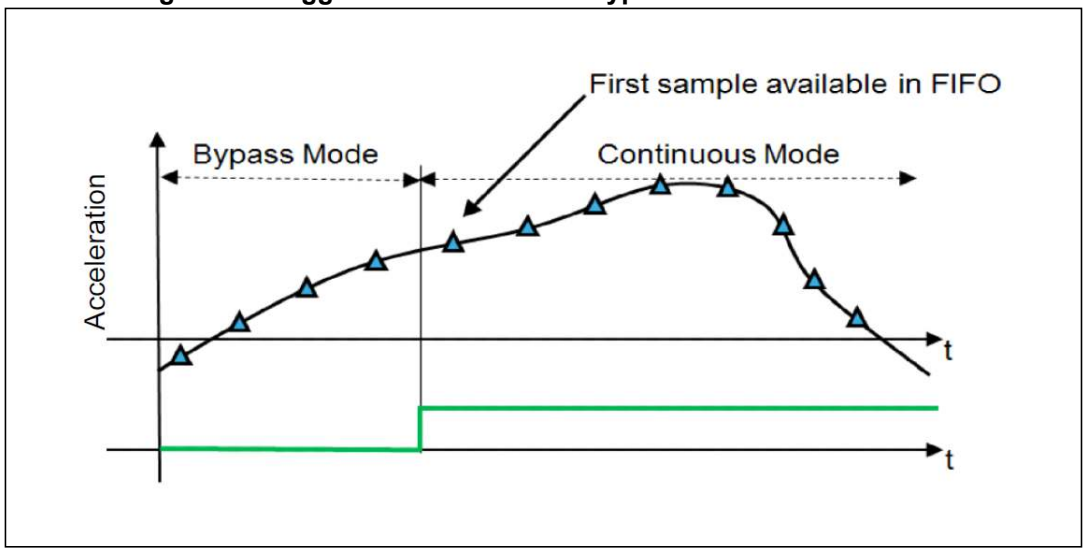


Figure 10. Trigger event to FIFO for Bypass-to-Continuous mode



5.4.6 Module-to-FIFO

When the MODULE_TO_FIFO bit in the *FIFO_CTRL (25h)* register is set to '1', the 14-bit magnitude of the vector of the current axes is sent as FIFO input instead of axes data. X-, Y- and Z-axis data are replaced with 3 times the adjacent data generated by the module routine, as shown in *Figure 11*, so a row of FIFO is written every 3 axes data ready.

The module routine must be previously enabled by writing to the *FUNC_CTRL (3Fh)* register.

The LIS2DS12 calculates the vector sum of the acceleration of the X-, Y-, Z-axis using the following formula:

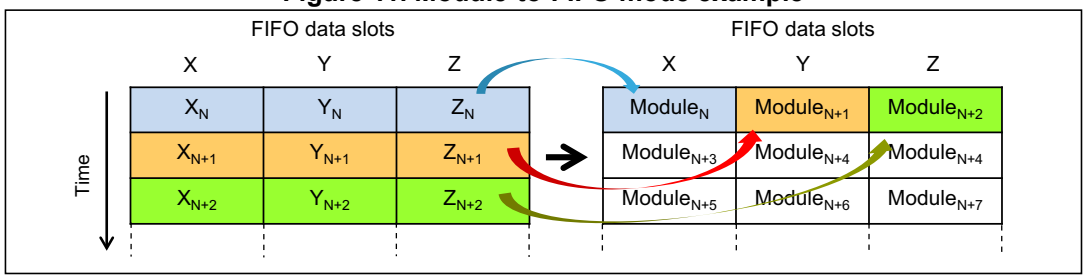
module (14-bit) = Sqrt(x^2+y^2+z^2)

The implementation is based on an approximation of this formula (error below noise level).

If this calculation is used in the application, the FIFO must be increased by 3 since only this one value is stored in FIFO instead.

Please note that a 14-bit value is stored in FIFO when an 8-bit value is available in each sample in register *Module_8bit (0Ch)* (MSBs of original 14-bit value).

Figure 11. Module-to-FIFO mode example



5.5 Embedded functions

The LIS2DS12 embeds internal logic able to implement the following functions:

- Step detector
- Step counter
- Significant motion
- Sensor hub
- Tilt

Pedometer, significant motion, sensor hub, and tilt functions can work in parallel according to *Table 15*. Step detector, step counter, tilt function, and significant motion function work at 25 Hz, so the user can configure ODR at 25 Hz or higher.

Table 15. ODR function settings

	Sensor hub	Pedometer	Tilt function	Event recognition
ODR ≥ 1600 Hz	Y	Y	Y	X
ODR < 1600 Hz	Y	Y	Y	Y
ODR 25-50 Hz	Y	Y	Y	Y
ODR 12.5 Hz	Y	X	X	Y

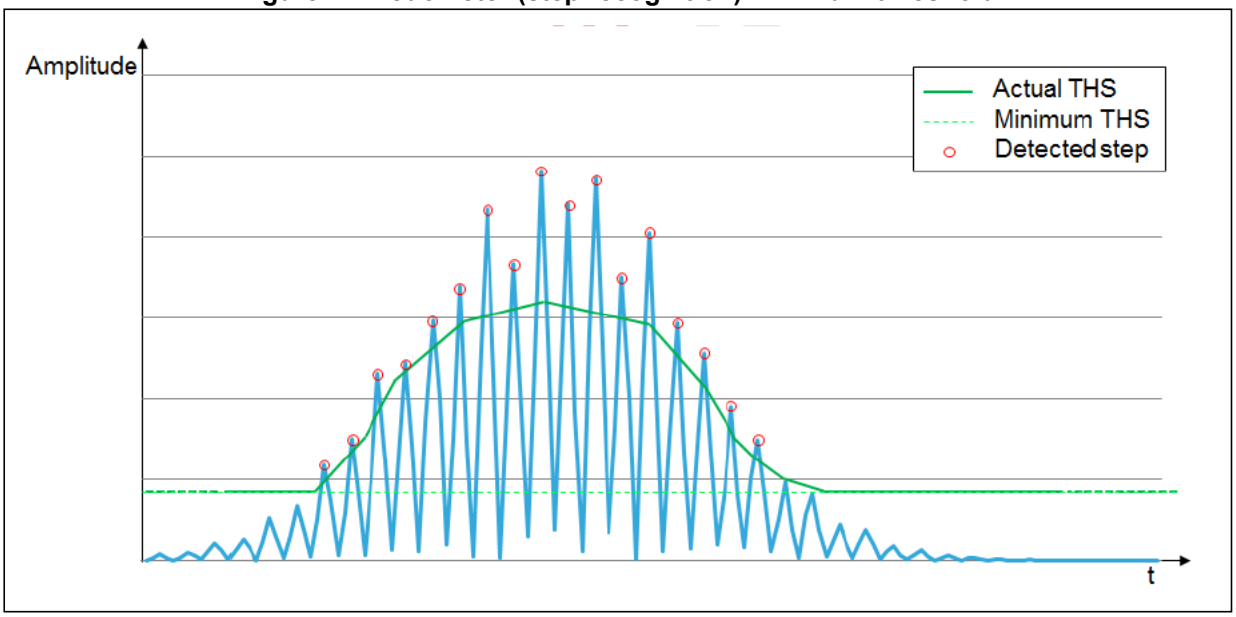
5.5.1 Step detector/Step counter

The step detector function generates an interrupt when a step is recognized, the step counter (automatically enabled when step detector is on) counts the number of the steps detected.
Step Detector/Step Counter (SD/SC) are enabled by setting to '1'-logic the STEP_CNT_ON bit in the *FUNC_CTRL (3Fh)* register. Additional pedometer advanced configurations can be used if the FUNC_CFG_EN bit in *CTRL2 (21h)* is set to "1". Details of the pedometer advanced configuration registers are available in *Section 9: Advanced configuration register mapping* and *Section 10: Advanced configuration registers description*. To disable the pedometer advanced configurations, the FUNC_CFG_EN bit in *CTRL2 (3Fh)* must be set to '0'. Refer to *Section 10.8: CTRL2 (3Fh)*.
The "step detected" interrupt can be read in the *FUNC_CK_GATE (3Dh)* register and by writing the INT2 STEP DET bit to '1'-logic in the *CTRL5 (24h)* register, it can be routed on INT2. The number of steps detected can be read from *STEP_COUNTER_L (3Bh)* and *STEP_COUNTER_H (3Ch)* registers (65535 steps max).

Writing the register *STEP_COUNTER_MINTHS (3Ah)* it is possible to configure the SD/SC minimum threshold, enable 4 *g* operation and reset the number of steps:

- Minimum threshold is the value at which the threshold for step recognition asymptotically tends if no steps are detected and below which it cannot descend (refer to *Figure 12*).

Figure 12. Pedometer (step recognition) minimum threshold



- As default, SD/SC operates with data scaled at 2 *g* of full scale (device full-scale independent), but it is possible to make it work with a FS of 4 *g* by setting the PEDO4g bit to '1'-logic.
- The number of steps can be reset by writing the bit RST nSTEP to '1'-logic in *STEP_COUNTER_MINTHS (3Ah)*: this is a synchronous reset activated at the first data valid and before the algorithm execution. The bit is auto-reset once the counter has been successfully set to 0000h. This bit does not reset the algorithm and its variables.

The algorithm and its variables can be reset just by writing the STEP_CNT_ON bit to '0'-logic, i.e. turning off the SD/SC routine. The RST PEDO bit in the *FUNC_CK_GATE (3Dh)* register signals that a SD/SC reset has to be done, so it goes high and remains at '1'-logic value until the algorithm ends the reset procedure, which is carried out at the first execution after the SD/SC routine has been re-enabled, before the algorithm starts.

5.5.2 Significant motion

The significant motion functionality can be used in location-based applications in order to receive a notification indicating when the user is changing location. This function has been implemented in hardware and works at 25 Hz, so the accelerometer ODR must be set at 25 Hz or higher values.

The significant motion interrupt signal can be driven to the interrupt pin by setting to 1 the INT2_SIG_MOT bit of the *CTRL5 (24h)* register; it can also be checked by reading the SIG_MOT_DET bit of the *FUNC_CK_GATE (3Dh)* register.

The significant motion function generates an interrupt when the difference between the number of steps from its initialization is higher or equal than a threshold. The threshold value corresponds to the number of steps to be performed by the user upon a change of location before the significant motion interrupt is generated.

The threshold has a default value equal to 6. This threshold is configurable in the *SM_THS (34h)* register in the advanced configuration registers (refer to *Section 9: Advanced configuration register mapping* and *Section 10: Advanced configuration registers description*). The significant motion threshold can be used if the FUNC_CFG_EN bit in *CTRL2 (21h)* is set to "1".

5.5.3 Sensor hub

The embedded sensor hub allows acquiring data (up to 6 acquisition) from one external sensor and collecting them in dedicated registers using the I^2C master interface. These data can be read by the external application processor accessing the registers through the SPI/I^2C interfaces.

The frequency of the serial clock is 40 kHz. Lines used for communication are: INT2_PAD as auxiliary SCL bus and SDO_PAD as auxiliary SDA bus.

Sensor hub configurations can be used if the FUNC_CFG_EN bit in *CTRL2 (21h)* is set to '1'.

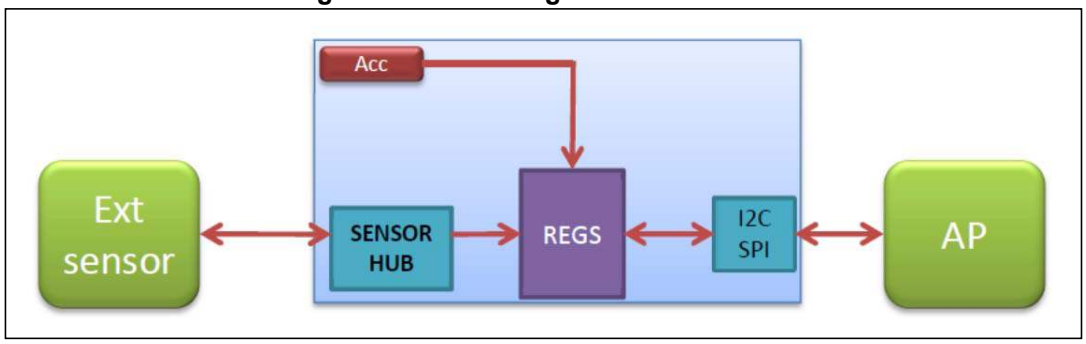
Details of sensor hub configuration registers are available in *Section 9: Advanced configuration register mapping* and *Section 10: Advanced configuration registers description*.

To disable the sensor hub configurations, the FUNC_CFG_EN bit in *CTRL2 (3Fh)* must be set to '0'. Refer to *Section 10.8: CTRL2 (3Fh)*.

Once the sensor hub configuration is completed, to enable the master I^2C functionality, the MASTER_ON bit in *FUNC_CTRL (3Fh)* must be set to '1'.

The I^2C master can read up to 6 bytes (registers SensorHub_out_1/6 from 06h to 0Bh).

Figure 13. Block diagram of sensor hub



The master can operate synchronously with the accelerometer: the master starts to execute the operations synchronously with the accelerometer internal Data-Ready signal.

6 Digital interfaces

The registers embedded inside the LIS2DS12 may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped to the same pins. To select/exploit the I^2C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 16. Serial interface pin description

Pin name	Pin description
CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SA0 SDO	I^2C address selection (SA0) SPI serial data output (SDO)

6.1 I^2C serial interface

The LIS2DS12 I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 17. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the Serial DAta line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through an external pull-up resistor. When the bus is free, both the lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with normal mode.

In order to disable the I^2C block, *CTRL2 (21h)* (I2C_DISABLE) = 1 must be set.

6.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a high-to-low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The Slave Address (SAD) associated to the LIS2DS12 is 00111xxb where the xx bits are modified by the SA0/SDO pin in order to modify the device address. If the SA0/SDO pin is connected to the supply voltage, the address is 0011101b, otherwise if the SA0/SDO pin is connected to ground, the address is 0011110b. This solution permits to connect and address two different accelerometers to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LIS2DS12 behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent. Once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSb represents the actual register address while the *CTRL2 (21h)* (IF_ADD_INC) bit defines the address increment.

The slave address is completed with a Read/Write bit. If the bit is '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes. If the bit is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 18* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 18. SAD+Read/Write patterns

Command	SAD[6:2]	SAD[1] = $\overline{SA0}$	SAD[0] = SA0	R/W	SAD+R/W
Read	00111	1	0	1	00111101
Write	00111	1	0	0	00111100
Read	00111	0	1	1	00111011
Write	00111	0	1	0	00111010

Table 19. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 20. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 21. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 22. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low-to-high transition on the SDA line while the SCL line is high is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

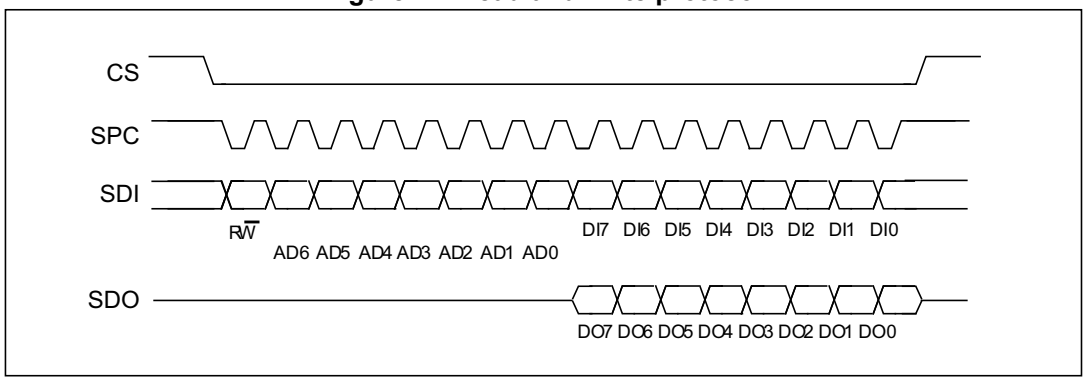
In the presented communication format MAK is Master acknowledge and NMAK is No Master Acknowledge.

6.2 SPI bus interface

The LIS2DS12 SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 14. Read and write protocol



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

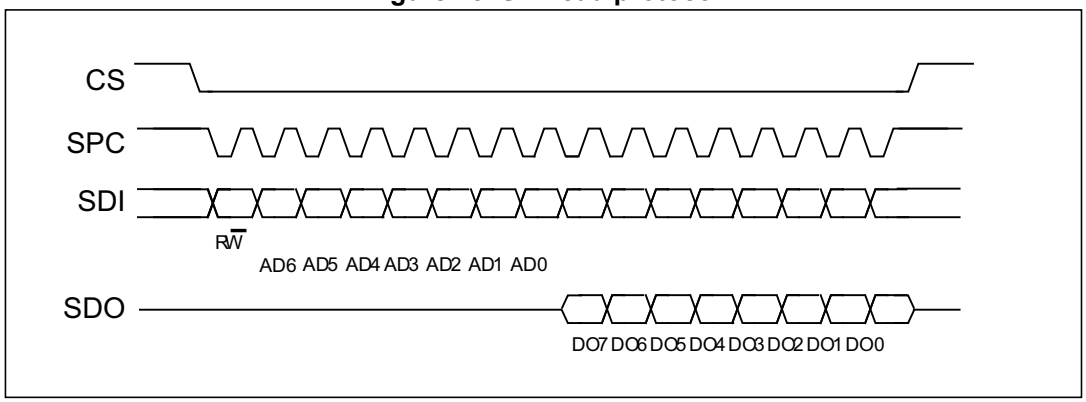
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands additional blocks of 8 clock periods will be added. When the *CTRL2 (21h)* (IF_ADD_INC) bit is '0', the address used to read/write data remains the same for every block. When the *CTRL2 (21h)* (IF_ADD_INC) bit is '1', the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

6.2.1 SPI read

Figure 15. SPI read protocol



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

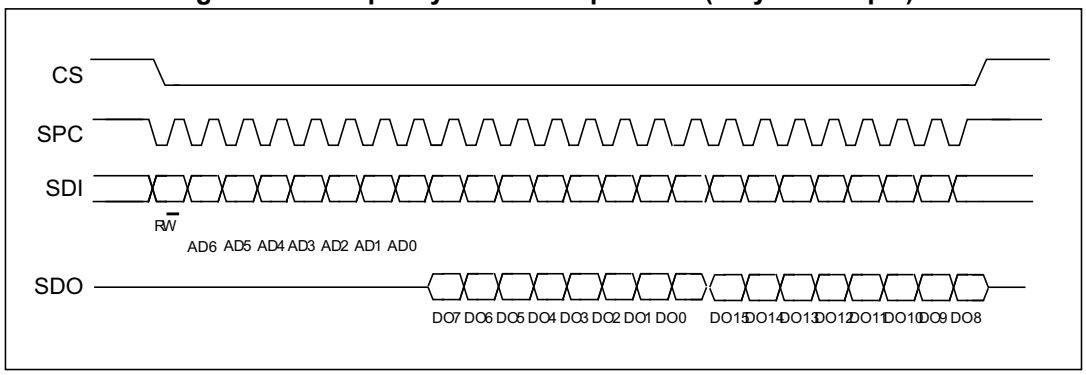
bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

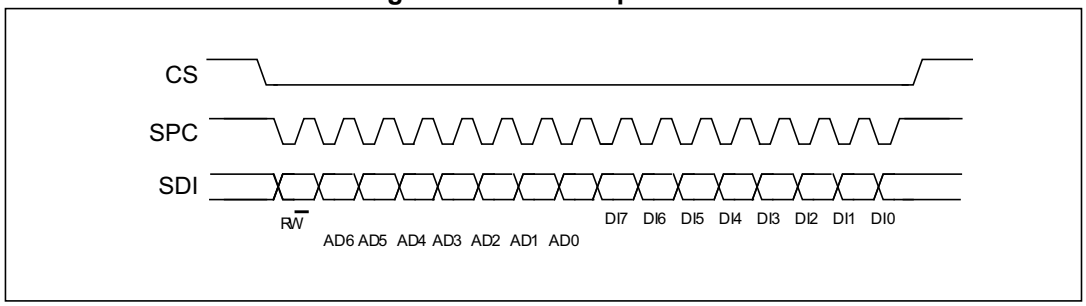
bit 16-... : data DO(...-8). Additional data in multiple byte reads.

Figure 16. Multiple byte SPI read protocol (2-byte example)



6.2.2 SPI write

Figure 17. SPI write protocol



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

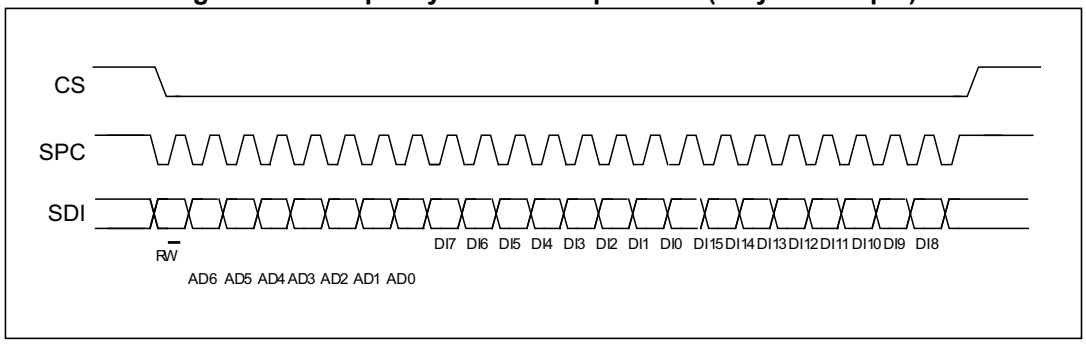
bit 0: WRITE bit. The value is 0.

bit 1 -7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Additional data in multiple byte writes.

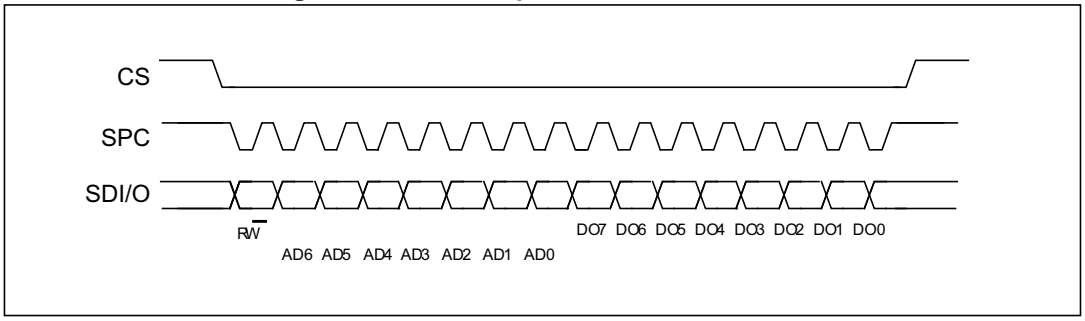
Figure 18. Multiple byte SPI write protocol (2-byte example)



6.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the *CTRL2 (21h)* (SIM) bit equal to '1' (SPI serial interface mode selection).

Figure 19. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

7 Register mapping

The table given below provides a list of the 8-bit registers embedded in the device and the corresponding addresses.

Table 23. Register map

Name	Type(1)	Register address		Default	Comment
		Hex	Binary		
RESERVED	-	00-05		-	RESERVED
SENSORHUB1_REG	R	06	0000 0110	output	Sensor hub output registers
SENSORHUB2_REG	R	07	0000 0111	output	
SENSORHUB3_REG	R	08	0000 1000	output	
SENSORHUB4_REG	R	09	0000 1001	output	
SENSORHUB5_REG	R	0A	0000 1010	output	
SENSORHUB6_REG	R	0B	0000 1011	output	
Module_8bit	R	0C	00001100	output	
RESERVED	-	0D-0E		-	RESERVED
WHO_AM_I	R	0F	00001111	01000011	Who I am ID
RESERVED	-	10-1F		-	RESERVED
CTRL1	R/W	20	00100000	00000000	Control registers
CTRL2	R/W	21	00100001	00000100	
CTRL3	R/W	22	00100010	00000000	
CTRL4	R/W	23	00100011	00000000	
CTRL5	R/W	24	00100100	00000000	
FIFO_CTRL	R/W	25	00100101	00000000	FIFO control reg
OUT_T	R	26	00100110	output	Temp sensor output
STATUS	R	27	00100111	output	Status data register
OUT_X_L	R	28	00101000	output	Output registers
OUT_X_H	R	29	00101001		
OUT_Y_L	R	2A	00101010		
OUT_Y_H	R	2B	00101011		
OUT_Z_L	R	2C	00101100		
OUT_Z_H	R	2D	00101101		
FIFO_THS	R/W	2E	00101110	00000000	FIFO registers
FIFO_SRC	R	2F	00101111	output	FIFO SRC
FIFO_SAMPLES	R/W	30	00110000	00000000	Unread samples stored in FIFO

Table 23. Register map (continued)

Name	Type(1)	Register address		Default	Comment
		Hex	Binary		
TAP_6D_THS	R/W	31	00110001	00000000	TAP, 4D, 6D threshold
INT_DUR	R/W	32	00110010	00000000	Interrupt duration
WAKE_UP_THS	R/W	33	00110011	00000000	TAP/D-TAP selection, Inactivity EN, Wakeup threshold
WAKE_UP_DUR	R/W	34	00110100	00000000	Wakeup duration
FREE_FALL	R/W	35	00110101	00000000	Free-fall config.
STATUS_DUP	R	36	00110110	output	Status register
WAKE_UP_SRC	R	37	00110111	output	Wakeup SRC
TAP_SRC	R	38	00111000	output	TAP SRC
6D_SRC	R	39	00111001	output	6D SRC
STEP_COUNTER_ MINTHS	R/W	3A	00111010	00010000	STEP C config
STEP_COUNTER_L	R	3B	00111011	output	Steps detected LSB
STEP_COUNTER_H	R	3C	00111100	output	Steps detected MSB
FUNC_CK_GATE	R	3D	00111110	output	ST FUNCTION setting
FUNC_SRC	R	3E	00000100	output	FUNCTION SRC
FUNC_CTRL	R/W	3F	00000100	00000000	FUNCTION CTRL

1. R = read-only register, R/W = readable/writable register

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

8 Register description

8.1 SENSORHUB1_REG (06h)

First byte associated to external sensor.

Table 24. SENSORHUB1_REG register

SHub1_7	SHub1_6	SHub1_5	SHub1_4	SHub1_3	SHub1_2	SHub1_1	SHub1_0

Table 25. SENSORHUB1_REG description

SHub1_[7:0]	First byte associated to external sensor

8.2 SENSORHUB2_REG (07h)

Second byte associated to external sensor.

Table 26. SENSORHUB2_REG register

SHub2_7	SHub2_6	SHub2_5	SHub2_4	SHub2_3	SHub2_2	SHub2_1	SHub2_0

Table 27. SENSORHUB2_REG register description

SHub2_[7:0]	Second byte associated to external sensor

8.3 SENSORHUB3_REG (08h)

Third byte associated to external sensor.

Table 28. SENSORHUB3_REG register

SHub3_7	SHub3_6	SHub3_5	SHub3_4	SHub3_3	SHub3_2	SHub3_1	SHub3_0

Table 29. SENSORHUB3_REG register description

SHub3_[7:0]	Third byte associated to external sensor

8.4 SENSORHUB4_REG (09h)

Fourth byte associated to external sensor.

Table 30. SENSORHUB4_REG register

SHub4_7	SHub4_6	SHub4_5	SHub4_4	SHub4_3	SHub4_2	SHub4_1	SHub4_0

Table 31. SENSORHUB4_REG register description

SHub4_[7:0]	Fourth byte associated to external sensor

8.5 SENSORHUB5_REG (0Ah)

Fifth byte associated to external sensor.

Table 32. SENSORHUB5_REG register

SHub5_7	SHub5_6	SHub5_5	SHub5_4	SHub5_3	SHub5_2	SHub5_1	SHub5_0

Table 33. SENSORHUB5_REG register description

SHub5_[7:0]	Fifth byte associated to external sensor

8.6 SENSORHUB6_REG (0Bh)

Sixth byte associated to external sensor.

Table 34. SENSORHUB6_REG register

SHub6_7	SHub6_6	SHub6_5	SHub6_4	SHub6_3	SHub6_2	SHub6_1	SHub6_0

Table 35. SENSORHUB6_REG register description

SHub6_[7:0]	Sixth byte associated to external sensor

8.7 Module_8bit (0Ch)

Module out value (r). This register is a read-only register.

Table 36. Module_8bit register

Module_7	Module_6	Module_5	Module_4	Module_3	Module_2	Module_1	Module_0

Table 37. Module_8bit register description

Module [7:0]	Module output value (8-bit). Default value: 0

8.8 WHO_AM_I (0Fh)

Who_AM_I register (r). This register is a read-only register. Its value is fixed at 43h.

Table 38. WHO_AM_I register default values

0	1	0	0	0	0	1	1

8.9 CTRL1 (20h)

Control register 1 (r/w)

Table 39. Control register 1

ODR3	ODR2	ODR1	ODR0	FS1	FS0	HF_ODR	BDU

Table 40. Control register 1 description

ODR [3:0]	Output data rate & power mode selection. Default value: 0000 (see *Table 41*)
FS [1:0]	Full-scale selection. Default value: 00 (00: ±2 *g*; 01: ±16 *g*; 10: ±4 *g*; 11: ±8 *g*)
HF_ODR	High-frequency ODR mode enable. Default value: 0
BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB read)

ODR [3:0] is used to set the power mode and ODR selection. The following table lists the bit settings for power-down mode and each available frequency.

Table 41. ODR register setting: power down (PD) and low power (LP)

ODR[3:0]	HF_ODR	ODR selection [Hz]	Bit resolution	Mode
0000	-	-	-	PD
1000	-	1	10	LP
1001	-	12.5	10	LP
1010	-	25	10	LP
1011	-	50	10	LP
1100	-	100	10	LP
1101	-	200	10	LP
1110	-	400	10	LP
1111	-	800	10	LP

Table 42. ODR register setting: high resolution (HR) and high frequencies (HF)

ODR[3:0]	HF_ODR	ODR selection [Hz]	Bit resolution	Mode
0001	-	12.5	14	HR
0010	-	25	14	HR
0011	-	50	14	HR
0100	-	100	14	HR
0101	0	200	14	HR
0110	0	400	14	HR
0111	0	800	14	HR
0101	1	1600	12	HF
0110	1	3200	12	HF
0111	1	6400	12	HF

The BDU bit is used to inhibit the update of the output registers until both upper and lower register parts are read. In default mode (BDU = ‘0’) the output register values are updated continuously. When the BDU is activated (BDU = ‘1’), the content of the output registers is not updated until both MSB and LSB are read which avoids reading values related to different sample times.

8.10 CTRL2 (21h)

Control register 2 (r/w)

Table 43. Control register 2

BOOT	SOFT_ RESET	0(1)	FUNC_CFG_ EN(2)(3)(4)	FDS_ SLOPE	IF_ADD_ INC	I2C_ DISABLE	SIM

1. This bit must be set to '0' for the correct operation of the device.
2. When this bit is enabled, only advanced configuration registers can be written. For proper functionality of the device, all the other registers must not be modified.
3. Details of advanced configuration registers are available in *Section 9: Advanced configuration register mapping* and *Section 10: Advanced configuration registers description*.
4. To disable the advanced configuration, bit FUNC_CFG_EN in *CTRL2 (3Fh)* must be set to '0'. Refer to *Section 10.8: CTRL2 (3Fh)*.

Table 44. Control register 2 description

BOOT	Forces the reboot of the flash content in the trimming and configuration registers. Default value: 0 (0: disable; 1: Reboot enable)
SOFT_RESET	Soft reset acts as reset for all control registers, then goes to 0. Default value: 0 (0: disabled; 1: enabled)
FUNC_CFG_ EN	Access to pedometer/sensor hub advanced configuration registers from address 2Bh to 3Fh. Default value: 0 (0: disable the access to pedometer/sensor hub advanced configuration registers; 1: enable the access to pedometer/sensor hub advanced configuration registers)
FDS_SLOPE	High-pass filter data selection on output register and FIFO. Default value: 0 (0: internal filter bypassed; 1: internal filter enabled on output register and FIFO)
IF_ADD_INC	Register address automatically incremented during multiple byte access with a serial interface (I^2C or SPI). Default value: 1 (0: disabled; 1: enabled)
I2C_DISABLE	Disable I^2C communication protocol. Default value: 0 (0: SPI and I^2C interfaces enabled; 1: I^2C mode disabled)
SIM	SPI serial interface mode selection. Default value: 0 0: 4-wire interface; 1: 3-wire interface

8.11 CTRL3 (22h)

Control register 3 (r/w)

Table 45. Control register 3

ST2	ST1	TAP_X_EN	TAP_Y_EN	TAP_Z_EN	LIR	H_LACTIVE	PP_OD

Table 46. Control register 3 description

ST [2:1]	Self-test enable. Default value: 00 (00: Self-test disabled; Other: see *Table 47*)
TAP_X_EN	Tap recognition on X direction enable. Default value: 0 (0: disabled; 1: enabled)
TAP_Y_EN	Tap recognition on Y direction enable. Default value: 0 (0: disabled; 1: enabled)
TAP_Z_EN	Tap recognition on Z direction enable. Default value: 0 (0: disabled; 1: enabled)
LIR	Latched Interrupt. Switches between latched ('1'-logic) and pulsed ('0'-logic) mode for function source signals and interrupts routed to pins (wakeup, tap, double-tap, tilt, pedometer, significant motion). Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)
H_LACTIVE	Interrupt active high, low. Default value: 0 (0: active high; 1: active low)
PP_OD	Push-pull/open-drain selection on interrupt pad. Default value: 0 (0: push-pull; 1: open-drain)

Table 47. Self-test mode selection

ST2	ST1	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Negative sign self-test
1	1	Not allowed

8.12 CTRL4 (23h)

Control register 4 (r/w): interrupt 1 configuration

Table 48. Control register 4

INT1_MASTER_DRDY	INT1_S_TAP	INT1_WU	INT1_FF	INT1_TAP	INT1_6D	INT1_FTH	INT1_DRDY

Table 49. Control register 4 description

INT1_MASTER_DRDY	Manage the Master DRDY signal on INT1 pad. Default: 0 (0: disable Master DRDY on INT1; 1: enable Master DRDY on INT1)
INT1_S_TAP	Single-tap recognition is routed on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_WU	Wakeup recognition is routed on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_FF	Free-fall recognition is routed on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_TAP	Double-tap recognition is routed on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_6D	6D recognition is routed on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_FTH	FIFO threshold interrupt is routed on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_DRDY	Data-Ready is routed on INT1 pad. Default value: 0 (0: disabled; 1: enabled)

8.13 CTRL5 (24h)

Control register 5 (r/w): interrupt 2 configuration

Table 50. Control register 5

DRDY_ PULSED	INT2_ BOOT	INT2_ ON_INT1	INT2_ TILT	INT2_ SIG_MOT	INT2_ STEP_ DET	INT2_ FTH	INT2_ DRDY

Table 51. Control register 5 description

DRDY_ PULSED	Data-ready interrupt mode selection: latched mode / pulsed mode. Default value: 0 (0: latched mode; 1: pulsed mode for data-ready)
INT2 _BOOT	Boot state routed on INT2 pad. Default value: 0 (0: disabled; 1: enabled)
INT2 _ON INT1	All signals routed on INT2 are also routed on INT1. Default value: 0 (0: disabled; 1: enabled)
INT2 _TILT	Tilt event is routed on INT2 pad. Default value: 0 (0: disabled; 1: enabled)
INT2 _SIG_ MOT	Significant motion detection is routed on INT2 pad. Default value: 0 (0: disabled; 1: enabled)
INT2 _ STEP_DET	Step detection is routed on INT2 pad. Default value: 0 (0: disabled; 1: enabled)
INT2_FTH	FIFO threshold interrupt is routed on INT2 pad. Default value: 0 (0: disabled; 1: enabled)
INT2_DRDY	Data-Ready is routed on INT2 pad. Default value: 0 (0: disabled; 1: enabled)

8.14 FIFO_CTRL (25h)

FIFO control register 5 (r/w).

Table 52. FIFO control register

FMODE2	FMODE1	FMODE0	INT2_STEP_ COUNT_OV	MODULE_ TO_FIFO	0(1)	0(1)	IF_CS_PU_ DIS

1. This bit must be set to '0' for correct device operation.

Table 53. FIFO control register description

FMODE [2:0]	FIFO mode selection bits. Default: 000. For further details refer to *Table 54.*
INT2_STEP_ COUNT_OV	Step counter overflow interrupt enable on INT2 pad. Default value: 0 (0: disabled; 1: enabled)
MODULE_TO_ FIFO	When set to '1'-logic, module routine result is send to FIFO instead of X,Y,Z acceleration data
IF_CS_PU_DIS	When '1'-logic disconnects pull-up in if_cs pad. Default: 0

When the FIFO has been enabled, data acquired has been stored at the accelerometer ODR and the trigger signal of FIFO writing is the accelerometer internal data-ready.

FIFO data can be stored in default configuration where inertial data as been stored as X, Y, Z data or in module configuration:

Default configuration: 256-level inertial data (14-bit stored data for X, Y, Z)

User-selectable: 768 module data (14-bit each module)

Table 54. FIFO mode selection

FMODE2	FMODE1	FMODE0	Mode
0	0	0	Bypass mode: FIFO turned off
0	0	1	FIFO mode: Stops collecting data when FIFO is full.
0	1	0	Reserved
0	1	1	Continuous-to-FIFO: Stream mode until trigger is deasserted, then FIFO mode
1	0	0	Bypass-to-Continuous: Bypass mode until trigger is deasserted, then FIFO mode
1	0	1	Reserved
1	1	0	Continuous mode: data If the FIFO is full, the new sample over-writes the older sample.
1	1	1	Reserved

8.15 OUT_T (26h)

Temperature output register (r).

Table 55. OUT_T register

TEMP7	TEMP6	TEMP5	TEMP4	TEMP3	TEMP2	TEMP1	TEMP0

Table 56. OUT_T register description

Temp [7:0]	Temperature sensor output data. The value is expressed as two's complement sign. Sensitivity = 1 °C/LSB 0 LSB represents T=25 °C ambient.

8.16 STATUS (27h)

Status register (r)

Table 57. Status register

FIFO_THS	WU_IA	SLEEP_ STATE	DOUBLE_ TAP	SINGLE_ TAP	6D_IA	FF_IA	DRDY

Table 58. Status register description

FIFO_THS	FIFO threshold status flag. (0: FIFO filling is lower than threshold level; 1: FIFO filling is equal to or higher than the threshold level.)
WU_IA	Wakeup event detection status. (0: WU event not detected; 1: Wakeup event detected)
SLEEP_ STATE	Sleep event status. (0: Sleep event not detected; 1: Sleep event detected)
DOUBLE_ TAP	Double-tap event status (0: Double-tap event not detected; 1: Double-tap event detected)
SINGLE_ TAP	Single-tap event status (0: Single-tap event not detected; 1: Single-tap event detected)
6D_IA	Source of change in position portrait/landscape/face-up/face-down. (0: no event detected; 1: a change in position detected)
FF_IA	Free-fall event detection status. (0: free-fall event not detected; 1: free-fall event detected)
DRDY	Data-ready status. (0: not ready; 1: X-, Y- and Z-axis new data available)

8.17 OUT_X_L (28h)

X-axis LSB output register (r)

Table 59. OUT_X_L register default values

X_L7	X_L6	X_L5(2)	X_L4(2)	X_L3(1)(2)	X_L2(1)(2)	0	0

1. If HF mode is enabled, this bit is set to 0.
2. If LP mode is enabled, this bit is set to 0.

The 8 least significant bits of linear acceleration sensor X-axis output. Together with the *OUT_X_H (29h)* register it forms the output value expressed as a 16-bit word in 2's complement.

8.18 OUT_X_H (29h)

X-axis MSB output register (r)

Table 60. OUT_X_H register default values

X_H7	X_H6	X_H5	X_H4	X_H3	X_H2	X_H1	X_H0

The 8 most significant bits of linear acceleration sensor X-axis output. Together with the *OUT_X_L (28h)* register it forms the output value expressed as a 16-bit word in 2's complement.

8.19 OUT_Y_L (2Ah)

Y-axis LSB output register (r)

Table 61. OUT_Y_L register default values

Y_L7	Y_L6	Y_L5(2)	Y_L4(2)	Y_L3(1)(2)	Y_L2(1)(2)	0	0

1. If HF mode is enabled, this bit is set to 0.
2. If LP mode is enabled, this bit is set to 0.

The 8 least significant bits of linear acceleration sensor Y-axis output. Together with the *OUT_Y_H (2Bh)* register it forms the output value expressed as a 16-bit word in 2's complement.

8.20 OUT_Y_H (2Bh)

Y-axis MSB output register (r)

Table 62. OUT_Y_H register default values

Y_H7	Y_H6	Y_H5	Y_H4	Y_H3	Y_H2	Y_H1	Y_H0

The 8 most significant bits of linear acceleration sensor Y-axis output. Together with the *OUT_Y_L (2Ah)* register it forms the output value expressed as a 16-bit word in 2's complement.

8.21 OUT_Z_L (2Ch)

Z-axis LSB output register (r)

Table 63. OUT_Z_L register default values

Z_L7	Z_L6	Z_L5(2)	Z_L4(2)	Z_L3(1)(2)	Z_L2(1)(2)	0	0

1. If HF mode is enabled, this bit is set to 0.
2. If LP mode is enabled, this bit is set to 0.

The 8 least significant bits of linear acceleration sensor Z-axis output. Together with the *OUT_Z_H (2Dh)* register it forms the output value expressed as a 16-bit word in 2's complement.

8.22 OUT_Z_H (2Dh)

Z-axis MSB output register (r)

Table 64. OUT_Z_H register default values

Z_H7	Z_H6	Z_H5	Z_H4	Z_H3	Z_H2	Z_H1	Z_H0

The 8 most significant bits of linear acceleration sensor Z-axis output. Together with the *OUT_Z_L (2Ch)* register it forms the output value expressed as a 16-bit word in 2's complement.

8.23 FIFO_THS (2Eh)

FIFO threshold level setting (r/w).

Table 65. FIFO_THS register

FTH7	FTH6	FTH5	FTH4	FTH3	FTH2	FTH1	FTH0

8.24 FIFO_SRC (2Fh)

FIFO_SRC register (r)

Table 66. FIFO_SRC register

FTH	FIFO OVR	DIFF8	0	0	0	0	0

Table 67. FIFO_SRC register description

FTH	FIFO threshold status. (0: FIFO filling is lower than FTH level; 1: FIFO filling is equal to or higher than threshold level)
OVR	FIFO overrun status. (0: FIFO is not completely filled; 1: FIFO is completely filled and at least one sample has been overwritten)
DIFF8	Concatenated with *FIFO_SAMPLES (30h)* register, it represents the number of unread samples stored in FIFO. (000000000 = FIFO empty; 100000000 = FIFO full, 256 unread samples).

8.25 FIFO_SAMPLES (30h)

FIFO_SAMPLES control register (r)

Table 68. FIFO SAMPLES register

DIFF7	DIFF6	DIFF5	DIFF4	DIFF3	DIFF2	DIFF1	DIFF0

Table 69. FIFO SAMPLES register description

DIFF [7:0]	Concatenated with DIFF8 bit in *FIFO_SRC (2Fh)* register, it represents the number of unread samples stored in FIFO. (000000000 = FIFO empty; 100000000 = FIFO full, 256 unread samples).

8.26 TAP_6D_THS (31h)

4D configuration enable and TAP threshold configuration (r/w)

Table 70. TAP_6D_THS register

4D_EN	6D_THS1	6D_THS0	TAP_ THS4	TAP_ THS3	TAP_ THS2	TAP_ THS1	TAP_ THS0

Table 71. TAP_6D_THS register description

4D_EN	4D detection portrait/landscape position enable. (0: no position detected; 1: portrait/landscape detection and face-up/face-down position enabled).
6D_THS [1:0]	Threshold for 4D/6D function (refer to *Table 72*)
TAP_THS [4:0]	Threshold for TAP recognition. 1 LSB = FS/32

Table 72. 4D/6D threshold setting

6D_THS1	6D_THS0	Threshold decoding (degrees)
0	0	6 (80 degrees)
0	1	11 (70 degrees)
1	0	16 (60 degrees)
1	1	21 (50 degrees)

8.27 INT_DUR (32h)

Interrupt duration register (r/w)

Table 73. INT_DUR register

LAT3	LAT2	LAT1	LAT0	QUIET1	QUIET0	SHOCK1	SHOCK0

Table 74. INT_DUR register description

LAT [3:0]	Duration of maximum time gap for double-tap recognition. When double-tap recognition is enabled, this register expresses the maximum time between two successive detected taps to determine a double-tap event. 1 LSB = 32 TODR.
QUIET [1:0]	Expected quiet time after a tap detection: this register represents the time after the first detected tap in which there must not be any over-threshold event. 1 LSB = 4 TODR.
SHOCK [1:0]	Maximum duration of over-threshold event: this register represents the maximum time of an over-threshold signal detection to be recognized as a tap event. 1 LSB = 8 TODR

8.28 WAKE_UP_THS (33h)

Wakeup threshold register (r/w)

Table 75. WAKE_UP_THS register

SINGLE_ DOUBLE_ TAP	SLEEP_ ON	WU_ THS_ 5	WU_ THS_4	WU_ THS_3	WU_ THS 2	WU_ THS 1	WU_ THS 0

Table 76. WAKE_UP_THS register description

SINGLE_ DOUBLE_ TAP	Single/double-tap enable (0: single-tap is enabled; 1: double-tap is enabled)
SLEEP_ON	Sleep (inactivity) enable (0: sleep disabled; 1: sleep enabled)
WU_THS [5:0]	Wakeup threshold, 6-bit unsigned 1 LSB = 1/64 of FS

8.29 WAKE_UP_DUR (34h)

Wakeup and sleep duration configuration register (r/w)

Table 77. WAKE_UP_DUR register

FF_DUR5	WU_DUR1	WU_DUR0	INT1_ FSS7	SLEEP_ DUR3	SLEEP_ DUR2	SLEEP_ DUR1	SLEEP_ DUR0

Table 78. WAKE_UP_DUR register description

FF DUR5	Free-fall duration. In conjunction with FF_DUR [4:0] bit in *FREE_FALL (35h)* register. 1 LSB = 1 TODR
WU_DUR [1:0]	Wakeup duration. 1 LSB = 1 TODR
INT1_FSS7	FIFO flag FSS7 is routed on INT1 pad (0: disabled; 1: enabled)
SLEEP_DUR [3:0]	Duration to go in sleep mode. 1 LSB = 512 TODR

8.30 FREE_FALL (35h)

Free-fall duration and threshold configuration register (r/w)

Table 79. FREE_FALL register

FF_DUR4	FF_DUR3	FF_DUR2	FF_DUR1	FF_DUR0	FF_THS2	FF_THS1	FF_THS0

Table 80. FREE_FALL register description

FF_DUR [4:0]	Free-fall duration. In conjunction with FF_DUR5 bit in *WAKE_UP_DUR (34h)* register. 1 LSB = 1 TODR.
FF_THS [2:0]	Free-fall threshold. 1 LSB = 31.25 m*g* (refer to *Table 81*)

Table 81. FREE_FALL threshold decoding

FF_THS2	FF_THS1	FF_THS0	Threshold decoding (LSB)
0	0	0	5
0	0	1	7
0	1	0	8
0	1	1	10
1	0	0	11
1	0	1	13
1	1	0	15
1	1	1	16

8.31 STATUS_DUP (36h)

Event detection status register (r)

Table 82. STATUS_DUP register

OVR	WU_IA	SLEEP_ STATE	DOUBLE_ TAP	SINGLE_ TAP	6D_IA	FF_IA	DRDY

Table 83. STATUS_DUP register description

OVR	FIFO overrun status flag. (0: FIFO filling is not completely filled; 1: FIFO is completely filled and at least one sample has been overwritten)
WU_IA	Wakeup event detection status. (0: WU event not detected; 1: Wake up event detected)
SLEEP_ STATE	Sleep event status. (0: Sleep event not detected; 1: Sleep event detected)
DOUBLE_ TAP	Double-tap event status: (0: Double-tap event not detected; 1: Double-tap event detected)
SINGLE_ TAP	Single-tap event status: (0: Single-tap event not detected; 1: Single-tap event detected)
6D_IA	Source of change in position portrait/landscape/face-up/face-down. (0: no event detected; 1: a change in position is detected)
FF_IA	Free-fall event detection status. (0: free-fall event not detected; 1: free-fall event detected)
DRDY	Data-ready status. (0: not ready; 1: X-, Y- and Z-axis new data available)

8.32 WAKE_UP_SRC (37h)

Wakeup source register (r)

Table 84. WAKE_UP_SRC register

0	0	FF_IA	SLEEP STATE IA	WU_IA	X_WU	Y_WU	Z_WU

Table 85. WAKE_UP_SRC register description

FF_IA	Free-fall event detection status. (0: FF event not detected; 1: FF event detected)
SLEEP STATE IA	Sleep event status. (0: Sleep event not detected; 1: Sleep event detected)
WU_IA	Wakeup event detection status. (0: Wakeup event not detected; 1: Wakeup event is detected)
X_WU	Wakeup event detection status on X-axis. (0: Wakeup event on X not detected; 1: Wakeup event on X-axis is detected)
Y_WU	Wakeup event detection status on Y-axis. (0: Wakeup event on Y not detected; 1: Wake up event on Y-axis is detected)
Z_WU	Wakeup event detection status on Z-axis. (0: Wakeup event on Z not detected; 1: Wake up event on Z-axis is detected)

8.33 TAP_SRC (38h)

TAP source register (r)

Table 86. TAP_SRC register

0	TAP_IA	SINGLE TAP	DOUBLE TAP	TAP SIGN	X_TAP	Y_TAP	Z_TAP

Table 87. TAP_SRC register description

TAP_IA	TAP event status. (0: Tap event not detected; 1: Tap event detected)
SINGLE TAP	Single-tap event status. (0: Single-tap event not detected; 1: Single-tap event detected)
DOUBLE TAP	Double-tap event status. (0: Double-tap event not detected; 1: Double-tap event detected)
TAP_SIGN	Sign of acceleration detected by tap event. (0: positive sign of acceleration detected; 1: negative sign of acceleration detected).
X_TAP	Tap event detection status on X-axis. (0: Tap event on X not detected; 1: Tap event on X-axis is detected)
Y_TAP	Tap event detection status on Y-axis. (0: Tap event on Y not detected; 1: TAP event on Y-axis is detected)
Z_TAP	Tap event detection status on Z-axis. (0: Tap event on Z not detected; 1: Tap event on Z-axis is detected)

8.34 6D_SRC (39h)

6D source register (r)

Table 88. 6D_SRC register

0	6D_IA	ZH	ZL	YH	YL	XH	XL

Table 89. 6D_SRC register description

6D_IA	Source of change in position portrait/landscape/face-up/face-down. (0: no event detected; 1: a change in position is detected)
ZH	ZH over threshold (0: ZH does not exceed the threshold; 1: ZH is over the threshold)
ZL	ZL over threshold (0: ZL does not exceed the threshold; 1: ZL is over the threshold)
YH	YH over threshold (0: YH does not exceed the threshold; 1: YH is over the threshold)
YL	YL over threshold (0: YL does not exceed the threshold; 1: YL is over the threshold)
XH	XH over threshold: (0: XH does not exceed the threshold; 1: XH is over the threshold)
XL	XL over threshold (0: XL does not exceed the threshold; 1: XL is over the threshold)

8.35 STEP_COUNTER_MINTHS (3Ah)

Step counter configuration register (r/w).

Table 90. STEP_COUNTER_MINTHS configuration register

RST_ nSTEP	PEDO4g	SC_ MTHS5	SC_ MTHS4	SC_ MTHS3	SC_ MTHS2	SC_ MTHS1	SC_ MTHS0

Table 91. STEP_COUNTER_MINTHS configuration register description

RST_nSTEP	Step number synchronous reset bit: when '1'-logic forces pedometer to reset the number of steps in *STEP_COUNTER_L (3Bh)* and *STEP_COUNTER_H (3Ch)* registers. Default value: 0.
PEDO4g	4 *g* operation mode for pedometer routines enable. Default: 0 (0: 4 *g* operation mode for pedometer routines disabled; 1 = 4 *g* operation mode for pedometer routines enabled)
SC_MTHS [5:0]	Minimum threshold value for step counter routine. Default: 01 0000

8.36 STEP_COUNTER_L (3Bh)

Step counter register (r)

Table 92. STEP_COUNTER_L configuration register

nSTEP_ L7	nSTEP_ L6	nSTEP_ L5	nSTEP_ L4	nSTEP_ L3	nSTEP_ L2	nSTEP_ L1	nSTEP_ L0

Table 93. STEP_COUNTER_L configuration register description

nSTEP_L [7:0]	Least significant part of number of steps detected by step counter routine. Unsigned representation.

8.37 STEP_COUNTER_H (3Ch)

Step counter register (r)

Table 94. STEP_COUNTER_H register

nSTEP_ H7	nSTEP_ H6	nSTEP_ H5	nSTEP_ H4	nSTEP_ H3	nSTEP_ H2	nSTEP_ H1	nSTEP_ H0

Table 95. STEP_COUNTER_H register description

nSTEP_H [7:0]	Most significant part of number of steps detected by step counter routine. Unsigned representation.

8.38 FUNC_CK_GATE (3Dh)

Functional source register (r)

Table 96. FUNC_CK_GATE register

TILT_INT	FS_SRC_1	FS_SRC_0	SIG_MOT _ DETECT	RST_SIGN _MOT	RST_ PEDO	STEP_ DETECT	CK_GATE _FUNC

Table 97. FUNC_CK_GATE register description

TILT_INT	Tilt event detection status. (0: tilt event not detected; 1: tilt event detected)
FS_ SRC [1:0]	Full-scale SRC bit. (00: Same as *CTRL1 (20h)* - no scaling; 01: 2 *g*; 10: 4 *g*; 11: same as *CTRL1 (20h)* - no scaling)
SIGN_MOT_ DETECT	Significant motion event detection status. (0: significant motion event not detected; 1: significant motion event detected)
RST_SIGN MOT	Pedometer significant motion initialization reset. (0: disabled; 1: pedometer significant motion initialization has to be executed at the next routine execution or is actually ongoing)
RST_ PEDO	Pedometer reset. (0: disabled; 1: indicates that pedometer step counter initialization has to be executed at the next routine execution or is actually ongoing)
STEP_DETECT	Step detection status. (0: Step not detected; 1: Step detected)
CK_GATE_ FUNC	Function clocking gate signal. (0: Power down; 1: FUNC is in power mode)

8.39 FUNC_SRC (3Eh)

Functional source register (r)

Table 98. FUNC_SRC register

0	0	0	0	0	RST_TILT	MODULE_ READY	SENSORHUB _END_OP

Table 99. FUNC_SRC register description

RST_TILT	Tilt reset. (0: disabled; 1: indicates that tilt initialization has to be executed at the next routine execution or is actually ongoing)
MODULE_READY	Module status. (0: new module data not available, 1: new module data available)
SENSORHUB _END_OP	Sensor hub communication status. Default value: 0 (0: sensor hub communication not concluded; 1: sensor hub communication concluded)

8.40 FUNC_CTRL (3Fh)

Functional control register (r/w)

Table 100. FUNC_CTRL register

0(1)	0(1)	MODULE_ ON	TILT_ON	TUD_EN	MASTER_ ON	SIGN_ MOT_ON	STEP_ CNT_ON

1. This bit must be set to '0' for the correct operation of the device.

Table 101. FUNC_CTRL register description

MODULE_ON	Module processing enable. Default value: 0 (0: disabled; 1: module)
TILT_ON	Tilt on. Default value: 0 (0: new module data not available; 1: new module data available)
TUD_EN	Internal pull-up on auxiliary I^2C line. Default value: 0 (0: disabled; 1: internal pull-up on auxiliary I^2C line enabled)
MASTER_ON(1)	Sensor hub I^2C master enable. (0: master I^2C of sensor hub disabled; 1: master I^2C of sensor hub enabled)
SIGN_MOT_ON	Pedometer significant motion routine enable. Default value: 0 (0: disabled, 1: pedometer significant motion routine enabled)
STEP_CNT_ON	Step counter routine enable. Default value: 0 (0: disabled, 1: pedometer step counter routine enabled)

1. In order to work correctly, the accelerometer has to be on.

9 Advanced configuration register mapping

The table below provides a list of the registers for the advanced configuration available in the device and the corresponding addresses.

Advanced configuration registers are accessible when FUNC_CFG_EN is set to '1' in *CTRL2 (21h)*. Once enabled, access to the advanced configuration registers can be disabled by setting the FUNC_CFG_EN bit to ‘0’ in *CTRL2 (3Fh)*.

Table 102. Register map - embedded functions

Name	Type	Register address		Default	Comment
		Hex	Binary		
RESERVED	R/W	00-2A			
PEDO_DEB_REG	R/W	2B	00101011	01101110	
RESERVED	R/W	2C-2F			
SLV0_ADD	R/W	30	00110000	00000000	
SLV0_SUBADD	R/W	31	00110001	00000000	
SLV0_CONFIG	R/W	32	00110010	00000000	
DATAWRITE_SLV0	R/W	33	00110011	00000000	
SM_THS	R/W	34	00110100	00000110	
RESERVED	R/W	35-39			
STEP_COUNT_DELTA	R/W	3A	00111010	00000000	
RESERVED	R/W	3B-3E			
CTRL2	R/W	3F	00111111	00010100	

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

10 Advanced configuration registers description

10.1 PEDO_DEB_REG (2Bh)

Table 103. PEDO_DEB_REG register default values

DEB_ TIME4	DEB_ TIME3	DEB_ TIME2	DEB_ TIME1	DEB_ TIME0	DEB_ STEP2	DEB_ STEP1	DEB_ STEP0

Table 104. PEDO_DEB_REG register description

DEB_TIME[4:0]	Debounce time. If the time between two consecutive steps is greater than DEB_TIME*80ms, the debouncer is reactivated. Default value: 01101
DEB_STEP[2:0]	Debounce threshold. Minimum number of steps to increment step counter (debounce). Default value: 110

10.2 SLV0_ADD (30h)

I^2C slave address of the first external sensor (Sensor1) register (r/w).

Table 105. SLV0_ADD register

Slave0_ add6	Slave0_ add5	Slave0_ add4	Slave0_ add3	Slave0_ add2	Slave0_ add1	Slave0_ add0	rw_0

Table 106. SLV0_ADD register description

Slave0_add6[6:0]	I^2C slave address of Sensor1 that can be read by sensor hub. Default value: 0000000
rw_0	Read/write operation on Sensor1. Default value: 0 (0: write operation; 1: read operation)

10.3 SLV0_SUBADD (31h)

Address of register on the first external sensor (Sensor1) register (r/w).

Table 107. SLV0_SUBADD register

Slave0_ reg7	Slave0_ reg6	Slave0_ reg5	Slave0_ reg4	Slave0_ reg3	Slave0_ reg2	Slave0_ reg1	Slave0_ reg0

Table 108. SLV0_SUBADD register description

Slave0_reg[7:0]	Address of register on Sensor1 that has to be read/written according to the rw_0 bit value in SLV0_ADD (30h). Default value: 00000000

10.4 SLV0_CONFIG (32h)

First external sensor (Sensor1) configuration and sensor hub settings register (r/w).

Table 109. SLV0_CONFIG register

					Slave0_ numop2	Slave0_ numop1	Slave0_ numop0

Table 110. SLV0_CONFIG register description

Slave0_numop[2:0]	Number of read operations on Sensor1.

10.5 DATAWRITE_SLV0 (33h)

Data to be written into the slave device register (r/w).

Table 111. DATAWRITE_SLV0 register

Slave_ dataw7	Slave_ dataw6	Slave_ dataw5	Slave_ dataw4	Slave_ dataw3	Slave_ dataw2	Slave_ dataw1	Slave_ dataw0

Table 112. DATAWRITE_SLV0 register description

Slave_ dataw[7:0]	Data to be written into the slave device according to the rw_0 bit in *SLV0_ADD (30h)* register or address to be read in source mode. Default value: 00000000

10.6 SM_THS (34h)

Defines the threshold value (r/w).

Table 113. SM_THS configuration register

SM_THS _7	SM_THS _6	SM_THS _5	SM_THS _4	SM_THS _3	SM_THS _2	SM_THS _1	SM_THS _0

Table 114. SM_THS configuration register description

SM_THS_[7:0]	These bits define the threshold value which corresponds to the number of steps to be performed by the user upon a change of location before the significant motion interrupt is generated. It is expressed as an 8-bit unsigned value. The default value of this field is equal to 6 (= 00000110b).

10.7 STEP_COUNT_DELTA (3Ah)

Step counter configuration register (r/w).

Table 115. STEP_COUNT_DELTA configuration register

STEP_COUNT_D7	STEP_COUNT_D6	STEP_COUNT_D5	STEP_COUNT_D4	STEP_COUNT_D3	STEP_COUNT_D2	STEP_COUNT_D1	STEP_COUNT_D0

Table 116. STEP_COUNT_DELTA configuration register description

STEP_COUNT_D[7:0]	Period of time to detect at least one step to generate step recognition. Default value: 0 1 LSB = 1.6384 s

10.8 CTRL2 (3Fh)

Functional control register (r/w)

Table 117. CTRL2 configuration register

BOOT(1)	SOFT_RESET(1)	0(2)	FUNC_CFG_EN(3)	FDS_SLOPE(1)	IF_ADD_INC(1)	I2C_DISABLE(1)	SIM(1)

1. Read-only bits. These bits are copied from *CTRL2 (21h)*.
2. This bit must be set to '0' for the correct operation of the device.
3. To disable the advanced configuration, bit FUNC_CFG_EN in *CTRL2 (3Fh)* must be set to '0'.

Table 118. CTRL2 configuration register description

BOOT	Forces the reboot of the flash content in the trimming and configuration registers. READ ONLY.
SOFT_RESET	Soft reset acts as a reset for all control registers, then goes to 0. READ ONLY.
FUNC_CFG_EN	Default value: 1 (0: disable pedometer/sensor hub advanced functionalities; 1: enable pedometer/sensor hub advanced functionalities)
FDS_SLOPE	High-pass filter data selection on output register and FIFO. READ ONLY.
IF_ADD_INC	Register address automatically incremented during multiple byte access with a serial interface (I^2C or SPI). READ ONLY.
I2C_DISABLE	Disable I^2C communication protocol. READ ONLY.
SIM	SPI serial interface mode selection. READ ONLY.

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

11.1 Soldering information

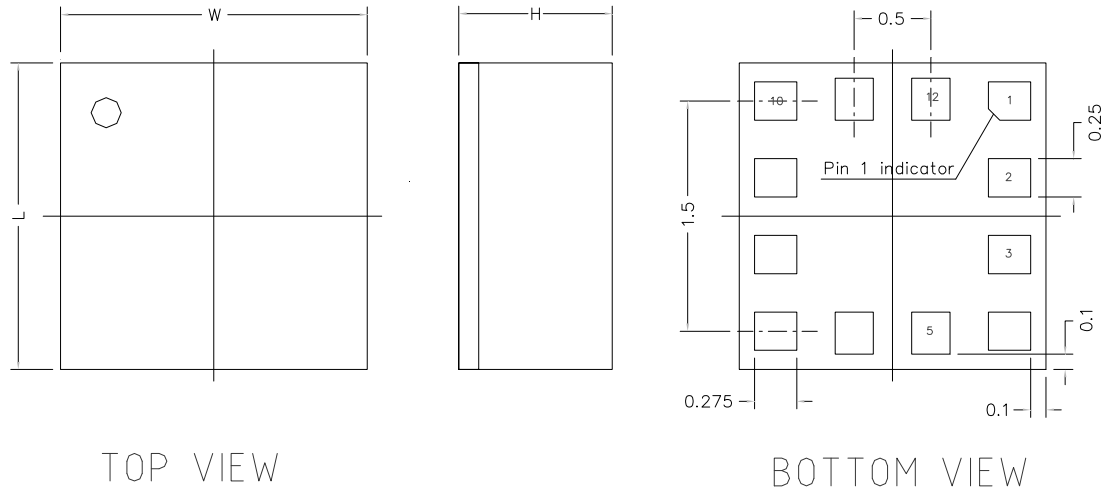
The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com.

11.2 LGA-12 package information

Figure 20. LGA-12 2x2x0.86 mm package outline and mechanical data



Dimensions are in millimeter unless otherwise specified

OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2.00	±0.1
Width [W]	2.00	±0.1
Height [H]	0.86	MAX

8566956_1

11.3 LGA-12 packing information

Figure 21. Carrier tape information for LGA-12 package

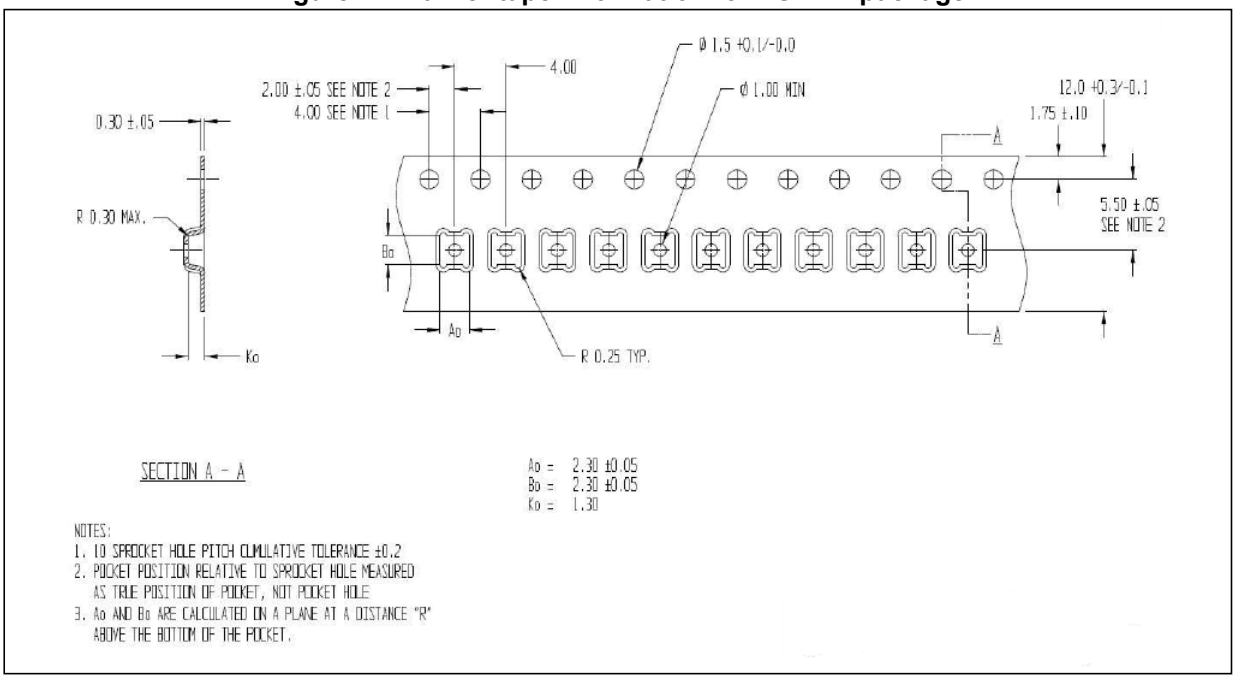


Figure 22. LGA-12 package orientation in carrier tape

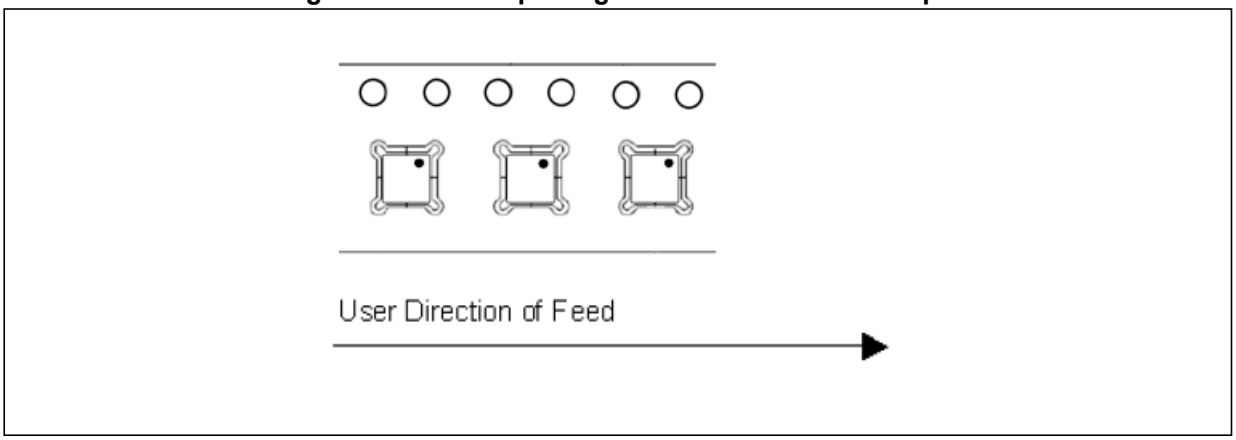


Figure 23. Reel information for carrier tape of LGA-12 package

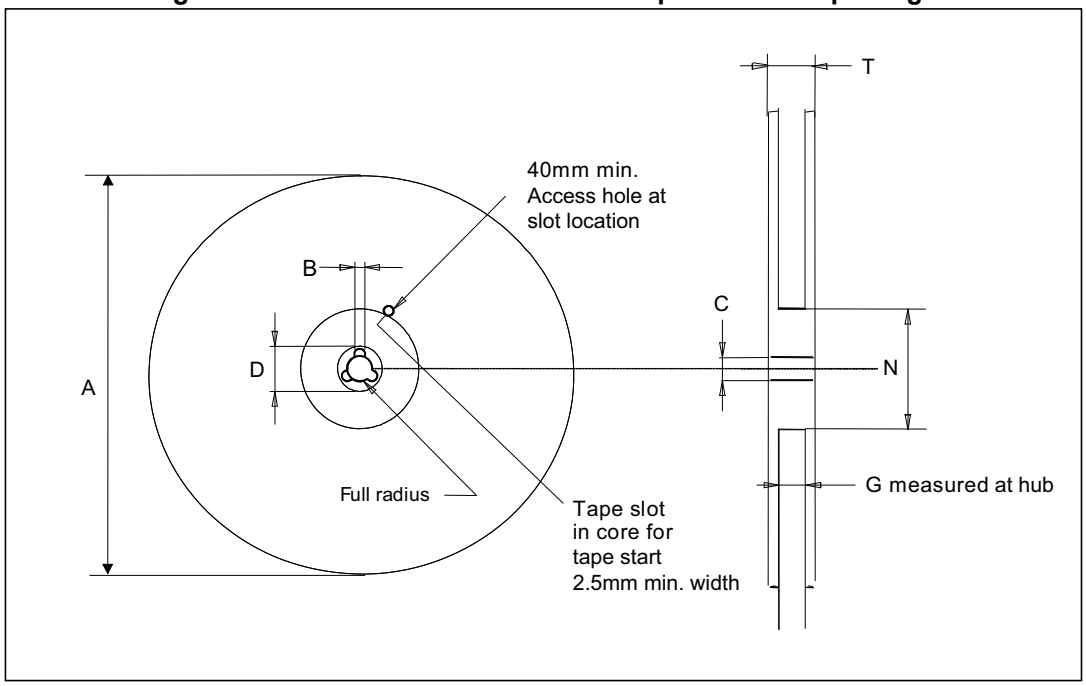


Table 119. Reel dimensions for carrier tape of LGA-12 package

Reel dimensions (mm)	
A (max)	330
B (min)	1.5
C	13 ±0.25
D (min)	20.2
N (min)	60
G	12.4 +2/-0
T (max)	18.4

12 Revision history

Table 120. Document revision history

Date	Revision	Changes
28-Sep-2017	7	Added *Table 10: Internal pin status* Updated *Figure 3: SPI slave timing diagram*