QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 750
10/12 BIT 135, 170 AND 185 MSPS ADC

LTC2231, LTC2221, LTC2230, LTC2220, OR LTC2220-1

DESCRIPTION

Demonstration circuit 750 supports a family of 10/12 BIT 135 and 170 MSPS ADCs. Each assembly features one of the following devices: LTC2231, LTC2221, LTC2230, LTC2220, OR LTC2220-1 high speed, high dynamic range ADCs.

Several versions of the 750A demo board supporting the LTC2230/1 10 BIT, LTC2220/1 and LTC2220-1 12 BIT series of A/D converters are listed in Table 1. Depending on the required resolution, sample rate and input frequency, the DC750 is supplied with the appropriate A/D and with an optimized input circuit. The circuitry on the analog inputs is optimized for analog input frequencies below 100 MHz or between 100 MHz to 250 MHz. For higher operating frequencies, contact the factory for support.

Design files for this circuit board are available. Call the LTC factory.

Table 1. DC750A Variants

DC750 VARIANTS	ADC PART NUMBER	RESOLUTION	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
750A-A	LTC2220	12-Bit	170 Msps	1MHz < A_{IN} < 100MHz
750A-B	LTC2221	12-Bit	135Msps	1MHz < A_{IN} < 100MHz
750A-C	LTC2230	10-Bit	170 Msps	1MHz < A_{IN} < 100MHz
750A-D	LTC2231	10-Bit	135Msps	1MHz < A_{IN} < 100MHz
750A-E	LTC2220	12-Bit	170 Msps	100MHz <A_{IN} < 250MHz
750A-F	LTC2221	12-Bit	135Msps	100MHz <A_{IN} < 250MHz
750A-G	LTC2230	10-Bit	170 Msps	100MHz <A_{IN} < 250MHz
750A-H	LTC2231	10-Bit	135Msps	100MHz <A_{IN} < 250MHz
750A-J	LTC2220-1	12-Bit	185Msps	1MHz < A_{IN} < 100MHz
750A-K	LTC2220-1	12-Bit	185Msps	100MHz <A_{IN} < 250MHz

Table 2. Performance Summary (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Supply Voltage	Depending on sampling rate and the A/D converter provided, this supply must provide up to 500mA.	Optimized for 3.3V [3.1V ⇔3.5V min/max]
Analog input range	Depending on Sense Pin Voltage	1V_{PP} to 2V_{PP}
Logic Input Voltages: $\overline{OE}$, SHDN	Minimum Logic High	2.0V
	Maximum Logic Low	0.8V
Logic Output Voltage (FIN1108T LVDS Buffer)	Minimum Logic High @ -3.4mA w/100Ω Termination	1.2V +170mV
	Maximum Logic Low @ +3.4mA w/100Ω Termination	1.2V – 170mV
Sampling Frequency (Convert Clock Frequency)	See Table 1	
Encode Clock Level	50 Ω Source Impedance. (Convert Clock input is capacitor coupled on board and terminated with 50Ω.)	2V_{P-P} ⇔2.5V_{P-P} Sine Wave or Square wave
Resolution	See Table 1	
Input frequency range	See Table 1	
SFDR	See Applicable Data Sheet	
SNR	See Applicable Data Sheet	

QUICK START PROCEDURE

Demonstration circuit 750 is easy to set up to evaluate the performance of any of the LTC2220 family of High Speed LVDS output A/D converters - LTC2231, LTC2221, LTC2230, LTC2220 OR LTC2220-1. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

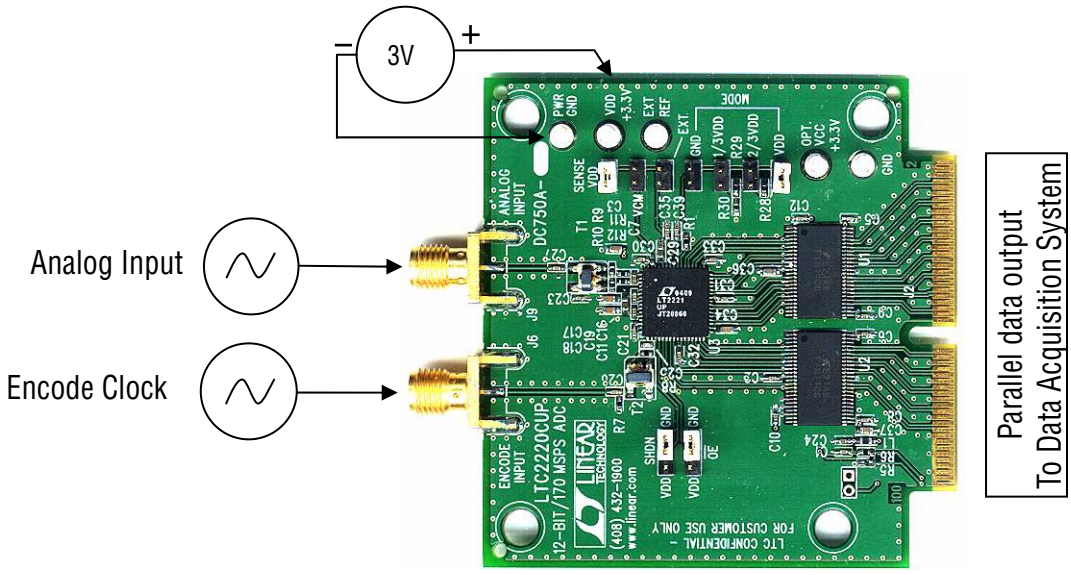

Figure 1. DC750 Setup

DC750 DEMONSTRATION CIRCUIT BOARD JUMPERS

The DC750 demonstration circuit board should have the following jumper settings:

JP1: $\overline{OE}$: Ground enables outputs.

JP3: SHDN: Ground, enables ADC Core.

JP20-22: SENSE: Select VDD for the $2V_{PP}$ input range
SENSE: Select VCM for the $1V_{PP}$ input range.

JP7, JP13, JP14, JP19: MODE: Select VDD (For 2's complement output format for PScope compatibility) and disable Clock Duty Cycle Stabilizer for sine and square wave capacitive coupled inputs.

APPLYING POWER AND SIGNALS TO THE DC750 DEMONSTRATION CIRCUIT BOARD

If a DC890B is used to acquire data from the DC750, the DC890B should be connected to a USB port and provided an external 6V, 1Amp power supply. The DC890B will not enable LVDS mode without externally applied power present. Apply +3.3V across the pins marked "+3.3V" and "GND" on the DC750. The DC750 demonstration circuit requires up to 500 mA depending on the sampling rate and the A/D converter supplied.

NOTE: If a DC890 is NOT used to collect the data, PIN 99 on the edge connector must be connected to 3.3V to enable the output buffers U1 and U2.

NOTE: WHILE THE DC890B DATA COLLECTION BOARD IS POWERED BY THE USB CABLE IT REQUIRES AN EXTERNAL POWER SUPPLY OF 6V ON THE 2.1MM POWER JACK OR THE ADJACENT TURRETS (+) AND (-) BEFORE THE DC890B WILL ENABLE LVDS MODE.

NOTE: IF A DC890 IS USED TO COLLECT DATA, THE ENCODE CLOCK FREQUENCY MUST BE > 50MHZ TO OPERATE THE FPGA'S DIGITAL CLOCK MODULE (DCM).

ENCODE CLOCK

NOTE: THIS IS NOT A LOGIC LEVEL INPUT.

Apply an encode clock to the SMA connector on the DC750 demonstration circuit board marked "ENCODE INPUT". Refer to Table 2 for recommended level, impedance and coupling. For the very best noise performance (SNR AND SFDR), the ENCODE INPUT must be driven with a very low jitter source. When using a sinusoidal generator, the amplitude should be as large as possible, up to $3V_{P-P}$. Using band pass filters on the ENCODE INPUT and the ANALOG INPUT will improve the noise performance by reducing the wideband noise power of the signals. Data sheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broad band noise. The very high sampling bandwidth of the LTC2220 family of parts will fold several Nyquist bands of noise if present down to base band raising the noise floor. Low phase noise Agilent 8664B generators are used with TTE band pass filters for both the Clock input and the Analog input.

[The LTC2220 family of ADCs provides a very flexible and capable Encode Clock interface capable of accommodating both single ended and differential sources from LVDS to CMOS logic levelsw. See the LTC2220 data sheet for other Encode Clock drive options.]

Apply the analog input signal of interest to the SMA connector on the DC750 demonstration circuit board marked "ANALOG INPUT". This input is capacitive coupled to the primary of transformer T1.

The LVDS conversion clock output is available on pins [50, 52] of J2. The LVDS data samples are available on Pins [8-46, 56-82] for 12 BITS or [8-46, 56-70] for 10 BITS as LVDS pairs isolated by a ground pin between each set. The data samples can be collected via a logic analyzer, cabled to a development system through a SHORT 100 pin ribbon cable (available from Samtec - HSC8 series of high speed connectors) or collected by the DC890 FastDAACS Data Acquisition Board. The DC890 is controlled by the *PScope System Software* provided or down loaded from the Linear Technology website at http://www.linear.com/software/.

If a DC890 was provided, follow the DC890 Quick Start Guide and the instructions below.

To start the data collection software if "*PScope.exe*", is installed (by default) in \Program Files\LTC\PScope\, double click the PScope Icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

Configure PScope for the appropriate variant of the DC750 demonstration circuit by selecting the correct A/D Converter as installed on the DC750. Under the "Configure" menu, go to "Device." Under the "Device" pull down menu, select the device, either the LTC2231, LTC2221, LTC2230, LTC2220 OR LTC2220-1. When evaluating 10 BIT performance using a 12 BIT part, select the 10 Bit part and PScope will automatically blank the last two LSBs when using a DC750 supplied with a 12 BIT ADC.

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the "Collect" button should result in time and frequency plots displayed in the PScope window. Additional information and help for *PScope* is available in the DC890 Quick Start Guide and in the online help available within the *PScope* program itself.

ANALOG INPUT NETWORK

For optimal distortion and noise performance the RC network on the analog inputs are optimized for different analog input frequencies on the different versions of the DC750. For input frequencies below about 100 MHz, the circuit in Fig. 2 is recommended (this is installed on DC750 versions A,B,C,D). For input frequencies above 100 MHz and below 250 MHz, the circuit in Fig. 3 is recommended (this is installed on versions E,F,G,H).

For input frequencies between 250 MHz and 500 MHz, the circuit in Fig. 4 is recommended. For input frequencies greater than 250 MHz contact the factory for support.

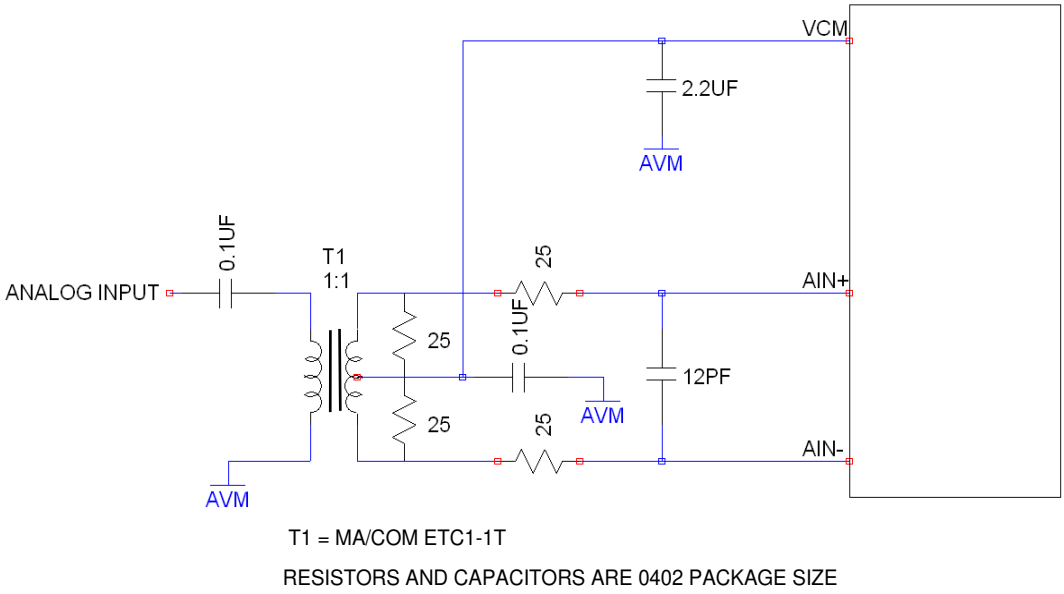

Figure 2. Analog Front End Circuit For 1MHz < A_{IN} < 100MHz

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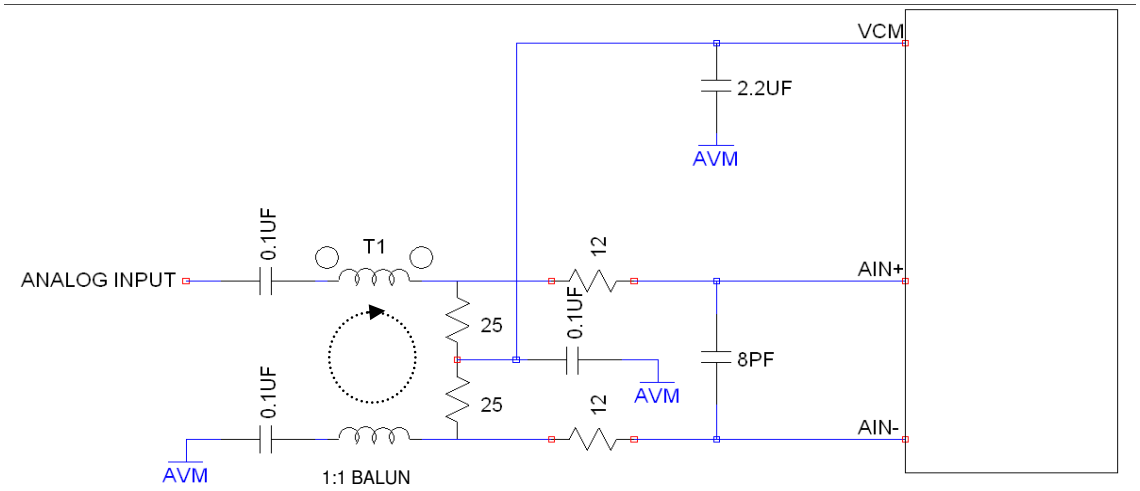
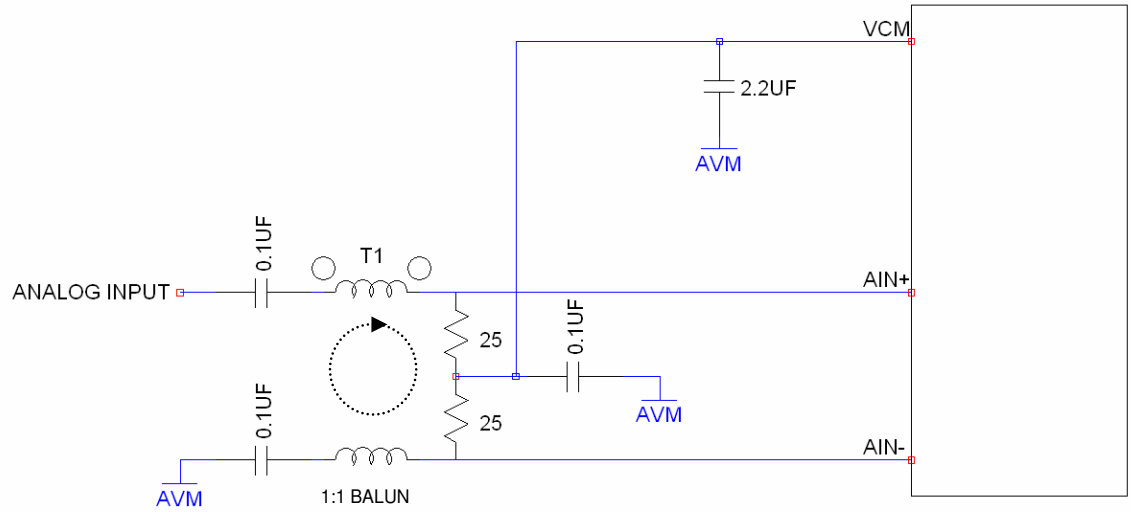


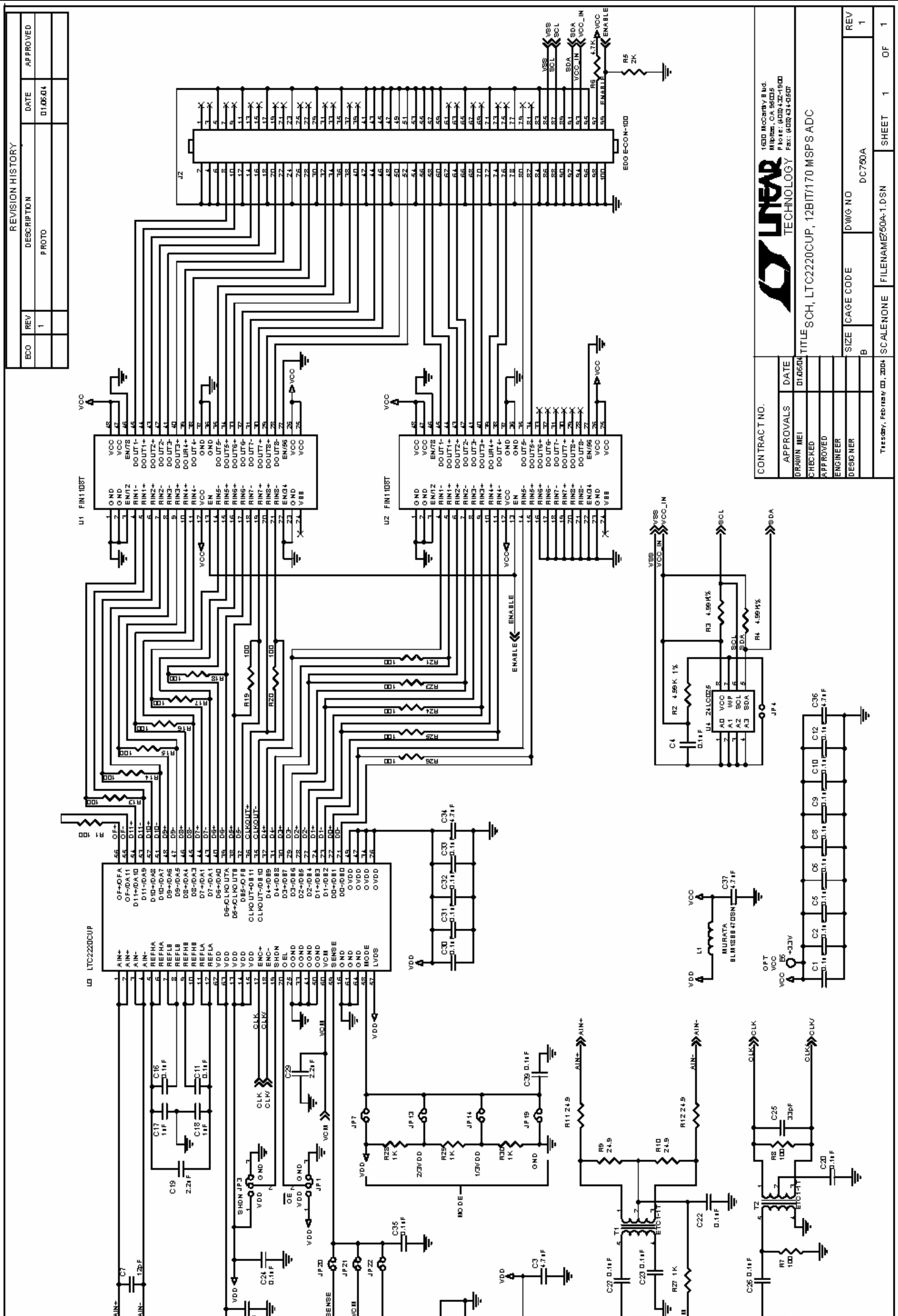
T1 = MA/COM ETC1-1-13
RESISTORS AND CAPACITORS ARE 0402 PACKAGE SIZE

Figure 3. Analog Front End Circuit For 100MHz < A_{IN} < 250MHz



T1 = MA/COM ETC1-1-13
RESISTORS AND CAPACITORS ARE 0402 PACKAGE SIZE

Figure 4. Analog Front End Circuit For 250MHz < A_{IN} < 500MHz



REVISION HISTORY
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ANALOG INPUT
ENCODE INPUT