SN74BCT29822 10-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCBS089B - FEBRUARY 1989 - REVISED NOVEMBER 1993

 State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ} 	DW OR NT PACKAGE (TOP VIEW)
 ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0) 	$ \overline{OE} \begin{bmatrix} 1 & 24 \\ 24 \end{bmatrix} V_{CC} 1D \begin{bmatrix} 2 & 23 \\ 3D \end{bmatrix} 1Q 2D \begin{bmatrix} 3 & 22 \\ 21 \end{bmatrix} 2Q 3D \begin{bmatrix} 4 & 21 \\ 30 \end{bmatrix} $
 3-State Buffer-Type Outputs Drive Bus Lines Directly 	$4\overline{D}$ $\begin{bmatrix} 5 & 20 \end{bmatrix}$ $4Q$ $5D$ $\begin{bmatrix} 6 & 19 \end{bmatrix}$ $5Q$
 Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (NT) 	6D [7 18] 6Q 7D [8 17] 7Q 8D [9 16] 8Q
description	9D[10 15]9Q 10D[11 14]10Q
This 10-bit bus-interface flip-flop features 3-state	GND [12 13] CLK

This 10-bit bus-interface flip-flop features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be complementary to the data (\overline{D}) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output enable (\overline{OE}) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74BCT29822 is characterized for operation from 0°C to 70°C.

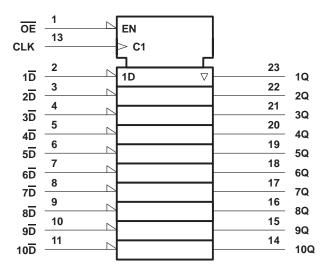
	INPUTS		OUTPUT
OE	CLK	D	Q
L	\uparrow	Н	L
L	\uparrow	L	н
L	L	Х	Q ₀ Z
н	Х	Х	Z

FUNCTION TABLE (each flip-flop)

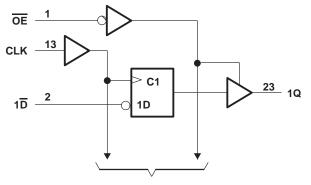
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logic symbol[†]



logic diagram (positive logic)



To Nine Other Channels

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V _{CC} Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the disabled or power-off state, V_{O}	
Voltage range applied to any output in the high state, V_0	
Input clamp current, I _{IK} (V _I < 0)	
Current into any output in the low state, IO	
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			V
VIL	Low-level input voltage			0.8	V
IIK	Input clamp current			-18	mA
ЮН	High-level output current			-24	mA
IOL	Low-level output current			48	mA
TA	Operating free-air temperature	0		70	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	Ij = -18 mA			-1.2	V
Vou	V _{CC} = 4.5 V	$I_{OH} = -15 \text{ mA}$	2.4	3.3		V
VOH	VCC = 4.5 V	$I_{OH} = -24 \text{ mA}$	2			v
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 48 mA		0.42	0.55	V
lj	V _{CC} = 5.5 V,	$V_{I} = 7 V$			0.1	mA
Чн	V _{CC} = 5.5 V,	$V_I = 2.7 V$	-10		-75	μΑ
Ι _{ΙL}	V _{CC} = 5.5 V,	$V_{I} = 0.5 V$			-0.2	mA
los‡	V _{CC} = 5.5 V,	$V_{O} = 0$	-75		-250	mA
IOZH	V _{CC} = 5.5 V,	$V_{O} = 2.7 V$			20	μΑ
I _{OZL}	V _{CC} = 5.5 V,	$V_{O} = 0.5 V$			-20	μΑ
ICCL	V _{CC} = 5.5 V,	Outputs open		25	40	mA
ІССН	V _{CC} = 5.5 V,	Outputs open		6	15	mA
ICCZ	V _{CC} = 5.5 V,	Outputs open		2	10	mA
Ci	V _{CC} = 5 V,	V _I = 2.5 V or 0.5 V		5.5		pF
Co	$V_{CC} = 5 V,$	V_{O} = 2.5 V or 0.5 V		7		pF

[†] All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$.

[‡]Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} = T _A = 2	= 5 V, 25°C	MIN	МАХ	UNIT
			MIN	MAX			
fclock	Clock frequency		0	125	0	125	MHz
tw Pulse duration, CLK high or low					4		ns
	the time data had an OLVA	High	2.5		2.5		
t _{su}	Setup time, data before CLK↑	Low			6		ns
t _h Ho	Hold time, data after CLK↑	High	0		0		ns
		Low	1.5		1.5		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			MIN	мах	UNIT
		(001201)	MIN	TYP	MAX]		
fmax			125			125		MHz
^t PLH	CLK	CLK Q	3.3	6.8	8.8	3.3	10.3	ns
^t PHL		Ŷ	4.1	6.4	7.9	4.1	8.4	115
^t PZH	OE	Q	2.8	6.1	7.9	2.8	9.3	ns
^t PZL	ÛE	Q	4.5	7.6	9.3	4.5	10.9	115
^t PHZ	OE	Q	1.6	4.7	6.3	1.6	6.7	ns
^t PLZ		Υ V	1.5	3.8	5.3	1.5	5.8	115

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74BCT29822DW	OBSOLETE	SOIC	DW	24	TBD	Call TI	Call TI
SN74BCT29822DWR	OBSOLETE	SOIC	DW	24	TBD	Call TI	Call TI
SN74BCT29822NT	OBSOLETE	PDIP	NT	24	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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