

Description

The 9QXL2000B is a 20-output very-low-additive phase jitter fanout buffer for PCIe Gen4 and Gen5. It offers integrated terminations for 85Ω transmission lines.

PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum

Typical Applications

- Servers
- Storage
- Networking
- SSDs

Features

- Low-Power HCSL (LP-HCSL) 85Ω outputs eliminate 80 resistors, saving 130mm² of area
- Low-Power HCSL (LP-HCSL) outputs reduce device power consumption by 50%
- 8 OE# pins configurable to control up to 20 outputs
- 9 selectable SMBus addresses
- Spread spectrum compatible
- 10 × 10 mm 72-VFQFPN package

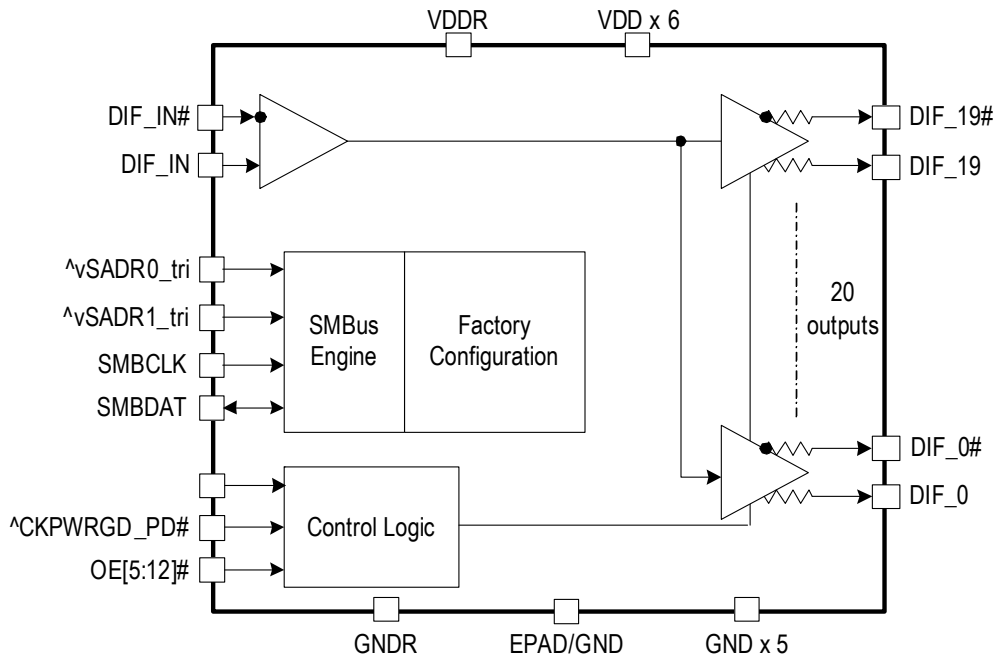
Output Features

- 20 Low-Power HCSL (LP-HCSL) 85Ω output pairs

Key Specifications

- Output-to-output skew: < 50ps
- Additive phase jitter: DB2000Q filter < 40fs rms
- Additive Phase jitter: PCIe Gen4 filter < 40fs rms
- Additive Phase jitter: PCIe Gen5 filter < 20fs rms
- DB2000Q v1.1 pinout

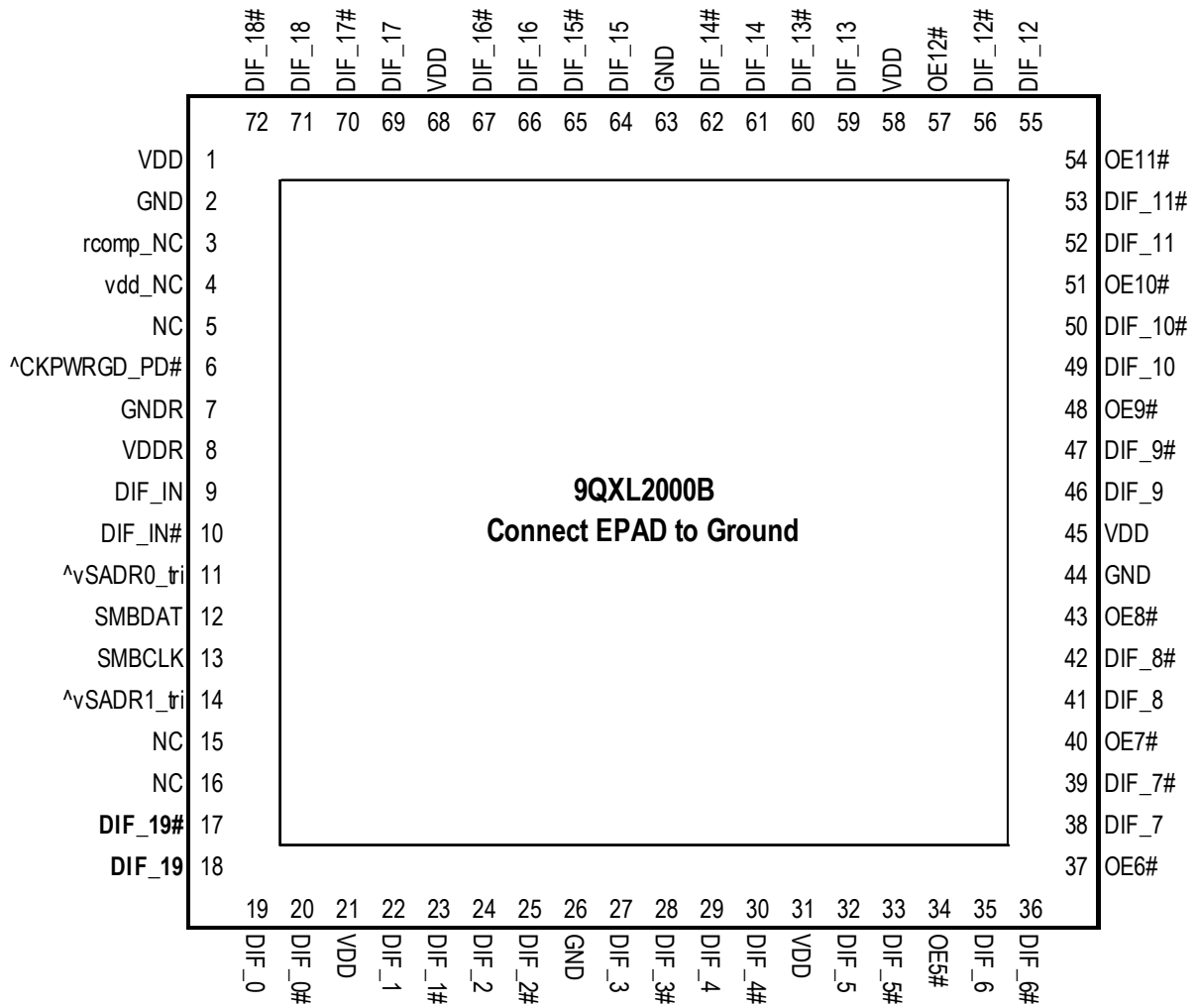
Block Diagram



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Pin Assignments



72-VFQFPN (10 x 10 mm, 0.5mm pad pitch)

- ^ prefix indicates an internal pull-up resistor
- v prefix indicates an internal pull-down resistor
- ^v prefix indicates an internal pull-up and pull-down resistor

Pin Descriptions

Table 1. Pin Descriptions

| Number | Name | Type | Description |
|--------|--------------|--------|--|
| 1 | VDD | Power | Power supply, nominally 3.3V. |
| 2 | GND | GND | Ground pin. |
| 3 | rcomp_NC | - | The DB2000Q specification calls this pin RCOMP. This pin is a true No Connect on the Renesas 9QXL2000 device, since it is not needed. Any existing connections on the board may remain to support non-Renesas DB2000Q devices. |
| 4 | vdd_NC | - | The DB2000Q specification calls this pin VDD. This pin is a true No Connect on the Renesas 9QXL2000 device, since it is not needed. Any existing connections on the board may remain to support non-Renesas DB2000Q devices. |
| 5 | NC | - | No connection. |
| 6 | ^CKPWRGD_PD# | Input | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor. |
| 7 | GNDR | GND | Analog ground pin for the differential input (receiver). |
| 8 | VDDR | Power | Power supply for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. Nominally 3.3V. |
| 9 | DIF_IN | Input | HCSL true input. |
| 10 | DIF_IN# | Input | HCSL complementary input. |
| 11 | ^vSADR0_tri | Input | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. It has internal pull up/down resistors to bias to VDD/2. See the SMBus Addressing table. |
| 12 | SMBDAT | I/O | Data pin of SMBUS circuitry |
| 13 | SMBCLK | Input | Clock pin of SMBUS circuitry |
| 14 | ^vSADR1_tri | Input | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. It has internal pull up/down resistors to bias to VDD/2. See the SMBus Addressing table. |
| 15 | NC | - | No connection. |
| 16 | NC | - | No connection. |
| 17 | DIF_19# | Output | HCSL complementary clock output. |
| 18 | DIF_19 | Output | HCSL true clock output. |
| 19 | DIF_0 | Output | HCSL true clock output. |
| 20 | DIF_0# | Output | HCSL complementary clock output. |
| 21 | VDD | Power | Power supply, nominally 3.3V. |
| 22 | DIF_1 | Output | HCSL true clock output. |
| 23 | DIF_1# | Output | HCSL complementary clock output. |
| 24 | DIF_2 | Output | HCSL true clock output. |
| 25 | DIF_2# | Output | HCSL complementary clock output. |
| 26 | GND | GND | Ground pin. |

Table 1. Pin Descriptions (Cont.)

| Number | Name | Type | Description |
|--------|---------|--------|--|
| 27 | DIF_3 | Output | HCSL true clock output. |
| 28 | DIF_3# | Output | HCSL complementary clock output. |
| 29 | DIF_4 | Output | HCSL true clock output. |
| 30 | DIF_4# | Output | HCSL complementary clock output. |
| 31 | VDD | Power | Power supply, nominally 3.3V. |
| 32 | DIF_5 | Output | HCSL true clock output. |
| 33 | DIF_5# | Output | HCSL complementary clock output. |
| 34 | OE5# | Input | Active low input for enabling output 5. 1 = disable output, 0 = enable output. |
| 35 | DIF_6 | Output | HCSL true clock output. |
| 36 | DIF_6# | Output | HCSL complementary clock output. |
| 37 | OE6# | Input | Active low input for enabling output 6. 1 = disable output, 0 = enable output. |
| 38 | DIF_7 | Output | HCSL true clock output. |
| 39 | DIF_7# | Output | HCSL complementary clock output. |
| 40 | OE7# | Input | Active low input for enabling output 7. 1 = disable output, 0 = enable output. |
| 41 | DIF_8 | Output | HCSL true clock output. |
| 42 | DIF_8# | Output | HCSL complementary clock output. |
| 43 | OE8# | Input | Active low input for enabling output 8. 1 = disable output, 0 = enable output. |
| 44 | GND | GND | Ground pin. |
| 45 | VDD | Power | Power supply, nominally 3.3V. |
| 46 | DIF_9 | Output | HCSL true clock output. |
| 47 | DIF_9# | Output | HCSL complementary clock output. |
| 48 | OE9# | Input | Active low input for enabling output 9. 1 = disable output, 0 = enable output. |
| 49 | DIF_10 | Output | HCSL true clock output. |
| 50 | DIF_10# | Output | HCSL complementary clock output. |
| 51 | OE10# | Input | Active low input for enabling output 10. 1 = disable output, 0 = enable output. |
| 52 | DIF_11 | Output | HCSL true clock output. |
| 53 | DIF_11# | Output | HCSL complementary clock output. |
| 54 | OE11# | Input | Active low input for enabling output 11. 1 = disable output, 0 = enable output. |
| 55 | DIF_12 | Output | HCSL true clock output. |

Table 1. Pin Descriptions (Cont.)

| Number | Name | Type | Description |
|--------|---------|--------|--|
| 56 | DIF_12# | Output | HCSL complementary clock output. |
| 57 | OE12# | Input | Active low input for enabling output 12. 1 = disable output, 0 = enable output. |
| 58 | VDD | Power | Power supply, nominally 3.3V. |
| 59 | DIF_13 | Output | HCSL true clock output. |
| 60 | DIF_13# | Output | HCSL complementary clock output. |
| 61 | DIF_14 | Output | HCSL true clock output. |
| 62 | DIF_14# | Output | HCSL complementary clock output. |
| 63 | GND | GND | Ground pin. |
| 64 | DIF_15 | Output | HCSL true clock output. |
| 65 | DIF_15# | Output | HCSL complementary clock output. |
| 66 | DIF_16 | Output | HCSL true clock output. |
| 67 | DIF_16# | Output | HCSL complementary clock output. |
| 68 | VDD | Power | Power supply, nominally 3.3V. |
| 69 | DIF_17 | Output | HCSL true clock output. |
| 70 | DIF_17# | Output | HCSL complementary clock output. |
| 71 | DIF_18 | Output | HCSL true clock output. |
| 72 | DIF_18# | Output | HCSL complementary clock output. |
| 73 | EPAD | GND | Connect EPAD to ground. |

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9QXL2000B. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 2. Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Unit | Notes |
|----------------------|--------------------|---|-----------|---------|----------------|------|-------|
| Supply Voltage | V_{DDx} | | - | - | 3.9 | V | 1,2 |
| Input Low Voltage | V_{IL} | | GND - 0.5 | - | - | V | 1 |
| Input High Voltage | V_{IH} | Except for SMBus interface. | - | - | $V_{DD} + 0.5$ | V | 1,3 |
| Input High Voltage | $V_{IH\text{SMB}}$ | SMBus clock and data pins. | - | - | 3.9 | V | 1 |
| Storage Temperature | T_s | | -65 | - | 150 | °C | 1 |
| Junction Temperature | T_j | Maximum operating junction temperature. | - | - | 125 | °C | 1 |
| Input ESD Protection | ESD prot | Human Body Model. | 2000 | - | - | V | 1 |

¹ Confirmed by design and characterization, not 100% tested in production.

² Operation under these conditions is neither implied nor guaranteed.

³ Not to exceed 3.9V.

Electrical Characteristics

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

Table 3. SMBus Parameters

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Unit | Notes |
|---------------------------|---------------------|---|---------|---------|--------------------|------|-------|
| SMBus Input Low Voltage | $V_{IL\text{SMB}}$ | | - | - | 0.8 | V | - |
| SMBus Input High Voltage | $V_{IH\text{SMB}}$ | | 2.1 | - | $V_{DD\text{SMB}}$ | V | - |
| SMBus Output Low Voltage | $V_{OL\text{SMB}}$ | At I_{PULLUP} . | - | - | 0.4 | V | - |
| SMBus Sink Current | I_{PULLUP} | At V_{OL} . | 4 | - | - | mA | - |
| Nominal Bus Voltage | $V_{DD\text{SMB}}$ | | 2.7 | - | 3.6 | V | 1 |
| SCLK/SDATA Rise Time | t_{RSMB} | (Max $V_{IL} - 0.15V$) to (Min $V_{IH} + 0.15V$). | - | - | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | t_{FSMB} | (Min $V_{IH} + 0.15V$) to (Max $V_{IL} - 0.15V$). | - | - | 300 | ns | 1 |
| SMBus Operating Frequency | $f_{SMB\text{MAX}}$ | Maximum SMBus operating frequency. | - | - | 400 | kHz | 5 |

¹ Confirmed by design and characterization, not 100% tested in production.

² Control input must be monotonic from 20% to 80% of input swing.

³ Time from deassertion until outputs are > 200mV.

⁴ DIF_IN input.

⁵ The differential input clock must be running for the SMBus to be active.

Table 4. DIF_IN Clock Input Parameters

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Unit | Notes |
|----------------------------------|-------------|---|---------|---------|---------|---------|-------|
| Input Crossover Voltage – DIF_IN | V_{CROSS} | Cross over voltage. | 100 | - | 900 | mV | 1 |
| Input Swing – DIF_IN | V_{SWING} | Differential value. | 200 | - | - | mV | 1 |
| Input Slew Rate – DIF_IN | dv/dt | Measured differentially. | 0.7 | - | - | V/ns | 1,2 |
| Input Leakage Current | I_{IN} | $V_{IN} = V_{DD}$, $V_{IN} = GND$. | -5 | - | 5 | μA | - |
| Input Duty Cycle | d_{tin} | Measurement from differential waveform. | 45 | - | 55 | % | 1 |

¹ Confirmed by design and characterization, not 100% tested in production.

² Slew rate measured through $\pm 75mV$ window centered around differential zero.

Table 5. Input/Supply/Common Parameters

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Unit | Notes |
|-------------------------------|-----------------|--|-----------|------------|----------------|-------------|-------|
| Supply Voltage | V_{DDx} | Supply voltage for core and analog. | 3.135 | 3.3 | 3.465 | V | - |
| Ambient Operating Temperature | T_{AMB} | Industrial range (T_{IND}). | -40 | 25 | 85 | $^{\circ}C$ | - |
| Input High Voltage | V_{IH} | Single-ended inputs, except SMBus, tri-level inputs. | 2 | - | $V_{DD} + 0.3$ | V | - |
| Input Low Voltage | V_{IL} | Single-ended inputs, except SMBus, tri-level inputs. | GND - 0.3 | - | 0.8 | V | - |
| Input High Voltage | V_{IH} | Tri-level inputs. | 2.2 | - | $V_{DD} + 0.3$ | V | - |
| Input Mid Voltage | V_{IM} | Tri-level inputs. | 1.2 | $V_{DD}/2$ | 1.8 | V | - |
| Input Low Voltage | V_{IL} | Tri-level inputs. | GND - 0.3 | - | 0.8 | V | - |
| Input Current | I_{IN} | Single-ended inputs, $V_{IN} = GND$, $V_{IN} = V_{DD}$. | -5 | - | 5 | μA | - |
| | I_{INP} | Single-ended inputs. $V_{IN} = 0V$; inputs with internal pull-up resistors. $V_{IN} = V_{DD}$; inputs with internal pull-down resistors. | -50 | - | 50 | μA | - |
| Input Frequency | F_{ibyp} | $V_{DD} = 3.3V$. | 1 | - | 400 | MHz | - |
| Pin Inductance | L_{pin} | | | - | 7 | nH | 1 |
| Capacitance | C_{IN} | Logic inputs, except DIF_IN. | 1.5 | - | 5 | pF | 1 |
| | C_{INDIF_IN} | DIF_IN differential clock inputs. | 1.5 | - | 2.7 | pF | 1,4 |
| | C_{OUT} | Output pin capacitance. | - | - | 6 | pF | 1 |
| Clk Stabilization | T_{STAB} | From V_{DD} power-up and after input clock stabilization or deassertion of PD# to 1st clock. | - | 1.0 | 1.8 | ms | 1,2 |
| OE# Latency | $t_{LATOE\#}$ | DIF start after OE# assertion. DIF stop after OE# deassertion. | 4 | 5 | 10 | clocks | 1,2,3 |

Table 5. Input/Supply/Common Parameters (Cont.)

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Unit | Notes |
|------------|--------------------|--|---------|---------|---------|------|-------|
| Tdrive_PD# | t _{DRVDP} | DIF output enable after PD# deassertion. | - | 76 | 300 | μs | 1,3 |
| Tfall | t _F | Fall time of control inputs. | - | - | 5 | ns | 2 |
| Trise | t _R | Rise time of control inputs. | - | - | 5 | ns | 2 |

¹ Confirmed by design and characterization, not 100% tested in production.

² Control input must be monotonic from 20% to 80% of input swing.

³ Time from deassertion until outputs are > 200mV.

⁴ DIF_IN input.

Table 6. Current Consumption

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Unit | Notes |
|--------------------------|------------------------|---|---------|---------|---------|------|-------|
| Operating Supply Current | I _{DDVDD} | All outputs 100MHz, C _L = 2pF; Z _o = 85Ω. | - | 177 | 219 | mA | - |
| | I _{DDVDDA/R} | All outputs 100MHz, C _L = 2pF; Z _o = 85Ω. | - | 3 | 5 | mA | - |
| Power Down Current | I _{DDVDDP} | All differential pairs low-low. | - | 0.6 | 1 | mA | - |
| | I _{DDVDDA/RP} | All differential pairs low-low. | - | 0.8 | 1.1 | mA | - |

Table 7. Skew and Differential Jitter Parameters

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Unit | Notes |
|-----------------------|--------------------------|---|---------|---------|---------|-------|-------------|
| CLK_IN, DIF[x:0] | t _{PD} | Input-to-output skew. | 2.3 | 2.7 | 3 | ns | 1,2,3,4,5,7 |
| CLK_IN, DIF[x:0] | t _{PDVARIATION} | Input-to-output skew variation for a given device at a given voltage. | - | - | 2 | ps/°C | 1,2,3,5,8 |
| DIF[x:0] | t _{SKREW_ALL} | Output-to-output skew across all outputs. | - | 28 | 50 | ps | 1,2,3,7 |
| Duty Cycle Distortion | t _{DCD} | Measured differentially at 100MHz. | -0.6 | -0.3 | 0 | % | 1,6,7 |

¹ Measured into fixed 2pF load cap. Input to output skew is measured at the first output edge following the corresponding input.

² Measured from differential cross-point to differential cross-point.

³ All input-to-output specs refer to the timing between an input edge and the specific output edge created by it.

⁴ Measured with scope averaging on to find mean value.

⁵ Confirmed by design and characterization, not 100% tested in production.

⁶ Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in Bypass Mode.

⁷ Measured from differential waveform.

⁸ This is the amount of input-to-output delay variation with respect to temperature. This is equivalent to 250ps over the -40°C to +85°C temperature range.

Table 8. LP-HCSL Outputs Driving High Impedance Receiver

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limits | Unit | Notes |
|------------------------|------------|--|---------|---------|---------|-----------------|------|---------|
| Slew Rate | dV/dt | Scope averaging on, fast setting. | 2 | 2.4 | 4 | 1 – 4 | V/ns | 1,2,3 |
| Rise/Fall Matching | ΔtR/tF | Single-ended measurement. | | 5.3 | 16 | 20 | % | - |
| Maximum Voltage | Vmax | Measurement on single-ended signal using absolute value (scope averaging off). | 700 | 790 | 875 | 660 – 1150 | mV | 7,8 |
| Minimum Voltage | Vmin | | -150 | -50 | 25 | -300 – +150 | | 1,5,7,8 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off. | 250 | 370 | 550 | 250 – 550 | mV | 1,6,7 |
| Crossing Voltage (var) | Δ-Vcross | Scope averaging off. | - | 15 | 50 | 140 | mV | 1,6,7 |

¹ Confirmed by design and characterization, not 100% tested in production.

² Measured from differential waveform.

³ Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a ±150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

⁷ At default SMBus settings.

⁸ Includes 300mV of overshoot for Vmax and 300mV of undershoot for Vmin.

Table 9. Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Specification Limits | Unit | Notes |
|------------------------------------|----------------------|--|---------|---------|---------|----------------------|----------|---------|
| Additive Phase Jitter, Bypass Mode | $t_{jphPCIeG1-CC}$ | PCIe Gen1. | - | 0.21 | 1.3 | Not Applicable | ps (p-p) | 1,2,3,4 |
| | $t_{jphPCIeG2-CC}$ | PCIe Gen2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz). | - | 0.0041 | 0.0045 | | ps (rms) | 1,2,4,6 |
| | | PCIe Gen2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz). | - | 0.07 | 0.1 | | ps (rms) | 1,2,4,6 |
| | $t_{jphPCIeG3/4-CC}$ | PCIe Gen3, Gen4 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz). | - | 0.03 | 0.04 | | ps (rms) | 1,2,4,6 |
| | $t_{jphPCIeG5-CC}$ | PCIe Gen5 (see PCIe Gen5 specifications for details). | - | 0.01 | 0.02 | | ps (rms) | 1,2,4,6 |

Table 10. Filtered Phase Jitter Parameters – PCIe Independent Reference (IR) Architectures

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limits | Unit | Notes |
|------------------------------------|----------------------|---|---------|---------|---------|-----------------|----------|---------|
| Additive Phase Jitter, Bypass Mode | $t_{jphPCIeG2-SRIS}$ | PCIe Gen2 (PLL BW of 16MHz, CDR = 5MHz). | - | 0.09 | 0.104 | Not applicable | ps (rms) | 1,2,4,6 |
| | $t_{jphPCIeG3-SRIS}$ | PCIe Gen3 (PLL BW of 2–4MHz, CDR = 10MHz). | - | 0.02 | 0.03 | | ps (rms) | 1,2,4,6 |

Notes for PCIe Filtered Phase Jitter tables (CC) and (IR).

- ¹ Applies to all differential outputs, guaranteed by design and characterization.
- ² Applies to all outputs when driven by a low phase noise source.
- ³ Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1⁻¹².
- ⁴ For RMS values, additive jitter is calculated by solving for “b” [$b = \sqrt{c^2 - a^2}$] where “a” is rms input jitter and “c” is rms total jitter.
- ⁵ IR is the new name for Separate Reference Independent Spread (SRIS) and Separate Reference no Spread (SRNS) PCIe clock architectures. According to the PCIe Base Specification Rev4.0 version 1.0, the jitter transfer functions and corresponding jitter limits are not defined for the IR clock architecture. The IR filters from the PCIe Base Specification, Rev 3.1a are used to populate this table. There are no accepted filters or limits for IR clock architectures at PCIe Gen1 or Gen4 data rates at the time of publication.
- ⁶ Measured using SMA100B signal source, or equivalent, and a phase noise analyzer.

Table 11. Filtered Phase Jitter Parameters – DB2000Q Filter

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Specification Limits | Unit | Notes |
|-----------------------|---------------------|------------|---------|---------|---------|----------------------|----------|-------|
| Additive Phase Jitter | $t_{jphDB2000Qadd}$ | 100MHz. | - | 24 | 40 | 80 | fs (rms) | 1,2,3 |

¹ Applies to all outputs when driven by a low phase noise source.

² After applying DB2000Q filter.

³ For RMS values, additive jitter is calculated by solving for “b” [$b = \sqrt{c^2 - a^2}$] where “a” is rms input jitter and “c” is rms total jitter.

Table 12. Unfiltered Phase Jitter Parameters – 12kHz to 20MHz

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limits | Unit | Notes |
|-----------------------|---------------------|------------|---------|---------|---------|-----------------|----------|-------|
| Additive Phase Jitter | $t_{jph12k-20Madd}$ | 100MHz. | - | 97 | 121 | N/A | fs (rms) | 1,2,3 |
| | | 156.25MHz. | - | 86 | 103 | | | |

¹ Applies to all outputs when driven by a low phase noise source.

² 12kHz to 20MHz brick wall filter.

³ For RMS values, additive jitter is calculated by solving for “b” [$b = \sqrt{c^2 - a^2}$] where “a” is rms input jitter and “c” is rms total jitter.

Power Management

| Inputs | | | | | Outputs |
|-------------|---------|-------------------|--------------------------|----------|---------|
| CKPWRGD_PD# | DIF_IN | OEx bit Byte[2:0] | OE Pin CFG bit Byte[8,9] | OEx# Pin | DIFx |
| 0 | X | X | X | X | Low/Low |
| 1 | Running | 0 | X | X | Low/Low |
| | | 1 | 0 | X | Running |
| 1 | Running | 1 | 1 | 0 | Running |
| | | 1 | 1 | 1 | Low/Low |

Power Connections

| Pin Number | | Description |
|-----------------------|---------------|-------------|
| V _{DD} | GND | |
| 8 | 7 | Analog Rx |
| 1, 21, 31, 45, 58, 68 | 2, 26, 44, 63 | DIF clocks |

SMBus Addressing

| Pin | | SMBus Address (Read/Write bit = 0) |
|------------|------------|------------------------------------|
| SMB_A1_tri | SMB_A0_tri | |
| 0 | 0 | D8 |
| 0 | M | DA |
| 0 | 1 | DE |
| M | 0 | C2 |
| M | M | C4 |
| M | 1 | C6 |
| 1 | 0 | CA |
| 1 | M | CC |
| 1 | 1 | CE |

Test Loads

Figure 1. AC/DC Test Load for High Impedance Receivers

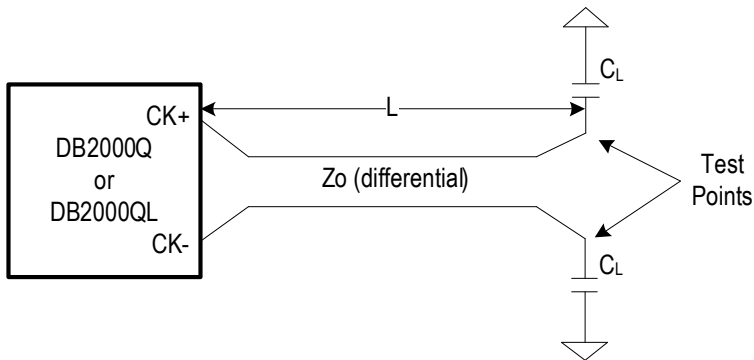


Figure 2. Test Setup for DB2000Q Additive Phase Jitter Measurement

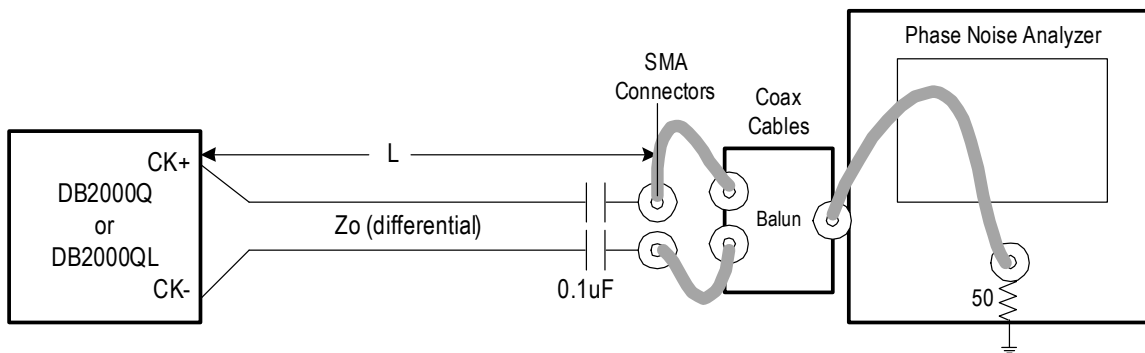


Table 13. Parameters for Test Loads

| Rs (Ω) | Zo (Ω) | L (cm) | C _L (pF) |
|-----------------|-----------------|--------|---------------------|
| Internal | 85 | 30.5 | 2 |

Alternate Terminations

The LP-HCSL output can easily drive other logic families. See [“AN-891 Driving LVPECL, LVDS, and CML Logic with “Universal” Low-Power HCSL Outputs”](#) for termination schemes for LVPECL, LVDS, CML and SSTL.

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending ByteN – ByteN + X -1
- Renesas clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a stop bit

| Index Block Write Operation | | |
|-----------------------------|-----------|--------------------------|
| Controller (Host) | | Renesas (Slave/Receiver) |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| Data Byte Count = X | | |
| | | ACK |
| Beginning Byte N | | |
| | | ACK |
| O | | O |
| O | | O |
| O | | O |
| | | |
| Byte N + X - 1 | | |
| | | ACK |
| P | stoP bit | |

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends ByteN + X - 1
- Renesas clock sends **Byte0 – ByteX (if X_(H) was written to Byte8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | |
|----------------------------|-----------------|--------------------------|
| Controller (Host) | | Renesas (Slave/Receiver) |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| RT | Repeat starT | |
| Slave Address | | |
| RD | ReaD | |
| | X Byte | ACK |
| | | |
| ACK | | Data Byte Count=X |
| ACK | | Beginning Byte N |
| | | O |
| | | O |
| | | O |
| | | |
| ACK | | Byte N + X - 1 |
| N | Not acknowledge | |
| P | stoP bit | |

SMBus Table: Output Enable Register

| Byte 0 | Name | Control Function | Type | 0 | 1 | Default |
|--------|-----------|------------------|------|---------|--------|---------|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | DIF_19_En | Output Enable | RW | Low/Low | Enable | 1 |
| Bit 5 | DIF_18_En | Output Enable | RW | Low/Low | Enable | 1 |
| Bit 4 | DIF_17_En | Output Enable | RW | Low/Low | Enable | 1 |
| Bit 3 | DIF_16_En | Output Enable | RW | Low/Low | Enable | 1 |
| Bit 2 | Reserved | | | | | 0 |
| Bit 1 | Reserved | | | | | 0 |
| Bit 0 | Reserved | | | | | 0 |

SMBus Table: Output Enable Register

| Byte 1 | Name | Control Function | Type | 0 | 1 | Default |
|--------|----------|------------------|------|---------|---|---------|
| Bit 7 | DIF_7_En | Output Enable | RW | Low/Low | Pin Control (See Byte 8, 9 or 10) | 1 |
| Bit 6 | DIF_6_En | Output Enable | RW | | | 1 |
| Bit 5 | DIF_5_En | Output Enable | RW | | | 1 |
| Bit 4 | DIF_4_En | Output Enable | RW | | | 1 |
| Bit 3 | DIF_3_En | Output Enable | RW | | | 1 |
| Bit 2 | DIF_2_En | Output Enable | RW | | | 1 |
| Bit 1 | DIF_1_En | Output Enable | RW | | | 1 |
| Bit 0 | DIF_0_En | Output Enable | RW | | | 1 |

SMBus Table: Output Enable Register

| Byte 2 | Name | Control Function | Type | 0 | 1 | Default |
|--------|-----------|------------------|------|---------|---|---------|
| Bit 7 | DIF_15_En | Output Enable | RW | Low/Low | Pin Control (See Byte 8, 9 or 10) | 1 |
| Bit 6 | DIF_14_En | Output Enable | RW | | | 1 |
| Bit 5 | DIF_13_En | Output Enable | RW | | | 1 |
| Bit 4 | DIF_12_En | Output Enable | RW | | | 1 |
| Bit 3 | DIF_11_En | Output Enable | RW | | | 1 |
| Bit 2 | DIF_10_En | Output Enable | RW | | | 1 |
| Bit 1 | DIF_9_En | Output Enable | RW | | | 1 |
| Bit 0 | DIF_8_En | Output Enable | RW | | | 1 |

SMBus Table: Reserved Register

| Byte 3 | Name | Control Function | Type | 0 | 1 | Default |
|--------|---------|-----------------------------|------|-------------|--------------|-----------|
| Bit 7 | RB_OE12 | Real Time Readback of OE#12 | R | OE# pin Low | OE# Pin High | Real-time |
| Bit 6 | RB_OE11 | Real Time Readback of OE#11 | R | | | Real-time |
| Bit 5 | RB_OE10 | Real Time Readback of OE#10 | R | | | Real-time |
| Bit 4 | RB_OE9 | Real Time Readback of OE#9 | R | | | Real-time |
| Bit 3 | RB_OE8 | Real Time Readback of OE#8 | R | | | Real-time |
| Bit 2 | RB_OE7 | Real Time Readback of OE#7 | R | | | Real-time |
| Bit 1 | RB_OE6 | Real Time Readback of OE#6 | R | | | Real-time |
| Bit 0 | RB_OE5 | Real Time Readback of OE#5 | R | | | Real-time |

Byte 4 is Reserved and reads back 0h00.

SMBus Table: Vendor & Revision ID Register

| Byte 5 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------|------------------|------|---------------|---|---------|
| Bit 7 | RID3 | REVISION ID | R | B rev is 0001 | | 0 |
| Bit 6 | RID2 | | R | | | 0 |
| Bit 5 | RID1 | | R | | | x |
| Bit 4 | RID0 | | R | | | x |
| Bit 3 | VID3 | VENDOR ID | R | Renesas/IDT | | 0 |
| Bit 2 | VID2 | | R | | | 0 |
| Bit 1 | VID1 | | R | | | 0 |
| Bit 0 | VID0 | | R | | | 1 |

SMBus Table: Device ID

| Byte 6 | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------------------|------------------|------|------------|---|---------|
| Bit 7 | Device ID 7 (MSB) | | R | 2000 is C8 | | 1 |
| Bit 6 | Device ID 6 | | R | | | 1 |
| Bit 5 | Device ID 5 | | R | | | 0 |
| Bit 4 | Device ID 4 | | R | | | 0 |
| Bit 3 | Device ID 3 | | R | | | 1 |
| Bit 2 | Device ID 2 | | R | | | 0 |
| Bit 1 | Device ID 1 | | R | | | x |
| Bit 0 | Device ID 0 | | R | | | 0 |

SMBus Table: Byte Count Register

| Byte 7 | Name | Control Function | Type | 0 | 1 | Default |
|--------|----------|---|------|-------------------------|---|---------|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | Reserved | | | | | 0 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | BC4 | Writing to this register configures how many bytes will be read back. | RW | Default value is 8 hex. | | 0 |
| Bit 3 | BC3 | | RW | | | 1 |
| Bit 2 | BC2 | | RW | | | 0 |
| Bit 1 | BC1 | | RW | | | 0 |
| Bit 0 | BC0 | | RW | | | 0 |

SMBus Table: OE Pin Configuration A Register

| Byte8 | Name | Control Function | Type | 0 | 1 | Default |
|-------|-------------|------------------|------|------------------|----------|---------|
| Bit 7 | OE12#_CFG A | Controls DIF_12 | RW | Does not Control | Controls | 1 |
| Bit 6 | OE11#_CFG A | Controls DIF_11 | RW | | | 1 |
| Bit 5 | OE10#_CFG A | Controls DIF_10 | RW | | | 1 |
| Bit 4 | OE09#_CFG A | Controls DIF_9 | RW | | | 1 |
| Bit 3 | OE08#_CFG A | Controls DIF_8 | RW | | | 1 |
| Bit 2 | OE07#_CFG A | Controls DIF_7 | RW | | | 1 |
| Bit 1 | OE06#_CFG A | Controls DIF_6 | RW | | | 1 |
| Bit 0 | OE05#_CFG A | Controls DIF_5 | RW | | | 1 |

SMBus Table: OE Pin Configuration B Register

| Byte 9 | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------------|------------------|------|------------------|----------|---------|
| Bit 7 | OE12#_CFG B | Controls DIF_13 | RW | Does not Control | Controls | 0 |
| Bit 6 | OE11#_CFG B | Controls DIF_14 | RW | | | 0 |
| Bit 5 | OE10#_CFG B | Controls DIF_15 | RW | | | 0 |
| Bit 4 | OE09#_CFG B | Controls DIF_0 | RW | | | 0 |
| Bit 3 | OE08#_CFG B | Controls DIF_1 | RW | | | 0 |
| Bit 2 | OE07#_CFG B | Controls DIF_2 | RW | | | 0 |
| Bit 1 | OE06#_CFG B | Controls DIF_3 | RW | | | 0 |
| Bit 0 | OE05#_CFG B | Controls DIF_4 | RW | | | 0 |

SMBus Table: OE Pin Configuration C and Output Amplitude Register

| Byte 10 | Name | Control Function | Type | 0 | 1 | Default |
|---------|-----------|------------------------------------|------|-----------------------------------|----------|---------|
| Bit 7 | OE12#_CFG | Controls DIF_16 | | Does not Control | Controls | 0 |
| Bit 6 | OE11#_CFG | Controls DIF_17 | | | | 0 |
| Bit 5 | OE10#_CFG | Controls DIF_18 | | | | 0 |
| Bit 4 | OE09#_CFG | Controls DIF_19 | | | | 0 |
| Bit 3 | Reserved | | | | | 0 |
| Bit 2 | AMP[2] | Global Differential Output Control | RW | 0.3V–1V 100mV/step Default = 0.8V | | 1 |
| Bit 1 | AMP[1] | | RW | | | 0 |
| Bit 0 | AMP[0] | | RW | | | 1 |

Bytes 11–20 are Reserved.

SMBus Table: PD_RESTORE

| Byte 21 | Name | Control Function | Type | 0 | 1 | Default |
|---------|-------------|----------------------------------|------|----------------|--------------|---------|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | Reserved | | | | | 0 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | PD_RESTORE# | Save Configuration in Power Down | RW | Config Cleared | Config Saved | 1 |
| Bit 2 | Reserved | | | | | 0 |
| Bit 1 | Reserved | | | | | 0 |
| Bit 0 | Reserved | | | | | 0 |

Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see [Ordering Information](#) for POD links). The package information is the most current data available and is subject to change without revision of this document.

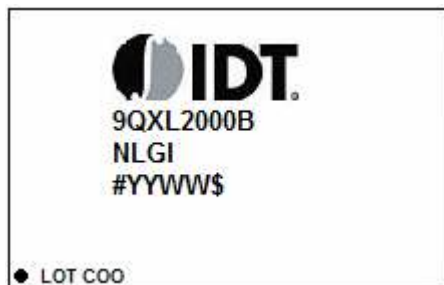
Ordering Information

| Orderable Part Number | Package | Carrier Type | Temperature |
|-----------------------|--|--------------|----------------|
| 9QXL2000BNLGI | 10 x 10 mm, 0.50mm pitch 72-VFQFPN | Trays | -40°C to +85°C |
| 9QXL2000BNLGI8 | 10 x 10 mm, 0.50mm pitch 72-VFQFPN | Reel | -40°C to +85°C |

“G” designates PB-free configuration, RoHS compliant.

“B” is the device revision designator (will not correlate with the datasheet revision).

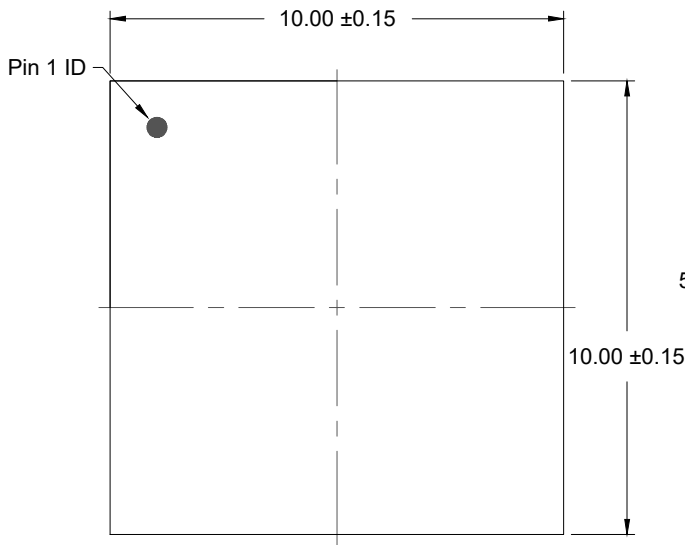
Marking Diagram



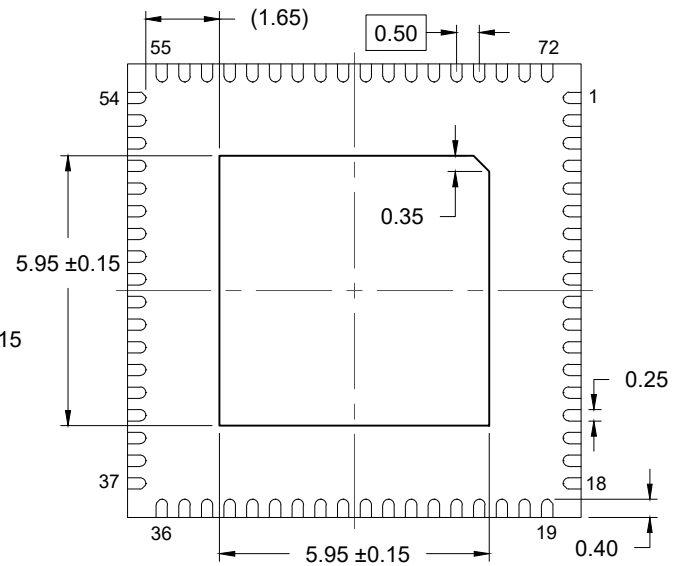
- Lines 2 and 3: part number
 - “I” denotes industrial temperature range
- Line 4:
 - “#” denotes the stepping number.
 - “YYWW” denotes the last two digits of the year and work-week the part was assembled.
 - “\$” denotes the mark code.
- “LOT” denotes the lot number.
- “COO” denotes country of origin.

Revision History

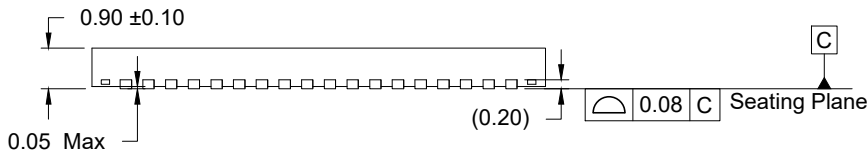
| Revision Date | Description of Change |
|-------------------|---|
| March 9, 2022 | Updated front page description. |
| June 10, 2021 | <ul style="list-style-type: none"> ▪ Removed bytes 11–20 and noted them as reserved. |
| May 8, 2020 | <ul style="list-style-type: none"> ▪ Added $t_{PDVARIATION}$ specification to Table 7. Footnote 3 updated and footnote 8 added. ▪ “Slew Rate Matching” changed to “Rise/Fall Matching” in Table 8. |
| February 22, 2019 | Updated Test Loads length (L) parameter. |
| February 15, 2019 | Initial release. |



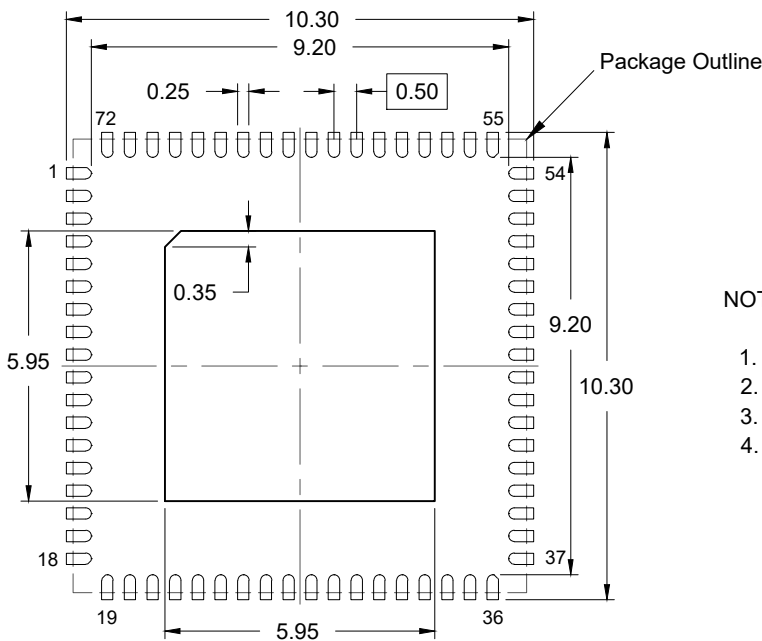
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Numbers in () are for references only.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
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