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March 2014

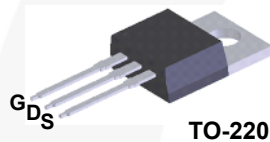
# FCP11N60/FCPF11N60

## General Description

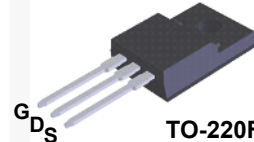
SuperFET® MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.

## Features

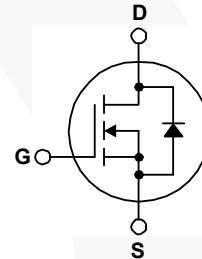
- 650V @ $T_j = 150^\circ\text{C}$
- Typ.  $R_{ds(on)} = 0.32\Omega$
- Ultra low gate charge (typ.  $Q_g = 40\text{nC}$ )
- Low effective output capacitance (typ.  $C_{oss,eff} = 95\text{pF}$ )
- 100% avalanche tested
- RoHS Compliant



TO-220



TO-220F



## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FCP11N60	FCPF11N60	Units
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	11	11*	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	7	7*	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	33	33*	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$		V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	340		mJ
$I_{AR}$	Avalanche Current (Note 1)	11		A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	12.5		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	125	36	W
	- Derate above $25^\circ\text{C}$	1.0	0.29	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

\* Drain current limited by maximum junction temperature

## Thermal Characteristics

Symbol	Parameter	FCP11N60	FCPF11N60	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.0	3.5	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	0.5	--	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	$^\circ\text{C}/\text{W}$

FCP11N60 / FCPF11N60 — N-Channel SuperFET® MOSFET

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP11N60	FCP11N60	TO-220	Tube	N/A	N/A	50 units
FCPF11N60	FCPF11N60	TO-220F	Tube	N/A	N/A	50 units
FCPF11N60T	FCPF11N60T	TO-220F	Tube	N/A	N/A	50 units

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_J = 25^\circ\text{C}$	600	--	--	V
		$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_J = 150^\circ\text{C}$	--	650	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.6	--	$\text{V}^\circ\text{C}$
$BV_{DS}$	Drain-Source Avalanche Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 11\text{ A}$	--	700	--	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 5.5\text{ A}$	--	0.32	0.38	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 5.5\text{ A}$ (Note 4)	--	9.7	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	1148	1490	pF
$C_{oss}$	Output Capacitance		--	671	870	pF
$C_{rss}$	Reverse Transfer Capacitance		--	63	82	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	35	--	pF
$C_{oss\text{ eff.}}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$	--	95	--	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 11\text{ A},$ $R_G = 25\ \Omega$	--	34	80	ns
$t_r$	Turn-On Rise Time		--	98	205	ns
$t_{d(off)}$	Turn-Off Delay Time		--	119	250	ns
$t_f$	Turn-Off Fall Time		(Note 4, 5)	--	56	120
$Q_g$	Total Gate Charge	$V_{DS} = 480\text{ V}, I_D = 11\text{ A},$ $V_{GS} = 10\text{ V}$	--	40	52	nC
$Q_{gs}$	Gate-Source Charge		--	7.2	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4, 5)	--	21	--

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	11	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	33	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 11\text{ A}$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 11\text{ A},$	--	390	--	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	5.7	--	$\mu\text{C}$

#### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $I_{AS} = 5.5\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 11\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\ \mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

## Typical Characteristics

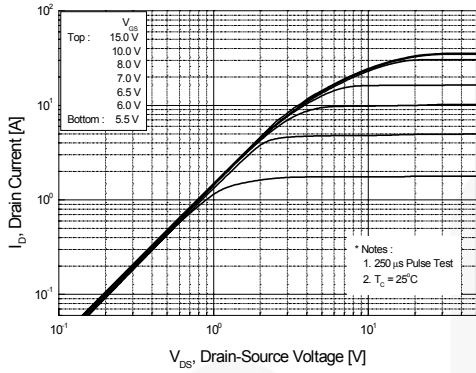


Figure 1. On-Region Characteristics

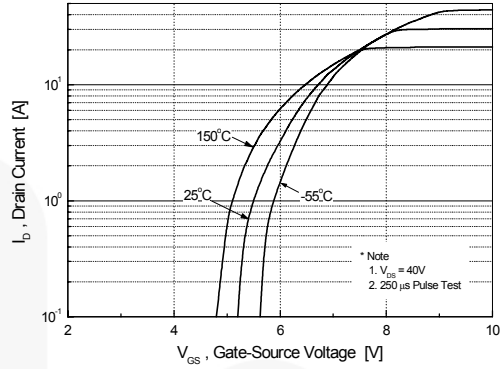


Figure 2. Transfer Characteristics

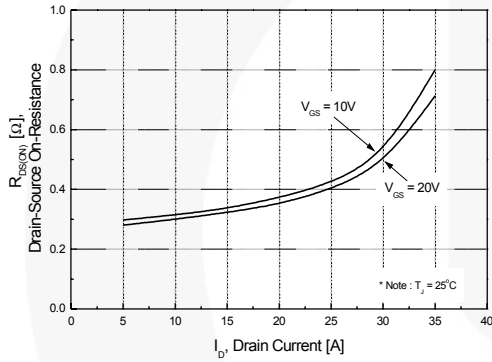


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

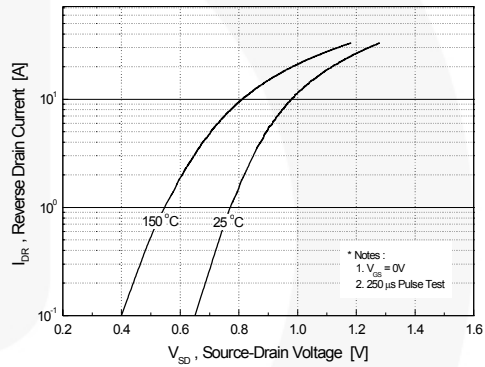


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

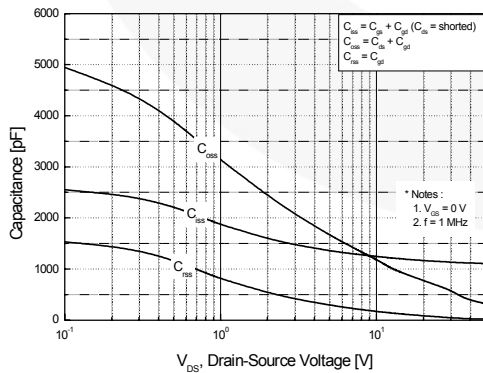


Figure 5. Capacitance Characteristics

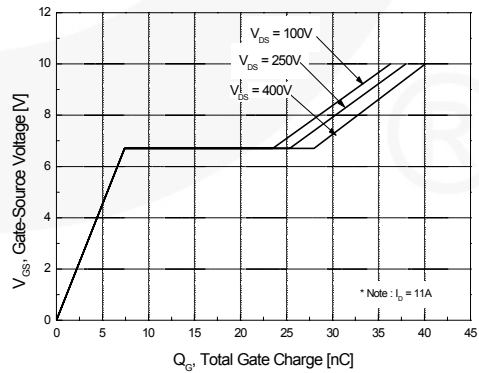
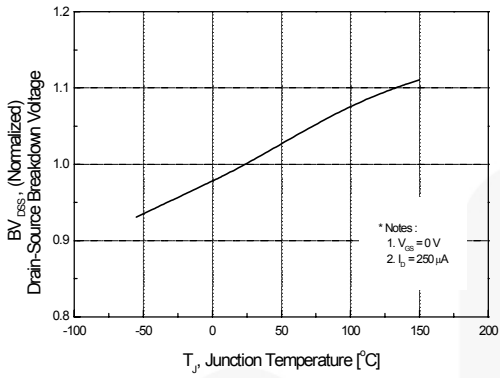
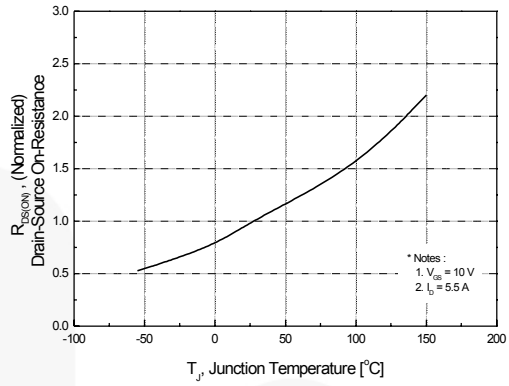


Figure 6. Gate Charge Characteristics

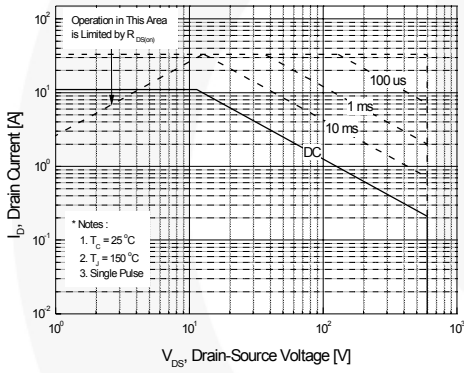
**Typical Characteristics** (Continued)



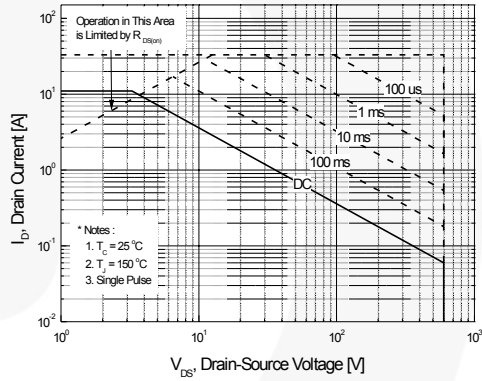
**Figure 7. Breakdown Voltage Variation vs. Temperature**



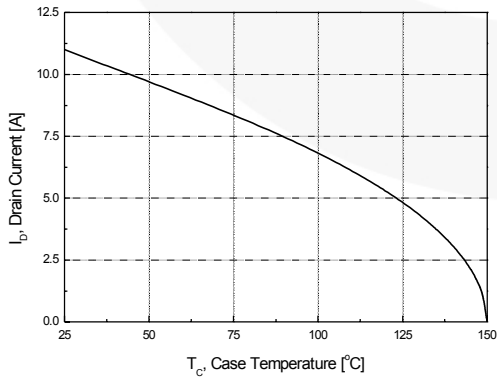
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9-1. Maximum Safe Operating Area for FCP11N60**

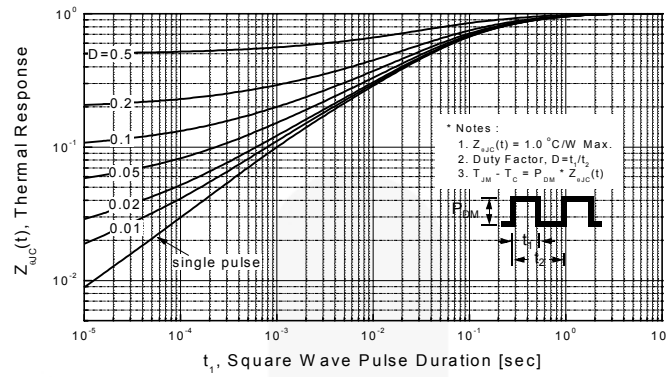


**Figure 9-2. Maximum Safe Operating Area for FCPF11N60**

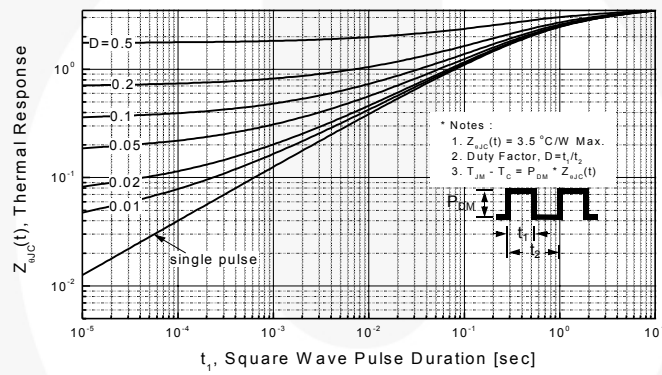


**Figure 10. Maximum Drain Current vs. Case Temperature**

**Typical Characteristics** (Continued)



**Figure 11-1. Transient Thermal Response Curve for FCP11N60**



**Figure 11-2. Transient Thermal Response Curve for FCPF11N60**

Figure 12. Gate Charge Test Circuit & Waveform

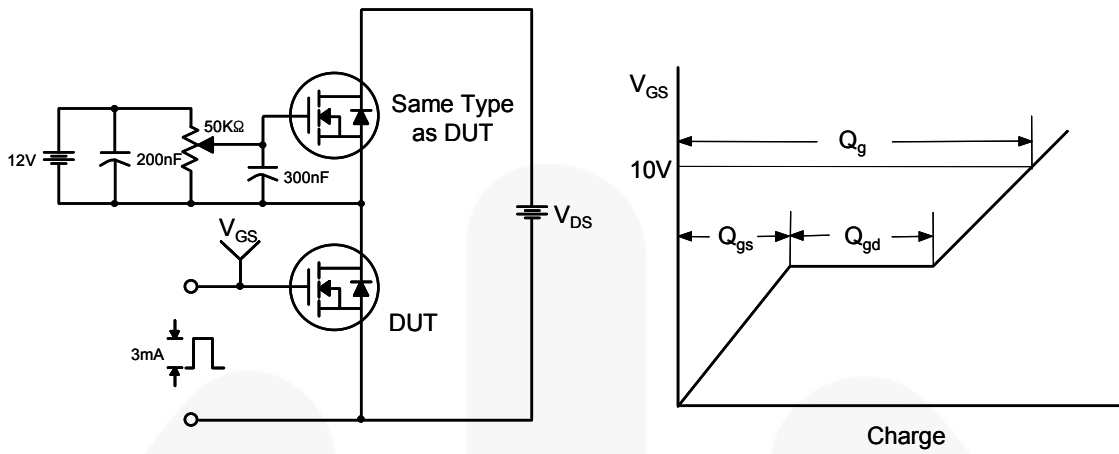


Figure 13. Resistive Switching Test Circuit & Waveforms

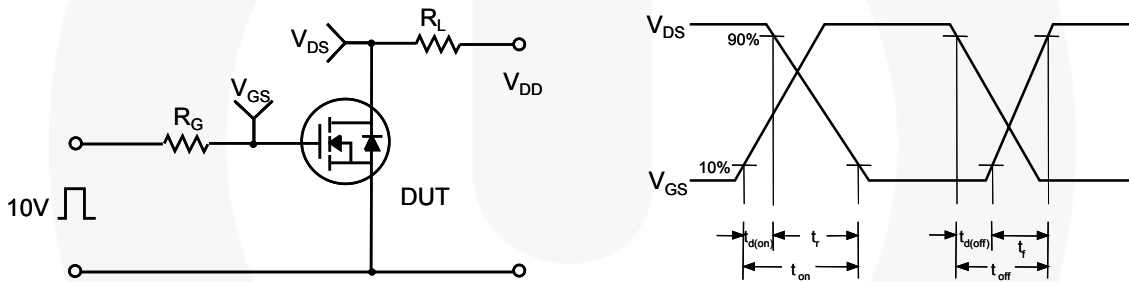


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

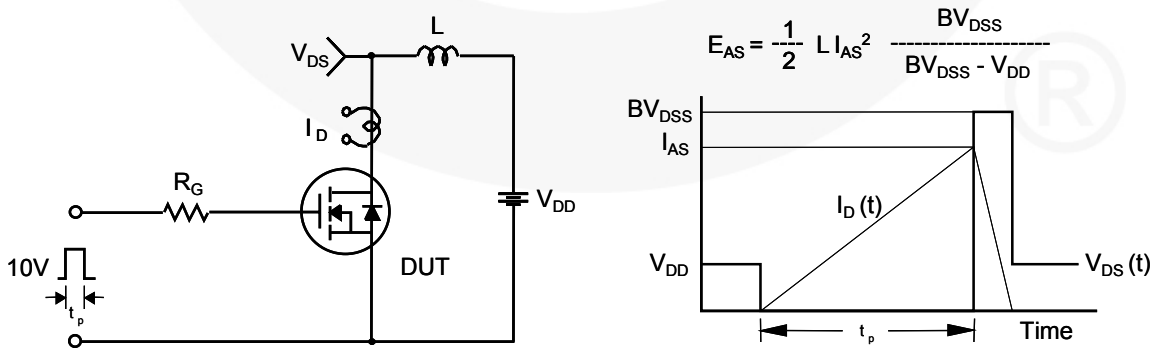
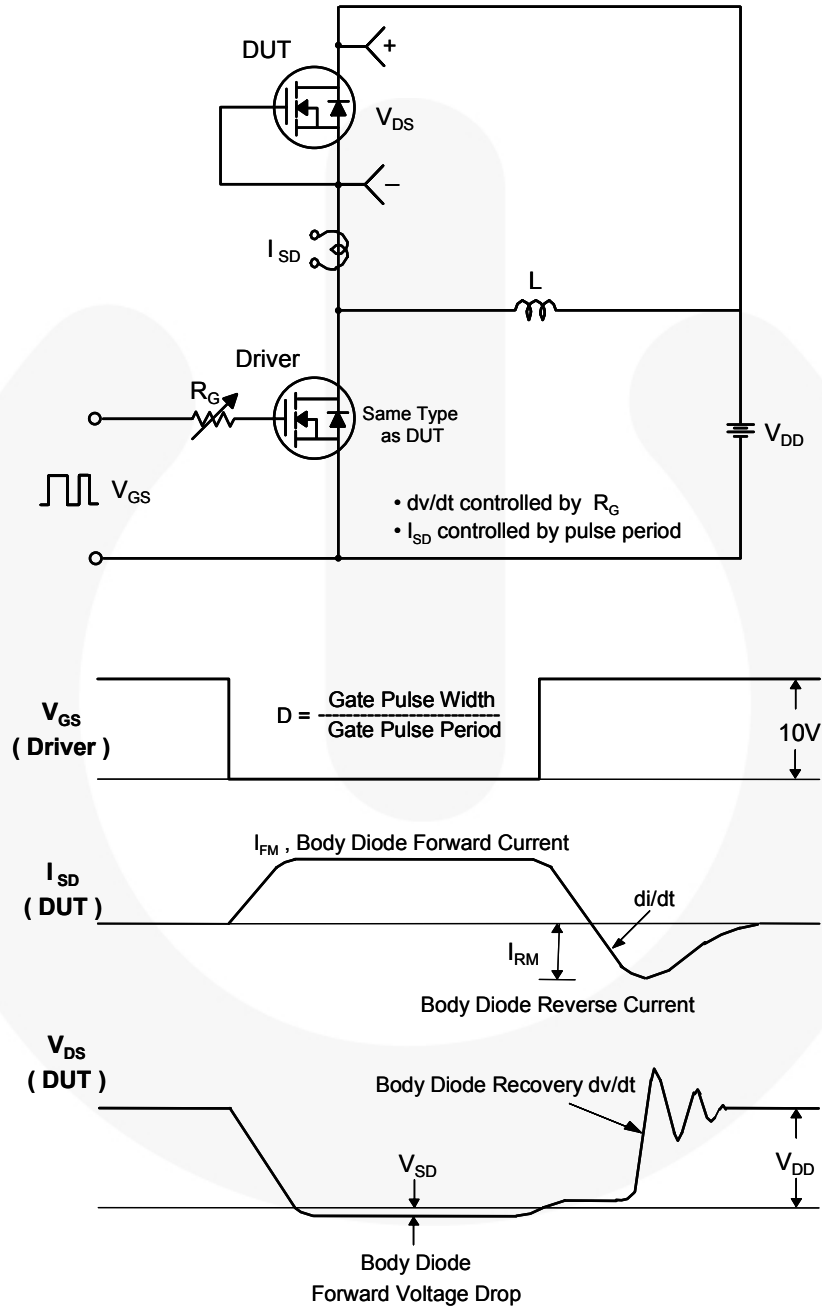
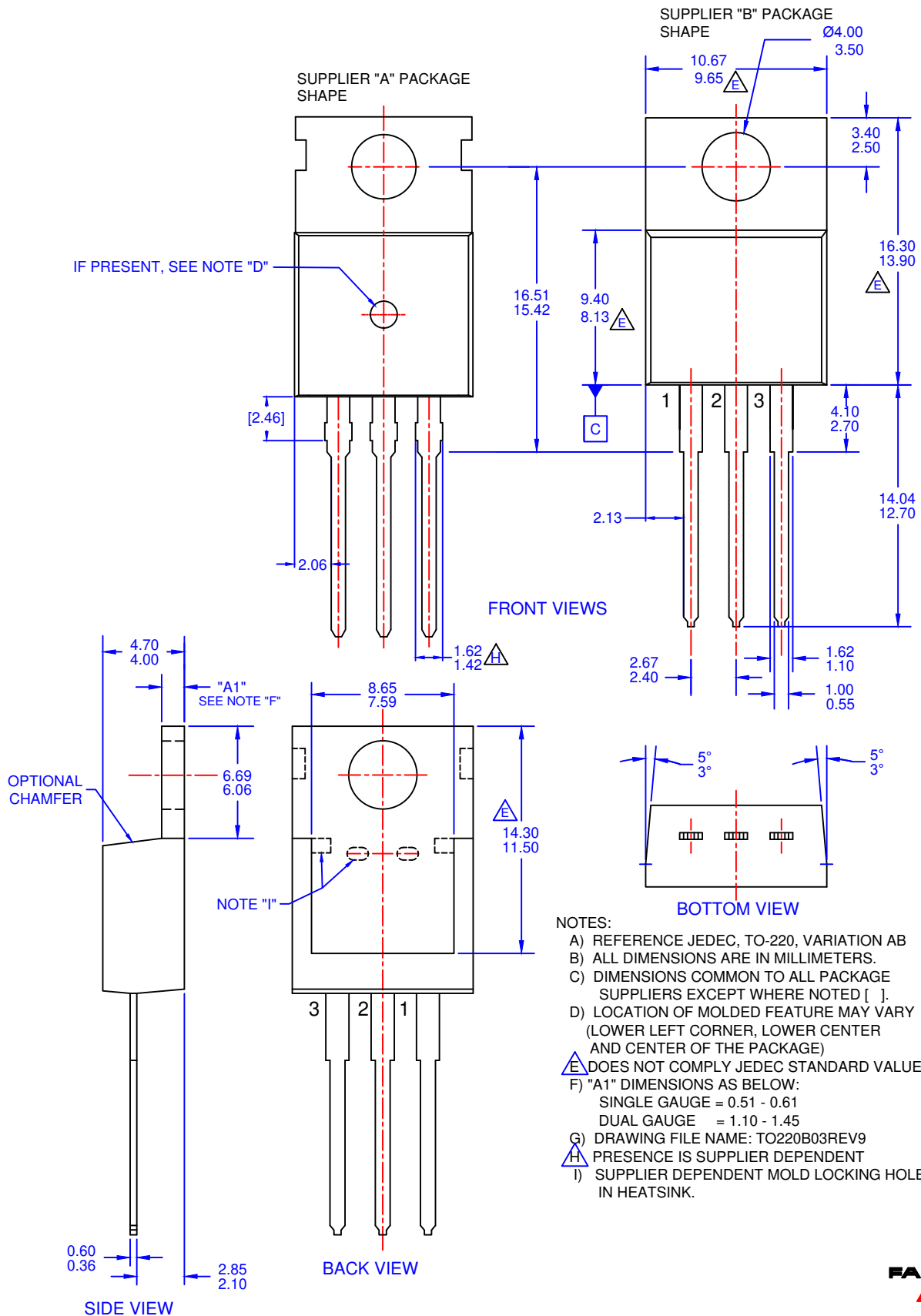
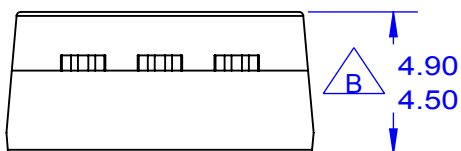
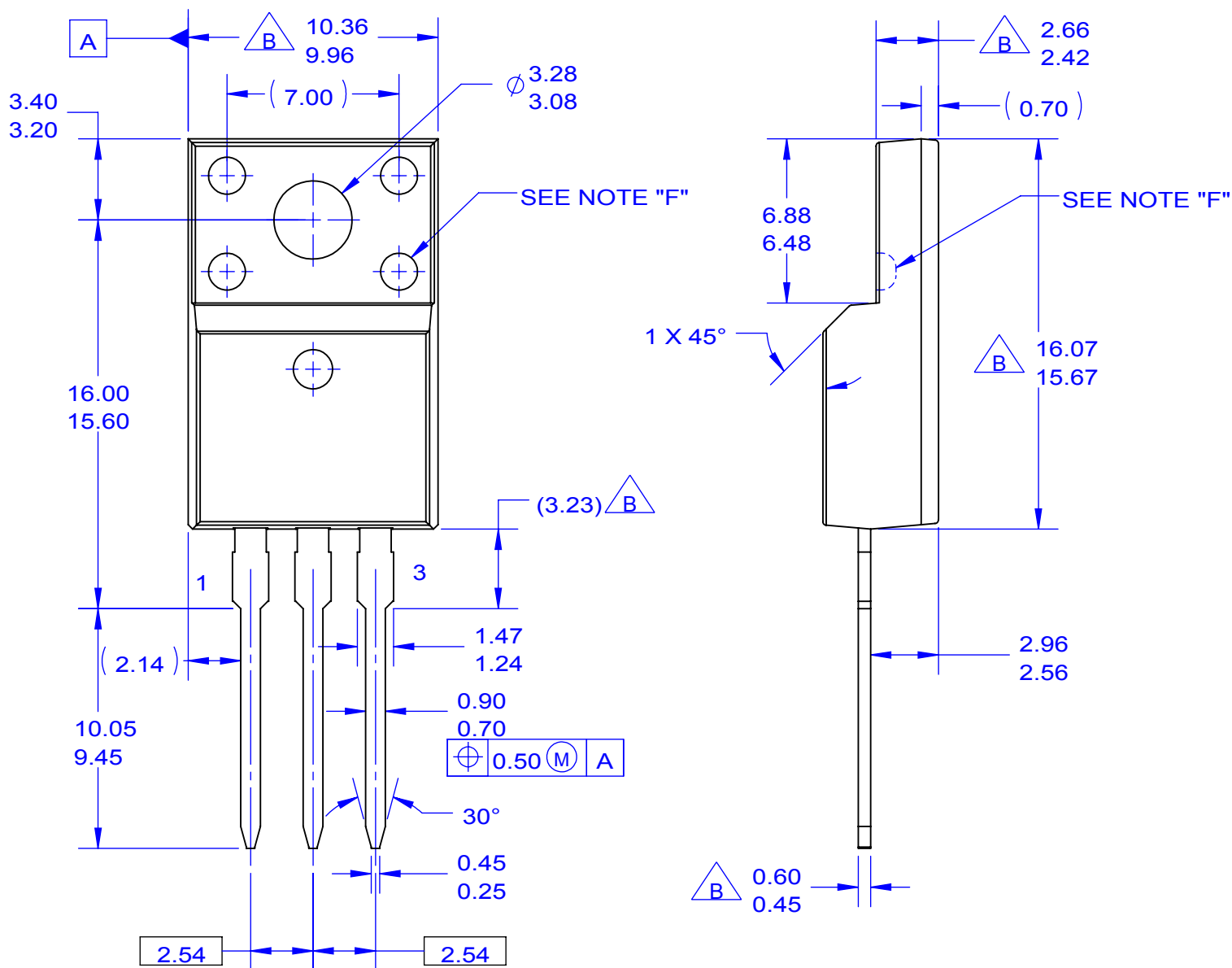


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms









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NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
- B. DOES NOT COMPLY EIAJ STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- F. OPTION 1 - WITH SUPPORT PIN HOLE.  
OPTION 2 - NO SUPPORT PIN HOLE.
- G. DRAWING FILE NAME: TO220M03REV5

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