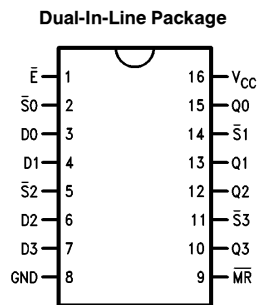


9314/DM9314 Quad Latch

General Description

The '9314 is a multifunctional 4-bit latch designed for general purpose storage applications in high speed digital systems. All outputs have active pull-up circuitry to provide high capacitance drive and to provide low impedance in both logic states for good noise immunity.

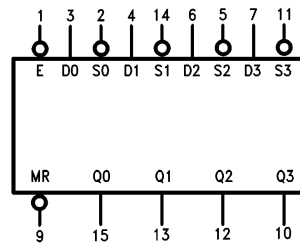
Connection Diagram



TL/F/9788-1

Order Number 9314DMQB, 9314FMQB or DM9314N
See NS Package Number J16A, N16E or W16A

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

TL/F/9788-2

Pin Names	Description
\bar{E}	Enable Input (Active LOW)
D0–D3	Data Inputs
$\bar{S}0$ – $\bar{S}3$	Set Inputs (Active LOW)
\bar{MR}	Master Reset Input (Active LOW)
Q0–Q3	Latch Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.8			0.8	V
I _{OH}	High Level Output Current			−0.8			−0.8	mA
I _{OL}	Low Level Output Current			16			16	mA
T _A	Free Air Operating Temperature	−55		125	0		70	°C
t _s (H)	Setup Time HIGH or LOW	5.0			5.0			ns
t _s (L)	D _n to \bar{E}	18			18			ns
t _h (H)	Hold Time HIGH or LOW	0			0			ns
t _h (L)	D _n to \bar{E}	5.0			5.0			ns
t _s (H)	Setup Time HIGH, D _n to \bar{S}_n	8.0			8.0			ns
t _h (L)	Hold Time LOW, D _n to \bar{S}_n	8.0			8.0			ns
t _w (L)	\bar{E} Pulse Width LOW	18			18			ns
t _w (L)	\overline{MR} Pulse Width LOW	18			18			ns
t _{rec}	Recovery Time, \overline{MR} to \bar{E}	0			0			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = −12 mA			−1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IL} = Max	2.4	3.4		V
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IH} = Min		0.2	0.4	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Min, V _I = 5.5V			1	mA
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.4V			40	μA
		Data Inputs			60	
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V			−1.6	mA
		Data Inputs			−2.7	
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	MIL	−20	−70	mA
			COM	−20	−70	
I _{CC}	Supply Current	V _{CC} = Max			55	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25^\circ C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$C_L = 15\text{ pF}$		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay \bar{E} to Q_n		24	ns
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n		12 24	ns
t_{PLH}	Propagation Delay \overline{MR} to Q_n		18	ns
t_{PHL}	Propagation Delay \bar{S}_n to Q_n		24	ns

Functional Description

The '9314 consists of four latches with a common active LOW Enable input and active LOW Master Reset input. When the Enable goes HIGH, data present in the latches is stored and the state of the latch is no longer affected by the \bar{S}_n and D_n inputs. The Master Reset when activated overrides all other input conditions forcing all latch outputs LOW. Each of the four latches can be operated in one of two modes:

D-TYPE LATCH—For D-type operation the \bar{S} input of a latch is held LOW. While the common Enable is active the latch output follows the D input. Information present at the latch output is stored in the latch when the Enable goes HIGH.

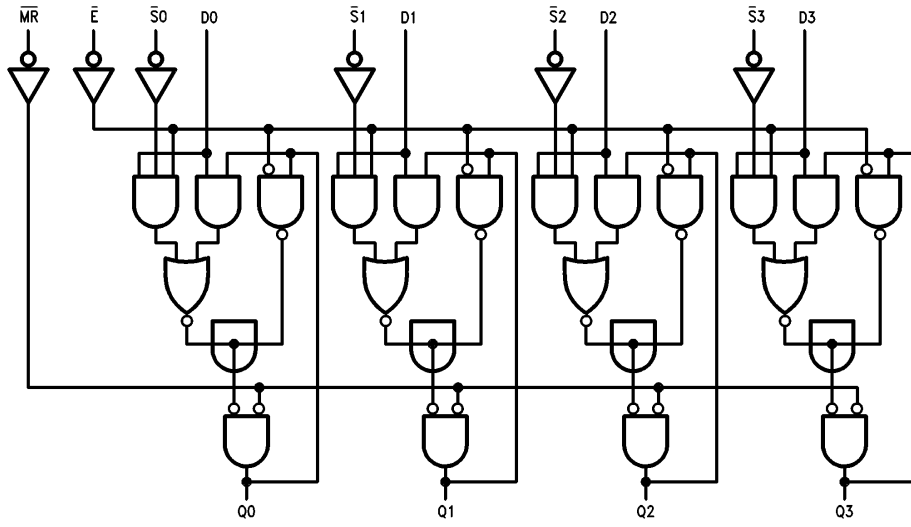
SET/RESET LATCH—During set/reset operation when the common Enable is LOW a latch is reset by a LOW on the D input, and can be set by a LOW on the \bar{S} input if the D input is HIGH. If both \bar{S} and D inputs are LOW, the D input will dominate and the latch will be reset. When the Enable goes HIGH, the latch remains in the last state prior to disablement. The two modes of latch operation are shown in the Truth Table.

Truth Table

\overline{MR}	\bar{E}	D	\bar{S}	Q_n	Operation
H	L	L	L	L	D Mode
H	L	H	L	H	
H	H	X	X	Q_{n-1}	
H	L	L	L	L	R/S Mode
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	Q_{n-1}	
L	X	X	X	Q_{n-1}	Reset

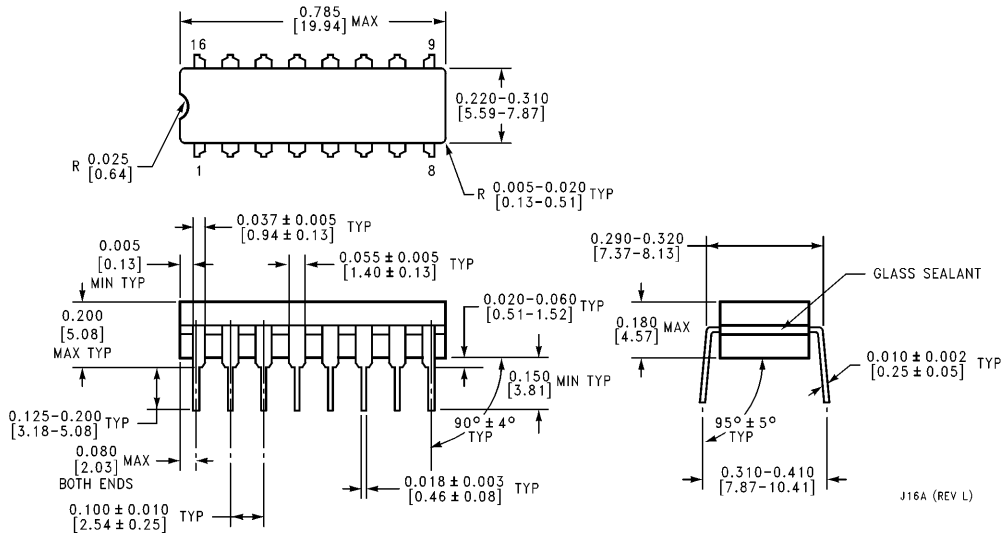
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
 Q_{n-1} = Previous Output State
 Q_n = Present Output State

Logic Diagram

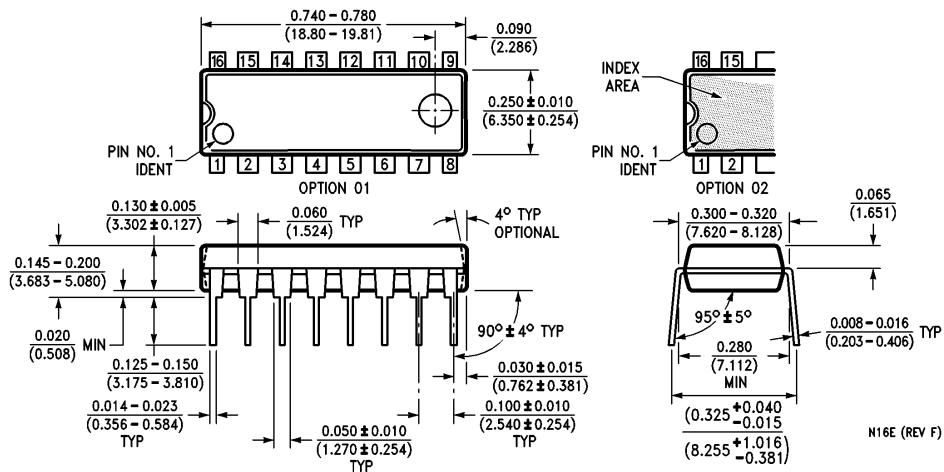


TL/F/9788-3

Physical Dimensions inches (millimeters)

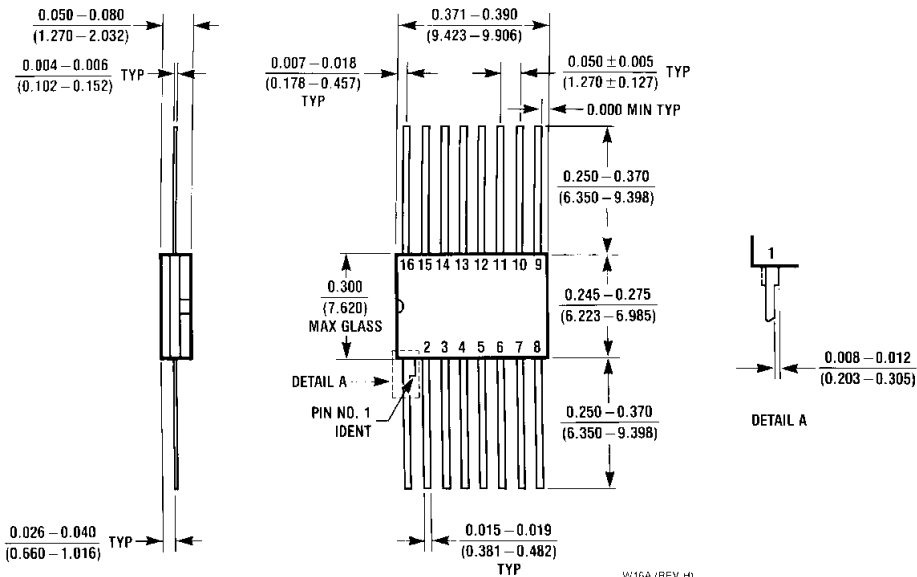


16-Lead Ceramic Dual-In-Line Package (J)
 Order Number 9314DMQB
 NS Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
 Order Number DM9314N
 NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 9314FMQB
NS Package Number W16A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
 1111 West Bardin Road
 Arlington, TX 76017
 Tel: 1(800) 272-9959
 Fax: 1(800) 737-7018

National Semiconductor Europe
 Fax: (+49) 0-180-530 85 86
 Email: cnjwge@tevm2.nsc.com
 Deutsch Tel: (+49) 0-180-530 85 85
 English Tel: (+49) 0-180-532 78 32
 Français Tel: (+49) 0-180-532 93 58
 Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
 19th Floor, Straight Block,
 Ocean Centre, 5 Canton Rd.
 Tsimshatsui, Kowloon
 Hong Kong
 Tel: (852) 2737-1600
 Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
 Tel: 81-043-299-2309
 Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.