Thermoelectric Cooler (TEC) Controller

Data Sheet **ADN8831**

FEATURES

- Two integrated zero drift, rail-to-rail, chop amplifiers
- TEC voltage and current operation monitoring
- Programmable TEC maximum voltage and current
- Programmable TEC current heating and cooling limits
- Configurable PWM switching frequency up to 1 MHz
- Power efficiency: > 90%
- Temperature lock indication
- Optional internal or external clock source
- Clock phase adjustment for multiple drop operation
- Supports negative temperature coefficient (NTC) thermistors or positive temperature coefficient (PTC) resistance thermal detectors (RTDs)
- 5 V typical and optional 3 V supplies
- Standby and shutdown mode availability
- Adjustable soft start feature
- 5 mm × 5 mm 32-lead LFCSP

APPLICATIONS

- Thermoelectric cooler (TEC) temperature control
- DWDM optical transceiver modules
- Optical fiber amplifiers
- Optical networking systems
- Instruments requiring TEC temperature control

GENERAL DESCRIPTION

The ADN8831[1] is a monolithic TEC controller. It has two integrated, zero drift, rail-to-rail comparators, and a PWM driver. A unique PWM driver works with an analog driver to control external selected MOSFETs in an H-bridge. By sensing the thermal detector feedback from the TEC, the ADN8831 can drive a TEC to settle the programmable temperature of a laser diode or a passive component attached to the TEC module.

The ADN8831 supports NTC thermistors or positive temperature coefficient (PTC) RTDs. The target temperature is set as an analog voltage input either from a DAC or from an external resistor divider driven by a reference voltage source.

A proportional integral differential (PID) compensation network helps to quickly and accurately stabilize the ADN8831 thermal control loop. An adjustable PID compensation network example is described in the AN-695 Application Note, *Using the ADN8831 TEC Controller Evaluation Board*. A typical reference voltage of 2.5 V is available from the ADN8831 for thermistor temperature sensing or for TEC voltage/current measuring and limiting in both cooling and heating modes.

FUNCTIONAL BLOCK DIAGRAM

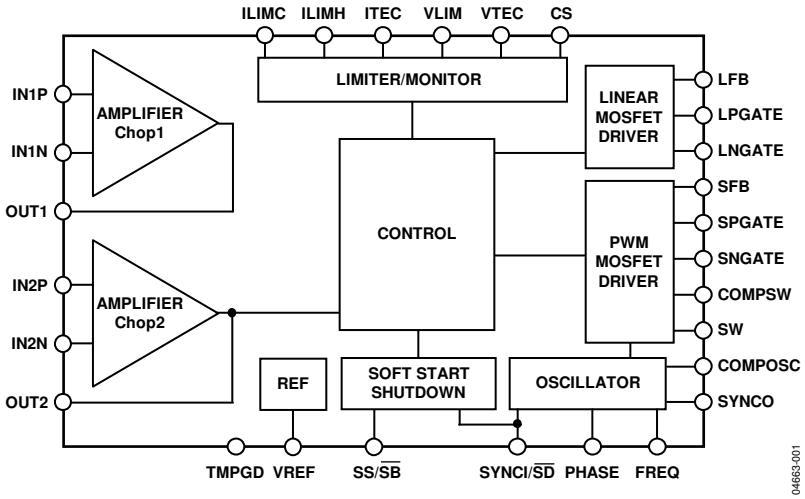

Figure 1.

[1] Product is covered by U.S. Patent No. 6,486,643.

Rev. C
Document Feedback

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DETAILED BLOCK DIAGRAM

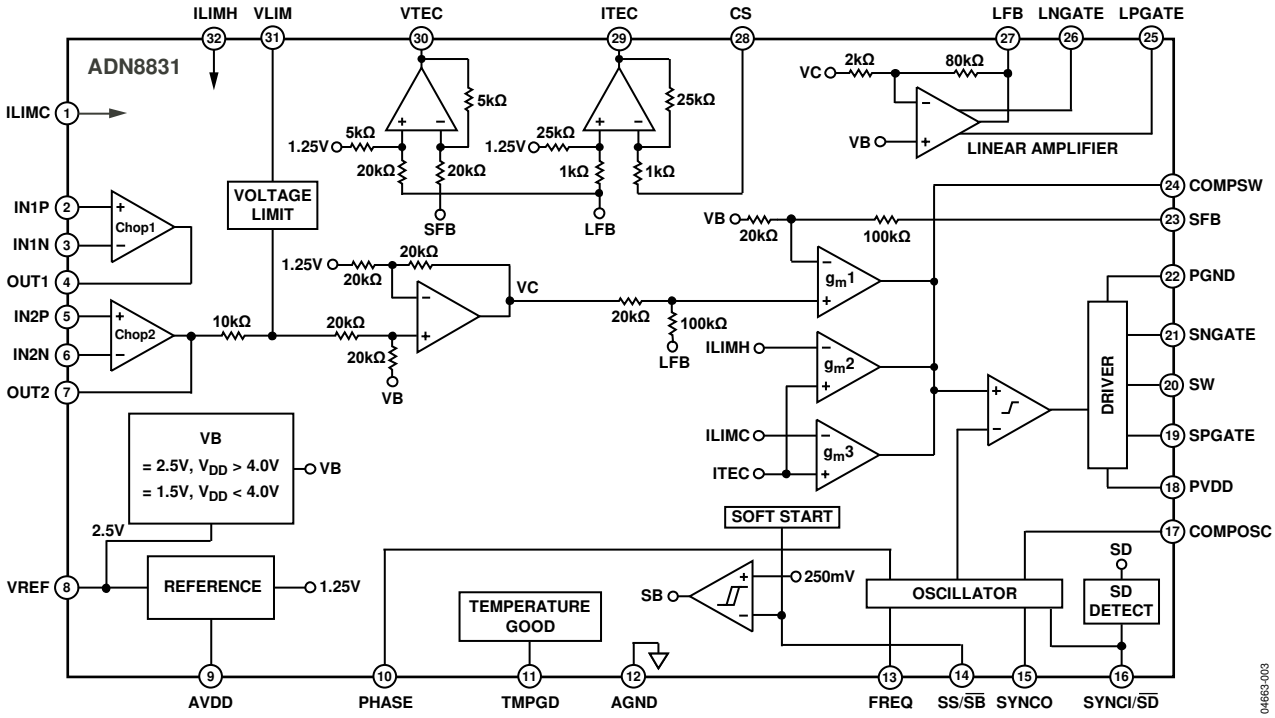


Figure 2. Detailed Block Diagram

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{DD} = 3.0 V to 5.0 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter[1]	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
PWM OUTPUT DRIVER						
Output Transition Time	t_R, t_F	C_L = 3300 pF		20		ns
Nonoverlapping Clock Delay			40	80		ns
Output Resistance	$R_{O (SNGATE, SPGATE)}$	I_L = 10 mA, V_{DD} = 3.0 V		6		Ω
Output Voltage Swing[2]	SFB	V_{LIM} = VREF	0		V_{DD}	V
LINEAR OUTPUT AMPLIFIER						
Output Resistance	$R_{O, LNGATE}$	I_{OUT} = 2 mA, V_{DD} = 3.0 V		200		Ω
	$R_{O, LPGATE}$	I_{OUT} = 2 mA, V_{DD} = 3.0 V		100		Ω
Output Voltage Swing[2]	LFB		0		V_{DD}	V
POWER SUPPLY						
Power Supply Voltage	V_{DD}		3.0		5.5	V
Supply Current	I_{SY}	PWM not switching		8	12	mA
		−40°C ≤ T_A ≤ +85°C			15	mA
Shutdown Current	I_{SD}	SYNCI/$\overline{SD}$ = 0 V		8		µA
Soft Start Charging Current	I_{SS}	V_{SS} = 0 V		8		µA
Undervoltage Lockout[3]	UVLO	Low to high threshold		2.2	2.6	V
Standby Current	I_{SB}	SYNCI/$\overline{SD}$ = V_{DD}, SS/$\overline{SB}$ = 0 V		2		mA
Standby Threshold	V_{SB}	SYNCI/$\overline{SD}$ = V_{DD}		150	200	mV
ERROR/COMPENSATION AMPLIFIERS						
Input Offset Voltage	V_{OS1}	V_{CM1} = 1.5 V, V_{IN1P} − V_{IN1M}		10	100	µV
	V_{OS2}	V_{CM2} = 1.5 V, V_{IN2P} − V_{IN2M}		10	100	µV
Input Voltage Range	V_{CM1}, V_{CM2}		0		V_{DD}	V
Common-Mode Rejection Ratio	$CMRR_1$, $CMRR_2$	V_{CM1}, V_{CM2} = 0.2 V to V_{DD} − 0.2 V		120		dB
Output Voltage High	V_{OH1}, V_{OH2}		V_{DD} − 0.03			V
Output Voltage Low	V_{OL1}, V_{OL2}				25	mV
Power Supply Rejection Ratio	$PSRR_1$, $PSRR_2$	3.0 V ≤ V_{DD} ≤ 5.0 V		110		dB
Output Current	I_{OUT1}, I_{OUT2}	Sourcing and sinking	5			mA
Gain Bandwidth Product	GBW_1, GBW_2	V_{OUT} = 0.5 V to (V_{DD} − 1 V)		2		MHz
OSCILLATOR						
Sync Range	f_{CLK}	SYNCI/$\overline{SD}$ connected to external clock	300		1000	kHz
Oscillator Frequency	f_{CLK}	COMPOSC = V_{DD}, R_{FREQ} = 118 kΩ, SYNCI/$\overline{SD}$ = V_{DD}, V_{DD} = 5.0 V	800	1000	1250	kHz
Nominal Free-Run Oscillation Frequency	$f_{CLK-NOMINAL}$	COMPOSC = V_{DD}, SYNCI/$\overline{SD}$ = V_{DD}	200		1000	kHz
Phase Adjustment Range[2]	Φ_{CLK}	V_{PHASE} = 0.13 V, $f_{SYNCI/\overline{SD}}$ = 1 MHz			50	Degrees
		V_{PHASE} = 2.3 V, $f_{SYNCI/\overline{SD}}$ = 1 MHz	330			Degrees
Phase Adjustment Default	Φ_{CLK}	PHASE = open		180		Degrees
REFERENCE VOLTAGE						
Reference Voltage	V_{REF}	I_{REF} = 2 mA		2.35		V
		I_{REF} = 0 mA	2.37	2.47	2.57	V

Parameter[1]	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC Controls						
Logic Low Output Voltage	V_{OL}	TMPGD, SYNCO, I_{OUT} = 0 A			0.2	V
Logic High Output Voltage	V_{OH}	TMPGD, SYNCO, I_{OUT} = 0 A	V_{DD} − 0.2			V
Logic Low Input Voltage	V_{IL}				0.2	V
Logic High Input Voltage	V_{IH}		3			V
Output High Impedance		V_{DD} = 5.0 V		35		Ω
Output Low Impedance		V_{DD} = 5.0 V		20		Ω
Output High Impedance		V_{DD} = 3.0 V		50		Ω
Output Low Impedance		V_{DD} = 3.0 V		25		Ω
TEC CURRENT MEASUREMENT						
ITEC Gain	$A_{V, ITEC}$	$(V_{ITEC} – V_{REF}/2) / (V_{LFB} – V_{CS})$		25		V/V
ITEC Output Range High	$V_{ITEC, HIGH}$	No load	V_{DD} − 0.05			V
ITEC Output Range Low	$V_{ITEC, LOW}$				0.05	V
ITEC Input Range[2]	V_{CS}, V_{LFB}		0		V_{DD}	V
ITEC Bias Voltage	$V_{ITEC, B}$	$V_{LFB} = V_{CS}$ = 0	1.10	1.20	1.30	V
Maximum ITEC Driving Current	$I_{OUT, TEC}$			±1.5		mA
TEC VOLTAGE MEASUREMENT						
VTEC Gain	$A_{V, VTEC}$	$(V_{VTEC} – V_{REF}/2)/(V_{LFB} – V_{SFB})$	0.23	0.25	0.28	V/V
VTEC Output Range[2]	V_{VTEC}	V_{DD} = 5.0 V	0.05		2.5	V
VTEC Bias Voltage[2]	$V_{VTEC, B}$	$V_{LFB} = V_{SFB}$ = 0 V	1.20	1.25	1.35	V
VTEC Output Load Resistance	R_{VTEC}	I_{VTEC} = 300 µA		35		Ω
VOLTAGE LIMIT						
VLIM Gain	$A_{V, LIM}$	$(V_{LFB} – V_{SFB})/V_{VLIM}$		5		V/V
VLIM Input Range[2]	V_{VLIM}		0		V_{DD}	V
VLIM Input Current, Cooling	$I_{VLIM, COOL}$	$V_{OUT2} < V_{REF}/2$			100	nA
VLIM Input Current, Heating	$I_{VLIM, HEAT}$	$V_{OUT2} > V_{REF}/2$		I_{FREQ}		mA
VLIM Input Current Accuracy, Heating	$I_{VLIM, HEAT}$	I_{VLIM}/I_{FREQ}	0.8	1.0	1.18	A/A
CURRENT LIMIT						
ILIMC Input Voltage Range	V_{ILIMC}		$V_{REF}/2$		V_{DD} − 1	V
ILIMH Input Voltage Range	V_{ILIMH}		0.1		$V_{REF}/2$	V
ILIMC Limit Threshold	$V_{TH, ILIMC}$	V_{ITEC} = 2.0 V, R_S = 20 mΩ	1.98	2.0	2.02	V
ILIMH Limit Threshold	$V_{TH, ILIMH}$	V_{ITEC} = 0.5 V	0.48	0.5	0.52	V
TEMPERATURE GOOD						
High Threshold	$V_{OUT1, TH1}$	IN2M tied to OUT2, V_{IN2P} = 1.5 V		1.55	1.60	V
Low Threshold	$V_{OUT1, TH2}$	IN2M tied to OUT2, V_{IN2P} = 1.5 V	1.40	1.45		V

[1] Logic inputs meet typical CMOS I/O conditions for source/sink current (~1 µA).
[2] Guaranteed by design or indirect test methods.
[3] The ADN8831 does not work when the supply voltage is less than UVLO.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings at 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to V_S + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	125°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-lead LFCSP (ACPZ)	33.4	1.02	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

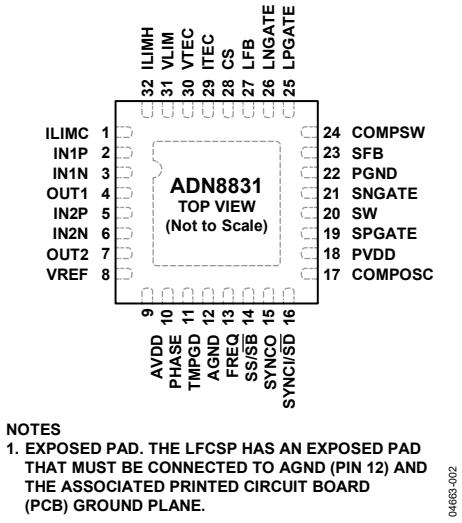


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	ILIMC	Analog Input	Sets TEC Cooling Current Limit.
2	IN1P	Analog Input	Noninverting Input to Error Amplifier.
3	IN1N	Analog Input	Inverting Input to Error Amplifier.
4	OUT1	Analog Output	Output of Error Amplifier.
5	IN2P	Analog Input	Noninverting Input to Compensation Amplifier.
6	IN2N	Analog Input	Inverting Input to Compensation Amplifier.
7	OUT2	Analog Output	Output of Compensation Amplifier.
8	VREF	Analog Output	2.5 V Voltage Reference Output.
9	AVDD	Power	Power for Nondriver Sections. 3.0 V minimum; 5.5 V maximum.
10	PHASE	Analog Input	Sets SYNCO Clock Phase Relative to SYNCI/$\overline{SD}$ Clock.
11	TMPGD	Digital Output	Logic Output. Active high. Indicates when the OUT1 voltage is within ±100 mV of IN2P voltage.
12	AGND	Ground	Analog Ground. Connect to low noise ground.
13	FREQ	Analog Input	Sets Switching Frequency with an External Resistor.
14	SS/$\overline{SB}$	Analog Input	Sets Soft Start Time for Output Voltage. Pull low (VTEC = 0 V) to put the ADN8831 into standby mode.
15	SYNCO	Digital Output	Phase Adjustment Clock Output. Phase set from PHASE pin. Used to drive SYNCI/$\overline{SD}$ of other ADN8831 devices.
16	SYNCI/$\overline{SD}$	Digital Input	Optional Clock Input. If not connected, clock frequency is set by FREQ pin. Pull low to put the ADN8831 into shutdown mode. Pull high to negate shutdown mode.
17	COMPOSC	Analog Output	Compensation for Oscillator. Connect to PVDD when in free-run mode, connect to R-C network when in external clock mode.
18	PVDD	Power	Power for Output Driver Sections. 3.0 V minimum; 5.5 V maximum.
19	SPGATE	Analog Output	PWM Output Drives External PMOS Gate.
20	SW	Analog Input	Connects to PWM FET Drains.
21	SNGATE	Analog Output	PWM Output Drives External NMOS Gate.
22	PGND	Ground	Power Ground. External NMOS devices connect to PGND. Connect to digital ground.
23	SFB	Analog Input	PWM Feedback. Connect to the TEC module negative (–) terminal.
24	COMPSW	Analog Input	Compensation Pin for Switching Amplifier.
25	LPGATE	Analog Output	Linear Output Drives External PMOS Gate.
26	LNGATE	Analog Output	Linear Output Drives External NMOS Gate.
27	LFB	Analog Input	Linear Feedback. Connect to H-Bridge transistor output and current sense resistor.
28	CS	Analog Input	Linear Feedback. Connect to the TEC module positive (+) terminal.
29	ITEC	Analog Output	Indicates TEC Current.
30	VTEC	Analog Output	Indicates TEC Voltage.

Pin No.	Mnemonic	Type	Description
31	VLIM	Analog Input	Sets Maximum Voltage Across TEC Module.
32	ILIMH	Analog Input	Sets TEC Heating Current Limit.
	EP	Metal paddle at the back of package	Exposed Pad. The LFCSP has an exposed pad that must be connected to AGND (Pin 12) and the associated PCB ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

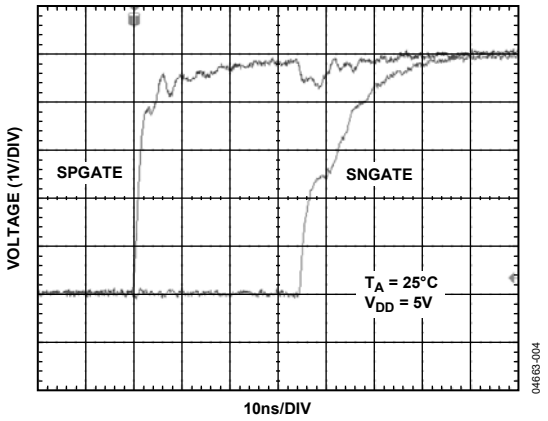


Figure 4. SPGATE and SNGATE Rise Time Using Circuit Shown Figure 12

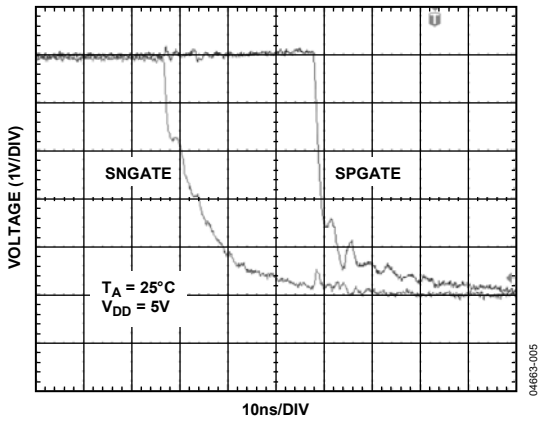


Figure 5. SNGATE and SPGATE Fall Time Using Circuit Shown in Figure 12

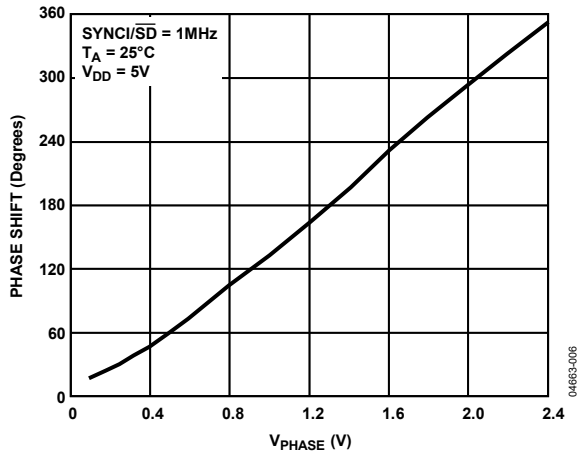


Figure 6. Clock Phase Shift vs. Phase Voltage

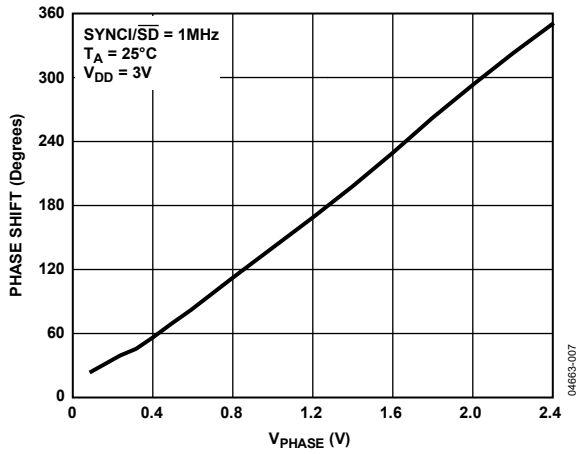


Figure 7. Clock Phase Shift vs. Phase Voltage

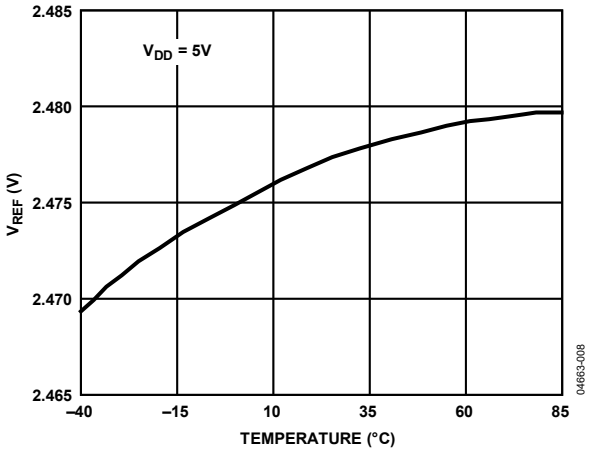


Figure 8. V_{REF} vs. Temperature

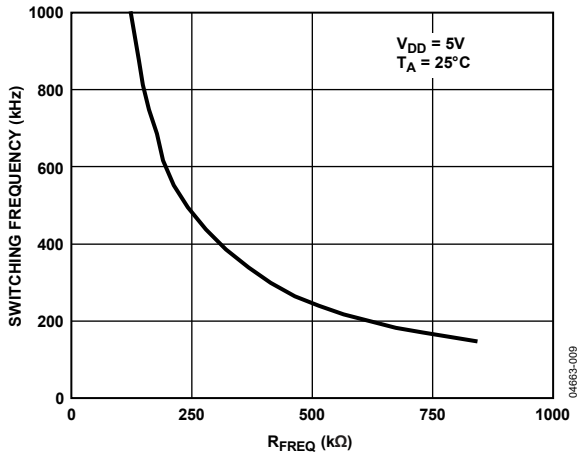


Figure 9. Switching Frequency vs. R_{FREQ}

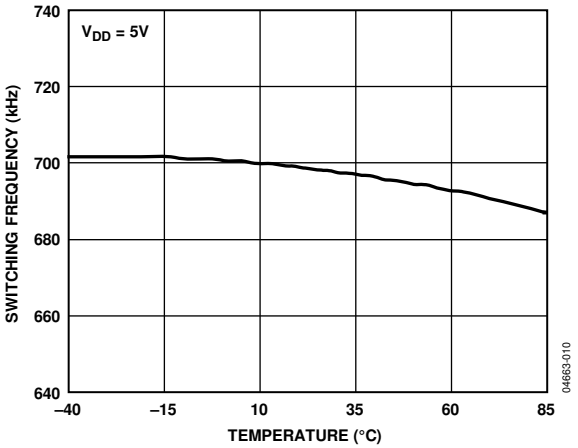


Figure 10. Switching Frequency vs. Temperature

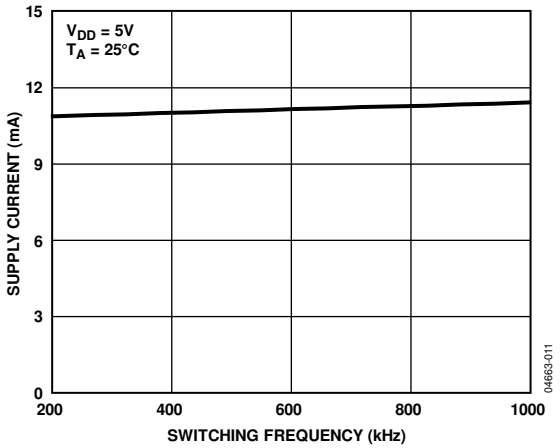


Figure 11. Supply Current vs. Switching Frequency

THEORY OF OPERATION

The ADN8831 is a single chip TEC controller that sets and stabilizes a TEC temperature. A voltage applied to the input of the ADN8831 corresponds to a target TEC temperature setpoint (TEMPSET). By controlling an external FET H-bridge, the appropriate current is then applied to the TEC to pump heat either to or away from an object attached to the TEC. The objective temperature is measured with a thermal sensor attached to the TEC and the sensed temperature (voltage) is fed back to the ADN8831 to complete a closed thermal control loop of the TEC. For best stability, the thermal sensor is to be closed to the object. In most laser diode modules, a TEC and a NTC thermistor are already mounted in the same package to regulate the laser diode temperature.

The ADN8831 integrates two self-correcting, auto-zero amplifiers (Chop1 and Chop2). The Chop1 amplifier usually takes a thermal sensor input and converts or regulates the input to a linear voltage output. The OUT1 (Pin 4) voltage is proportional to the object temperature. The OUT1 (Pin 4) voltage is fed into the compensation amplifier (Chop2) and compared with a temperature setpoint voltage, creating an error voltage that is proportional to the difference. When using the Chop2 amplifier, a PID network is recommended, as shown in Figure 12.

Adjusting the PID network optimizes the step response of the TEC control loop. A compromised settling time and the maximum current ringing become available when this is done. Details of how to adjust the compensation network are in the PID Compensation Amplifier (CHOP2) section. The TEC is differentially driven in an H-bridge configuration. The ADN8831 drives external MOSFET transistors to provide the TEC current. To further improve the power efficiency of the system, one side of the H-bridge uses a PWM driver. Only one inductor and one capacitor are required to filter out the switching frequency. The other side of the H-bridge uses linear output without requiring any additional circuitry. This proprietary configuration allows the ADN8831 to provide efficiency of >90%. For most applications, a 4.7 µH inductor, a 22 µF capacitor, and a switching frequency of 1 MHz, maintain less than 0.5% worst-case output voltage ripple across a TEC.

The maximum voltage across the TEC and current flowing through the TEC is to be set using the VLIM (Pin 31) and ILIMC (Pin 1)/ILIMH (Pin 32). Additional details are in the Maximum TEC Voltage Limit section and the Maximum TEC Current Limit section.

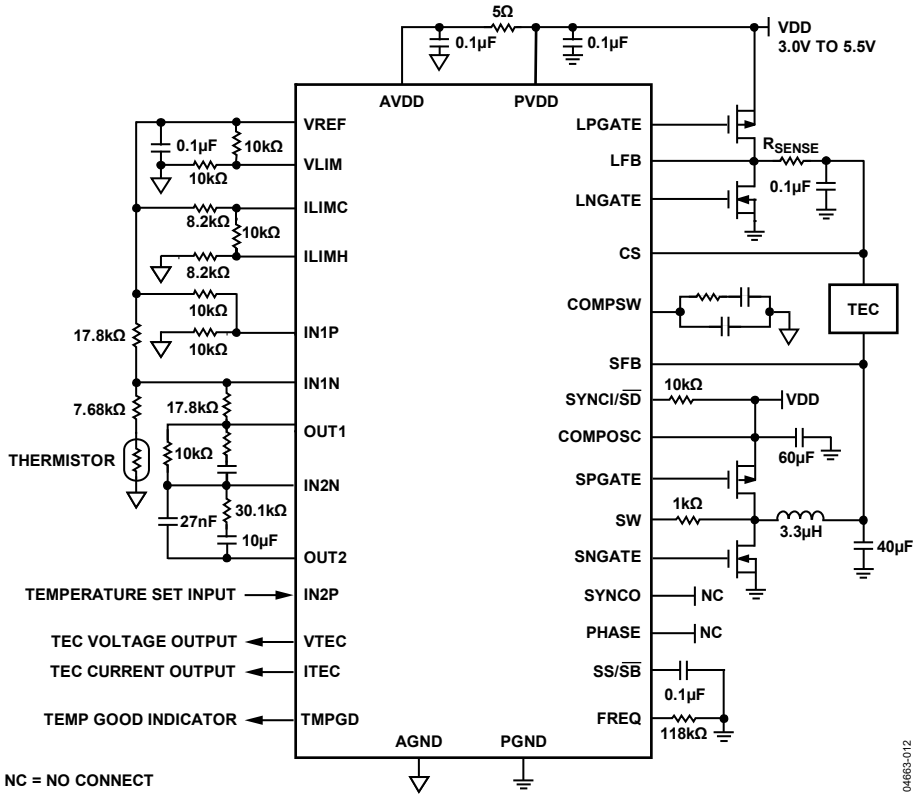


Figure 12. Typical Application Circuit 1

OSCILLATOR CLOCK FREQUENCY

The ADN8831 has an internal oscillator to generate the switching frequency for the output stage. This oscillator can be set in either free-run mode or synchronized to an external clock signal.

Free-Run Operation

The switching frequency is set by a single resistor connected from FREQ (Pin 13) to ground. Table 5 shows R_{FREQ} for some common switching frequencies. For free-run operation, connect SYNCI/$\overline{SD}$ (Pin 16) and COMPOSC (Pin 17) to PVDD (Pin 18).

Table 5. Switching Frequencies vs. R_{FREQ}

f_{SWITCH}	R_{FREQ}
250 kHz	484 kΩ
500 kHz	249 kΩ
750 kHz	168 kΩ
1 MHz	118 kΩ

Higher switching frequencies reduce the voltage ripple across the TEC. However, high switching frequencies create more power dissipation in the external transistors due to the more frequent charging and discharging of the transistor gate capacitances.

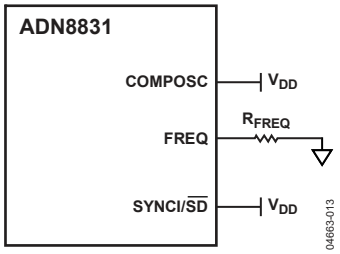


Figure 13. Free-Run Mode

External Clock Operation

The switching frequency of the ADN8831 can be synchronized with an external clock. Connect the clock signal to SYNCI/$\overline{SD}$ (Pin 16) and connect COMPOSC (Pin 17) to an R-C network. This network compensates a PLL to lock on to the external clock.

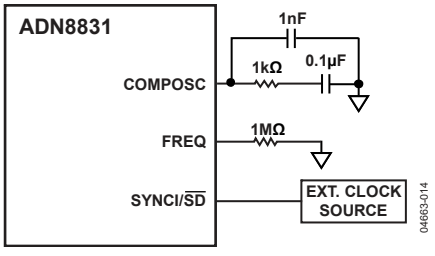


Figure 14. Synchronize to an External Clock

Connecting Multiple ADN8831 Devices

Connecting SYNCO (Pin 15) to the SYNCI/$\overline{SD}$ pin of another ADN8831 allows for multiple ADN8831 devices to work together using a single clock. Multiple ADN8831 devices can be driven from a single master ADN8831 device, by connecting the SYNCO pin of the master device to each slave SYNCI/$\overline{SD}$ pin, or by daisy-chaining by connecting the SYNCO pin of each device to the SYNCI/$\overline{SD}$ pin of the next device. When multiple ADN8831 devices are clocked at the same frequency, the phase is to be adjusted to reduce power supply ripple.

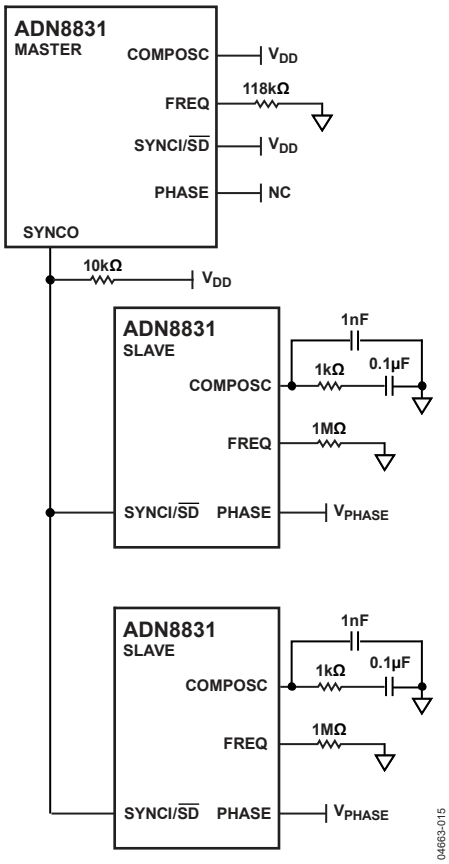


Figure 15. Multiple ADN8831 Devices Driven from a Master Clock

OSCILLATOR CLOCK PHASE

Adjust the oscillator clock phase using a simple resistor divider at PHASE (Pin 10). Phase adjustment allows two or more ADN8831 devices to operate from the same clock frequency and not have all outputs switched simultaneously. This avoids the potential of an excessive power supply ripple.

To ensure the correct operation of the oscillator, V_{PHASE} is to remain in the range of 100 mV to 2.4 V. PHASE (Pin 10) is internally biased at 1.2 V. If PHASE (Pin 10) remains open, the clock phase is set at 180° as the default.

TEMPERATURE LOCK INDICATOR

The TMPGD (Pin 11) outputs a logic high when the OUT1 (Pin 4) voltage reaches the IN2P (Pin 5) temperature setpoint (TEMPSET) voltage. The TMPGD has a detection range of ±25 mV and a 10 mV typical hysteresis. This allows direct interfacing either to the microcontrollers or to the supervisory circuitry.

SOFT START ON POWER-UP

The ADN8831 can be programmed to ramp up for a specified time after the power supply is turned on or after the $\overline{SD}$ pin is deasserted. This feature, called soft start, is useful for gradually increasing the duty cycle of the PWM amplifier. The soft start time is set with a single capacitor connected from SS (Pin 14) to ground. The capacitor value is calculated by the following equation:

$$\tau_{SS} = 150 \times C_{SS}$$

where:
C_{SS} is the value of the capacitor in microfarads.
τ_{SS} is the soft start time in milliseconds.

To set a soft start time of 15 ms, C_{SS} is to equal 0.1 µF.

SHUTDOWN MODE

The shutdown mode sets the ADN8831 into an ultralow current state. The current draw in shutdown mode is typically 8 µA. The shutdown input, $\overline{SD}$ (Pin 16), is active low. To shut down the device, drive $\overline{SD}$ to logic low. Once a logic high is applied, the ADN8331 is reactivated after the time delay set by the soft start circuitry. Refer to the Soft Start on Power-Up section for more details.

STANDBY MODE

The ADN8831 has a standby mode that deactivates a MOSFET driver stage. The current draw for the ADN8831 in standby mode is less than 2 mA. The standby input SS/$\overline{SB}$ (Pin 14) is active low. After applying a logic high, the ADN8331 reactivates following the delay. In standby mode, only SYNCO (Pin 15) has a clock output. All the other function blocks are powered off.

TEC VOLTAGE/CURRENT MONITOR

The TEC real time voltage and current are detectable at VTEC (Pin 30) and ITEC (Pin 29), respectively.

Voltage Monitor

VTEC (Pin 30) is an analog voltage output pin with a voltage proportional to the actual voltage across the TEC. A center VTEC voltage of 1.25 V corresponds to 0 V across a TEC. The output voltage is calculated using the following equation:

$$V_{VTEC} = 1.25\ \text{V} + 0.25 \times (V_{LFB} - V_{SFB})$$

Current Monitor

ITEC (Pin 29) is an analog voltage output pin with a voltage proportional to the actual current through the TEC. A center ITEC voltage of 1.25 V corresponds to 0 A through the TEC. The output voltage is calculated using the following equation:

$$V_{ITEC} = 1.25\ \text{V} + 25 \times (V_{LFB} - V_{CS})$$

The equivalent TEC current is calculated using the following equation:

$$I_{TEC} = \frac{V_{ITEC} - 1.25\ \text{V}}{25 \times R_{SENSE}}$$

MAXIMUM TEC VOLTAGE LIMIT

The maximum TEC voltage is set by applying a voltage at VLIM (Pin 31) to protect the TEC. This voltage can be set with a resistor divider or a DAC. The voltage limiter operates in bidirectional TEC voltage, and cooling and heating voltage.

Using a DAC

Both the cooling and heating voltage limits are set at the same levels when a voltage source directly drives VLIM (Pin 31). The maximum TEC voltage is calculated using the following equation:

$$V_{TEC(MAX)} = 5 \times V_{VLIM}$$

where:
$V_{TEC\ (MAX)}$ is the maximum TEC voltage.
V_{VLIM} is the voltage applied at VLIM (Pin 31).

Using a Resistor Divider

Separate voltage limits are set using a resistor divider. The internal current sink circuitry connected to VLIM (Pin 31) draws a current when the ADN8831 drives the TEC in a heating direction, which lowers the voltage at VLIM (Pin 31). The current sink is not active when the TEC is driven in a cooling direction; therefore, the TEC heating voltage limit is always lower than the cooling voltage limit.

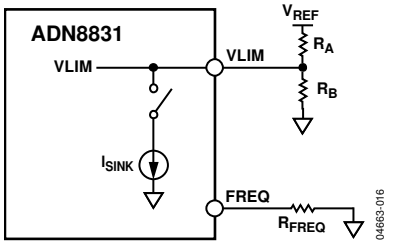


Figure 16. Using a Resistor Divider

The sink current is set by the resistor connected from FREQ (Pin 13) to ground. The sink current is calculated using the following equation:

$$I_{SINK} = \frac{1.25\ \text{V}}{R_{FREQ}}$$

where:
I_{SINC} is the sink current at VLIM (Pin 31).
R_{FREQ} is the resistor connected at FREQ (Pin 13).

The cooling and heating limits are calculated using the following equations:

$$V_{VLIM,COOL} = \frac{V_{REF} \times R_B}{R_A + R_B}$$

$$V_{VLIM,HEAT} = V_{VLIM,COOL} - I_{SINK} \times R_A \| R_B$$

MAXIMUM TEC CURRENT LIMIT

To protect the TEC, separate maximum TEC current limits in cooling and heating directions are set by applying a voltage at ILIMC (Pin 1) and ILIMH (Pin 32). Maximum TEC currents are calculated using the following equations:

$$I_{TEC,MAX,COOL} = \frac{V_{ILIMC} - 1.25\ \text{V}}{25 \times R_{SENSE}}$$

$$I_{TEC,MAX,HEAT} = \frac{1.25\ \text{V} - V_{ILIMH}}{25 \times R_{SENSE}}$$

APPLICATIONS INFORMATION

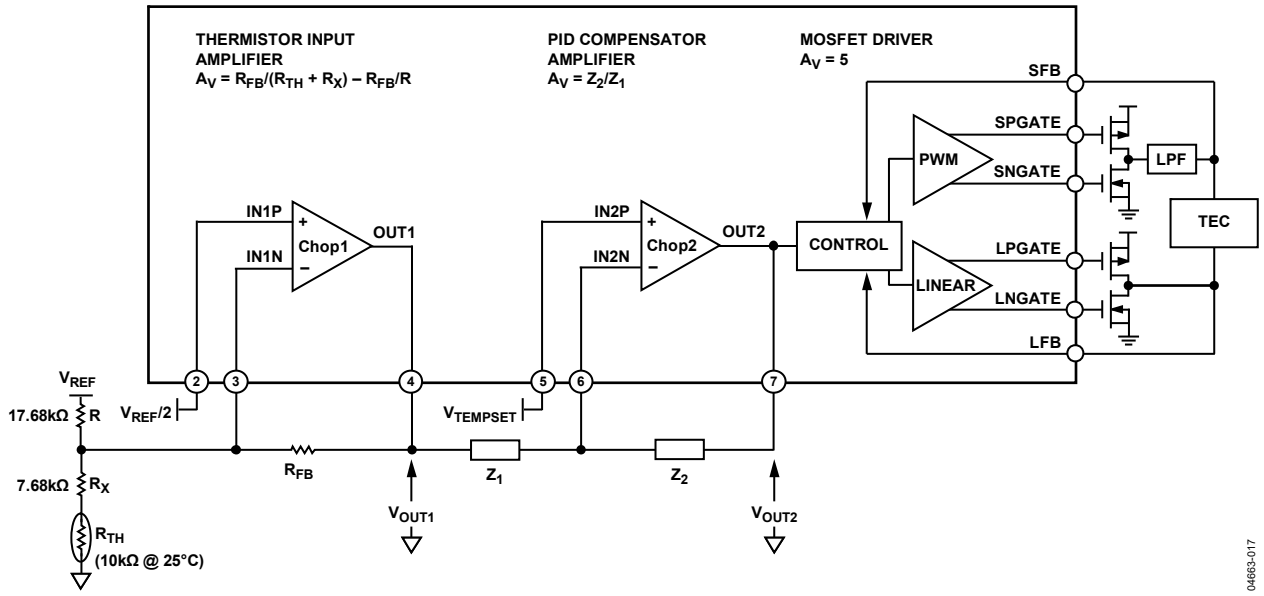


Figure 17. Signal Flow Block Diagram

SIGNAL FLOW

The ADN8831 integrates two auto-zero amplifiers defined as the Chop1 amplifier and the Chop2 amplifier. Both of the amplifiers can be used as standalone amplifiers, therefore, the implementation of temperature control can vary. Figure 17 shows the signal flow through the ADN8831, and a typical implementation of the temperature control loop using the Chop1 amplifier and the Chop2 amplifier.

In Figure 17, the Chop1 amplifier and the Chop2 amplifier are configured as the thermistor input amplifier and the PID compensation amplifier, respectively. The thermistor input amplifier gains the thermistor voltage then outputs to the PID compensation amplifier. The PID compensation amplifier then compensates a loop response over the frequency domain.

The output from the compensation loop at OUT2 is fed to the linear MOSFET gate driver. The voltage at LFB is fed with OUT2 into the PWM MOSFET gate driver. Including the external transistors, the gain of the differential output section is fixed at 5. For details on the output drivers, see the MOSFET Driver Amplifier section.

THERMISTOR SETUP

The thermistor has a nonlinear relationship to temperature; near optimal linearity over a specified temperature range can be achieved with the proper value of R_X placed in series with the thermistor. First, the resistance of the thermistor must be known, where

$$R_{LOW} = R_{TH} @ T_{LOW}$$
$$R_{MID} = R_{TH} @ T_{MID}$$
$$R_{HIGH} = R_{TH} @ T_{HIGH}$$

T_{LOW} and T_{HIGH} are the endpoints of the temperature range and T_{MID} is the average. In some cases, with only B constant available , R_{TH} is calculated using the following equation:

$$R_{TH} = R_R \exp\left\{B\left(\frac{1}{T} - \frac{1}{T_R}\right)\right\}$$

where:
R_{TH} is a resistance at T[K].
R_R is a resistance at T_R[K].

R_X is calculated using the following equation:

$$R_X = \left(\frac{R_{LOW}R_{MID} + R_{MID}R_{HIGH} - 2R_{LOW}R_{HIGH}}{R_{LOW} + R_{HIGH} - 2R_{MID}}\right)$$

THERMISTOR AMPLIFIER (Chop1)

The Chop1 amplifier can be used as a thermistor input amplifier. In Figure 17, the output voltage is a function of the thermistor temperature. The voltage at OUT1 is expressed as

$$V_{OUT1} = \left(\frac{R_{FB}}{R_{TH} + R_X} - \frac{R_{FB}}{R} + 1\right) \times \frac{V_{REF}}{2}$$

where:
R_{TH} is a thermistor.
R_X is a compensation resistor.

R is calculated using the following equation:

$$R = R_X + R_{TH@25°C}$$

V_{OUT1} is centered around $V_{REF}/2$ at 25°C. With the typical values shown in Figure 17, an average temperature-to-voltage coefficient is −25 mV/°C at a range of +5°C to +45°C.

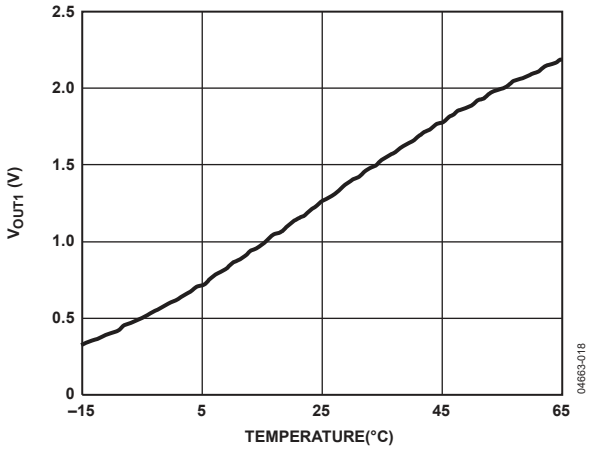


Figure 18. V_{OUT1} vs. Temperature

PID COMPENSATION AMPLIFIER (Chop2)

Use the Chop2 amplifier as the PID compensation amplifier. The voltage at OUT1 feeds into the PID compensation amplifier. The frequency response of the PID compensation amplifier is dictated by the compensation network. Apply the temperature set voltage at IN2P. In Figure 17, the voltage at OUT2 is calculated using the following equation:

$$V_{OUT2} = V_{TEMPSET} - \frac{Z2}{Z1}(V_{OUT1} - V_{TEMPSET})$$

The user sets the exact compensation network. This network varies from a simple integrator to PI, PID, or any other type of network. The user also determines the type of compensation and component values because they are dependent on the thermal response of the object and the TEC. One method for empirically determining these values is to input a step function to IN2P, therefore changing the target temperature, and adjusting the compensation network to minimize the settling time of the TEC temperature.

A typical compensation network for temperature control of a laser module is a PID loop consisting of a very low frequency pole and two separate zeros at higher frequencies. Figure 19 shows a simple network for implementing PID compensation. To reduce the noise sensitivity of the control loop, an additional pole is added at a higher frequency than the zeros. The bode plot of the magnitude is shown in Figure 20. The unity-gain crossover frequency of the feedforward amplifier is calculated using the following equation:

$$f_{0\,dB} = \frac{1}{2\pi R3C1} \times 80 \times TECGAIN$$

To ensure stability, the unity-gain crossover frequency is to be lower than the thermal time constant of the TEC and thermistor. However, this thermal time constant is sometimes unspecified making it difficult to characterize. There are many texts written on loop stabilization, and it is beyond the scope of this data sheet to discuss all methods and trade offs in optimizing compensation networks.

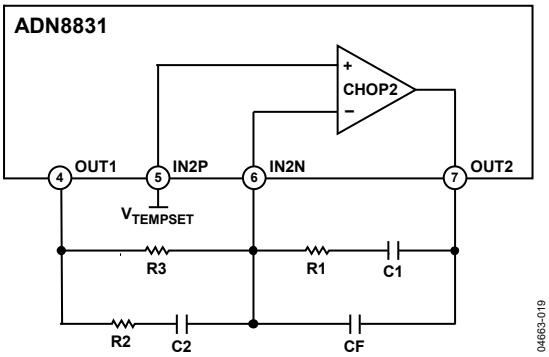


Figure 19. Implementing a PID Compensation Loop

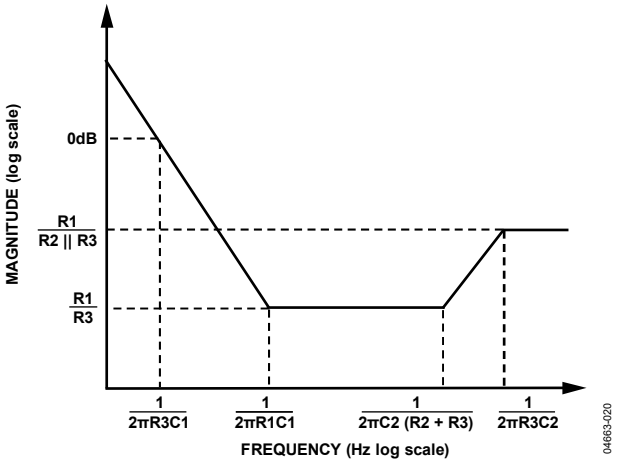


Figure 20. Bode Plot for PID Compensation

With an ADN8831-EVALZ board, AN-695, an application note shows how to determine the PID network components for a stable TEC subsystem performance.

MOSFET DRIVER AMPLIFIER

The ADN8831 has two separate MOSFET drivers: a switched output or pulse-width modulated (PWM) amplifier, and a high gain linear amplifier. Each amplifier has a pair of outputs that drive the gates of external MOSFETs which, in turn, drive the TEC as shown in Figure 17. A voltage across the TEC is monitored via SFB (Pin 23) and LFB (Pin 27). Although both MOSFET drivers achieve the same result, to provide constant voltage and high current, their operation is different. The exact equations for the two outputs are

$$V_{LFB} = V_B - 40(V_{OUT2} - 1.25)$$

$$V_{SFB} = V_{LFB} + 5(V_{OUT2} - 1.25)$$

where:
V_{OUT2} is the voltage at OUT2 (Pin 7).
V_B is determined by V_{DD} as

$$V_B = 1.5\ \text{V}[V_{DD} < 4.0\ \text{V}]$$

$$V_B = 2.5\ \text{V}[V_{DD} > 4.0\ \text{V}]$$

The voltage at OUT2 (Pin 7) is determined by the compensation network that receives temperature set voltage and thermistor voltage fed by the input amplifier. V_{LFB} has a low limit of 0 V and an upper limit of V_{DD}. Figure 21 shows the graphs of these equations.

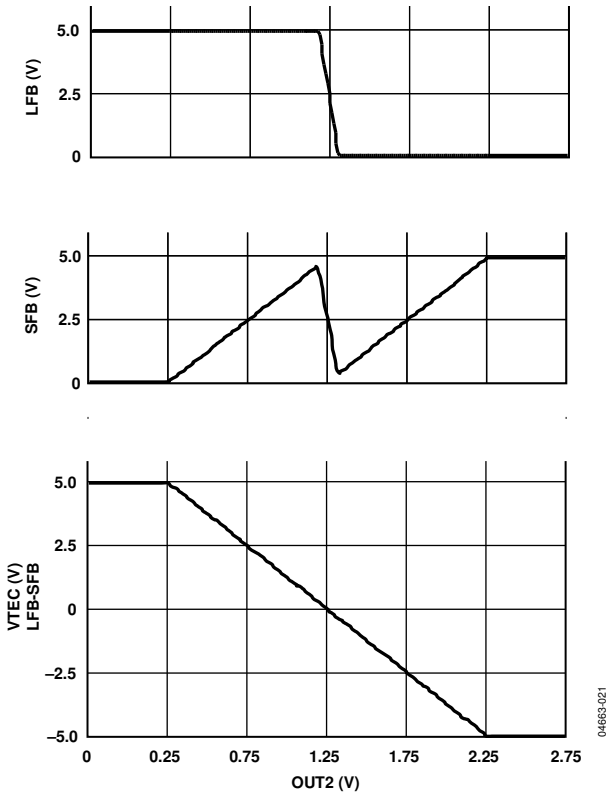
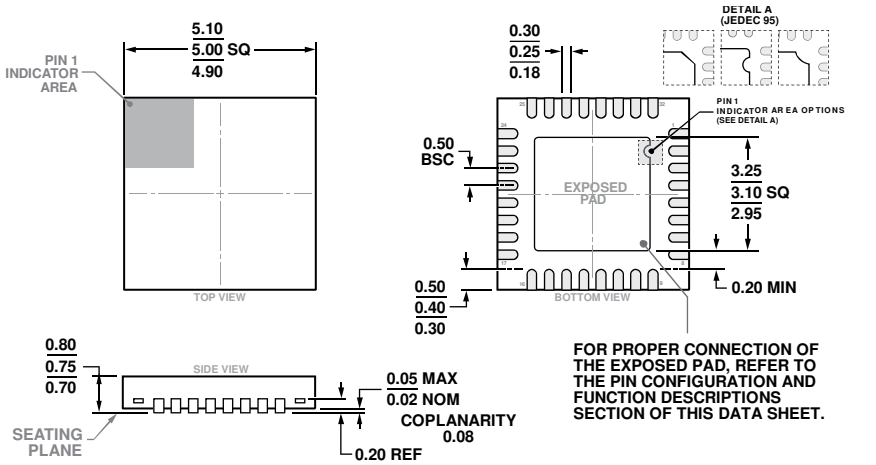


Figure 21. OUT2 Voltage vs. TEC Voltage

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD

Figure 22. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm× 5 mm Body and 0.75 mm Package Height
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADN8831ACPZ-R2	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-7
ADN8831ACPZ-REEL7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-7
ADN8831-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.