Micropower 500 mA CMOS LDO Regulator with Error Flag/Power-On-Reset

DESCRIPTION

The Si9185 is a 500 mA CMOS LDO (low dropout) voltage regulator. The device features ultra low ground current and dropout voltage to prolong battery life in portable electronics. The Si9185 offers line/load transient response and ripple rejection superior to that of bipolar or BiCMOS LDO regulators, and is designed to drive lower cost ceramic, as well as tantalum, output capacitors. An external noise bypass capacitor connected to the device's C_{NOISE} pin will lower the LDO's output noise for low noise applications. The Si9185 also includes an out-of-regulation error flag. If a capacitor is connected to the device's delay pin, the error flag output pin will generate a delayed power-on-reset signal. The device is guaranteed stable from maximum load current down to 0 mA load.

The Si9185 is available in both standard and lead (Pb)-free MLP33 PowerPAK packages and is specified to operate over the industrial temperature range of - 40 °C to 85 °C. MLP33 PowerPAK packaging allows enhanced heat transfer to the PC board.

FEATURES

Pb-free Available

RoHS* COMPLIANT

- Input voltage 2 V to 6 V
- Low 150 mV dropout at 500 mA load
- Guaranteed 500 mA output current
- Uses low ESR ceramic output capacitor
- Fast load and line transient response
- Only 100 μV_{RMS} noise with noise bypass capacitor
- 1 µA maximum shutdown current
- Built-in short circuit and thermal protection
- Out-of-regulation error flag (power good or POR)
- Fixed 1.215 V, 1.8 V, 2.5 V, 2.8 V, 3.0 V, 3.3 V, 5.0 V, or adjustable output voltage options
- Other output voltages available by special order
- 1.1 W power dissipation
- Thin, thermally enhanced MLP33 PowerPAK® package
- Compliant to RoHS directive 2002/95/EC

APPLICATIONS

- Laptop and palm computers
- Desktop computers
- Cellular phones
- PDA, digital still cameras

TYPICAL APPLICATIONS CIRCUITS

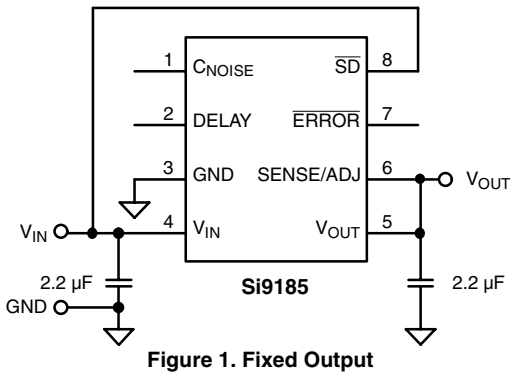


Figure 1. Fixed Output

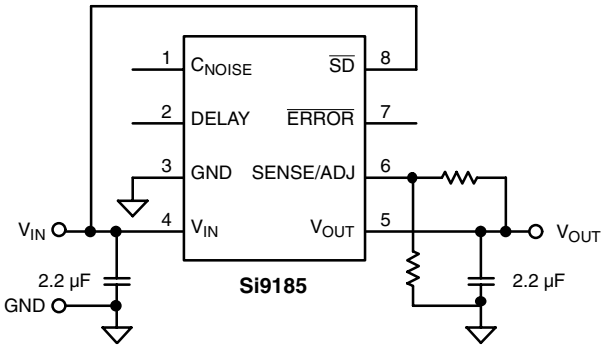


Figure 2. Adjustable Output

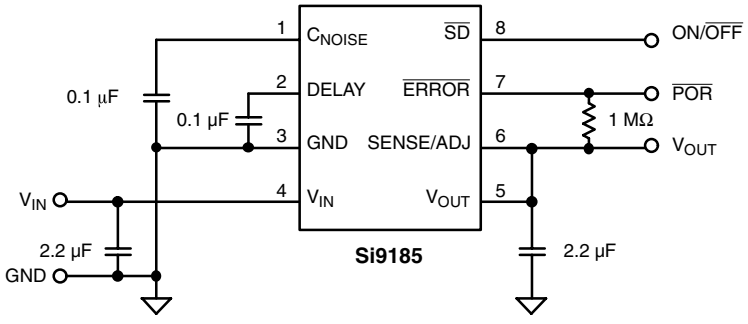


Figure 3. Low Noise, Full Features Application

* Pb containing terminations are not RoHS compliant, exemptions may apply.

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Input Voltage, V_{IN}		6.5	V
$\overline{SD}$ Input Voltage, $V_{\overline{SD}}$		- 0.3 to V_{IN}	
Output Current, I_{OUT}		500 mA Continuous, Short Circuit Protected	mA
Output Voltage, V_{OUT}		- 0.3 to $V_{O(nom)}$ + 0.3	V
Maximum Junction Temperature, $T_{J(max)}$		150	°C
Storage Temperature, T_{STG}		- 55 to 150	
ESD (Human Body Model)		2	kV
Power Dissipation[a]		2.5	W
Thermal Resistance (Θ_{JA})[a]	$R_{\Theta JA}$	50	°C/W
	$R_{\Theta JC}$	4	

Notes:
a. Device Mounted with all leads soldered or welded to PC board. (PC board - 2" x 2", 4-layer, FR4, 0.25 square inch spreading copper).
b. Derate 20 mW/°C above T_A = 25 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Limit	Unit
Input Voltage, V_{IN}	2 to 6	V
Output Voltage, V_{OUT} (Adjustable Version)	1.215 to 5	
R2	25 to 150	kΩ
Operating Ambient Temperature, T_A	- 40 to 85	°C
Operating Junction Temperature, T_J	- 40 to 125	

Notes:
C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF (ceramic, X5R or X7R type), C_{NOISE} = 0.1 µF (ceramic)
C_{OUT}Range = 1 µF to 10 µF (± 10 %, x5R or x7R type)
$C_{IN} \geq C_{OUT}$

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_{IN} = V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, $V_{\overline{SD}}$ = 1.5 V	Temp.[a]	Limits - 40 °C to 85 °C Min.[b]	Typ.[c]	Max.[b]	Unit
Output Voltage Range	V_{OUT}	Adjustable Version	Full	1.215		5	V
Output Voltage Accuracy (Fixed Versions)		1 mA ≤ I_{OUT} ≤ 500 mA	Room	- 1.5		1.5	% $V_{O(nom)}$
			Full	- 2.5		2.5	
Feedback Voltage (ADJ Version)	V_{ADJ}		Room	1.191	1.215	1.239	V
			Full	1.179		1.251	
Line Regulation ($V_{ADJ} \leq V_{OUT} \leq 4$ V)	$\frac{\Delta V_{OUT} \times 100}{V_{IN} \times V_{OUT}}$	From $V_{IN} = V_{OUT}$ + 1 V to V_{OUT} + 2 V	Full	- 0.18		0.18	%/V
Line Regulation (4 V $V_{OUT} \leq$ 5 V)		From V_{IN} = 5.5 V to 6 V	Full	- 0.18		0.18	
Dropout Voltage[d] (at $V_{OUT(nom)} \geq$ 2 V)	$V_{IN} - V_{OUT}$	I_{OUT} = 10 mA	Room		5	20	mV
		I_{OUT} = 200 mA	Room		145	215	
		I_{OUT} = 500 mA	Room		320	480	
			Full			600	
Dropout Voltage[d] (at $V_{OUT(nom)} \geq$ 2.5 V)		I_{OUT} = 200 mA	Room		115	175	
		I_{OUT} = 500 mA	Room		250	400	
			Full			480	

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_{IN} = V_{OUT(nom)} + 1$ V, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, $V_{\overline{SD}}$ = 1.5 V		Temp.[a]	Limits - 40 °C to 85 °C Min.[b]	Typ.[c]	Max.[b]	Unit
Dropout Voltage[d] (at $V_{OUT(nom)} \geq 3.3$ V)	$V_{IN} - V_{OUT}$	I_{OUT} = 200 mA		Room		90	135	mV
		I_{OUT} = 500 mA		Room		200	300	
				Full			400	
Dropout Voltage[d] (at $V_{OUT(nom)} \geq 5$ V)	$V_{IN} - V_{OUT}$	I_{OUT} = 200 mA		Room		60	100	
		I_{OUT} = 500 mA		Room		150	210	
				Full			300	
Dropout Voltage[d] (at $V_{OUT(nom)} < 2$ V, $V_{IN} \geq 2$ V)	$V_{IN} - V_{OUT}$	I_{OUT} = 200 mA		Room		170	250	
		I_{OUT} = 500 mA		Room		415	625	
				Full			825	
Ground Pin Current	I_{GND}	I_{OUT} = 0 mA		Room		150		µA
		I_{OUT} = 200 mA		Room		1000		
				Full			1500	
		I_{OUT} = 500 mA		Room		2500		
				Full			4000	
Shutdown Supply Current	$I_{IN(off)}$	$V_{\overline{SD}}$ = 0 V		Room		0.1	1	µA
ADJ Pin Current	I_{ADJ}	ADJ = 1.2 V		Room		5	100	nA
Peak Output current	$I_{O(peak)}$	$V_{OUT} \geq 0.95 \times V_{OUT(nom)}$, t_{pw} = 2 ms		Room	600			mA
Output Noise Voltage	e_N	BW = 50 Hz to 100 kHz I_{OUT} = 150 mA	w/o C_{NOISE}	Room		200		µV(rms)
			C_{NOISE} = 0.1 µF	Room		100		
Ripple Rejection	$\Delta V_{OUT}/\Delta V_{IN}$	I_{OUT} = 150 mA	f = 1 kHz	Room		60		dB
			f = 10 kHz	Room		60		
			f = 100 kHz	Room		40		
Dynamic Line Regulation	$\Delta V_{O(line)}$	V_{IN} : $V_{OUT(nom)}$ + 1 V to $V_{OUT(nom)}$ + 2 V t_R/t_F = 5 µs, I_{OUT} = 500 mA		Room		10		mV
Dynamic Load Regulation	$\Delta V_{O(load)}$	I_{OUT} : 1 mA to 150 mA, t_R/t_F = 2 µs		Room		30		
V_{OUT} Turn-On Time	t_{ON}	V_{IN} = 4.3 V V_{OUT} = 3.3 V	w/o C_{NOISE} Cap	Room		5		µs
			C_{NOISE} = 0.1 µF	Room		2		mS
Thermal Shutdown								
Thermal Shutdown Junction Temperature	$t_{J(s/d)}$			Room		165		°C
Thermal Hysteresis	t_{HYST}			Room		20		
Short Circuit Current	I_{SC}	V_{OUT} = 0 V		Room		800		mA
Shutdown Input								
$\overline{SD}$ Input Voltage	V_{IH}	High = Regulator On (Rising)		Full	1.5		V_{IN}	V
	V_{IL}	Low = Regulator Off (Falling)		Full			0.4	
$\overline{SD}$ Input Current[e]	I_{IH}	$V_{\overline{SD}}$ = 0 V, Regulator OFF		Room		0.01		µA
	I_{IL}	$V_{\overline{SD}}$ = 6 V, Regulator ON		Room		1.0		
Shutdown Hysteresis	V_{HYST}			Full		100		mV

SPECIFICATIONS							
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** $V_{IN} = V_{OUT(nom)} + 1$ V, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, $V_{\overline{SD}}$ = 1.5 V	**Temp.[a]**	**Limits** - 40 °C to 85 °C **Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Error Output							
Output High Leakage	I_{OFF}	$\overline{ERROR} = V_{OUT(nom)}$	Full		0.01	2	µA
Output Low Voltage[g]	V_{OL}	I_{SINK} = 2 mA	Full			0.4	V
Out-of-Regulation Error Flag Threshold Voltage (Rising)[g]	V_{TH}		Full	0.93 x V_{OUT}	0.95 x V_{OUT}	0.97 x V_{OUT}	
Hysteresis[g]	V_{HYST}		Room		2 % x V_{OUT}		
Delay Pin Current Source	I_{DELAY}		Room	1.2	2.2	3.0	µA

Notes:
a. Room = 25 °C, Full = - 40 °C to 85 °C.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing. Typical values for dropout voltage at $V_{OUT} \geq 2$ V are measured at V_{OUT} = 3.3 V, while typical values for dropout voltage at $V_{OUT} < 2$ V are measured at V_{OUT} = 1.8 V.
d. Dropout voltage is defined as the input to output differential voltage at which the output voltage drops 2 % below the output voltage measured with a 1 V differential, provided that VIN does not drop below 2.0 V. When $V_{OUT(nom)}$ is less than 2.0 V, the output will be in regulation when 2.0 V - $V_{OUT(nom)}$ is greater than the dropout voltage specified.
e. The device's shutdown pin includes a typical 6 MΩ internal pull-down resistor connected to ground.
f. V_{OUT} is defined as the output voltage of the DUT at 1 mA.
g. The Error Output (Low) function is guaranteed for $V_{IN} \geq 2.0$ V.

TIMING WAVEFORMS

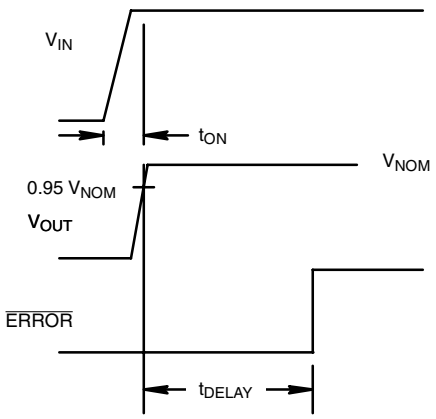
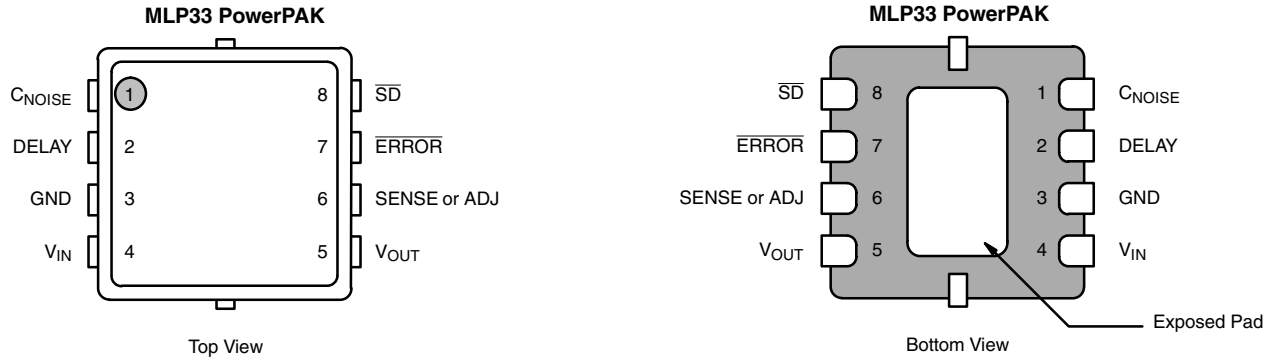


Figure 4. Timing Diagram for Power-Up

PIN CONFIGURATION



PIN DESCRIPTION

Pin Number	Name	Function
1	C_{NOISE}	Noise bypass pin. For low noise applications, a 0.01 µF or larger ceramic capacitor should be connected from this pin to ground.
2	DELAY	Capacitor connected from this pin to ground will allow a delayed power-on-reset signal at the $\overline{ERROR}$ (Pin 7) output. Refer to Figure 4.
3	GND	Ground pin. Local ground for C_{NOISE} and C_{OUT}.
4	V_{IN}	Input supply pin. Bypass this pin with a 2.2 µF ceramic or tantalum capacitor to ground.
5	V_{OUT}	Output voltage. Connect C_{OUT} between this pin and ground.
6	SENSE or ADJ	For fixed output voltage versions, this pin should be connected to V_{OUT} (Pin 5). For adjustable output voltage version, this voltage feedback pin sets the output voltage via an external resistor divider.
7	$\overline{ERROR}$	This open drain output is an error flag output which goes low when V_{OUT} drops 5 % below its nominal voltage. This pin also provides a power-on-reset signal if a capacitor is connected to the DELAY pin.
8	$\overline{SD}$	By applying less than 0.4 V to this pin, the device will be turned off. Connect this pin to V_{IN} if unused.
	Exposed Pad	The die substrate is attached to the exposed pad and must be electrically connected to GND.

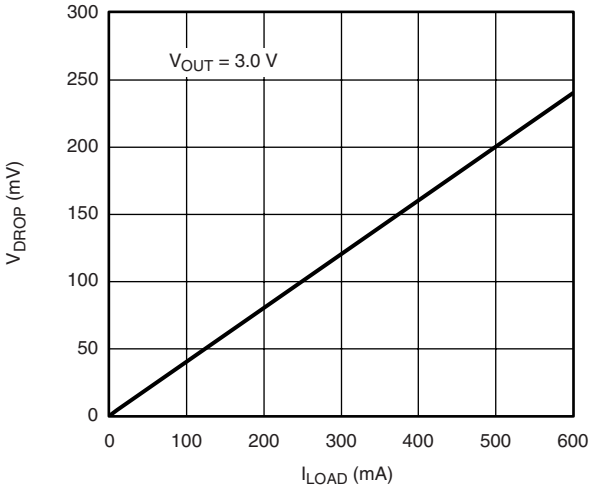
ORDERING INFORMATION

Standard Part Number	Lead (Pb)-free Part Number	Marking	Voltage	Temperature	Package
Si9185DMP-12-T1	Si9185DMP-12-T1-E3	8512	1.215 V	- 40 °C to 85 °C	MLP33 PowerPak
Si9185DMP-18-T1	Si9185DMP-18-T1-E3	8518	1.80 V		
Si9185DMP-25-T1	Si9185DMP-25-T1-E3	8525	2.50 V		
Si9185DMP-28-T1	Si9185DMP-28-T1-E3	8528	2.80 V		
Si9185DMP-30-T1	Si9185DMP-30-T1-E3	8530	3.00 V		
Si9185DMP-33-T1	Si9185DMP-33-T1-E3	8533	3.30 V		
Si9185DMP-50-T1	Si9185DMP-50-T1-E3	8550	5.00 V		
Si9185DMP-AD-T1	Si9185DMP-AD-T1-E3	85AD	Adjustable		

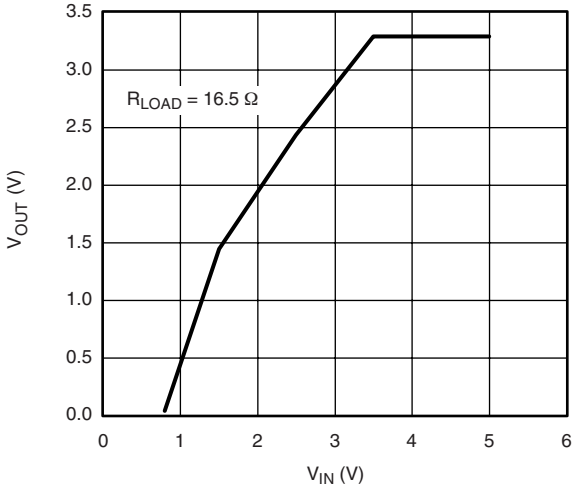
Additional voltage options are available.

Eval Kit	Temperature Range	Board Type
Si9185DB	- 40 to 85 °C	Surface Mount

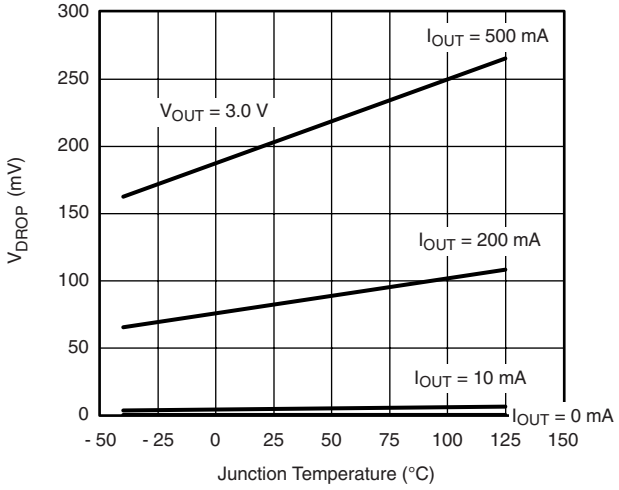
TYPICAL CHARACTERISTICS Internally Regulated, 25 °C, unless otherwise noted



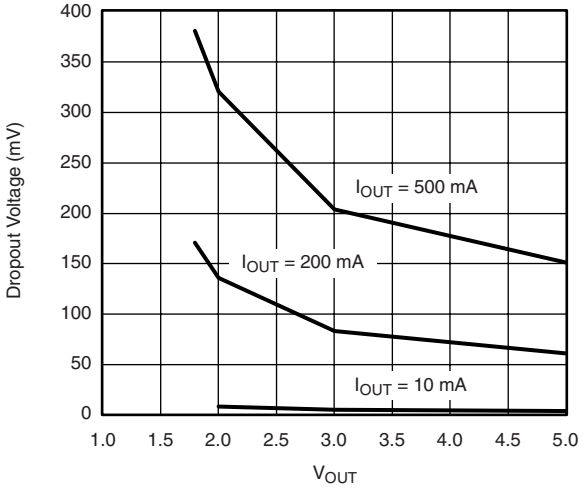
Dropout Voltage vs. Load Current



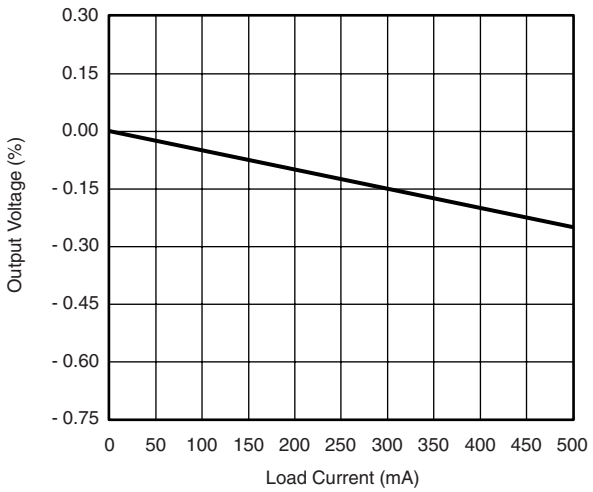
Dropout Characteristic



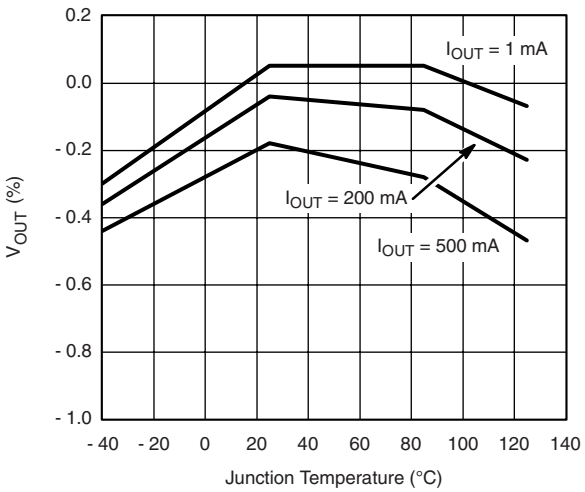
Dropout Voltage vs. Temperature



Dropout Voltage vs. V_{OUT}

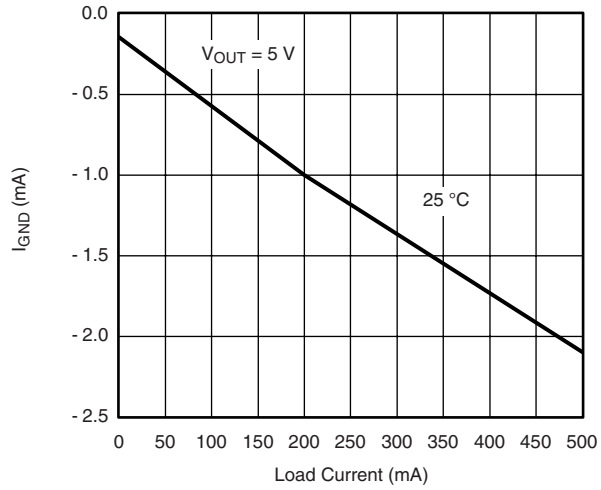


Normalized Output Voltage vs. Load Current

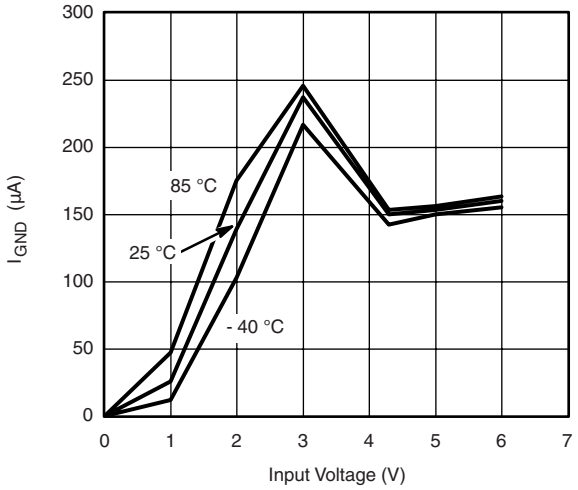


Normalized V_{OUT} vs. Temperature

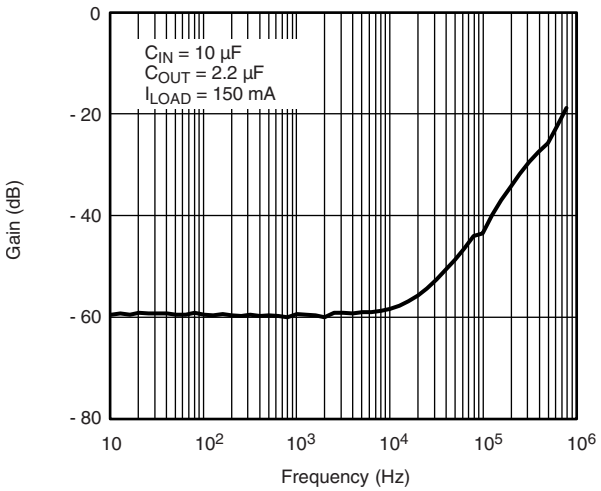
TYPICAL CHARACTERISTICS Internally Regulated, 25 °C, unless otherwise noted



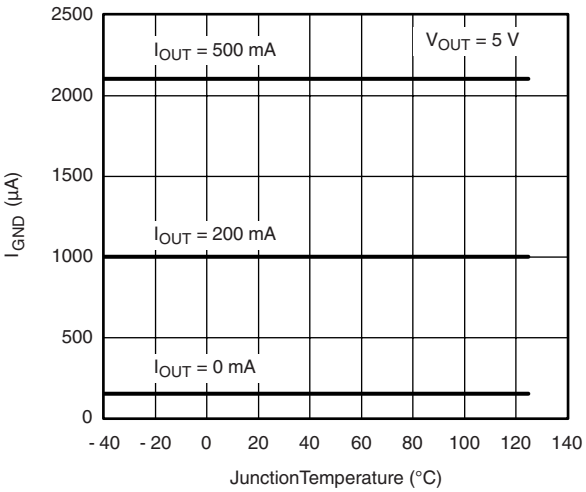
GND Current vs. Load Current



No Load GND Pin Current vs. Input Voltage

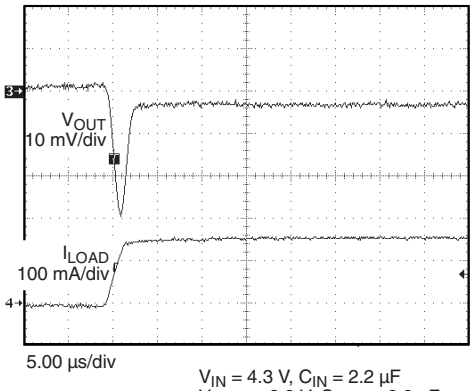


Power Supply Rejection



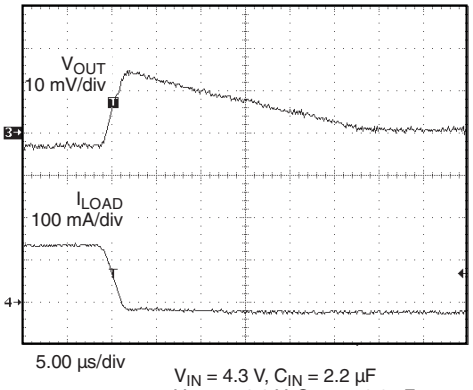
GND Pin Current vs. Temperature and Load

TYPICAL WAVEFORMS



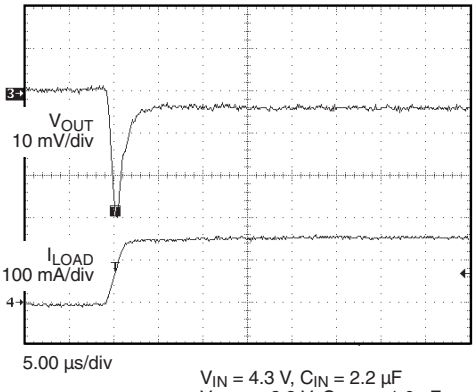
V_{IN} = 4.3 V, C_{IN} = 2.2 µF
V_{OUT} = 3.3 V, C_{OUT} = 2.2 µF
I_{LOAD} = 1 mA to 150 mA
t_{rise} = 2 µs

Load Transient Response-1



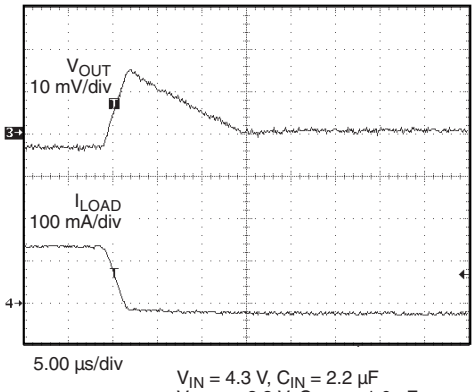
V_{IN} = 4.3 V, C_{IN} = 2.2 µF
V_{OUT} = 3.3 V, C_{OUT} = 2.2 µF
I_{LOAD} = 1 mA to 150 mA
t_{rise} = 2 µs

Load Transient Response-2



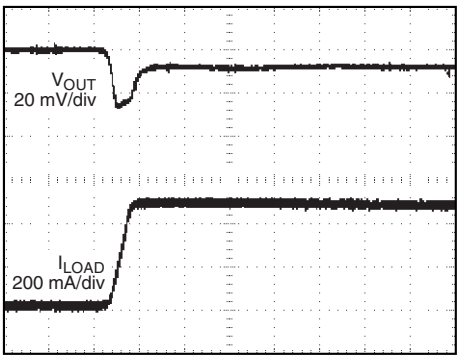
V_{IN} = 4.3 V, C_{IN} = 2.2 µF
V_{OUT} = 3.3 V, C_{OUT} = 1.0 µF
I_{LOAD} = 1 mA to 150 mA
t_{rise} = 2 µs

Load Transient Response-3



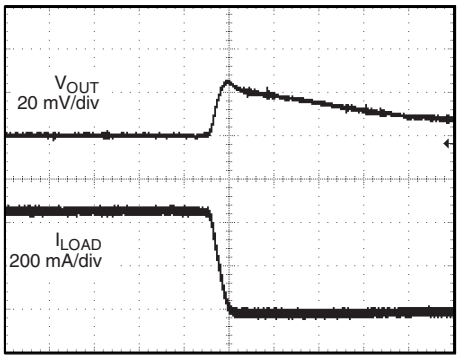
V_{IN} = 4.3 V, C_{IN} = 2.2 µF
V_{OUT} = 3.3 V, C_{OUT} = 1.0 µF
I_{LOAD} = 1 mA to 150 mA
t_{rise} = 2 µs

Load Transient Response-4



V_{IN} = 4.3 V, C_{IN} = 10 µF
V_{OUT} = 3.3 V, C_{OUT} = 10 µF
I_{LOAD} = 1 mA to 500 mA
t_{rise} = 2 µs

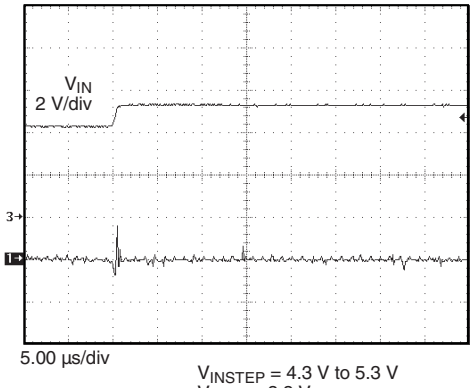
Load Transient Response-5



V_{IN} = 4.3 V, C_{IN} = 10 µF
V_{OUT} = 3.3 V, C_{OUT} = 10 µF
I_{LOAD} = 1 mA to 500 mA
t_{rise} = 2 µs

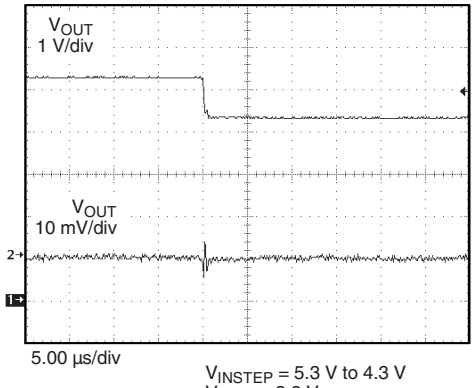
Load Transient Response-6

TYPICAL WAVEFORMS



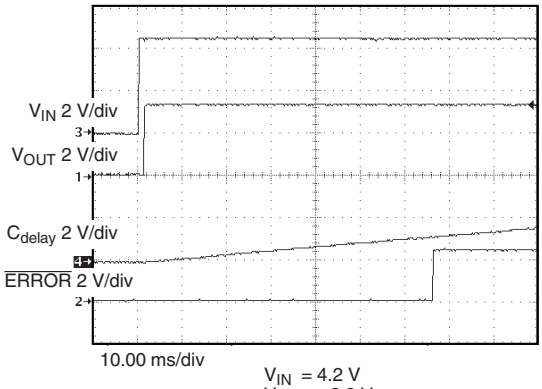
V_{INSTEP} = 4.3 V to 5.3 V
V_{OUT} = 3.3 V
C_{OUT} = 2.2 µF
C_{IN} = 10 µF
I_{LOAD} = 500 mA
t_{rise} = 5 µs

Line Transient Response-1



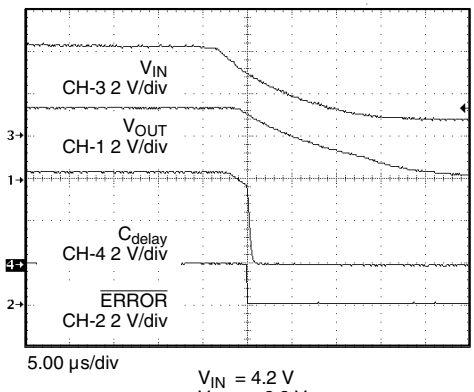
V_{INSTEP} = 5.3 V to 4.3 V
V_{OUT} = 3.3 V
C_{OUT} = 2.2 µF
C_{IN} = 10 µF
I_{LOAD} = 500 mA
t_{fall} = 5 µs

Line Transient Response-2



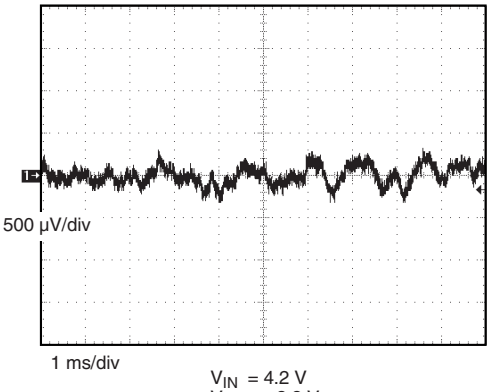
V_{IN} = 4.2 V
V_{OUT} = 3.3 V
C_{delay} = 0.1 µF
C_{NOISE} = 0.1 µF
I_{LOAD} = 350 mA

Turn-On Sequence



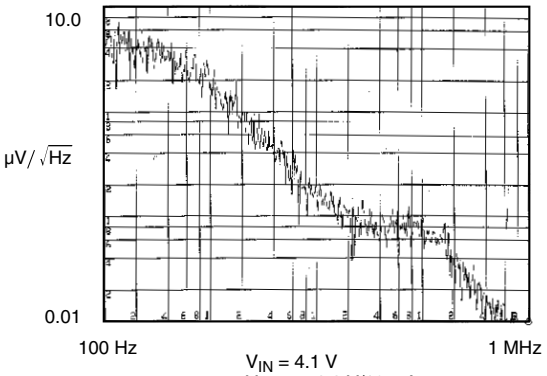
V_{IN} = 4.2 V
V_{OUT} = 3.3 V
C_{delay} = 0.1 µF
C_{NOISE} = 0.1 µF
I_{LOAD} = 350 mA

Turn-Off Sequence



V_{IN} = 4.2 V
V_{OUT} = 3.3 V
I_{OUT} = 150 mA
C_{NOISE} = 0.1 µF
BW = 10 Hz to 1 MHz

Output Noise



V_{IN} = 4.1 V
V_{OUT} = 3.3 V/10 mA
C_{NOISE} = 0.1 µF

Noise Spectrum

BLOCK DIAGRAM

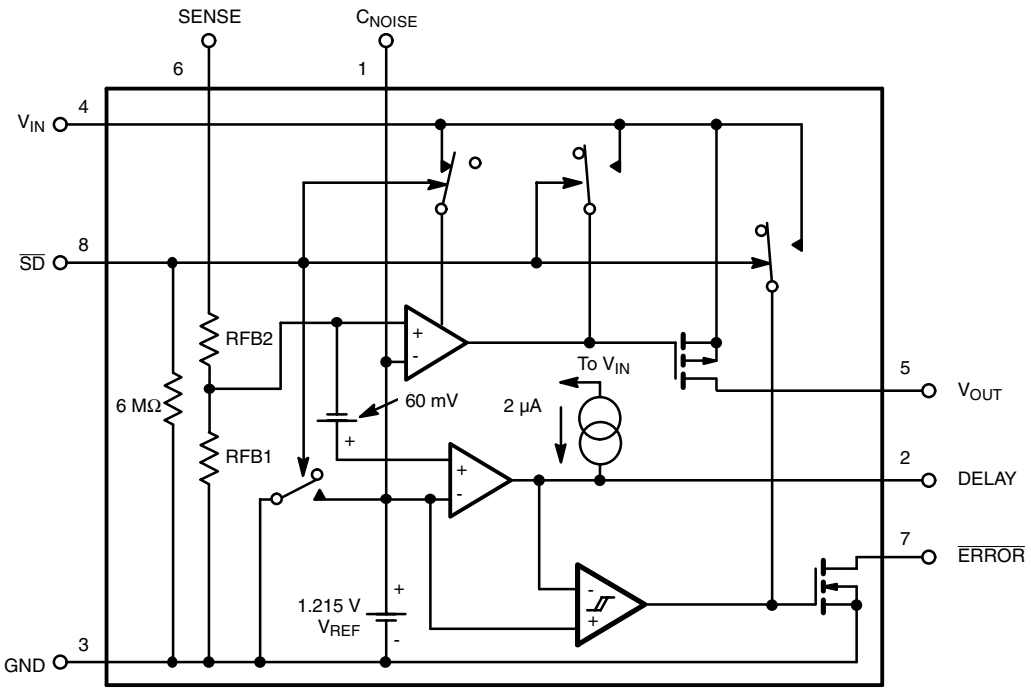


Figure 5.

DETAILED DESCRIPTION

The Si9185 is a low drop out, low quiescent current, and very linear regulator family with very fast transient response. It is primarily designed for battery powered applications where battery run time is at a premium. The low quiescent current allows extended standby time while low drop out voltage enables the system to fully utilize battery power before recharge. The Si9185 is a very fast regulator with bandwidth exceeding 50 kHz while maintaining low quiescent current at light load conditions. With this bandwidth, the Si9185 is the fastest LDO available today. The Si9185 is stable with any output capacitor type from 1 µF to 10.0 µF. However, X5R or X7R ceramic capacitors are recommended for best output noise and transient performance.

V_{IN}

V_{IN} is the input supply pin. The bypass capacitor for this pin is not critical as long as the input supply has low enough source impedance. For practical circuits, a 1.0 µF or larger ceramic capacitor is recommended. When the source impedance is not low enough and/or the source is several inches from the Si9185, then a larger input bypass capacitor is needed. It is required that the equivalent impedance (source impedance, wire, and trace impedance in parallel with input bypass capacitor impedance) must be smaller than the input impedance of the Si9185 for stable operation. When the source impedance, wire, and trace impedance are unknown, it is recommended that an input bypass capacitor be used of a value that is equal to or greater than the output capacitor.

V_{OUT}

V_{OUT} is the output voltage of the regulator. Connect a bypass capacitor from V_{OUT} to ground. The output capacitor can be any value from 1.0 µF to 10.0 µF. A ceramic capacitor with X5R or X7R dielectric type is recommended for best output noise, line transient, and load transient performance.

GND

Ground is the common ground connection for V_{IN} and V_{OUT}. It is also the local ground connection for C_{NOISE}, DELAY, SENSE or ADJ, and $\overline{SD}$.

SENSE or ADJ

SENSE is used to sense the output voltage. Connect SENSE to V_{OUT} for the fixed voltage version. For the adjustable output version, use a resistor divider R1 and R2, connect R1 from V_{OUT} to ADJ and R2 from ADJ to ground. R2 should be in the 25 kΩ to 150 kΩ range for low power consumption, while maintaining adequate noise immunity.

The formula below calculates the value of R1, given the desired output voltage and the R2 value,

$$R1 = \frac{(V_{OUT} - V_{ADJ})R2}{V_{ADJ}} \quad (1)$$

V_{ADJ} is nominally 1.215 V.

SHUTDOWN ($\overline{SD}$)

$\overline{SD}$ controls the turning on and off of the Si9185. V_{OUT} is guaranteed to be on when the $\overline{SD}$ pin voltage equals or is greater than 1.5 V. V_{OUT} is guaranteed to be off when the $\overline{SD}$ pin voltage equals or is less than 0.4 V. During shutdown mode, the Si9185 will draw less than 2 µA current from the source. To automatically turn on V_{OUT} whenever the input is applied, tie the $\overline{SD}$ pin to V_{IN}.

$\overline{ERROR}$

$\overline{ERROR}$ is an open drain output that goes low when V_{OUT} is less than 5 % of its normal value. As with any open drain output, an external pull up resistor is needed. When a capacitor is connected from DELAY to GROUND, the error signal transition from low to high is delayed (see Delay section). This delayed error signal can be used as the power-on reset signal for the application system. (Refer to Figure 4.)

The $\overline{ERROR}$ pin is disconnected if not used.

DELAY

A capacitor from DELAY to GROUND sets the time delay for $\overline{ERROR}$ going from low to high state. The time delay can be calculated using the following formula:

$$T_{delay} = \frac{(V_{ADJ})C_{delay}}{I_{delay}} \quad (2)$$

The DELAY pin should be an open circuit if not used.

C_{NOISE}

For low noise application, connect a high frequency ceramic capacitor from C_{NOISE} to ground. A 0.01 µF or a 0.1 µF X5R or X7R is recommended.

Safe Operating Area

The ability of the Si9185 to supply current is ultimately dependent on the junction temperature of the pass device. Junction temperature is in turn dependent on power dissipation in the pass device, the thermal resistance of the package and the circuit board, and the ambient temperature. The power dissipation is defined as

$$P_D = (V_{IN} - V_{OUT}) * I_{OUT} .$$

Junction temperature is defined as

$$T_J = T_A + ((P_D * (R\theta_{JC} + R\theta_{CA})).$$

To calculate the limits of performance, these equations must be rewritten.

Allowable power dissipation is calculated using the equation

$$P_D = (T_J - T_A)/ (R\theta_{JC} + R\theta_{CA})$$

While allowable output current is calculated using the equation

$$I_{OUT} = (T_J - T_A)/ (R\theta_{JC} + R\theta_{CA}) * (V_{IN} - V_{OUT}).$$

Ratings of the Si9185 that must be observed are

T_{Jmax} = 125 °C, T_{Amax} = 85 °C, $(V_{IN} - V_{OUT})_{max}$ = 5.3 V, $R\theta_{JC}$ = 4 °C/W.

The value of $R\theta_{CA}$ is dependent on the PC board used. The value of $R\theta_{CA}$ for the board used in device characterization is approximately 46 °C/W.

Figure 6 shows the performance limits graphically for the Si9185 mounted on the circuit board used for thermal characterization.

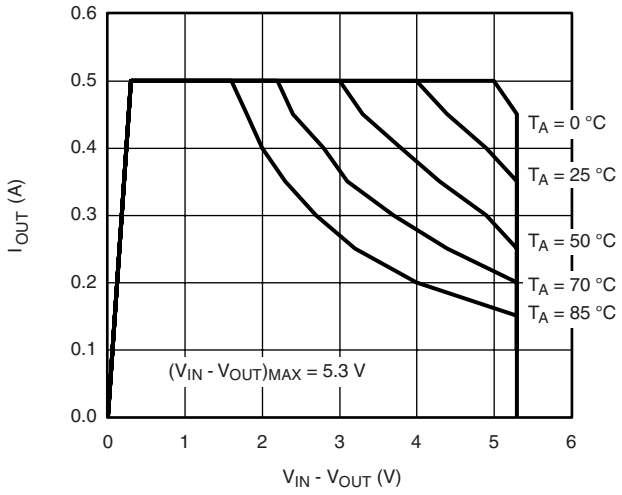


Figure 6.

PCB Footprint and Layout Considerations

The Si9185 comes in the MLP33 PowerPAK package with an exposed pad on the bottom to provide a low thermal impedance path into the PC board. When the PC board layout is designed, a copper plane, referred to as spreading copper, is recommended to be placed under the package to which the exposed pad is soldered. This spreading copper is the path for the heat to move away from the package into the PC board. With the Si9185 mounted on a four layer board measuring 2" x 2", a spreading copper area of 0.25 square inches will yield an $R\theta_{ja}$ of 50 °C/W. This allows for power dissipation in excess of 1 watt in an 80 °C ambient environment.

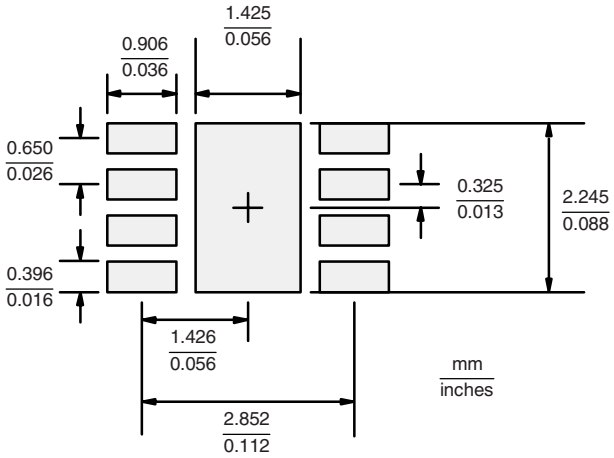


Figure 7. MLP33 PowerPAK Pad Pattern

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71765.

Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay’s terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.