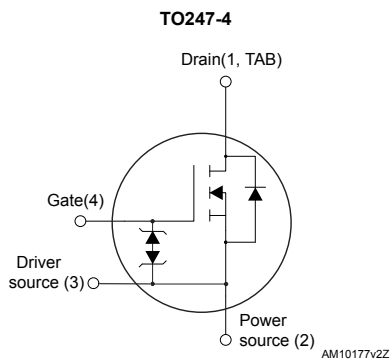
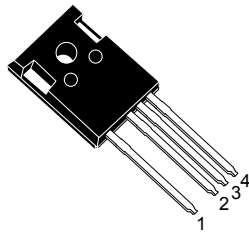


## N-channel 600 V, 60 mΩ typ., 42 A MDmesh M2 Power MOSFET in a TO247-4 package



### Features

Order code	$V_{DS} @ T_{Jmax.}$	$R_{DS(on)max.}$	$I_D$
STW48N60M2-4	650 V	70 mΩ	42 A

- Excellent switching performance thanks to the extra driving source pin
- Extremely low gate charge
- Excellent output capacitance ( $C_{OSS}$ ) profile
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using MDmesh M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.



#### Product status

STW48N60M2-4

#### Device summary

Order code	STW48N60M2-4
Marking	48N60M2
Package	TO247-4
Packing	Tube

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	42	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	26	A
$I_{DM}^{(1)}$	Drain current (pulsed)	168	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	300	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature range	- 55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 42\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS(peak)} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$
3.  $V_{DS} \leq 480\text{ V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.42	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	50	$^\circ\text{C}/\text{W}$

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax.}$ )	7	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ ; $V_{DD} = 50\text{ V}$ )	1	J

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off-states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero-gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}, T_C = 125\text{ °C}^{(1)}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 21\text{ A}$		60	70	$\text{m}\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$	-	3060	-	pF
$C_{oss}$	Output capacitance		-	143	-	pF
$C_{rss}$	Reverse transfer capacitance		-	4.3	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }480\text{ V}$	-	630	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0\text{ A}$	-	4.6	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 42\text{ A},$	-	70	-	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 0\text{ to }10\text{ V}$	-	10.5	-	nC
$Q_{gd}$	Gate-drain charge	(see Figure 14. Test circuit for gate charge behavior )	-	31	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}, I_D = 21\text{ A},$	-	TBD	-	ns
$t_r$	Rise time	$R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$	-	TBD	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Switching times test circuit for resistive load and Figure 17. Unclamped inductive waveform)	-	TBD	-	ns
$t_f$	Fall time		-	TBD	-	ns

**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		42	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		168	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 21\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 42\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	-	487		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	9.1		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	37.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 42\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	-	605		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	12.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	41.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

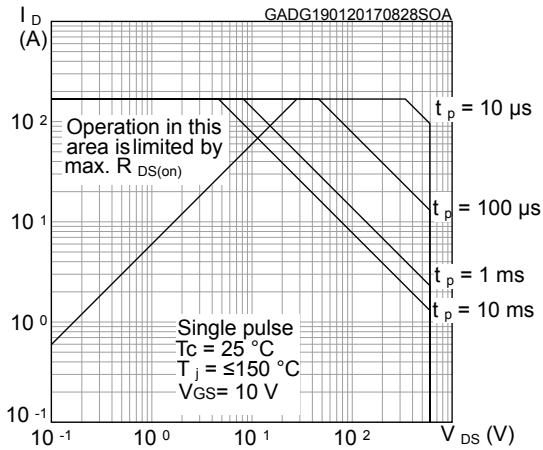


Figure 2. Thermal impedance

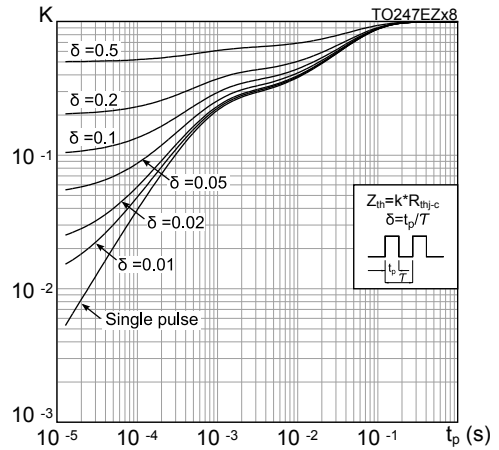


Figure 3. Output characteristics

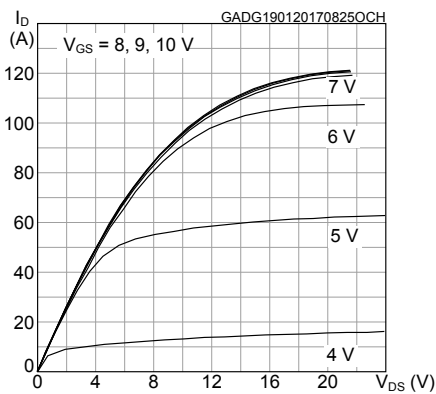


Figure 4. Transfer characteristics

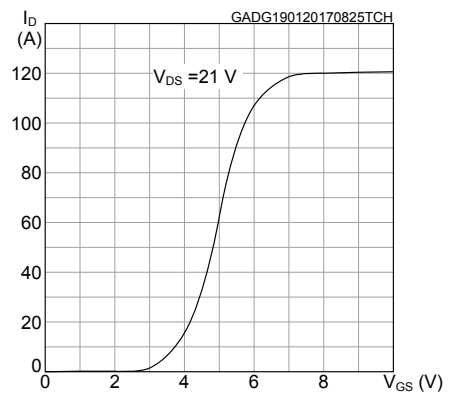


Figure 5. Gate charge vs gate-source voltage

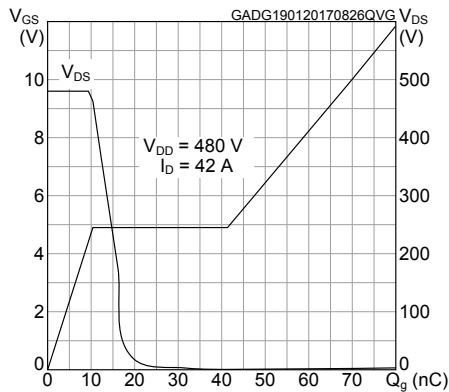
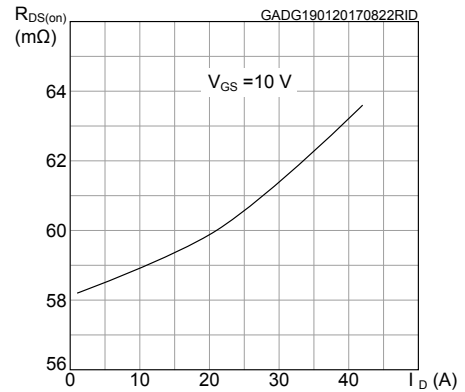
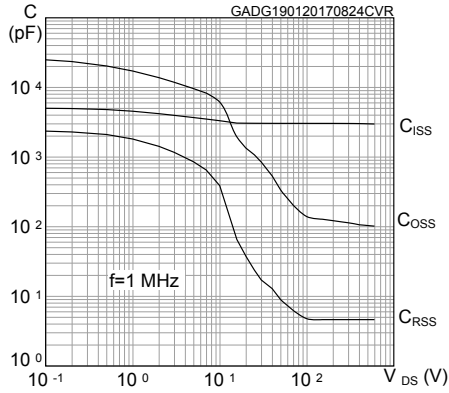


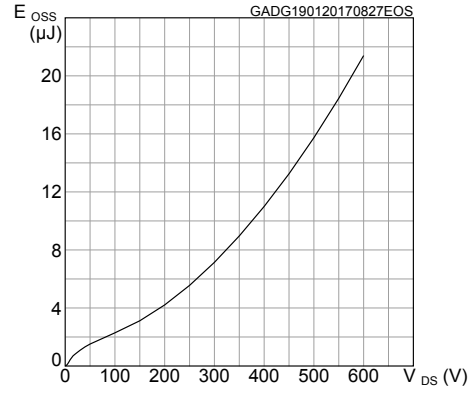
Figure 6. Static drain-source on-resistance



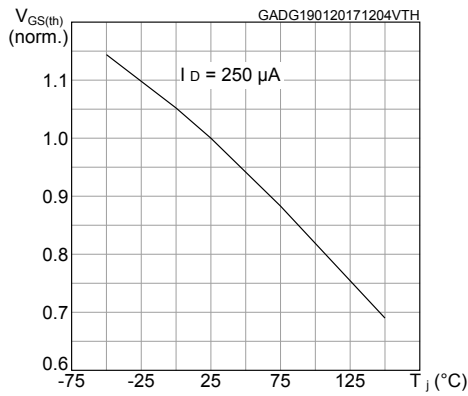
**Figure 7. Capacitance variations**



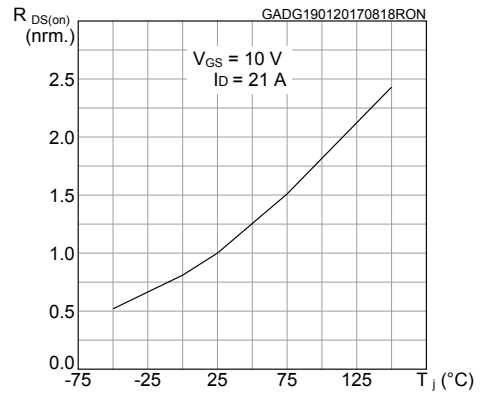
**Figure 8. Output capacitance stored energy**



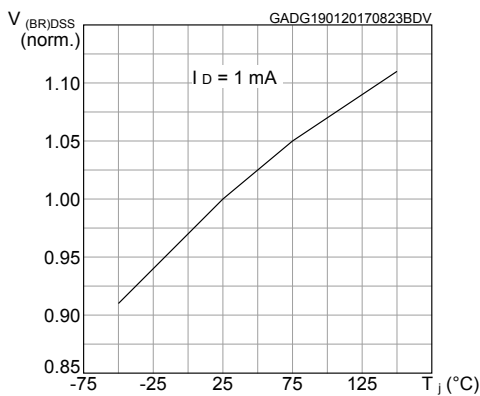
**Figure 9. Normalized gate threshold voltage vs temperature**



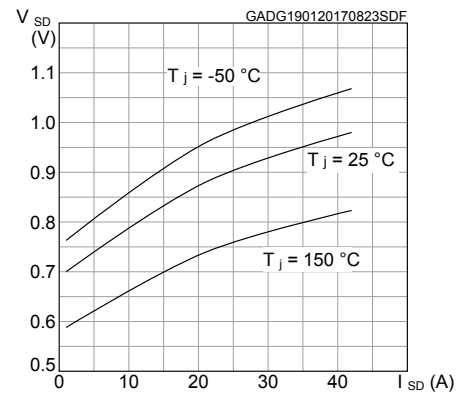
**Figure 10. Normalized on-resistance vs temperature**



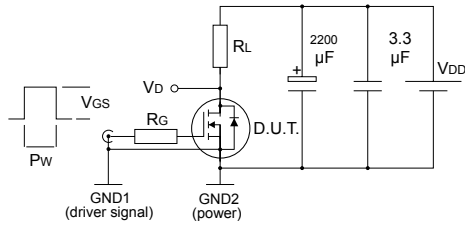
**Figure 11. Normalized  $V_{(BR)DSS}$  vs temperature**



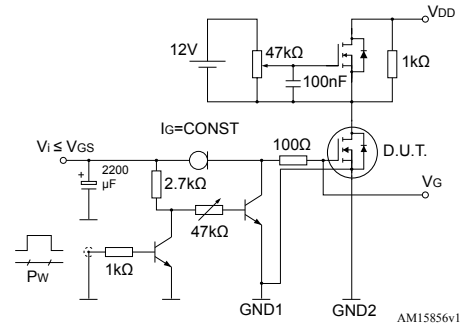
**Figure 12. Source-drain diode forward characteristics**



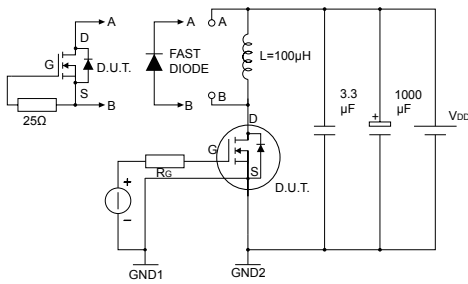
### 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**


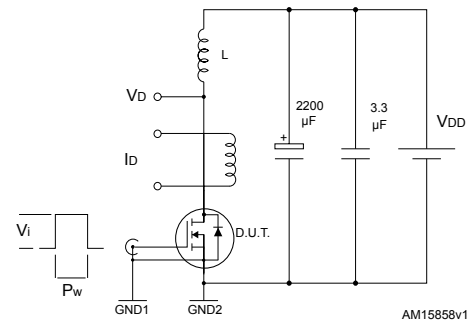
AM15855v1

**Figure 14. Test circuit for gate charge behavior**


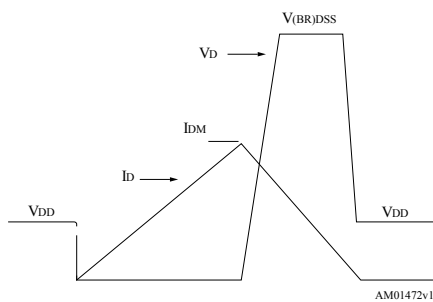
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**Figure 15. Test circuit for inductive load switching and diode recovery times**


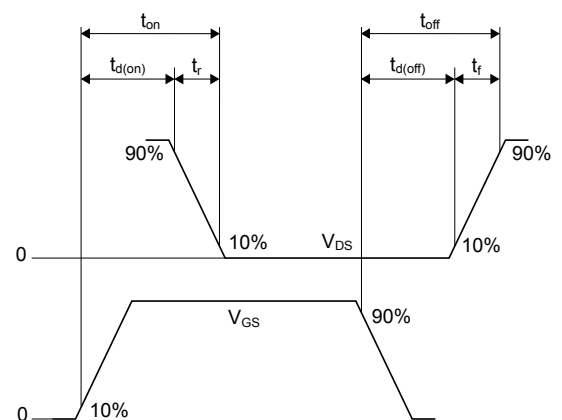
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**Figure 16. Unclamped inductive load test circuit**


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**Figure 17. Unclamped inductive waveform**


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**Figure 18. Switching time waveform**


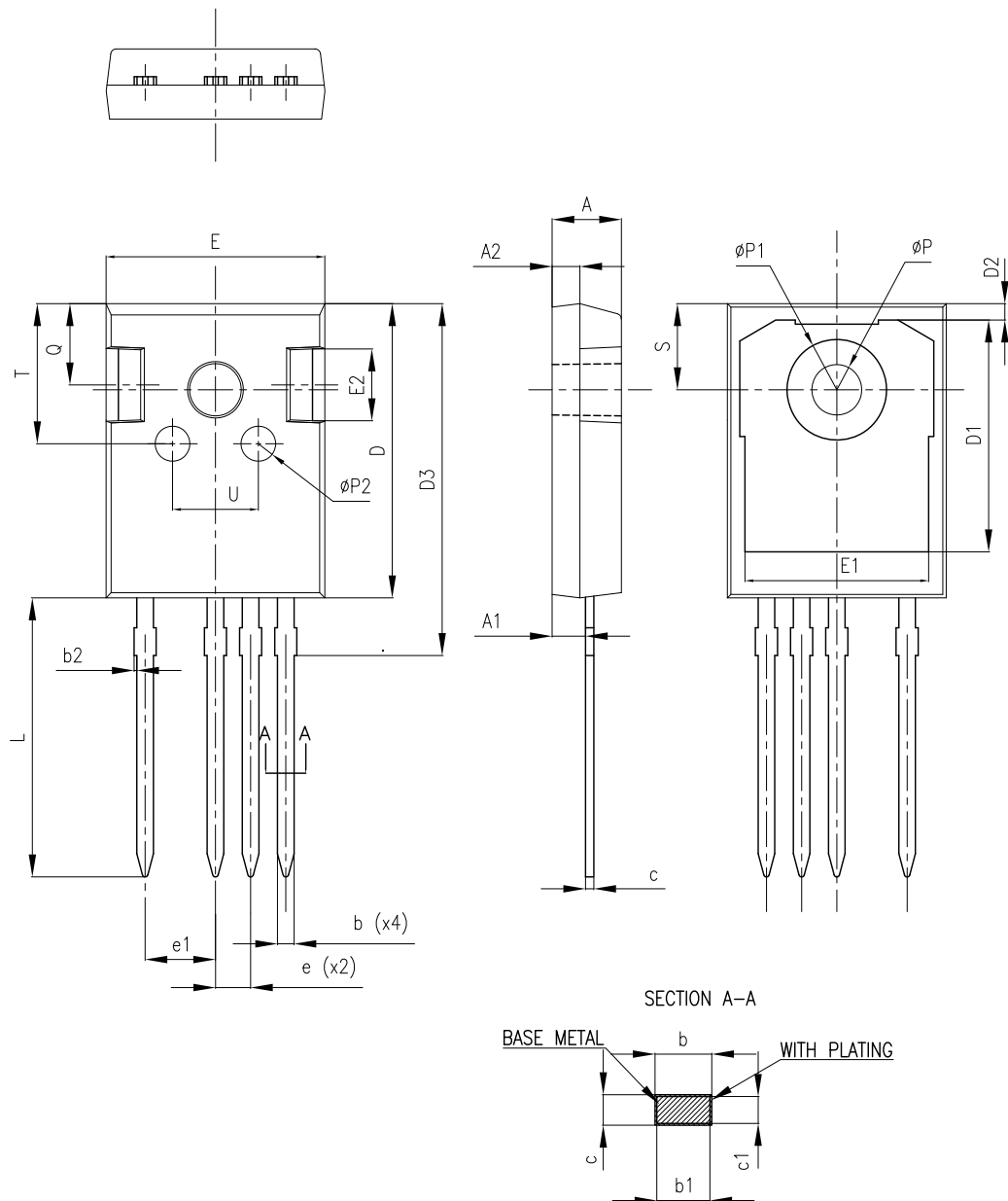
AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 TO247-4 package information

Figure 19. TO247-4 package outline



8405626\_2



**Table 8. TO247-4 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.29
b1	1.15	1.20	1.25
b2	0		0.20
c	0.59		0.66
c1	0.58	0.60	0.62
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
D2	1.05	1.20	1.35
D3	24.97	25.12	25.27
E	15.70	15.80	15.90
E1	13.10	13.30	13.50
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	2.44	2.54	2.64
e1	4.98	5.08	5.18
L	19.80	19.92	20.10
P	3.50	3.60	3.70
P1			7.40
P2	2.40	2.50	2.60
Q	5.60		6.00
S		6.15	
T	9.80		10.20
U	6.00		6.40

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
25-Jul-2014	1	Initial release.
30-Jan-2015	2	Added section <i>Electrical characteristics (curves)</i> .
20-Jan-2017	3	Updated <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 4: "On /off-states"</i> , <i>Table 5: "Dynamic"</i> , <i>Table 6: "Switching times"</i> and <i>Table 7: "Sourcedrain diode"</i> . Updated <i>Section 2.2: "Electrical characteristics (curves)"</i> .
02-Apr-2020	4	Updated <i>Table 6. Switching times</i> . Minor text changes.

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