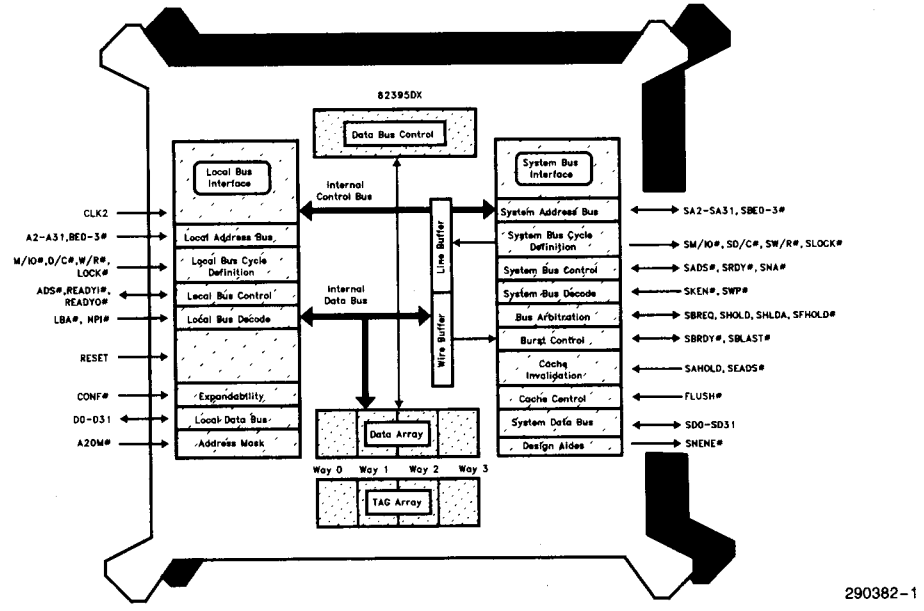
82395DX HIGH PERFORMANCE SMART CACHE

- **Optimized Intel386™ DX Microprocessor Companion**
- **Integrated 16KB Data RAM**
- **4 Way SET Associative with Pseudo LRU Algorithm**
- **Write Buffer Architecture**
- **Integrated 4 Double Word Write Buffer**
- **16 Byte Line Size**
- **Integrated Intel387™ DX Math Coprocessor and Weitek 3167 Floating Point Coprocessor Decode Logic**
- **Concurrent Line Buffer Cacheing**
- **Multiprocessor Support**
- **Expandable - up to 64KB**
- **Supports Intel486™ Microprocessor-like Burst**
- **Dual Bus Architecture — Snooping Maintains Cache Coherency**
- **20, 25 and 33MHz Clock**
- **196 lead PQFP package**

(See Packaging Handbook Order Number 240800-001, Package Type KU)

The 82395DX High Performance 82395DX Smart Cache is a low cost, high integration, 32-Bit peripheral for Intel's i386™ DX Microprocessor. It stores a copy of frequently accessed code or data from main memory to on chip data RAM that can be accessed in zero wait states. The 82395DX enables the 386 DX Microprocessor to run at near its full potential by reducing the average number of wait states seen by the CPU to nearly zero. The dual bus architecture allows another bus master to access the System Bus while the 386 DX Microprocessor can operate out of the 82395DX's cache on the Local Bus. The 82395DX has a snooping mechanism which maintains cache coherency during these cycles.

The 82395DX is completely software transparent, protecting the integrity of system software. High performance, low cost and board space saving are achieved due to the high integration and new write buffer architecture.



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82395DX Smart Cache

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82395DX
HIGH PERFORMANCE SMART CACHE

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0.0 DESIGNER SUMMARY

0.1 Pin Out

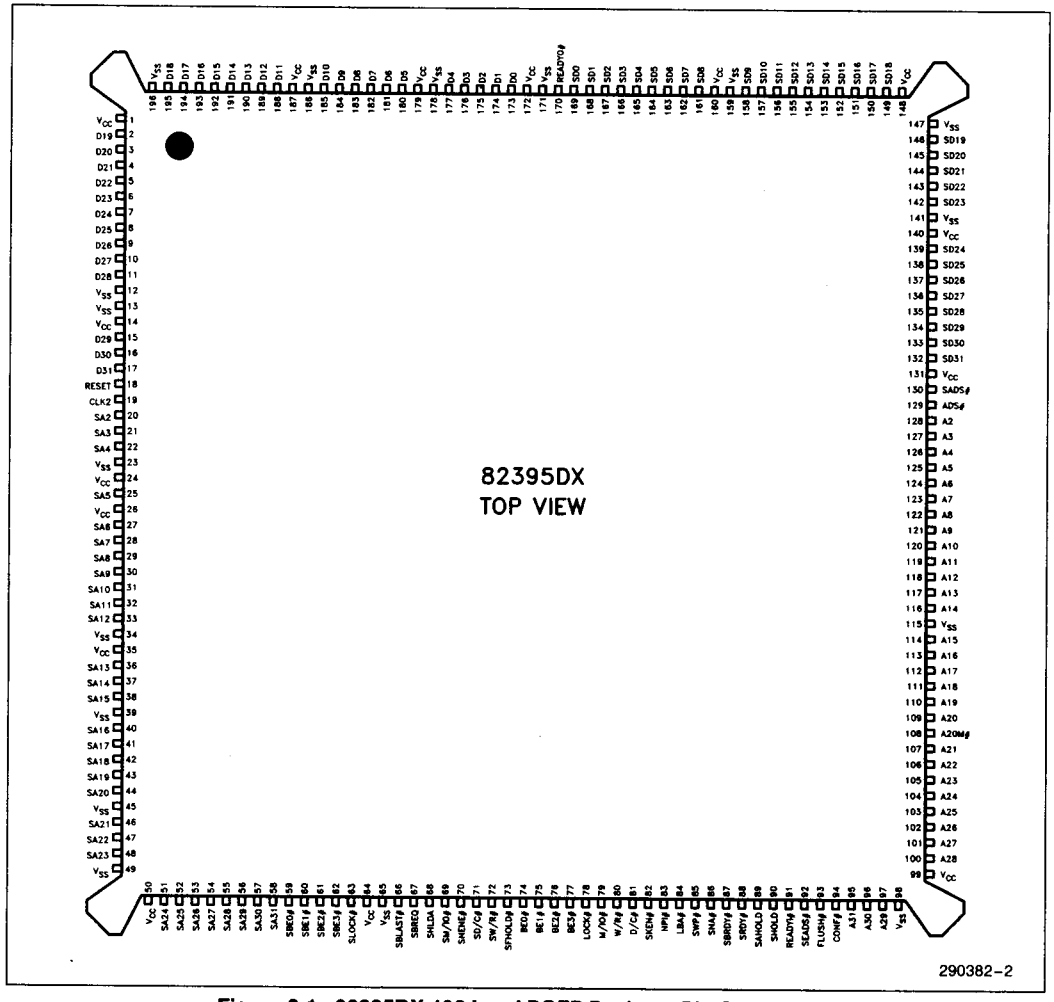

Figure 0.1 - 82385DX 196 Lead PQFP Package Pin Orientation

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VCC	50	VCC	99	VCC	148	VCC
2	D19	51	SA24	100	A28	149	SD18
3	D20	52	SA25	101	A27	150	SD17
4	D21	53	SA26	102	A26	151	SD16
5	D22	54	SA27	103	A25	152	SD15
6	D23	55	SA28	104	A24	153	SD14
7	D24	56	SA29	105	A23	154	SD13
8	D25	57	SA30	106	A22	155	SD12
9	D26	58	SA31	107	A21	156	SD11
10	D27	59	SBE0#	108	A20M#	157	SD10
11	D28	60	SBE1#	109	A20	158	SD9
12	VSS	61	SBE2#	110	A19	159	VSS
13	VSS	62	SBE3#	111	A18	160	VCC
14	VCC	63	SLOCK#	112	A17	161	SD8
15	D29	64	VCC	113	A16	162	SD7
16	D30	65	VSS	114	A15	163	SD6
17	D31	66	SBLAST#	115	VSS	164	SD5
18	RESET	67	SBREQ	116	A14	165	SD4
19	CLK2	68	SHLDA	117	A13	166	SD3
20	SA2	69	SM/IO#	118	A12	167	SD2
21	SA3	70	SNENE#	119	A11	168	SD1
22	SA4	71	SD/C#	120	A10	169	SD0
23	VSS	72	SW/R#	121	A9	170	READY0#
24	VCC	73	SFHOLD#	122	A8	171	VSS
25	SA5	74	BE0#	123	A7	172	VCC
26	VCC	75	BE1#	124	A6	173	D0
27	SA6	76	BE2#	125	A5	174	D1
28	SA7	77	BE3#	126	A4	175	D2
29	SA8	78	LOCK#	127	A3	176	D3
30	SA9	79	M/IO#	128	A2	177	D4
31	SA10	80	W/R#	129	ADS#	178	VSS
32	SA11	81	D/C#	130	SADS#	179	VCC
33	SA12	82	SKEN#	131	VCC	180	D5
34	VSS	83	NPI#	132	SD31	181	D6
35	VCC	84	LBA#	133	SD30	182	D7
36	SA13	85	SWP#	134	SD29	183	D8
37	SA14	86	SNA#	135	SD28	184	D9
38	SA15	87	SBRDY#	136	SD27	185	D10
39	VSS	88	SRDY#	137	SD26	186	VSS
40	SA16	89	SAHOLD	138	SD25	187	VCC
41	SA17	90	SHOLD	139	SD24	188	D11
42	SA18	91	READYI#	140	VCC	189	D12
43	SA19	92	SEADS#	141	VSS	190	D13
44	SA20	93	FLUSH#	142	SD23	191	D14
45	VSS	94	CONF#	143	SD22	192	D15
46	SA21	95	A31	144	SD21	193	D16
47	SA22	96	A30	145	SD20	194	D17
48	SA23	97	A29	146	SD19	195	D18
49	VSS	98	VSS	147	VSS	196	VSS

Table 0.1 - 82395DX 196-Pin PQFP Pin Description

0.2 Quick Pin Reference

What follows is a brief pin description. For more details refer to chapter 3.

Symbol	Type	Function
CLK2	I	This signal provides the fundamental timing for the 82395DX. All external timing parameters are specified with respect to the rising edge of CLK2.
Local Address Bus		
A2-31	I	A2-31 are the Local Bus address lines. These signals along with the byte enable signals, define the physical area of memory or input/output space accessed.
BE0-3#	I	The byte enable signals are used to determine which bytes are accessed in partial cache write cycles. These signals are ignored for Cache Read Hit cycles. For all System Bus memory read cycles (except the last three cycle of a Line Fill), these signals are mirrored by the SBE0-3# signals.
Local Bus Cycle Definition		
W/R# D/C# M/IO#	I I I	The write/read, data/code and memory/input-output signals are the primary bus definition signals directly connected to the 386 DX Microprocessor. They become valid as the ADS# signal is sampled active. The bus definition signals are not driven by the 386 DX Microprocessor during bus hold and follow the timing of the address bus.
LOCK#	I	The Local Bus LOCK# signal indicates that the current bus cycle is LOCK#ed. LOCK#ed cycles are treated as non-cacheable cycles, except that LOCK#ed write hit cycles update the cache.
Local Bus Control		
ADS#	I	The address status pin, an output of the 386 DX Microprocessor, indicates that new and valid information is currently available on the Local Bus. The signals that are valid when ADS# is activated are: A2-31, BE0-3#, W/R#, D/C#, M/IO#, LOCK#, NPI# and LBA#
READYI#	I	This is the READY input signal seen by the Local Bus master. Typically it is a logical OR between the 82395DX generated READYO# and READY# signals generated by other Local Bus masters (optional). It is used by the 82395DX, along with the ADS# signal, to keep track of the 386 DX Microprocessor bus state.
READYO#	I/O	This is the Local Bus READY output that is used to terminate all types of 386 DX Microprocessor bus cycles, except for 386 DX Microprocessor Local Bus cycles which must be terminated by the Local Bus device being accessed. This signal is wired-OR with parallel 82395DX READYO# signals in a multi-82395DX system. The READYO# pin may serve as READY# for the 387 DX Math Coprocessor.
RESET		
RESET	I	The RESET signal forces the 82395DX to begin execution at a known state. The RESET falling edge is used by the 82395DX to set the phase of its internal clock identical to the 386 DX Microprocessors internal clock. RESET falling edge must satisfy the appropriate setup and hold times (T14, T15b) for proper chip operation. RESET must remain active for at least 1ms after the power supply and CLK2 input have reached their proper DC and AC specifications.
Configuration		
CONF#	I	The activity on the CONF# input during and after RESET allows the 82395DX to configure itself to operate in the specified address range. Refer to chapter 4 for 1, 2 or 4 82395DX's operation.

0.2 Quick Pin Reference (Continued)

Symbol	Type	Function
Local Data Bus		
D0–31	I/O	These are the Local Bus data lines of the 82395DX. They must be connected to the D0–31 pins of the 386 DX Microprocessor.
Local Bus Decode Pins		
LBA#	I	This is the Local Bus Access indication. It instructs the 82395DX that the cycle currently in progress is targeted to a Local Bus device. This results in the cycle being ignored by the 82395DX. The 387 DX Math Coprocessor is considered a Local Bus devcie but LBA# need not be generated. If LBA# is asserted at the falling edge of RESET accesses to Weitek 3167 Floating-Point Coprocessor address space are decoded as Local Bus cycles. Note that LBA# cycles have priority over all other cycle types.
NPI#	I	The No Post Input signal instructs the 82395DX that the write cycle currently in progress must not be posted in the write buffer. NPI# is sampled at the falling edge of CLK at the end of T1 (see figure 5.1).
Address Mask		
A20M#	I	Address bit 20 Mask when active, forces the A20 input as seen by the 82395DX to logic "0", regardless of the actual value on the A20 input pin. A20M# emulates the address wraparound at 1 MByte which occurs on the 8086. This pin is asynchronous but must meet setup and hold times (t47 and t48) to guarantee recognition in a specific clock. It must be asserted two clock cycles before ADS# is sampled active (see figure 5.3). It must be stable throughout Local Bus memory cycles.
System Address Bus		
SA2–3 SA4–31	O I/O	These are the System Bus address lines of the 82395DX. When driven by the 82395DX, these signals, along with the System Bus byte enables define the physical area of memory or input/output space being accessed. During bus HOLD or address HOLD, the I/O signals serve as inputs for the cache invalidation cycle.
SB0–3#	O	These are the Byte Enable signals for the System Bus. The 82395DX drives these pins identically to BE0–3# in all System Bus cycles except Line Fills. In Line Fills these signals are driven identically to BE0–3# for the first read cycle of the Line Fill. They are all driven active in the remaining cycles of the Line Fill.
System Bus Cycle Definition		
SW/R# SD/C# SM/IO#	O O O	The System Bus write/read, data/code and memory/input-output signals are the System Bus cycle definition pins. When the 82395DX is the System Bus master, it drives these signals identically to the 386 DX Microprocessor cycle definition encoding.
SLOCK#	O	The System Bus LOCK# signal indicates that the current cycle is LOCK#ed. The 82395DX has exclusive access to the System Bus across bus cycle boundaries until this signal is negated. The 82395DX does not acknowledge a bus HOLD request while this signal is asserted. The 82395DX asserts SLOCK# when the System Bus is available and a LOCK#ed cycle was started on the Local Bus that requires System Bus service. SLOCK# is negated only after completion of all LOCK#ed System Bus cycles and negation of the LOCK# signal.

0.2 Quick Pin Reference (Continued)

Symbol	Type	Function
System Bus Control		
SADS#	O	The System Bus ADdress Status signal is used to indicate that new and valid information is currently being driven onto the System Bus. The signals that are valid when SADS# is driven low are: SA2-31, SBE0-3#, SW/R#, SD/C#, SM/IO# and SLOCK#
SRDY#	I	The System Bus ReaDY# signal indicates that the current System Bus cycle is complete. When SRDY# is sampled asserted it indicates one of two things. In response to a read request it indicates that the external system has presented valid data on the system data bus. In response to a write request it indicates that the external system has accepted the 82395DX's data. This signal is ignored when the System Bus is in STi, STH, ST1 or ST1P states. At the first read cycle of a Line Fill SRDY#, SBRDY# and SNA# determine if the Line Fill will proceed as a burst/non-burst, pipelined/non-pipelined Line Fill. Once a burst Line Fill has started, if SRDY# is returned in the 2nd or 3rd DW, the burst Line Fill will be interrupted and the cache will not be updated. The 1st DW will already have been transferred to the CPU. In the 4th DW of a Line Fill both SRDY# and SBRDY# have the same affect. They indicate the end of the Line Fill.
SNA#	I	The System Bus Next Address signal, when active, indicates that a pipelined address cycle will be executed. It is sampled by the 82395DX at the rising edge of CLK in ST2 and ST1P cycles. If this signal is sampled active then burst Line Fills are disabled. This signal is ignored once a burst Line Fill begins.
Bus Arbitration		
SBREQ	O	The System Bus REQuest signal is the internal cycle pending signal. This indicates to the outside world that internally the 82395DX has generated a bus request (due to the CPU's request that requires access to the System Bus). It is generated whether the 82395DX owns the bus or not and can be used to arbitrate among the various masters on the System Bus. If the bus is available and the cycle starts immediately this signal will not be activated for cache read miss cycles.
SHOLD	I	The System Bus HOLD request indicates that another master must have complete control of the entire System Bus. When SHOLD is sampled asserted the 82395DX completes the current System Bus cycle or sequence of LOCK#ed cycles, before driving SHLDA active. In the same clock that SHLDA went active all the System Bus outpus and I/O pins are floated (with the exception of SHLDA and SBREQ). The 82395DX stays in this state until SHOLD is negated. SHOLD is recognized during RESET.
SHLDA	O	The System Bus HOLD Acknowledge signal is driven active by the 82395DX in response to a hold request. It indicates that the 82395DX has given the bus to another System Bus master. It is driven active in the same clock that the 82395DX floats it's System Bus. When leaving a bus HOLD, SHLDA is driven inactive and the 82395DX resumes driving the bus in the same clock. The 82395DX is able to support CPU Local Bus activities during System Bus HOLD.

0.2 Quick Pin Reference (Continued)

Symbol	Type	Function
Bus Arbitration (Continued)		
SFHOLD#	I	The System Bus Fast HOLD Request signal indicates that another master needs immediate access to the System Bus. In response to SFHOLD# being sampled active, the 82395DX stops driving (in the next clock) the System Bus output and I/O pins (except SHLDA and SBREQ). Because the 82395DX always stops driving the System Bus in response to SFHOLD# active, no acknowledge is required. The System Bus output and I/O pins remain in the high impedance state until SFHOLD# is negated. It is the responsibility of the system designer to guarantee that bus cycles that are in progress when SFHOLD# is asserted are terminated correctly. This pin is recognized during RESET.
Burst Control		
SBRDY#	I	The System Bus Burst ReaDY signal performs the same function during a burst cycle that SRDY# does in a non-burst cycle. SBRDY# asserted indicates that the external system has presented valid data on the data pins in response to a burst Line Fill cycle. This signal is ignored when the System Bus is at STi, STH, ST1 or ST1P states. Note that in the fourth bus cycle of a Line Fill, SBRDY# and SRDY# have the same effect on the 82395DX. They indicate the end of the Line Fill. For all cycles other than burst Line Fills, SBRDY# and SRDY# have the same effect on the 82395DX.
SBLAST#	O	The System Bus Burst LAST cycle indicator signal indicates that the next time SBRDY# is returned the burst cycle is complete. It indicates to the external system that the next SBRDY# returned is treated as a normal SRDY# by the 82395DX. Another set of addresses will be driven with SADS# or the System Bus will go idle. SBLAST# is normally active. In a cache read miss cycle, which may proceed as a Line Fill, SBLAST# starts active. After determining whether or not the cycle is cacheable via SKEN#, SBLAST# is driven inactive. If it is a cacheable cycle, and SBRDY# terminates the first DW of the Line Fill, a burst Line Fill, SBLAST# will be driven active when the data is valid for the fourth DW of the Line Fill. If SRDY# terminates the first DW of the Line Fill, a non-burst Line Fill, SBLAST# is driven active in the cycle where SRDY# was sampled active.
Cache Invalidation		
SAHOLD	I	The System Bus Address HOLD request allows another bus master access to the address bus of the 82395DX. This is to indicate the address of an external cycle for performing an internal cache directory lookup and invalidation cycle. In response to this signal the 82395DX stops driving the System Bus address pins in the next cycle. No HOLD Acknowledge is required. Other System Bus signals can remain active during address hold. The 82395DX does not initiate another bus cycle during address hold. This pin is recognized during RESET.
SEADS#	I	The System Bus External ADress Strobe signal indicates that a valid external address has been driven onto the 82395DX System Bus address pins. This address will be used to perform an internal cache invalidation cycle. The maximum invalidation cycle rate is one every two clock cycles.

0.2 Quick Pin Reference (Continued)

Symbol	Type	Function
Cache Control		
FLUSH#	I	The FLUSH# pin, when sampled active for four clock cycles or more, causes the 82395DX to invalidate its entire TAG array. In addition, it is used to configure the 82395DX to enter various test modes. For details refer to chapter 7. This signal is asynchronous but must meet setup and hold times to guarantee recognition in any specific clock.
System Data Bus		
SD0–31	I/O	The System Bus Data lines of the 82395DX must be driven with appropriate setup and hold times for proper operation. These signals are driven by the 82395DX only during write cycles.
System Bus Decode Pins		
SKEN#	I	The System Cacheability ENable signal is used to determine if the current cycle running on the System Bus is cacheable or not. When the 82395DX generates a read cycle, SKEN# is sampled one clock before the first SBRDY# or SRDY# or one cycle before the first SNA# is sampled active (see chapter 6). If SKEN# is sampled active the cycle will be transformed into a Line Fill. Otherwise, the cache and cache directory will be unaffected. Note that SKEN# is ignored after the first cycle in a Line Fill. SKEN# is ignored for all System Bus cycles except for cache read miss cycles.
SWP#	I	The System Write Protect indicator signal is used to determine whether the current System Bus Line Fill cycle is write protected or not. In non-pipelined cycles, SWP# is sampled with the first SRDY# or SBRDY# of the Line Fill. In pipelined cycles, SWP# is sampled one clock phase after the first SNA# is sampled active (see figures 6.9-10). The Write Protect bit is sampled together with the TAG of each line in the 82395DX Cache Directory. In every cacheable write cycle the Write Protect bit is read. If active, the cycle will be a write protected cycle which is treated like a cacheable write miss cycle. It is buffered and it does not update the cache even if the addressed location is present in the cache.
Design Aides		
SNENE#	O	The System NExt NEar indicator signal indicates that the current System Bus memory cycle is to the same 2048 byte area as the previous memory cycle. Address lines A11–31 of the current System Bus memory cycle are identical to address lines A11–31 of the previous memory cycle. SNENE# can be used in an external DRAM system to run CAS# only cycles, thereby increasing the throughput of the memory system. SNENE# is valid for all memory cycles, and indicates that the current memory cycle is to the same 2048 byte area, even if there were idle or non-memory bus cycles since the last System Bus memory cycle. For the first cycle after the 82395DX has exited the HOLD state, or after SAHOLD was deactivated, this pin will be inactive.

1.0 82395DX FUNCTIONAL OVERVIEW

1.1 Introduction

The primary function of a cache is to provide local storage for frequently accessed memory locations. The cache intercepts memory references and handles them directly without transferring the request to the System Bus. This results in lower traffic on the System Bus and decreases latency on the local bus. This leads to improved performance for a processor on the Local Bus. By providing fast access to frequently used code and data, the cache is able to reduce the average memory access time of the 386 DX Microprocessor based system.

The 82395DX is a single chip cache subsystem specifically designed for use with the 386 DX Microprocessor. The 82395DX integrates 16KB cache, the Cache Directory and the Cache Control Logic onto one chip.

The 82395DX is expandable such that larger cache sizes are supported by cascading 82395DXs. In a single 82395DX system, the 82395DX can map 4 Giga bytes of main memory into a 16KB cache. In the maximum configuration of a four 82395DX system, the 4 Giga bytes of main memory are mapped into a 64KB cache. The cache is unified for code and data and is transparent to application software. The 82395DX provides a cache consistency mechanism which guarantees that the cache has the most recently updated version of the main memory. Consistency support has no performance impact on the 386 DX Microprocessor. Section 1.2 covers all the 82395DX features.

The 82395DX cache architecture is similar to the i486 Microprocessor's on-chip cache. The cache is four Way set associative with Pseudo LRU replacement algorithm. The line size is 16B and a full line is retrieved from the memory every cache miss. A TAG is associated with every 16B line.

The 82395DX architecture allows for cache read hit cycles to run on the Local Bus even when the System Bus is not available. 82395DX incorporates a new write buffer cache architecture, which allows the 386 DX Microprocessor to continue operation without waiting for write cycles to actually update the main memory.

A detailed description of the cache operation and parameters is included in chapter 2.

The 82395DX has an interface to two electrically isolated busses. The interface to the 386 DX Microprocessor bus is referred to as the Local Bus (LB) interface. The interface to the main memory and other system devices is referred to as the 82395DX System Bus (SB) interface. The SB interface emulates the 386 DX Microprocessor. The SB interface, as does the 386 DX Microprocessor, can be pipelined.

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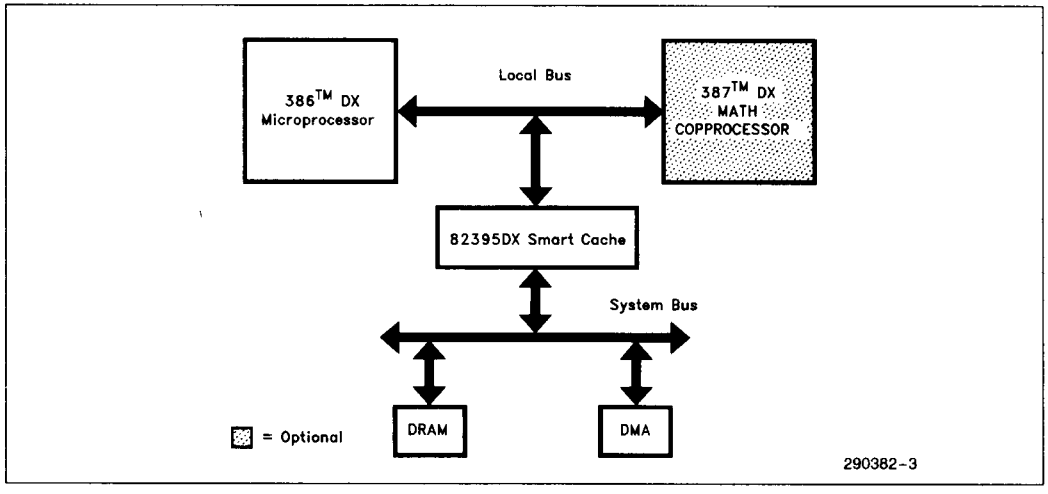


Figure 1.1 - System Block Diagram

In addition, it is enhanced by an optional burst mode for Line Fills. The burst mode provides faster line fills by allowing consecutive read cycles to be executed at a rate of up to one DW per clock cycle. Several bus masters (or several 82395DXs) can share the same System Bus and the arbitration is done via the SHOLD/SHLDA/SBREQ mechanism (similar to the i486 Microprocessor) along with SFHOLD#. Using these arbitration mechanisms, the 82395DX is able to support a multiprocessor system (multi 386 DX Microprocessor/82395DX systems sharing the same memory).

Cache consistency is maintained by the SAHOLD/SEADS# snooping mechanism, similar to the i486 microprocessor. The 82395DX is able to run a zero wait state 386 DX Microprocessor non-pipelined read cycle if the data exists in the cache. Memory write cycles can run with zero wait states if the write buffer is not full.

The 82395DX cache organization provides a higher hit rate than other standard configurations. The 82395DX, featuring the new high performance write buffer cache architecture, provides full concurrency between the electrically isolated Local Bus and System Bus. This allows the 82395DX to service read hit cycles on the Local Bus while running line fills or buffered write cycles on the System Bus. Moreover, the user has the option to expand his cache system up to 64KB.

1.2 Features

1.2.1 82385-LIKE FEATURES

- The 82395DX maps the entire physical address range of the 386 DX Microprocessor (4GB) into 16KB, 32KB, or 64KB cache (with one, two, or four 82395DXs respectively).
- Unified code and data cache.
- Cache attributes are handled by hardware. Thus the 82395DX is transparent to application software. This preserves the integrity of system software and protects the users software investment.
- Double Word, Word and Byte writes, Double Word reads.
- Zero wait states in read hits and in buffered write cycles. All 386 DX Microprocessor cycles are non- pipelined. (Note: The 386 DX Microprocessor must never be pipelined when used with the 82395DX - NA# must be tied to Vcc).
- A hardware cache FLUSH# option. The 82395DX will invalidate all the Tag Valid bits in the Cache Directory and clear the System Bus line buffer when FLUSH# is activated for a minimum of four CLK's. The line buffer is also FLUSH#ed.
- The 82395DX supports non-cacheable accesses. The 82395DX internally decodes the 387 DX Math Coprocessor accesses as Local Bus cycles.
- The system bus interface emulates a 386 DX Microprocessor interface.
- The 82395DX supports pipelined and non-pipelined system interface.
- Provides cache consistency (snooping): The 82395DX monitors the System Bus address via SEADS# and invalidates the cache address if the System Bus address matches a cached location.

1.2.2 NEW FEATURES

- 16KB on chip cache arranged in four banks, one bank for each way. In Read hit cycles, one DW is read. In a write hit cycle, any byte within the DW can be written. In cache fill cycle, the whole line (16B) is written. This large line size increases the hit rate over smaller line size caches.
- Cache architecture similar to the i486 Microprocessor cache: Four Way SET associative with Pseudo LRU replacement algorithm. Line size is 16B and a full line is retrieved from memory for every cache miss. Tag, Tag Valid Bit and Write Protect Bit are associated with every Line.
- New write buffer architecture with four DW deep write buffer provides zero wait state memory write cycles. I/O, Halt/Shutdown and LOCK#ed writes are not buffered.
- Concurrent Line Buffer Cacheing: The 82395DX has a line buffer that is used as additional memory. Before data gets written to the cache memory at the completion of a Line Fill it is stored in this buffer. Cache hit cycles to the line buffer can occur before the line is written to the cache.
- Expandable: two 82395DXs support 32KB cache memory, four 82395DXs support 64KB cache memory. This gives the user the option of configuring a system to meet their own performance requirements.
- In 387 DX Math Coprocessor accesses, the 82395DX drives the READYO# in one wait state if the READYI# was not driven in the previous clock.

  Note that the timing of the 82395's READYO# generation for 387 DX Math Coprocessor cycles is incompatible with 80287 timing.
- The 82395DX optionally decodes CPU accesses to Weitek 3167 Floating-Point Coprocessor address space (C0000000H–C1FFFFFFH) as Local Bus cycles. This option is enabled or disabled according to the LBA# pin value at the falling edge of RESET.

- An enhanced System Bus interface:
  a) Burst option is supported in line-fills similar to the i486 Microprocessor. SBRDY# (System Burst READY) is provided in addition to SRDY#. A burst is always a 16 byte cache update which is equivalent to four DW cycles. The i486 Microprocessor burst order is supported.
  b) System cacheability attribute is provided (SKEN#). SKEN# is used to determine whether the current cycle is cacheable. It is used to qualify Line Fill requests.
  c) SHOLD/SHLDA/SBREQ system bus arbitration mechanism is supported, the same as in the i486 Microprocessor. A Multi 386 DX/82395DX cluster can share the same System Bus via this mechanism.
  d) SNENE# output (Next Near) is provided to simplify the interface to DRAM controllers. DRAM page size of 2K is supported.
  e) Fast HOLD function (SFHOLD#) is provided. This function allows for multiprocessor support.
  f) Cache invalidation cycles supported via SEADS#. This is the mechanism used to provide cache coherency.
- Full Local Bus/System Bus concurrency is attained by:
  a) Servicing cache read hit cycles on the Local Bus while completing a Line Fill on the System Bus. The data requested by the 386 DX Microprocessor was provided over the local bus as the first part of the Line Fill.
  b) Servicing cache read hit cycles on the Local Bus while executing buffered write cycles on the system bus.
  c) Servicing cache read hit cycles on the Local Bus while another bus master is running (DMA, other 386 DX Microprocessor, 82395DX, i486 Microprocessor, etc . . .) on the System Bus.
  d) Buffering write cycles on the Local Bus while the system bus is executing other cycles.
- Write protected areas are supported by the SWP# input. This enables caching of ROM space or shadowed ROM space.
- No Post Input (NPI#) provided for disabling of write buffers per cycle. This option supports memory mapped I/O designs.
- A20M# input provided for emulation of 8086 address wrap-around.
- SRAM test mode, in which the TAGRAM and the cache RAM are treated as standard SRAM, is provided. A Tristate Output test mode is also provided for system debugging. In this mode the 82395DX is isolated from the other devices in the board by floating all its outputs.
- Single chip, 196 lead PQFP package, 1 micron CHMOS-IV technology.

2.0 82395DX CACHE SYSTEM DESCRIPTION

2.1 82395DX Cache Organization

The on chip cache memory is a unified code and data cache. The cache organization is 4 Way SET Associative and each Line is 16 bytes wide (see Figure 2.1). The 16K bytes of cache memory are logically organized as 4 4KB banks (4: 1 bank for each Way). Each bank contains 256 16B lines (256: 1 line for each SET).

The Cache Directory is used to determine whether the data in the cache memory is valid for the address being accessed. The Cache Directory contains 256 TAG's (each TAG is 22-bits wide) for each Way, for a total of 1K TAG's (See Figure 2.2). With each 20 bit TAG Address there is a TAG Valid Bit and a Write Protect bit. The Cache Directory also contains the LRU bits. The LRU bits are used to determine which Way to replace whenever the cache needs to be updated with a new line and all four ways contain data.

Table 2.1 lists the 82395DX cache organization.

Table 2.1 - 82395DX Cache Organization

Cache Element	82395DX Size/Qty	Comments
TAG	1K	Total number of TAGs
SET	256	Cache Directory Offset
LRU	256	3 bits per SET address
Way	4	4 TAG's per SET address
Line Size	16B	4 DW's
Sector Size	16B	4 DW's, one line per sector
Cache Size	16KB	Expandable to 64KB
Cache Directory	—	TAG address, TAG Valid Bit, and Write Protect Bit for each Way for each SET address (256 SET's × 4 Ways), and LRU bits.
TAG Valid Bit	1K	1 for each TAG in the cache directory, indicates valid data is in the cache memory.
Write Protect Bit	1K	1 for each TAG in the cache directory, indicates that the address is write protected.

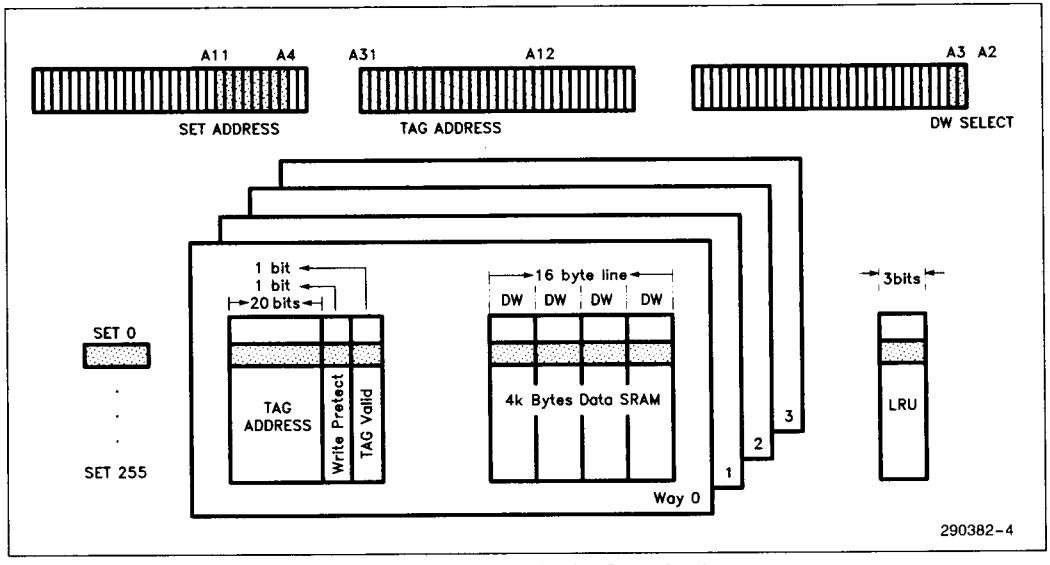


Figure 2.1 - 82395DX Cache Organization

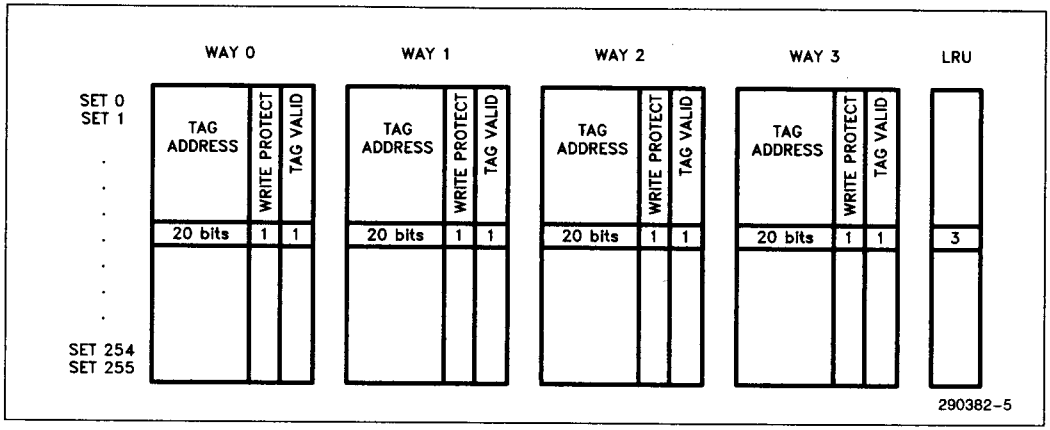


Figure 2.2 - 82395DX Cache Directory Organization

2.1.1 82395DX CACHE STRUCTURE AND TERMINOLOGY

A detailed description of the 82395DX cache parameters are defined here.

A **Line** is the basic unit of data transferred between the cache and main memory. In the 82395DX each Line is 16B. A Line is also known as a transfer block. The decision of a cache "hit or miss" is determined on a per Line basis. A cache hit results when the TAG address of the current address being accessed matches the TAG address in the Cache Directory (see Figure 2.3) and the TAG Valid bit is set. The 82395DX has 1K Lines.

A **TAG** is a storage element of the Cache Directory with which the hit/miss decision is made. The TAG consists of the TAG address (A31–A12), the TAG Valid bit and the Write Protect bit. Since many addresses map to a single line, the TAG is used to determine whether the data associated with the current address is present in the cache memory (a cache hit). This is done through a comparison of the TAG address bits of the current address and the contents of the Cache Directory, along with the TAG Valid bit. Each line in the cache memory has a TAG associated with it.

5

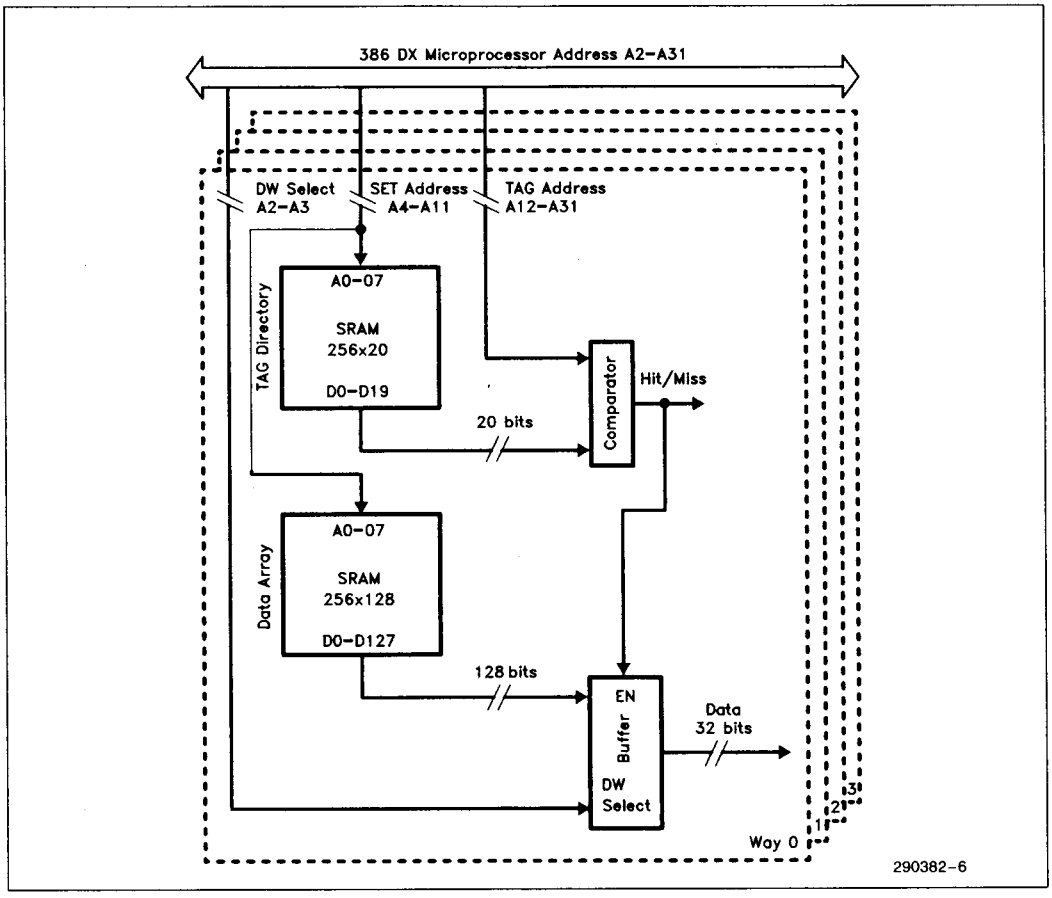


Figure 2.3 - 82395DX Cache Hit Logic

A **TAG Valid Bit** is associated with each TAG address in the Cache Directory. It determines if the data held in the cache memory for the particular TAG address is valid. It is used to determine whether the data in the cache is a match to data in main memory.

A **Write Protect Bit** is also associated with each TAG address in the Cache Directory. This field determines if the cache memory can be written to. It is set by the SWP# pin during Line Fill cycles (see chapter 6).

A **SET** address is a decoded portion of the Local Bus address that maps to 1 TAG address per Way in the Cache Directory. All the TAG's associated with a particular SET are simultaneously compared with the TAG field of the bus address to make the hit/miss decision. The 82395DX provides 256 SET addresses, each SET maps to four lines in the cache memory.

The term **Way** as in 4 Way SET Associative describes the degree of associativity of the cache system. Each Way provides TAG Address, TAG Valid bit, and Write Protect bit storage, 1 entry for each SET address. A simultaneous comparison of one TAG address from each Way with the bus address is done in order to make the hit/miss decision. The 82395DX is 4 Way SET Associative.

Other key 82395DX features include:

Cache Size - The 82395DX contains 16KB of cache memory. This can be expanded by connecting two or four 82395DX's in parallel to get up to 64KB of cache memory. Expanding the cache in this way results in an increased number of Tags with a constant number of lines per Tag. The cache is organized as four banks of 4KB. Each of the four banks corresponds to a particular Way.

Update Policy - The update policy deals with how main memory is updated when a cacheable write cycle is issued on the Local Bus. The 82395DX supports the write buffer policy, similar to the write through policy, which means that main memory is always updated in every write cycle. However, the cache is updated only when the write cycle hits the cache. Also, the 82395DX is able to cache write protected areas, e.g. ROMs, by preventing the cache update if the write cycle hits a write protected line. A write cycle to main memory is buffered as explained in chapter 6.

Replacement - When a new line is needed to update the cache, the Tag Valid bits are checked to see if any of the four ways are available. If they are all valid it is necessary to replace an old line that is already in the cache. In the 82395DX, the Pseudo LRU (least recently used) algorithm is adopted. The Pseudo LRU algorithm targets the least recently used line associated with the SET for replacement. (Pseudo LRU is described in section 2.2.).

Consistency - The 82395DX implements hooks for a consistency mechanism. This is to guarantee that in systems with multiple caches (and/or with multiple bus masters) all processor requests result in returning correct and consistent data. Whenever a system bus master performs memory accesses to data which also exists in the cache, the System Bus master can invalidate that entry in the 82395DX. This invalidation is done by using SEADS# (description in chapter 6).

The invalidation is performed by marking the TAG as invalid (the TAG Valid bit is cleared). Thus, the next time a Local Bus request is made to that location, the 82395DX accesses the main memory to get the most recent copy of the data.

2.2 Pseudo LRU Algorithm

When a line needs to be placed in the internal cache the 82395DX first checks to see if there is a non-valid line in the SET that can be replaced. The validity is checked by looking at the TAG Valid bit. The order that is used for this check is Way 0, Way 1, Way 2, and Way 3. If all four lines associated with the SET are valid, a pseudo Least Recently Used algorithm is used to determine which line will be replaced. If a non-valid line is found, that line is marked for replacement. All the TAG Valid bits are cleared when the 82395DX is RESET or when the cache is FLUSH#ed. Three bits, B0, B1, and B2, are defined for each of the 256 SETs. These bits are called the LRU bits and are stored in the cache directory. The LRU bits are updated for every access to the cache.

If the most recent access to the cache was to Way 0 or Way 1 then B0 is set to 1.

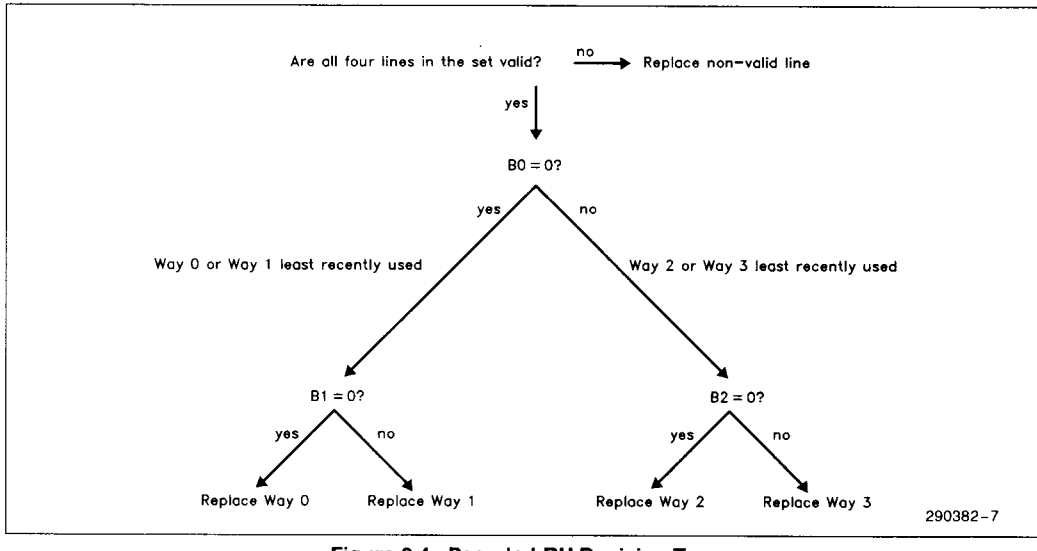


Figure 2.4 - Pseudo LRU Decision Tree

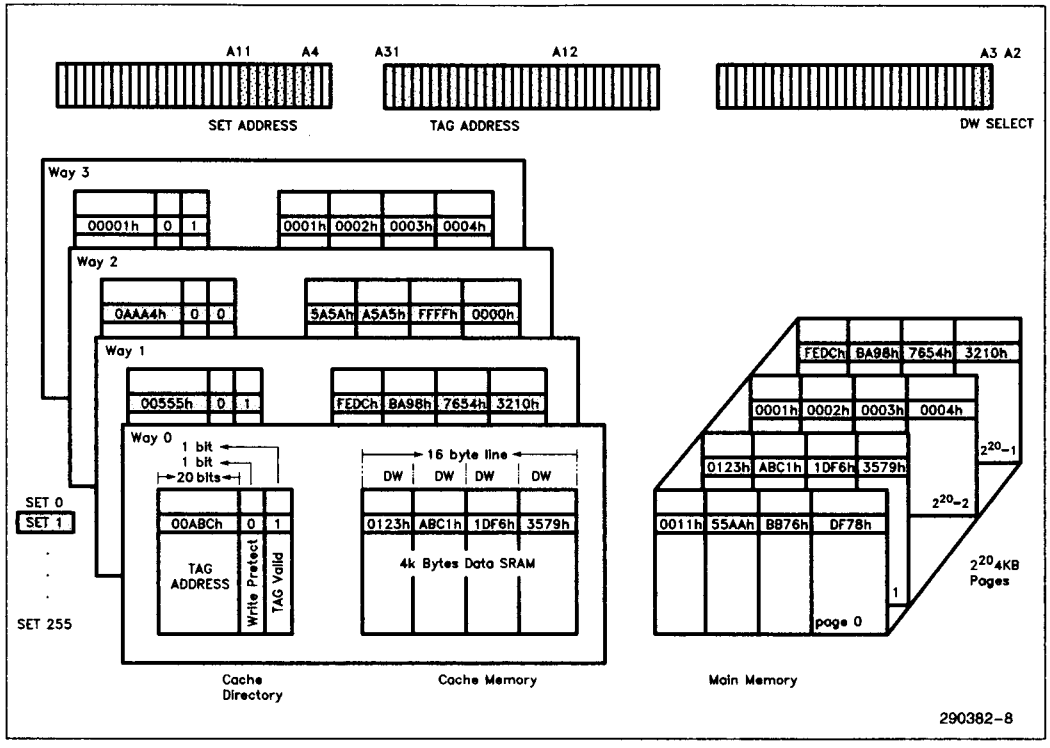


Figure 2.5 - Four Way Set Associative Cache Organization

B0 is set to 0 if the most recent access was to Way 2 or Way 3. If the most recent access to Way 0 or Way 1 was to Way 0, B1 is set to 1. Else B1 is set to 0. If the most recent access to Way 2 or Way 3 was to Way 2, B2 is set to 1. Else B2 is set to 0. See Table 2.2.

The Pseudo LRU algorithm works in the following manner. When a line must be replaced, the cache will first select which of Way 0 and Way 1 or Way 2 and Way 3 was least recently used. Then the cache will select which of the two lines was least recently used and mark it for replacement. The decision tree is shown in Figure 2.4. When the 82395DX is RESET or the cache is FLUSH#ed all the LRU bits are cleared along with the TAG Valid bits.

2.3 Four Way Set Associative Cache Organization

The 82395DX is a four Way SET Associative cache. Figure 2.5 shows the 82395DX's cache organization. For each of the 256 SET's there are four TAG's, one for each Way. The address currently being accessed is decoded into the SET and TAG addresses. If the access was to address 00555004h (SET = 001,TAG = 00555h), the four TAG's in the Cache Directory associated with SET 001 are simultaneously compared with the TAG of the address being accessed. The TAG Valid bits are also checked. If the TAG's match and the TAG Valid bit is set, the access is a hit to the Way where the hit was detected, in this example the hit occurred in Way 1. The data would be retrieved from Way 1 of the cache memory. If the next access was to address 0AAA4007h (SET = 001, TAG = 0AAA4h), the comparison would be done and a TAG match would be found in Way 2. However in this case the TAG Valid bit is cleared so the access is a miss and the data will be retrieved from main memory. The cache memory will also be updated. It is helpful to notice that the main memory is broken into pages by the TAG size. In this case with a 20-bit TAG address there are 2^{20} pages. The smaller the TAG size the fewer pages main memory is broken into. The SET breaks down these memory pages. The larger the SET size the more lines per page.

The following is a description of the interaction between the 386DX Microprocessor, the 82395DXs cache and Cache Directory.

2.3.1 CACHE READ HITS

When the 386 DX Microprocessor initiates a memory read cycle, the 82395DX uses the 8 bit SET address to select 1 of the 256 SET's in the Cache Directory. The four TAG's of this SET are simultaneously compared with address bits A12–A31. The four TAG Valid bits are checked. If any comparison produces a hit the corresponding bank of internal SRAM supplies the 32 bits of data to the 386 DX Microprocessor data bus based on the DW Select bits A2 and A3. The LRU bits are then updated according to the Pseudo LRU algorithm.

2.3.2 CACHE READ MISSES

Like the cache read hit the 82395DX uses the 8 bit SET address to select the 4 TAG's for comparison. If none of these match or if the TAG Valid bit associated with a matching TAG address is cleared the cycle is a miss and the 82395DX retrieves the requested data from main memory. A Line Fill is simultaneously started to read the line of data from system memory and write the line of data into the cache in the Way designated by the LRU bits.

2.3.3 OTHER OPERATIONS THAT AFFECT THE CACHE AND CACHE DIRECTORY

Other operations that affect the cache and Cache Directory include write hits, snoop hits, cache FLUSH#es and 82395DX RESETs. In write hits, the cache is updated along with main memory. The bank that detected the hit is the one that data is written to. The LRU bits are then adjusted according to the Pseudo LRU algorithm. When a cache invalidation cycle occurs (Snoop hit) the tag valid bit is cleared. RESETs and cache FLUSH#es clear all the TAG Valid bits.

2.4 Concurrent Line Buffer Cacheing

This feature of the 82395DX can be broken into two components, Concurrent Line Buffer and Line Buffer Cacheing.

A Concuurent Line Buffer indicates that the DW requested is returned to the 386 DX Microprocessor in the first cycle of a Line Fill. The Local Bus is then free to execute other cycles while the Line Fill is being completed on the System Bus.

Line Buffer Cacheing indicates that the 82395DX serves 386 DX Microprocessor cycles before it updates its Cache Directory. If the 386 DX Microprocessor cycle is to a line which resides in the cache memory, the 82395DX will serve that cycle as a regular cache hit cycle. The cache memory and cache directory are not updated until after the Line Fill is complete (see sections 2.8 and 2.9). The 82395DX keeps the address and data of the retrieved line in an internal buffer, the System Bus line buffer. Any 386 DX Microprocessor read cycle to the same line will be serviced from the line buffer. Until the cache memory and cache directory are updated, any

386 DX Microprocessor read cycle to a Doubleword, which has already been retrieved, will be serviced from the System Bus line buffer. On the other hand, any 386 DX Microprocessor write cycle to the same line will be done to the cache memory after updating the line in the cache. In this case, the write cycle is buffered and the READYO# is activated after updating the line in the cache. However, if the line is Write Protected, the write cycle will be handled as if it is a miss cycle.

A snooping cycle to a line which has not been updated in the cache will invalidate the SB Line Buffer and will prevent the cache update. Also, cache FLUSH will invalidate the buffer. More details about invalidation cycles can be found in chapter 6.

2.5 Cache Control

The cache can be controlled via the SWP# pin. By asserting this pin during the first DW in a Line Fill the 82395DX sets the write protect bit in the Cache Directory making the entry protected from writes.

2.6 Cache Invalidation

Cache invalidation cycles are activated using the SEADS# pin. SAHOLD or SHLDA asserted conditions the 82395DX's system address bus (SA4–SA31) to accept an input. The 82395DX floats its system address bus in the clock immediately after SAHOLD was asserted, or in the clock SHLDA is activated. No address hold acknowledge is required for SAHOLD. SEADS# asserted and the rising edge of CLK2 indicate that the address on the System Bus is valid. SEADS# is not conditioned by SAHOLD or SHLDA being asserted. The 82395DX will read the address and perform an internal cache invalidation cycle to the address indicated. The internal cache invalidation cycle is serviced 1 cycle after SEADS# was sampled active (or 2 cycles after SEADS# was sampled active if there is contention between the Cache Directory Snoop (CDS) cycle and a Cache Directory Lookup (CDL) cycle, see 2.8 and Figure 2.6). To actually invalidate the address the 82395DX clears the tag valid bit.

2.7 Cache Flushing

The user has an option of clearing the cache by activating the FLUSH# input. When sampling the FLUSH# input low for four clocks, the 82395DX resets all the tag valid bits and the LRU bits of the Cache Directory. Thus, all the banks of the cache are invalidated. Also, the SB Line Buffer is invalidated. The FLUSH# input must have at least eight CLK periods in order to be recognized. If FLUSH is activated for longer than four CLKs, the 82395DX will handle all accesses as misses and it will not update the Cache Directory (the Cache Directory will be FLUSH#ed as long as the FLUSH# input is low). The cache is also FLUSH#ed during RESET.

2.8 Cache Directory Accesses and Arbitration

There are five types of accesses to the cache directory. Each access is a one clock cycle:

1) Cache Directory Look-Up
2) Cache Directory Update
3) Cache Directory Snoop
4) Testability Accesses
5) Cache Directory FLUSH#

A description of each of these accesses follows:

1) **Cache Directory Look-up cycle (CDL):** A 386 DX Microprocessor access in which the hit/miss decision is made. The Cache Directory is accessed by the 386 DX Microprocessor address bus directly from the pins. CDL is executed whenever ADS# is activated, in both read and write cycles. The LRU bits are updated in every CDL hit cycle so the accessed "Way" becomes the most recently used. The LRU bits are read in every CDL miss cycle to indicate the "Way" to be updated in the Cache Directory Update cycle. Also, the WP bit is read.
2) **Cache Directory Update cycle (CDU):** A write cycle to the cache directory due to a previous miss. The CDU cycle can be caused by a TAG mismatch (either a Tag Address mismatch or a cleared TAG Valid bit). In both cases, the new TAG is written to the "Way" indicated by the LRU bits read by the previous CDL miss cycle. Also, the TAG Valid bit is turned on and the LRU algorithm is updated so the accessed "Way" becomes the most recently used. The WP bit is written according to the sampled SWP# input. The Cache Directory is accessed by the internally latched 386 DX Microprocessor address bus. Simultaneously with the CDU cycle, the cache memory is updated.
3) **Cache Directory Snooping cycle (CDS):** A Cache Directory look-up cycle initiated by the System Bus, in response to an access to a memory location that is shared with another system master, followed by a conditional invalidation of the TAG Valid bit. If the look-up cycle results in a hit, the corresponding TAG Valid bit in the Way which detected the HIT will be cleared. CDS cycles do not affect the LRU bits. The Cache Directory is accessed by the internally latched System Bus address.

4) **Testability accesses (CDT):** Cache Directory read and write cycles performed in SRAM test mode. During the TEST accesses, 25 bits of each entry (20 for the TAG, one for the TAG Valid BIT, one for the WP bit and 3 for the LRU bits) are read or written. No comparison is done. CDT cycles are used for debugging purposes so CDT cycles do not contend with other cycles.

5) **Cache Directory FLUSH cycle (CDF):** During RESET or as a result of a FLUSH# request generated by activating the FLUSH# input, all the TAG Valid bits and the LRU bits are cleared as well as the Line Buffer. CDF is a one clock cycle if FLUSH# is active for four clocks. If FLUSH# is activated longer, the CDF cycle is N−3 clocks, where N is the number of clocks FLUSH# is activated for. The actual clearing of the valid bits occurs seven clocks after the activation of FLUSH#. Two clocks are for internal synchronization and four for recognizing FLUSH# asserted. It has higher priority than all other cycles. CDF cycle may occur simultaneously with any other cycle but the result is always a FLUSH#ed Cache Directory.

The 82395DX performs the CDL cycle in T1 state. The CDU cycle, in general, is performed in the clock after the last SRDY# or SBRDY# of the Line Fill cycle and the CDS cycle one clock after sampling the SEADS# active (see more details on snooping cycles in chapter 6). Supporting concurrent activities on local and system busses causes CDL cycles to be requested in any clock during the execution with a maximum rate of a CDL cycle every other clock.

The following arbitration mechanism guarantees resolution of any possible contention between CDL, CDU and CDS cycles:

1. The priority order is CDL, CDS and CDU. CDL has the highest priority, CDU has the lowest.
2. In case of simultaneous CDL and CDS cycles, the CDS will be delayed by one clock. So, the maximum latency in executing the invalidation cycle is two clocks after sampling the SEADS# active. Since the maximum rate of each of the CDL and the CDS cycles is one every other clock, the 82395DX is able to interpose the CDL and CDS cycles such that both are serviced. Figure 2.6 clarifies the interposing in the Cache Directory between the 386 DX Microprocessor and the System Bus.
3. CDU cycle is executed in any clock after the last SRDY# or SBRDY# in which neither CDL nor CDS cycles are requested. The worst case is the case where immediately after the read miss, the 386 DX Microprocessor runs consecutive read hits while the System Bus is running invalidation cycles every other clock. In this case, the CDU cycle is postponed until a free clock is inserted, which may occur due to slower look-up rate (in case of read miss, non-cacheable read, etc...), or due to slower SEADS# rate.

   Since every CDU cycle is synchronized with the cache update (CU - writing the retrieved line into the cache), a possible contention on the cache can occur between a cache update cycle and a cache write cycle (CW - cache is written due to a write hit cycle). In this case, the CW cycle is executed, and the CDU and CU cycles are delayed.

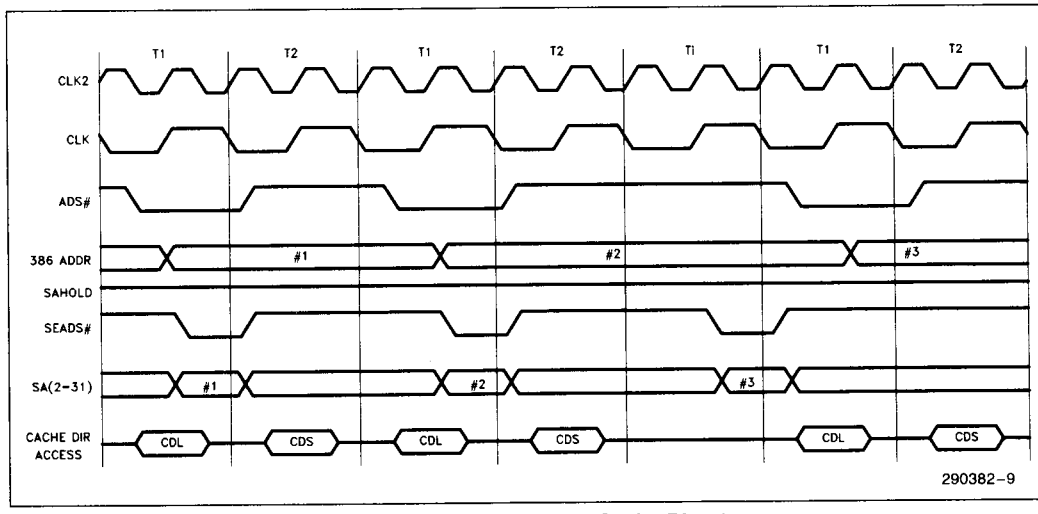


Figure 2.6 - Interposing in the Cache Directory

2.9 Cache Memory Description

The 82395DX cache memory is constructed of four banks, each bank is 1K double words (4KB) and represents a "Way". For example, if the read cycle is to Way 0, bank 0 will be read. The basic cache element is a Line. The cache is able to write a full line or any byte within the line. Reads are done by DW only.

There are four types of accesses to the cache data memory. Each access is a one clock cycle:

1) Cache Read cycle
2) Cache Write cycle
3) Cache Update cycle
4) Testability Access

A description of each type of access follows:

1) **Cache Read cycle (CR):** CR cycle occurs simultaneously with Cache Directory look-up (CDL) cycle if the cycle is a read. In case of a hit, the cache bank in which the hit was detected is read. In CR cycle, the A2–3 address lines select the requested DW within the line.
2) **Cache Write cycle (CW):** CW cycle occurs one clock after the Cache Directory look-up cycle (CDL) if the cycle is a write hit and the WP bit is not set. The cache bank in which the hit was detected is updated. In CW cycle, the A2–3 address lines and the four BE# lines select the required bytes within the line to be written. For all write hit cycles, READYO# is returned simultaneously with the CW cycle unless the write buffer is full. When the write buffer is full the first cycle buffered must be completed on the system bus before READYO# can be asserted.
3) **Cache Update cycle (CU):** CU cycle occurs simultaneously with every Cache Directory update cycle (CDU). The full line is written.
4) **Testability accesses (CT):** cache read and write cycles performed by the 82395DX TEST machine. During the TEST accesses, the cache memory acts as a standard RAM. CT cycles are used for debugging purposes so CT cycles do not contend with other cycles.

The Cache Directory arbitration rules guarantee that contention will not occur in the cache accesses. This is since CR is synchronized with the CDL cycle, CU is synchronized with CDU cycle, CW cannot occur simultaneously with CR cycles (ADS# not activated while READYO# is returned since 386 DX Microprocessor is not pipelined) and finally the possible contention of CW and CU is resolved. See figure 2.7 for an example of Cache Directory and cache memory accesses during a typical cycle execution.

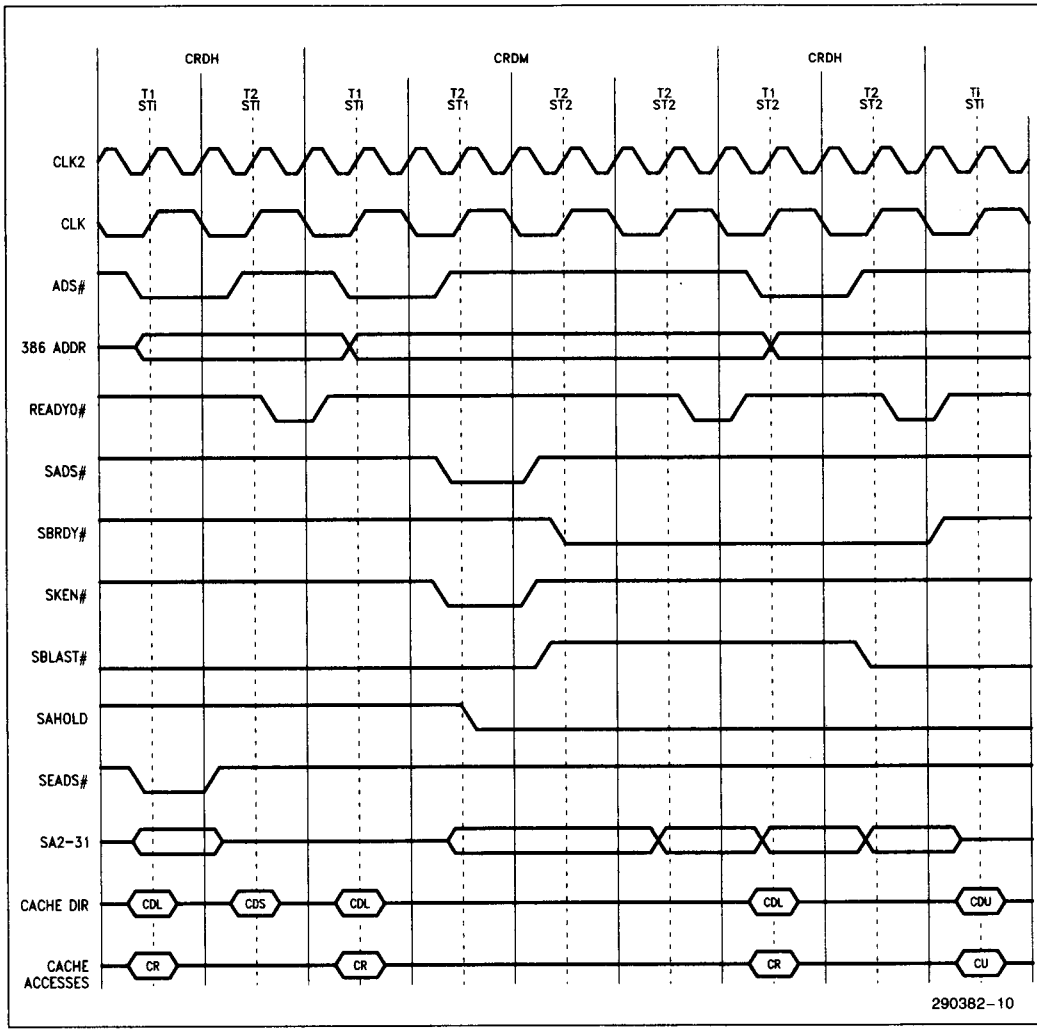


Figure 2.7 - Cache Directory and Cache Accesses

5

3.0 PIN DESCRIPTION

The 82395DX pins may be divided into 4 groups:

1. Local Bus interface pins
2. System Bus interface pins
3. Local Bus decode pins
4. System Bus decode pins

Some notes regarding these groups of pins follow:

1. All Pins - All input and I/O pins (when used as inputs) must be synchronous to CLK2, to guarantee proper operation. Exceptions are the RESET pin, where only the falling edge needs to be synchronous to CLK2, and A20M# and FLUSH# pin, which are asynchronous.
2. Local Bus Interface Pins - All Local Bus interface pins that have a corresponding 386DX Microprocessor signal (A2–31, W/R#, D/C#, M/IO#, LOCK#, and D0–31) must be connected directly to the corresponding 386 DX Microprocessor pins.
3. System Bus Interface Pins - In multi-82395DX mode, all System Bus output and I/O pins are driven by the primary 82395DX, with the exception of SADS#. See chapter 4 for more details.
4. Local / System Bus Decode Pins - These signals are generated by proper decoding of the Local and System Bus addresses. The decoding for the Local Bus decode pins, LBA# and NPI#, must be static. The decoding for the System Bus decode pins, SKEN# and SWP#, must be static over the line boundary. They must not change during a Line Fill. If a change in the decoding of these signals is made, the 82395DX must be FLUSH#ed or RESET.

3.1 Local Bus Interface Pins

3.1.1 386 DX MICROPROCESSOR/82395DX CLOCK (CLK2 I)

This signal provides the fundamental timing for the 82395DX. The 82395DX, like the 386 DX Microprocessor, divides CLK2 by two to generate the internal clock. The phase of the internal 82395DX clock is synchronized to the internal CPU clock phase by the RESET signal. All external timing parameters are specified with respect to CLK2.

3.1.2 LOCAL ADDRESS BUS

3.1.2.1 Local Bus Address Lines (A2–A31 I)

These signals, along with the byte enable signals, define the physical area of memory or I/O accessed.

3.1.2.2 Local Bus Byte Enables (BE3# –BE0# I)

These pins are used to determine which bytes are accessed in partial write cycles. On read-hit cycles these lines are ignored by the 82395DX. On write hit cycles they determine which bytes in the internal Cache SRAM must be updated, and passed to the System Bus along with the System Bus write cycle. In all system bus cycles (non-cacheable reads, read misses and all writes) these signals are mirrored by the SBE0-3# signals. These signals are active LOW.

3.1.3 LOCAL BUS CYCLE DEFINITION

3.1.3.1 Local Bus Cycle Definition Signals (W/R#,D/C#,M/IO# I)

The memory/input-output, data/code, write/read lines are the primary bus definition signals directly connected to the 386 DX Microprocessor. These signals become valid as the ADS# signal is sampled asserted. The bus cycle type encoding is identical to that of the 386 DX Microprocessor. The 386 DX Microprocessor encoding is shown in table 5.1. The bus definition signals are not driven by the 386 DX Microprocessor during bus hold and follow the timing of the address bus.

3.1.3.2 Local Bus Lock (LOCK# I)

This signal indicates a LOCK#ed cycle. LOCK#ed cycles are treated as non-cacheable cycles, except that LOCK#ed write hit cycles update the cache as well. LOCK#ed write cycles are not buffered.

The 82395DX asserts SLOCK# when the first LOCK#ed cycle is initiated on the System Bus. SLOCK# is deactivated only after all LOCK#ed System Bus cycles were executed, and LOCK# was deactivated.

3.1.4 LOCAL BUS CONTROL

3.1.4.1 Address Status (ADS# I)

The address status pin, an output of the 386 DX Microprocessor, indicates that new, valid address and cycle definition information is currently available on the Local Bus. The signals that are valid when ADS# is activated are:

A(2-31), BE(0-3)#, W/R#, D/C#, M/IO#, LOCK#, NPI# and LBA#

3.1.4.2 Local Bus Ready (READYI# I)

This is the ready input signal seen by the local bus master. Typically it is a logical OR between the 82395DX generated READYO# signal and other (optional) READY# signals generated by other Local Bus masters. It is used by the 82395DX, along with the ADS# signal, to keep track of the 386 DX Microprocessor bus state. Do not drive READYI# during T1. Do not delay READYI# from READYO#. (READYI# can be delayed from READYO# as long as the delay does not extend into the next clock cycle.)

3.1.4.3 Local Bus Ready Output (READYO# I/O)

This output is returned to the 386 DX Microprocessor to terminate all types of 386 DX Microprocessor bus cycles, except for Local Bus cycles. This signal is wire-ORed with parallel 82395DX READYO# signals (if more than one 82395DX is used on a 386 DX Microprocessor bus). For more details on READYO# functionality in a multi-82395DX system, refer to Chapter 4.

The READYO# may serve as READY# signal for the 387 DX Math Coprocessor. For details, refer to Chapter 5.

This pin is used during the self configuration sequence, after RESET. For details, refer to Chapter 4.

3.1.5 RESET (RESET I)

This signal forces the 82395DX to begin execution at a known state. RESET falling edge is used by the 82395DX to set the phase of its internal clock identical to the 386 DX Microprocessor internal clock. The RESET falling edge must satisfy the appropriate setup and hold times for proper chip operation. RESET must remain active for at least 1ms after power supply and CLK2 input have reached their proper DC and AC specifications.

The RESET input is used for three purposes: first, it RESETs the 82395DX and brings it to a known state. Second, it is used to synchronize the internal 82395DX clock phase to that of the 386 DX Microprocessor. Third, it initiates a self-configuration sequence in which the 82395DX determines the number of parallel 82395DX devices in the system and it's own configuration (Primary / Secondary and address space).

On power up, RESET must be active for at least 1 millisecond after power has stabilized to a voltage within spec, and after CLK2 input has stabilized to voltage and frequency within spec. This is to allow the internal circuitry to stabilize. Otherwise, RESET must be active for at least 10 clock cycles.

No access to the 82395DX is allowed for 128 clock cycles after the RESET falling edge. During RESET, all other input pins are ignored, except SHOLD, SAHOLD and SFHOLD#. Unlike the 386 DX Microprocessor, the 82395DX can respond to a System Bus HOLD request by floating its bus and asserting SHLDA even while RESET is asserted. Also the 82395DX can respond to a System Bus address HOLD request by floating its address bus. The status of the 82395DX outputs during RESET is shown in Table 3.2.

The 82395DX samples the LBA# pin during RESET and enables the decoding of Weitek 3167 Floating-Point Coprocessor address space if it is sampled low (active).

The user must make sure SAHOLD and FLUSH# are not asserted at the falling edge of RESET. If they are the Tristate Test Mode will be entered. The user must also insure that FLUSH# does not get asserted for one clock cycle while SAHOLD is negated for the same CLK cycle prior to RESET falling. If this condition exists a reserved mode will be entered.

3.1.6 CONFIGURATION (CONF# I)

The activity on this input during and after RESET allows the 82395DX to configure itself to operate in the specified address range.

Refer to Chapter 4 for more details. This pin is active LOW.

5

3.1.7 LOCAL DATA BUS

3.1.7.1 Local Bus Data Lines (D0–D31 I/O)

These are the Local Bus data lines of the 82395DX and must be connected to the D0–D31 signals of the Local Bus.

3.1.8 LOCAL BUS DECODE PINS

These signals are generated by proper decoding of the local bus address. The decoding of these signals must be static, the decoding must not change during normal operation of the 82395DX. If a change in the decoding of these signals is made, the 82395DX must be FLUSH#ed or RESET. These signals must be stable throughout the local bus cycle (refer to Figure 5.1).

3.1.8.1 Local Bus Access Indication (LBA# I)

This signal instructs the 82395DX that the cycle currently in progress is targeted to a Local Bus device, and must therefore be ignored by the 82395DX. The 387 DX Math Coprocessor is considered a Local Bus Device, but LBA# need not be generated for 387 DX Math Coprocessor accesses. Weitek 3167 Floating-Point Coprocessor address space may also be decoded internally as Local Bus cycles. Note that LBA# has priority over all other types of cycles. This signal is active LOW.

3.1.8.2 No Post Input (NPI# I)

This signal instructs the 82395DX that the write cycle currently in progress must not be posted (buffered) in the write buffer. NPI# is sampled on the falling edge of CLK following the address change, see figure 5.1. NPI# is ignored during read cycles. This signal is active LOW.

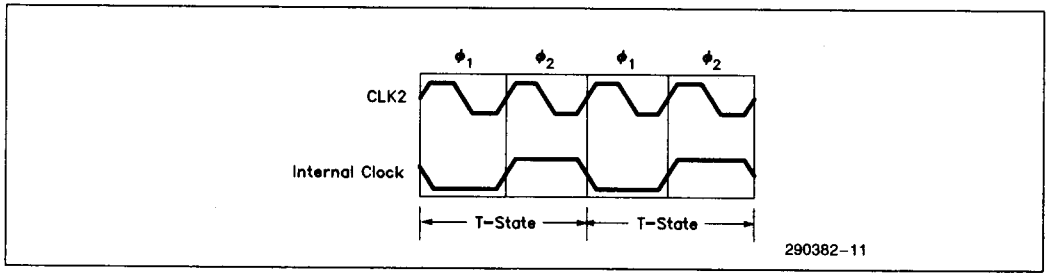


Figure 3.1 - CLK2 and Internal Clock

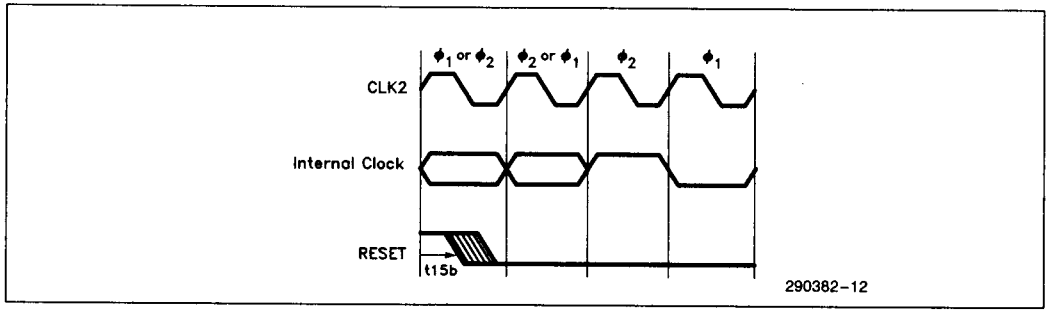


Figure 3.2 - RESET/Internal Phase Relationship

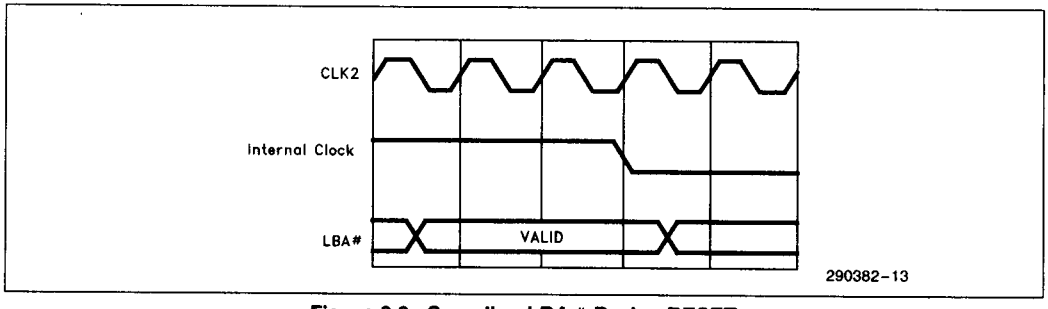


Figure 3.3 - Sampling LBA# During RESET

3.1.9 ADDRESS MASK

3.1.9.1 Address Bit 20 Mask (A20M# I)

This pin, when active (low), forces the A20 input as seen by the 82395DX to logic '0', regardless of the actual value on the A20 input pin. It must be asserted two clock cycles before ADS# for proper operation. A20M# emulates the address wraparound at 1 MByte which occurs on the 8086. This pin is asynchronous but must meet setup and hold times to guarantee recognition in a specific clock. It must be stable throughout Local Bus memory cycles.

3.2 System Bus Interface Pins

3.2.1 SYSTEM ADDRESS BUS

3.2.1.1 System Bus Address Lines (SA2–SA31 I/O *)

* SA2-3 are outputs only.

These are the SYSTEM BUS address lines of the 82395DX. When driven by the 82395DX, these signals, along with the System Bus byte enables define the physical area of memory or I/O accessed.

Activation of SEADS# conditions these signals to serve as inputs for the snooping cycle.

3.2.1.2 System Bus Byte Enables (SBE0#–SBE3# O)

These are the byte enable signals for the System Bus. The 82395DX drives these pins identically to BE0#–BE3# in all System Bus cycles except Line Fills. In Line Fills these signals are driven identically to BE0#–BE3# in the first read cycle of the Line Fill. They are all driven active in the remaining cycles of the Line Fill.

The system memory must ignore these pins during Line Fill, and return all four bytes. These signals are active low.

3.2.2 SYSTEM BUS CYCLE DEFINITION

3.2.2.1 System Bus Cycle Definition (SW/R#,SD/C#,SM/IO# O)

These are the System Bus cycle definition pins. When the 82395DX is the SYSTEM BUS master, it drives these signals identically to the 386 DX Microprocessor encoding.

3.2.2.2 System Bus Lock (SLOCK# O)

The SYSTEM BUS LOCK pin is one of the bus cycle definition pins. It indicates that the current bus cycle is LOCK#ed: that the 82395DX (on behalf of the CPU) must be allowed exclusive access to the System Bus across bus cycle boundaries until this signal is de-asserted. The 82395DX does not acknowledge a bus hold request when this signal is asserted. The 82395DX asserts SLOCK# when the first LOCK#ed cycle is initiated on the System Bus; SLOCK# is deactivated only after all LOCK#ed System Bus cycles were executed, and LOCK# was deactivated. SLOCK# is active LOW.

3.2.3 SYSTEM BUS CONTROL

3.2.3.1 System Bus Address Status (SADS# O)

The address status pin is used to indicate that new, valid address and cycle definition information is currently being driven onto the address, byte enables and cycle definition lines of the System Bus. SADS# can be used as an indication of a new cycle start. SADS# is driven active in the same clock as the addresses are driven. SADS# is not valid until a specified setup time before the CLK falling edge, and must be sampled by CLK falling edge before it is used by the system. This signal is active LOW.

SADS# can float from the active (low) state in pipelined cycles when SFHOLD# is activated in ST2P. SADS# floats from phi2 while being driven from phi1. It is always driven high before it is floated except for when SFHOLD# is asserted in ST2P. Drive SFHOLD# active to the 82395DX only after SADS# has been driven in pipelined cycles or use external latches to drive SADS# after SFHOLD# is deactivated.

3.2.3.2 System Bus Ready (SRDY# I)

The SRDY# signal indicates that the current bus cycle is complete. When SRDY# is sampled asserted it indicates that the external system has presented valid data on the data pins in response to a read cycle or that the external system has accepted the 82395DX data in response to a write request. This signal is ignored when the SYSTEM BUS is at STi, STH, ST1 or ST1P states.

At the first read cycle of a Line Fill, if SBRDY# is returned active and both SRDY# and SNA# are returned inactive, a burst Line Fill will be executed. If SRDY# is returned active and SNA# is returned inactive, a non-burst non-pipelined Line Fill will be executed. If SNA# is returned active and SRDY# is inactive, a non-burst pipelined line fill will be executed.

Once a burst Line Fill has started, if SRDY# is returned in the second or third DW of the transfer, the burst Line Fill will be interrupted and the cache will not be updated. The first DW will already have been transferred to the CPU. Note that in the last (fourth) bus cycle in a Line Fill, SBRDY# and SRDY# have the same effect on the 82395DX. They indicate the end of the Line Fill. This signal is active LOW.

3.2.3.3 System Bus Next Address (SNA# I)

This input, when active, indicates that a pipelined address cycle can be executed. It is sampled by the 82395DX in the same timing as the 386 DX Microprocessor samples NA#. If this signal is sampled active, then SBRDY# is treated as SRDY#, i.e. burst Line Fill is disabled. This signal is ignored once a burst Line Fill has started, as well as during the fourth DW of a Line Fill.

3.2.4 BUS ARBITRATION

3.2.4.1 System Bus Request (SBREQ O)

SBREQ is the internal cycle pending signal. This indicates to the outside world that internally the 82395DX has generated a bus request (due to a CPU's request that requires access to the System Bus). It is generated whether the 82395DX owns the bus or not and can be used to arbitrate among the various masters on the system bus. In read misses, if the bus is available and the cycle starts immediately, this signal will not be activated at all. This signal is active HIGH.

3.2.4.2 System Bus Hold Request (SHOLD I)

This signal allows another bus master complete control of the entire System Bus. In response to this pin, the 82395DX floats all its system bus interface output and input/output pins (With the exception of SHLDA and SBREQ) and asserts SHLDA after completing its current bus cycle or sequence of LOCK#ed cycles. The 82395DX maintains its bus in this state until SHOLD is deasserted. SHOLD is active HIGH. SHOLD is recognized during reset.

3.2.4.3 System Bus Hold Acknowledge (SHLDA O)

This signal goes active in response to a hold request presented on the SHOLD pin and indicates that the 82395DX has given the bus to another System Bus master. It is driven active in the same clock that the 82395DX floats its bus. When leaving a bus hold, SHLDA is driven inactive in one clock and the 82395DX resumes driving the bus. Depending on internal requests the 82395DX may, or may not begin a System Bus cycle in the clock where SHLDA is driven inactive. The 82395DX is able to support CPU Local Bus activities during System Bus hold, since the internal cache is able to satisfy the majority of those requests. This signal is active HIGH.

3.2.4.4 System Bus Fast Hold Request (SFHOLD# I)

This input allows another bus master immediate access to the System Bus. In response to this signal, the 82395DX stops driving the System Bus output and input/output pins (with the exception of SHLDA and SBREQ) in the next CLK cycle. Note that the same signals are tristated in response to a SHOLD request. Because the 82395DX always stops driving the System Bus in response to SFHOLD# active, no acknowledge is needed.

The bus remains in the high impedance state until SFHOLD# is negated.

Note that SRDY# is internally inactivated during SFHOLD# cycles. The only affect of SFHOLD# being asserted is forcing the System Bus output and I/O buffers into their high impedance state. It is the responsibility of the system designer to guarantee that bus cycles which are in progress when SFHOLD# is asserted are terminated correctly.

This pin is recognized during RESET and is active low.

3.2.5 BURST CONTROL

3.2.5.1 System Bus Burst Ready (SBRDY# I)

This signal performs the same function during a burst cycle that SRDY# does in a non-burst cycle. SBRDY# asserted indicates that the external system has presented valid data on the data pins in response to a burst Line Fill cycle. This signal is ignored when the SYSTEM BUS is at STi, STH, ST1 or ST1P states.

Note that in the last (fourth) bus cycle in a Line Fill, SBRDY# and SRDY# have the same effect on the 82395DX. They indicate the end of the Line Fill. For all cycles that cannot run in burst, e.g. noncacheable cycles, non Line Fill cycles (or pipelined Line Fill), SBRDY# has the same effect on the 82395DX as the normal SRDY# pin. This signal is active LOW.

3.2.5.2 System Bus Burst Last Cycle Indicator (SBLAST# O)

The system burst last cycle signal indicates that the next time SBRDY# is returned the burst transfer is complete. In other words, it indicates to the external

system that the next SBRDY# returned is treated as a normal SRDY# by the 82395DX, i.e., another set of addresses will be driven with SADS# or the System Bus will go idle. SBLAST# is normally active. In a cache read miss cycle, which may proceed as a Line Fill, SBLAST# starts active and later follows SKEN# by one clock. SBLAST# is active during non-burst Line Fill cycles. Refer to Chapter 6 for more details. This signal is active LOW.

3.2.6 CACHE INVALIDATION

3.2.6.1 System Bus Address Hold (SAHOLD I)

This is the Address Hold request. It allows another bus master access to the address bus of the 82395DX in order to indicate the address of an external cycle for performing an internal Cache Directory lookup and invalidation cycle. In response to this signal, the 82395DX immediately (in the next cycle) stops driving the entire system address bus (SA2–SA31). Because the 82395DX always stops driving the address bus, in response to system bus address hold request, no hold acknowledge is required. Only the address bus will be floated during address hold, other signals can remain active. For example, data can be returned for a previously specified bus cycle during address hold. The 82395DX does not initiate another bus cycle during address hold.

This pin is recognized during RESET. However, since the entire cache is invalidated by reset, any invalidation cycles run will be superfluous. This signal is active high.

3.2.6.2 System Bus External Address Strobe (SEADS# I)

This signal indicates that a valid external address has been driven onto the 82395DX pins and that this address must be used to perform an internal cache invalidation cycle. Maximum allowed invalidation cycle rate is one every two clock cycles. This signal is active low.

3.2.7 CACHE CONTROL

3.2.7.1 Flush (FLUSH# I)

This pin, when sampled active for four clock cycles or more, causes the 82395DX to invalidate its entire Tag Array. In addition, it is used to configure the 82395DX to enter various test modes. For details refer to Chapter 7. This pin is asynchronous but must meet setup and hold times to guarantee recognition in any specific clock. This signal is active LOW.

3.2.8 SYSTEM DATA BUS

3.2.8.1 System Bus Data Lines (SD0–SD31 I/O)

These are the System Bus data lines of the 82395DX. The lines must be driven with appropriate setup and hold times for proper operation. These signals are driven by the 82395DX only during write cycles.

3.2.9 SYSTEM BUS DECODE PINS

3.2.9.1 System Cacheability Enable (SKEN# I)

This is the cache enable pin. It is used to determine whether the current cycle running on the System Bus is cacheable or not. When the 82395DX generates a read cycle that may be cached, this pin is sampled 1 CLK before the first SBRDY#, SRDY# or SNA# is sampled active (for detailed timing description, refer to Chapter 6). If sampled active, the cycle will be transformed into a Line Fill. Otherwise, the Cache and Cache Directory will be unaffected. Note that SKEN# is ignored after the first cycle in a Line Fill. SKEN# is ignored during all System Bus cycles except for cacheable read miss cycles. This signal is active LOW.

3.2.9.2 System Write Protect Indication (SWP# I)

This is the write protect indicator pin. It is used to determine whether the address of the current system bus Line Fill cycle is write protected or not.

In non-pipelined cycles, the SWP# is sampled with the first SRDY# or SBRDY# of a system Line Fill cycle. In pipelined cycles, SWP# is sampled at the last ST2 stage, or at ST1P; in other words, one clock phase after SNA# is sampled active.

The write protect indicator is sampled together with the TAG address of each line in the 82395DX Cache Directory. In every cacheable write cycle, the write protect indicator is read. If active, the cycle will be a Write Protected cycle which is treated like a cacheable write miss cycle. It is buffered and it does not update the cache even if the addressed location is present in the cache. The signal is active LOW.

3.2.10 DESIGN AIDES

3.2.10.1 System Next Near Indication (SNENE# O)

This signal indicates that the current System Bus memory cycle is to the same 2048 Byte area as the

previous memory cycle. Address lines A11–A31 of the current System Bus memory cycle are identical to the address lines A11–A31 of the previous memory cycle.

This signal can be used in an external DRAM system to run CAS# only cycles, therefore increasing the throughput of the memory system. SNENE# is valid for all memory cycles, and indicates that the current memory cycle is to the same 2048 Byte area, even if there were idle or non-memory bus cycles since the last System Bus memory cycle.

For the first memory cycle after the 82395DX has exited the HOLD state, or after SAHOLD was deactivated, this pin will be inactive. This signal is active low.

3.3 Pinout Summary Tables

Table 3.1 - Input Pins

Name	Function	Synchronous/ Asynchronous	Active Level
CLK2	Clock		
RESET	Reset	Asynchronous*	High
BE0–3#	Local Bus Byte Enables	Synchronous	Low
A2–31	Local Bus Address Lines	Synchronous	—
W/R#	Local Bus Write/Read	Synchronous	—
D/C#	Local Bus Data/Control	Synchronous	—
M/IO#	Local Bus Memory/Input-Output	Synchronous	—
LOCK#	Local Bus LOCK	Synchronous	Low
ADS#	Local Bus Address Strobe	Synchronous	Low
READYI#	Local Bus READY	Synchronous	Low
LBA#	Local Bus Access Indication	Synchronous	Low
NPI#	No Post Input	Synchronous	Low
FLUSH#	FLUSH the 82395DX Cache	Asynchronous	Low
A20M#	Address Bit 20 Mask	Asynchronous	Low
CONF#	Configuration	Synchronous	Low
SHOLD	System Bus Hold Request	Synchronous	High
SRDY#	System Bus READY	Synchronous	Low
SNA#	System Bus Next Address Indication	Synchronous	Low
SBRDY#	System Bus Burst Ready	Synchronous	Low
SKEN#	System Cacheability Indication	Synchronous	Low
SWP#	System Write Protect Indication	Synchronous	Low
SAHOLD	System Bus Address HOLD	Synchronous	High
SEADS#	System Bus External Address Strobe	Synchronous	Low
SFHOLD#	System Bus Fast HOLD Request	Synchronous	Low

* The falling edge of RESET needs to be synchronous to CLK2 but the rising edge is asynchronous.

Table 3.2 - Output Pins

Name	Function	When Floated	State at RESET	Active Level
SBE0–3#	System Bus Byte Enables	SHLDA/SFHOLD#	Low	Low
SADS#	System Bus Address Strobe (1)	SHLDA/SFHOLD#	High	Low
SD/C#	System Bus Data/Control	SHLDA/SFHOLD#	High	—
SM/IO#	System Bus Memory/Input-Output	SHLDA/SFHOLD#	Low	—
SW/R#	System Bus Write/Read	SHLDA/SFHOLD#	Low	—
SHLDA	System Bus HOLD Acknowledge	—	Low (2)	High
SBREQ	System Bus Request	—	Low	High
SLOCK#	System Bus LOCK	SHLDA/SFHOLD#	High	Low
SBLAST#	System Bus Burst Last Cycle Indication	SHLDA/SFHOLD#	Low	Low
SA2–3	System Bus Address (2 lowest order bits)	SHLDA/SAHOLD/ SFHOLD#	High	—
SNENE#	System Bus Next Near Indication	SHLDA/SFHOLD#	High	Low

NOTES:
1. SADS# is driven active in ST1/ST2P and inactive for one phase in the first ST2/ST1P following the activation. SADS# is driven high before it is floated.
2. Unless SHOLD is asserted

Table 3.3 - Input-Output Pins

Name	Function	When Floated	State(1) at RESET	Active Level
D0–31	Local Data Bus (2)	Always Except READs	z	—
SD0–31	System Data Bus	Always Except WRITEs	z	—
SA4–31	System Bus Address (except the 2 lowest order bits)	SHLDA/SAHOLD/ SFHOLD#	High	—
READYO#	Local Bus READY	See Sec 4.6	High	Low

(1) Provided SHOLD, SAHOLD, and SFHOLD# are inactive
(2) Local Data is driven only in T2.

5

4.0 BASIC FUNCTIONAL DESCRIPTION

The 82395DX has an interface to the 386 DX Microprocessor (Local Bus) and to the System Bus. The System Bus interface emulates the 386 DX Microprocessor bus such that the system will view the 82395DX as the front end of a 386 DX Microprocessor. Some optional enhancements, like burst support, are provided to maximize the performance.

When ADS# is sampled active, the 82395DX decodes the 386 DX Microprocessor cycle definition signals (M/IO#, D/C#, W/R# and LOCK#), as well as two Local Bus decode signals (LBA# and NPI#), to determine how to respond. LBA# indicates that the current cycle is addressed to a Local Bus device; NPI# indicates that the current memory write cycle must not be buffered. In addition, the 82395DX internally decodes the 386 DX Microprocessor accesses to the 387 DX Math Coprocessor / Weitek 3167 Floating-Point Coprocessor as Local Bus accesses. The result of the address, cycle definition and cycle qualification decoding is two categories of accesses, the Local Bus accesses (LBA# active or 387 DX Math Coprocessor / Weitek 3167 Floating-Point Coprocessor accesses) and 82395DX accesses. In 387 DX Math Coprocessor accesses, the 82395DX drives the READYO# signal active after one wait state, if the READYI# was not sampled active. Local Bus accesses are ignored by the 82395DX.

Any 82395DX access can be either to a cacheable address or to a non-cacheable address. Non-cacheable addresses are all I/O and system accesses with SKEN# returned inactive. Non-cacheable cycles are all cycles to non-cacheable addresses, LOCK#ed read cycles and Halt/Shutdown cycles. All other cycles are cacheable. For more details about non-cacheable cycles, refer to section 4.2. Non-cacheable cycles pass through the cache. They are always forwarded to the System Bus.

Cacheable read cycles can be either hit or miss. Cacheable read hit cycles are serviced by the internal cache and they don't require System Bus service. A cacheable read miss cycle generates a series of four System Bus read cycles, called a Line Fill. Of

the four cycles, the first cycle is for reading the requested data while all four are for filling the cache line. The System Bus has the ability to provide the system cacheability attribute to the 82395DX Line Fill request, via the SKEN# input, and the system write protection indicator, via the SWP# input. Refer to chapter 6 for more information about Line Fill cycles.

Cacheable write cycles, as any write cycles, are forwarded to the system bus. The write buffer algorithm terminates the write cycle on the Local Bus, allowing the 386 DX Microprocessor to continue processing in 0 wait states, while the 82395DX executes the write cycles on the System Bus. All cacheable write hit cycles, except protected writes, update the cache in a byte basis i.e. only the selected bytes are updated. Cacheable write misses do not update the cache (the 82395DX does not allocate on writes). All cacheable write cycles, except LOCK#ed writes, are buffered (unless NPI# pin is sampled active).

Cache consistency is provided by the SAHOLD, SEADS# mechanism. If any bus master performs a memory cycle which disturbs the data consistency, the address of this cycle must be provided to the 82395DX using the SAHOLD, SEADS# mechanism. Then, the 82395DX checks if that memory location resides in the cache. If it does, the 82395DX invalidates that line in the cache by marking it as invalid in the Cache Directory. The 82395DX interposes the Cache Directory between the 386DX Microprocessor and the System Bus such that the 386 DX Microprocessor is not forced to wait due to snooping and none of the snooping cycles are missed due to 386 DX Microprocessor accesses (see figure 2.6). Cacheability is resolved on the system side using the SKEN# input. SKEN# is sampled one clock before the first SRDY#/SBRDY# in nonpipelined Line Fill cycles. In pipelined Line Fill cycles, SKEN# is sampled one clock phase before sampling SNA# active. SKEN# is always sampled at PHI1.

Note that the 82395DX does not support pipelining of the 386DX Microprocessor Local Bus. The NA# input on the 386 DX Microprocessor must be tied to Vcc.

4.1 Cacheable Accesses

In a cacheable access, the 82395DX performs a cache directory look-up cycle. This is to determine if the requested data exists in the cache and to read the write protection bit. In parallel, the 82395DX performs a cache read cycle if the access is a read, or prepares the cache for a write cycle if the access is a write.

4.1.1 CACHEABLE READ HIT ACCESSES

If the Cache Directory look-up for a cacheable read access results in a hit (the requested data exists in the cache), the 82395DX drives the local data bus by the data provided from the internal cache. It also drives the 386DX Microprocessor READY# (by activating the 82395DX READYO#), so that the 386 DX Microprocessor gets the required data directly from the cache without any wait states.

The 82395DX is a four Way SET associative cache, so only one of the four ways (four banks) is selected to supply data to the 386 DX Microprocessor. The Way in which the hit occurred will provide the data. Also, the replacement algorithm (LRU) is updated such that the Way in which the hit occurred is marked as the most recently used.

4.1.2 CACHEABLE READ MISS ACCESSES

READYO# is always activated in the first T2 of cache read miss cycles. In order to meet the timing requirements READYO# must be activated prior to the hit/miss decision. Once the hit/miss decision is made and the cycle is a miss, READYO# is deactivated. This activation only occurs prior to the max valid delay specification (t20 max). After the max valid delay spec, READYO# will always be stable. See Figure 4.0. READYO# must not be sent to any edge triggered logic.

If the Cache Directory look-up results in a miss, the 82395DX transfers the request to the System Bus in order to read the data from the main memory and for

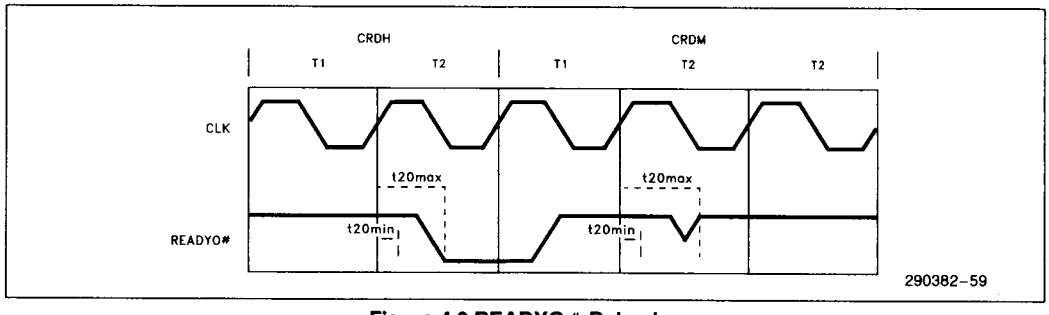


Figure 4.0 READYO# Behavior

updating the cache. A full line is updated in cache update cycle. As a result of a cache miss, the 82395DX performs four System Bus accesses to read four DWs from the DRAM, and write the four DWs to the cache. This is called a Line Fill cycle. The first DW accessed in a Line Fill cycle is for the DW which the 386 DX Microprocessor requested and the 82395DX provides the data and drives the READYO# one clock after it gets the first DW from the SB.

The 82395DX provides the option of supporting burst bus in order to minimize the latency of a line fill. Also, the 82395DX provides the SKEN# input, which, if inactive, converts a Line Fill cycle to a non-cacheable cycle. Write protection is also provided. The write protection indicator is stored together with the TAG Valid bit and the TAG field of every line in the Cache Directory. For more details refer to chapter 6.

The 82395DX features Line Buffer cacheing. In a Line Fill the data for the four DWs is stored in a buffer, the Line Buffer, as it is accumulated. After filling the Line Buffer, the 82395DX performs the Cache Update and the Cache Directory Update. The updated Way is the least recently used Way flagged by the Pseudo LRU algorithm during the Cache Directory Lookup cycle, if all the Ways are valid. If there is a non-valid Way it will be updated.

The SRDY# (System Bus READY#) active indicates the completion of the system bus cycle and SBRDY# (System Bus Burst READY#) active indicates the completion of a burst System Bus cycle. In a 386 DXMicroprocessor-like system, the 82395DX drives the 386 DX Microprocessor READY# one clock after the first SRDY# and, in a burst system, one clock after the first SBRDY#. This frees up the Local Bus, allowing the 386 DX Microprocessor to execute the next instruction, while filling the cache.

So, during Line Fills, there is no advantage in driving the 386 DX Microprocessor into the pipelined mode. **Therefore, the 82395DX does not drive the 386 DX Microprocessor's NA# at all. NA# must be tied to VCC.**

4.1.2.1 Burst Bus

The 82395DX offers an option to minimize the latency in Line Fills. This option is the burst bus and is only applicable to Line Fill cycles. By generation of a burst bus compatible DRAM controller, one which generates SBRDY# and SBLAST# to take advantage of the 82395DX's burst feature, the number of cycles required for a Line Fill to be completed is significantly reduced. Details of burst Line Fills can be found in chapter 6. The burst feature uses the i486 Microprocessor burst order to fill the 16 byte cache line (see Table 6.1).

4.1.3 CACHE WRITE ACCESSES

The 82395DX supports the write buffer policy, which means that main memory is always updated in any write cycle. However, the cache is updated only when the write cycle hits the cache and the accessed address is not write protected. In cache write misses, the cache is not updated (allocation in writes is not supported).

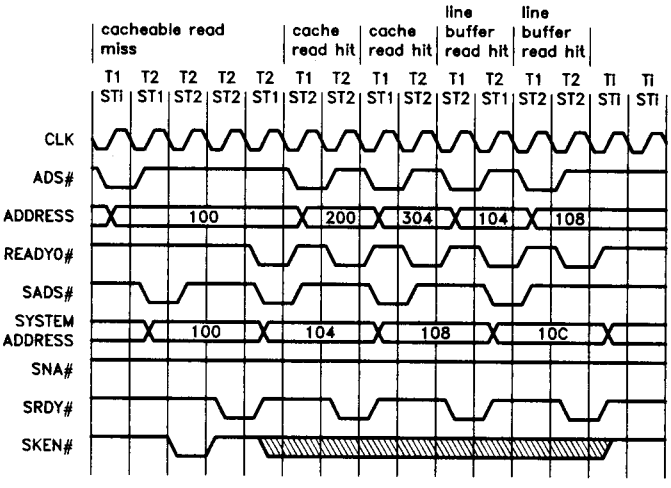
The 82395DX has a write buffer of four DWs. Only the cacheable write cycles, except LOCKed writes, are buffered so, if the write buffer is not full, the 82395DX buffers the cycle. This means that the data, address and cycle definition signals are written in one entry of the write buffer and the 82395DX drives the READYO# in the first T2 so all the buffered write cycles run without wait states. If the write buffer is full, the 82395DX delays the READYO# until the completion of the execution of the first buffered write cycle. The execution of the buffered write cycles depends on the availability of the System Bus. In non-buffered write cycles, e.g. I/O writes, the 386 DX Microprocessor is forced to wait until the execution of all the buffered writes and the non-buffered write (READYO# is driven one clock after the SRDY# of the non-buffered write). More details about the write buffer can be found in chapter 6.

In cacheable non-write protected write hit cycles, only the appropriate bytes within the line are updated. The updated bytes are selected by decoding the A2, A3 and the four BE# lines. The LRU is updated so that the hit Way is the most recently used, as in cache read hit cycles.

All cacheable writes, whether hits or misses, are executed on the system bus. The System Bus write cycle address, data and cycle definition signals are the same as the 386 DX Microprocessor signals. All buffered writes run with zero wait states if the write buffer is not full.

Table 4.1 - 386 DX Microprocessor Bus Cycle Definition with Cacheability

M/IO#	D/C#	W/R#	386 DX Microprocessor Cycle Definition	Cacheable/ Non-cacheable	Writes Posted
0	0	0	Interrupt Acknowledge	Non-cacheable	—
0	0	1	Undefined	—	—
0	1	0	I/O Read	Non-cacheable	—
0	1	1	I/O Write	Non-cacheable	No
1	0	0	Memory Code Read	Cacheable	—
1	0	1	Halt/Shutdown	Non-cacheable	—
1	1	0	Memory Data Read	Cacheable	—
1	1	1	Memory Data Write	Cacheable	Yes



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NOTE:
The second and third reads are to a different line and are serviced from the cache while the fourth and fifth reads are to the same line and are serviced from the line buffer.

Figure 4.1 - Read Hit Cycles During a Line Fill

4.2 Noncacheable System Bus Accesses

Non-cacheable cycles are any of the following 82395DX cycles:

1) All I/O cycles.
2) All LOCKed read cycles.
3) Halt/Shutdown cycles.
4) SRAM mode cycles not addressing the internal cache or Tagram.

All the above cycles are defined as non-cacheable by the Local Bus interface controller. In addition, Line Fill cycles in which the SKEN# signal was returned inactive are aborted. They are called Aborted Line Fills (ALF).

Non-cacheable cycles are never serviced from the cache and they don't update the cache. They are always referred to the System Bus. In non-cacheable cycles, the 82395DX transfers to the System Bus the exact 386 DX Microprocessor bus cycle.

Description of LOCKed cycles can be found in chapter 5.

4.3 Local and System Bus Concurrency

Concurrency between local and System Busses is supported in several cases:

1. Read hit cycles can run while executing a Line Fill on the System Bus. Refer to timing diagram 4.1.
2. Read hit cycles can run while executing buffered write cycles on System Bus. Refer to timing diagram 4.2.
3. Write cycles are buffered while the System Bus is running other cycles, including other buffered writes. They are also buffered when another bus master is using the System Bus (e.g. DMA, other CPU). Refer to timing diagram 4.3.
4. Read hit cycles can run while another System Bus master is using the System Bus.

The first case is established by providing the data which the 386 DX Microprocessor requested first and later the 82395DX continues filling its line while it is servicing new cache read hit cycles. The 82395DX updates its cache and cache directory after completing the System Bus Line Fill cycle. Meanwhile, any 386 DX Microprocessor read cycles will be serviced from the cache if they hit the cache. In case the 386 DX Microprocessor read cycles are consecutive such that the 386 DX Microprocessor is requesting a double-word which belongs to the same line currently retrieved by the System Bus Line Fill cycle and the requested DW was already retrieved, the 82395DX provides the requested DW in zero wait states (a Line Buffer hit). If the requested DW wasn't already retrieved, it will be read after completing the Line Fill.

The second and third cases are attained by having the Four DW deep write buffer which is described in chapter 6. The READYO# signal is driven active after latching the write cycle, so all buffered cycles will run without wait states. This releases the 386 DX Microprocessor to issue a new cycle, which can also run without wait states if it does not require system bus service. Two examples are in the case of a cache read hit cycle, or another buffered write cycle, which does not require immediate System Bus service. In the case of a write cycle to the same line currently retrieved, the write cycle will wait until the Line Fill is complete and then the selected bytes within the line are written in the cache. READYO# is returned after the cache is written.

Whenever the System Bus is released to any bus master, the 82395DX activates the snooping function. The maximum rate of snooping cycles is a cycle every other clock. Although the snooping support requires accessing the 82395DX cache directory, the 82395DX is able to interpose the cache directory accesses between the 386 DX Microprocessor cycles and the snooping device such that zero wait state cache read hit cycles are supported. All the snooping cycles are also serviced. This is how the fourth case is provided. For more details, refer to chapter 6.

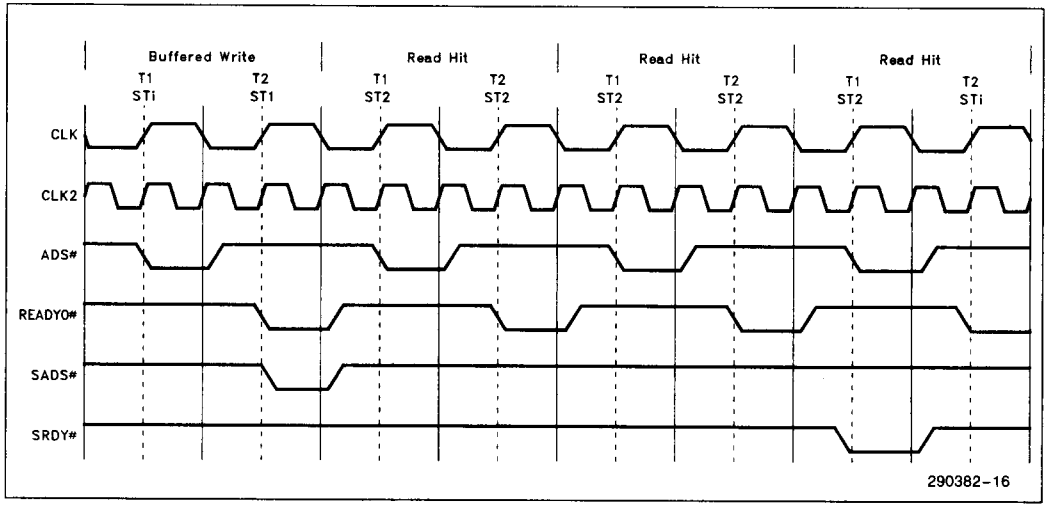


Figure 4.2 - Cache Read Hit Cycles while Executing a Buffered Write on the System Bus

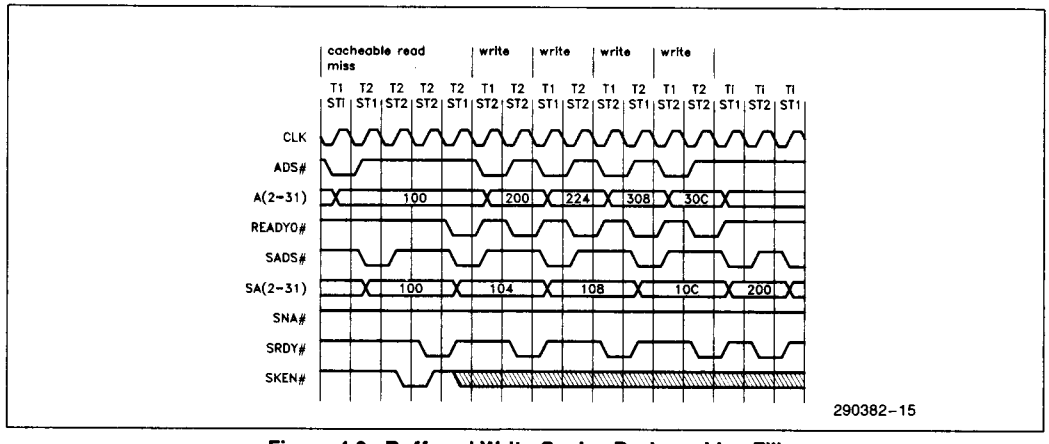
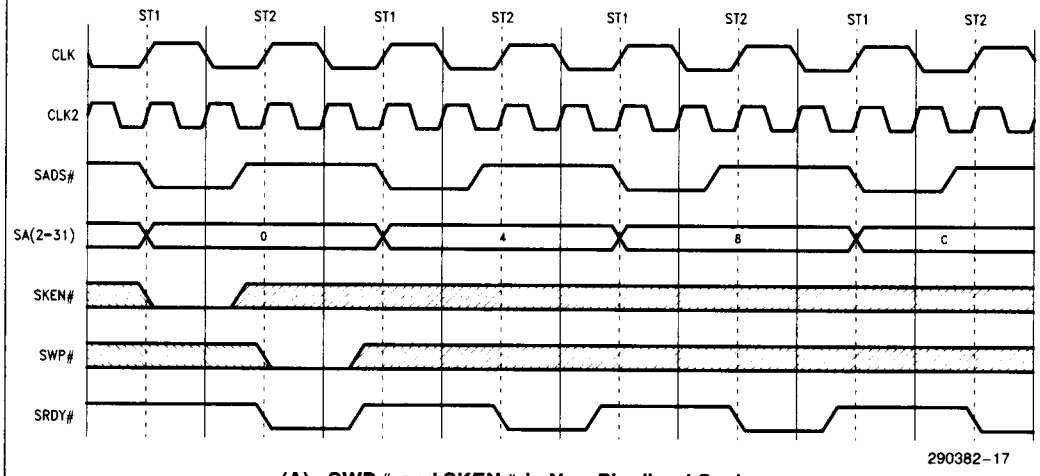
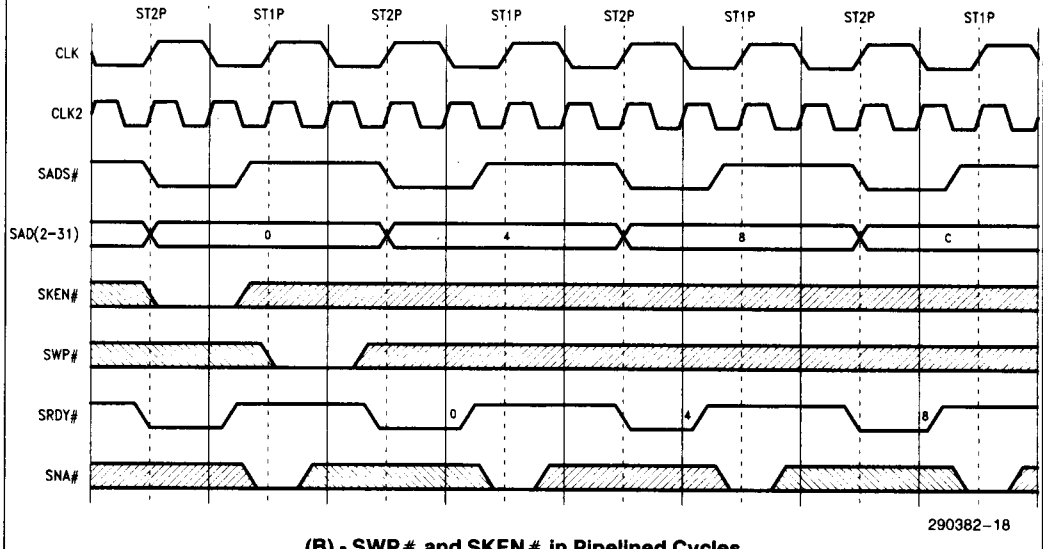


Figure 4.3 - Buffered Write Cycles During a Line Fill



(A) - SWP# and SKEN# in Non-Pipelined Cycles



(B) - SWP# and SKEN# in Pipelined Cycles

Figure 4.4 - SWP# and SKEN# Timing

5

4.4 Disabling the 82395DX

Cacheability is resolved by the SKEN# input from the system side. In order to disable the cache it is recommended to deactivate SKEN# and FLUSH the cache. This would cause all memory reads to be detected as misses and to be transferred to the System Bus. In order to disable the write buffer, NPI# must be asserted.

4.5 System Description and Device Selection

The expandability feature provides the following three configurations:

1) 16KB cache with one 82395DX device.

2) 32KB cache with two 82395DX devices.

3) 64KB cache with Four 82395DX devices.

In multi 82395DX configurations, the total Cache Directory and cache is partitioned between the various 82395DXs. For example, in the second configuration, the first 82395DX includes the first 16KB cache and the first 1K tags while the second 82395DX includes the second 16KB cache and the second 1K tags. Every 82395DX is programmed to handle a portion of the cache and the Cache Directory. The 82395DX selection is based on decoding the address of the cacheable cycle.

In multi 82395DX system, one device must be programmed as the Primary 82395DX to drive the system bus in System Bus cycles (non-cacheable cycles, write cycles and also in Line Fills). All other 82395DXs must be programmed as Secondary 82395DXs. They drive only the SADS# signal in Line Fill cycles. All other System Bus signals are driven by the Primary 82395DX. System diagram 4.6 describes the 64KB cache system. In the Local Bus, each 82395DX gets the 386 DX Microprocessor address, control and data signals. In cacheable reads, hits or misses, the selected 82395DX drives the READYO# and the local data bus. In all other cycles, the Primary drives these signals. The READYO#s of all the 82395DXs are wire-ORed together and they can be logically ORed with the READYC#s of local bus devices. An External pull-up must exist on the 82395DX READYO# to sustain it high. The selected 82395DX drives the READYO# low and keeps it low while the READYI# is not sampled active. Immediately with sampling the READYI# active, the selected 82395DX drives the READYO# high for one phase and floats it in the next phase. Therefore, zero wait state cycles are supported.

In the System Bus, the Primary 82395DX drives all the system bus outputs except SADS#. SADS# is a wire-ORed signal which is driven by the Primary 82395DX in non-cacheable reads and in write cycles. SADS# is driven by the selected 82395DX which requires a Line Fill cycle. A pull-up is required to sustain the SADS# high while not driven.

4.6 Auto Configuration

The 82395DX configures itself automatically during the first ten clocks after the falling edge of RESET. Information on the system configuration is passed to the 82395DXs through their configuration pin (CONF#), by connecting them as follows:

1. The configuration pin of first 82395DX (primary) must be connected to GND.
2. The configuration pin of second 82395DX (optional) must be connected to RESET signal.
3. The configuration pin of third 82395DX (optional) must be connected to READYO# signal.
4. The configuration pin of fourth 82395DX (optional) must be connected to VCC.

Auto configuration process works as follows:

1. If the 82395DX senses the configuration pin low during RESET, the device is configured as device #1 (primary).
2. Otherwise, if the 82395DX senses the configuration pin low one clock cycle after reset, the device is configured as device #2, and issues a READYO# pulse for one clock period.
3. Otherwise, if 82395DX senses the configuration pin low three clock cycles after RESET is sensed low, the device is configured as device #3.
4. Otherwise, the device is configured as device #4, and issues READYO# pulse for one clock period.

All the 82395DXs in the system monitor the number of pulses on READYO# during the first 4 clocks after RESET, to determine how many 82395DXs are present.

1. If no pulse was sensed, there is only one 82395DX.
2. If one pulse is sensed, there are two 82395DXs in the system.
3. If two pulses were sensed, there are 4 82395DXs in the system.

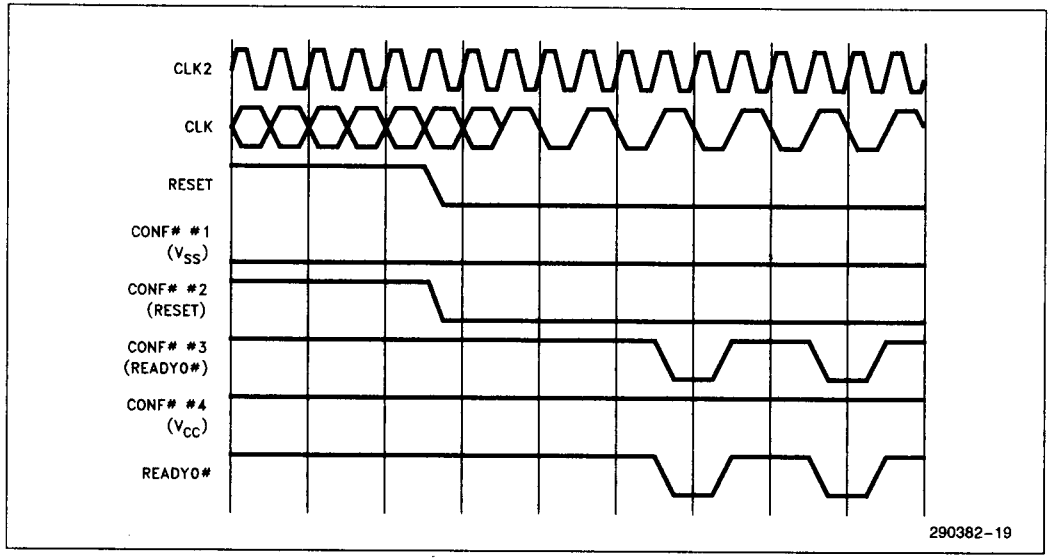


Figure 4.5 - Self Configuration of Four 82395DXs

4.7 Address Mapping

Table 4.2 shows the cache address configurations for 16K, 32K, and 64K cache sizes.

4.8 Multi 82395DX Operation Description

The following is a description of each cycle in a multi-82395DX environment:

Local Bus CYCLES: Cycles to any local bus device (e.g. 387 DX Math Coprocessor). The Primary 82395DX drives the READYO# in 387 DX Math Coprocessor accesses after one wait state, unless READYI# was sampled active one clock earlier. All the secondary 82395DXs are idle.

CACHEABLE READ HIT: this is the only 82395DX cycle which does not require system bus service. In this cycle, the selected 82395DX drives the local data bus and the READYO# in T2. Also, it updates its LRU bits.

CACHEABLE READ MISS: As soon as the system bus is available, the selected 82395DX, which detected the miss, drives the SADS#. In parallel, the Primary 82395DX drives the system bus address and control signals. After receiving the first SRDY# or SBRDY# and after sampling the SKEN# active, the selected 82395DX samples the system data and one clock later it provides it to the 386 DX Microprocessor and drives the READYO# active. Then, it continues in filling the line and, after collecting the four DWs, it updates its cache and Cache Directory.

CACHEABLE WRITE HITS: the selected 82395DX updates its cache, except for write protected cycles. The Primary 82395DX, however, executes the write cycle on the system bus. Notice that both the Primary and Secondary 82395DXs have the same write buffer and both handle the cycle in the same way, but the Primary 82395DX is the one which drives the system bus signals, including SADS# and READYO#. All other cycles i.e. cacheable write misses and non-cacheable cycles are handled only by the Primary 82395DX.

4.9 Signal Driving in Multi 82395DX Environment

4.9.1 Local Bus Signals

In the Local Bus, the data bus and the READYO# signals are the only signals driven by more than one 82395DX.

1. READYO#: normally not driven (floated), and must be sustained by an external pullup. In cacheable reads, the selected 82395DX drives READYO# active until READYI# is sensed active, than it drives READYO# inactive for one clock phase and then floats it. In other cycles, the primary 82395DX drives READYO# in the same manner.
2. Data Bus: The selected (or primary) 82395DX drives the data bus in the T2 state of read cycles, which ensures no contention with the 386 DX Microprocessor when a write cycle follows a read cycle.

4.9.2 SYSTEM BUS SIGNALS

In the System Bus, the Primary 82395DX drives all the System Bus signals except SADS#. So, the jeopardy of contention exists on the SADS# signal

Table 4.2 - Address Mapping for 1-4 82395DX Systems

Device No.	Total Devices in System	Address Decoding	Primary/ Secondary	Cache Data Mapping	Cache Directory SETs
1	1	——	P	0KB-16KB	0-255
1	2	A12#	P	0KB-16KB	0-255
2	2	A12	S	16KB-32KB	256-511
1	4	A13#*A12#	P	0KB-16KB	0-255
2	4	A13#*A12	S	16KB-32KB	256-511
3	4	A13 *A12#	S	32KB-48KB	512-767
4	4	A13 *A12	S	48KB-64KB	768-1023

only. SADS# is normally not driven (floated), and must be sustained by an external pullup. Every 82395DX, Primary or Secondary, after driving the SADS# active in ST1 or ST2P, will drive it inactive for one clock phase in ST2 or ST1P, and float it afterwards.

In Line Fills, the SADS# is driven by the selected 82395DX which detected the miss. In all other cycles e.g. write cycles, the SADS# is driven by the Primary 82395DX.

4.10 SHOLD/SHLDA/SBREQ Arbitration Mechanism

The Primary 82395DX is responsible for handling the SHOLD/SHLDA/SBREQ mechanism. Assuming that the SHOLD is acknowledged, the Primary 82395DX floats all its outputs immediately after completing the system bus cycle in which SHOLD was activated and it drives SHLDA active. This enables the bus master to get control of the bus. When the bus master completes its cycles, it drives the SHOLD signal inactive. Then the Primary 82395DX gets the bus back by driving the SHLDA inactive.

The Secondary 82395DXs get the SHOLD input in order to monitor the bus activity but they don't drive the SHLDA. Secondary 82395DXs do not drive the SADS# in Hold states. The Primary 82395DX drives the SBREQ signal in all System Bus cycles. In Line Fill cycles, the SBREQ signal is driven active one clock later than in other cycles. Of course, this is applicable for the case the System Bus is not available. If the System Bus is available, the SBREQ will not be driven in Line fill cycles. For more details about system arbitration, refer to Chapter 6.

4.11 System Description

A 386 DX Microprocessor/ 82395DX-based system includes the processor, optional Local bus devices (e.g. 387 DX Math Coprocessor), cache system (one 82395DX or more) and System Bus devices (memory, I/O devices and other non-cacheable devices). The 82395DX is the interface between the Local Bus and the System Bus.

A Local Bus address decoder must be used to generate LBA# and NPI# signals, and a System Bus address decoder must be used to generate SKEN# and SWP# signals.

The 82395DX READYO# may be logically ORed with READYO#s of other Local Bus devices. However, this is not required unless a Local Bus device, other than 387 DX Math Coprocessor, exists on the local bus (82395DX generates a READY signal for the 387 DX Math Coprocessor). The 386 DX Microprocessor READY# input signal must also be driven to the 82395DX READYI# pin, so that the 82395DX will be able to track the Local Bus cycles correctly.

Table 4.3 - Local Bus Signal Connections in Multi-82395DX Systems

Primary 82395DX Only		Each 82395DX in the System	
Signal	**Type**	**Signal**	**Type**
		CLK2	I
		D0–D31	I/O
		A2–A31	I
		RESET	I
		BE0-3#	I
		W/R#	I
		D/C#	I
		M/IO#	I
		LOCK#	I
		ADS#	I
		READYI#	I
		LBA#	I
		NPI#	I
		FLUSH#	I
		A20M#	I
		CONF#	I
		READYO#	I/O

To allow for expanding the cache system beyond 16KB, up to four 82395DX devices may be connected in parallel. Two 82395DX outputs are Wire-ORed between the parallel 82395DXs: READYO# and SADS#. Each of the 82395DXs' CONF# input must be tied to a different signal, to program each one of them to a distinct address decoding.

Figure 4.6 describes a maximum 386 DX Microprocessor/82395DX system, with 387 DX Math Coprocessor, four 82395DX devices, READY# generation logic and Local Bus/System Bus address decoders.

Note that optional elements in Figure 4.6 are drawn with dotted line. The Local Bus includes CLK2, RESET, BE3#–BE0#, A2–A31, D0–D31, W/R#, D/C#, M/IO#, LOCK# and ADS#. The System Bus can be broken into two groups. Those pins connected only to the primary 82395DX (82395DX #1) and those connected to each 82395DX in the system (82395DX #1–#4). See Table 4.4.

Table 4.4 - System Bus Signal Connections in Multi-82395DX Systems

Primary 82395DX Only		Each 82395DX in the System	
Signal	**Type**	**Signal**	**Type**
SA2–3	O	SD0–31	I/O
SW/R#	O	SA4–31*	I/O
SD/C#	O	SADS#	O
SM/IO#	O	SRDY#	I
SLOCK#	O	SBRDY#	I
SBREQ	O	SNA#	I
SHLDA	O	SHOLD	I
SBLAST#	O	SAHOLD	I
SNENE#	O	SEADS#	I
		SFHOLD#	I
		SKEN#	I
		SWP#	I

*SA4–31 are connected to each 82395DX in the system for snooping purposes but are driven only by the primary 82395DX.

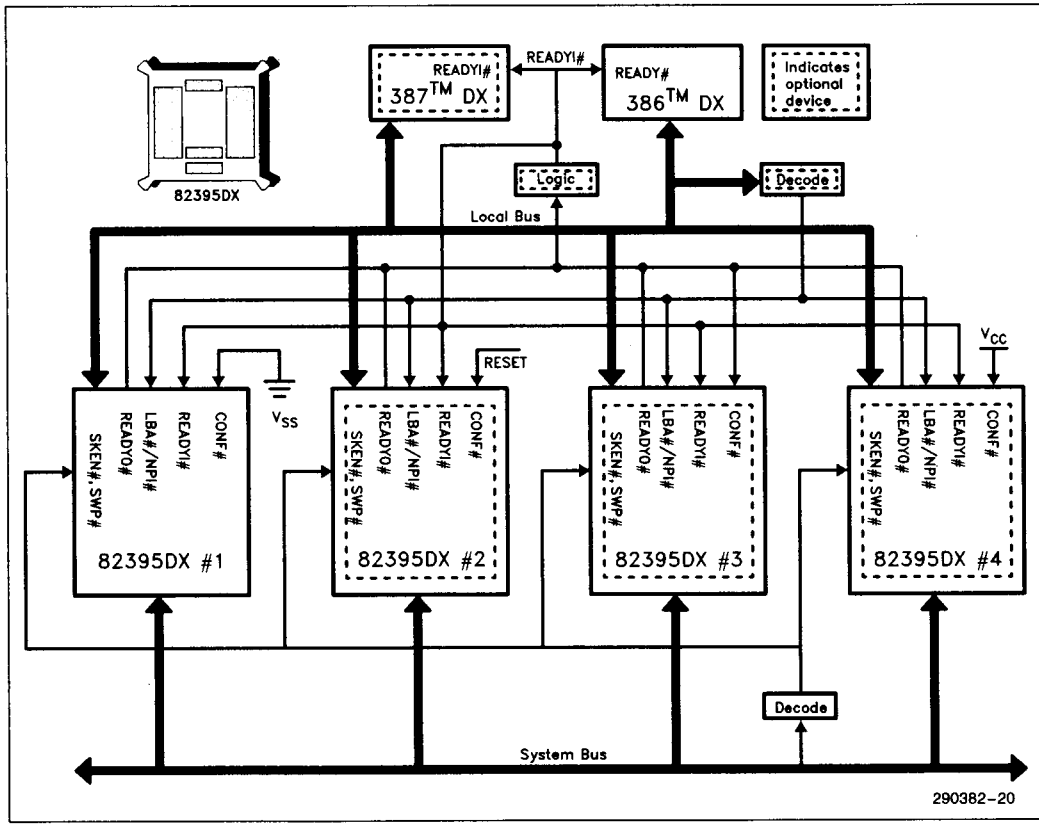


Figure 4.6 - System Description

5.0 PROCESSOR INTERFACE

The 82395DX runs synchronously with the 386 DX Microprocessor. It is a slave on the Local Bus, and it buffers between the Local Bus and the System Bus. Most of the 82395DX cycles are serviced from the internal cache, and some (82395DX cache misses, non cacheable accesses, etc.) require an access to the System Bus to complete the transaction.

To achieve maximum performance, the 82395DX serves cache hits and buffered write cycles in zero wait- state, non-pipelined cycles. The 82395DX requires that the CPU is never driven to pipelined cycles, i.e. the 386 DX Microprocessor NA# input must be strapped to inactive (high) state.

The 82395DX is directly connected to all local bus address and data lines, byte enable lines, and bus cycle definition signals. The 82395DX returns READYO# to the 386 DX Microprocessor, and keeps track of the 386 DX Microprocessor cycle status by receiving READYI# (which is the 386 DX Microprocessor READY#).

A multi 82395DX system description was presented in chapter 4.

5.1 Hardware Interface

The 82395DX requires minimal hardware on the Local Bus. Other than the 386 DX Microprocessor and other Local Bus resources (i.e. 387 DX Math Coprocessor) and the 82395DX(s) (1-4 depending on the system). Ready logic and a Local Bus decoder are optional since the user can wire OR the READYO#s and tie LBA# and NPI# high if no addresses are to be local or non-buffered. The SRAM and buffers have been integrated on chip to simplify the design. Refer to Figure 4.6.

5.2 Nonpipelined Local Bus

The 82395DX does not pipeline the Local Bus. READYO# gets returned to the 386 DX Microprocessor one cycle after SRDY# or SBRDY# are driven into the 82395DX after the first DW of a Line Fill. This allows the Local Bus to be free to execute 386 DX Microprocessor cycles while the System Bus fills the cache line (see chapter 6).This takes away the advantage gained by pipelining the Local Bus.

5.3 Local Bus Response Hit Cycles

The 82395DX's Local Bus response to hit cycles are described here:

1) Cache Read Hit (CRDH) Cycle — READYO# gets returned in T2. The Data is valid to the 386 DX Microprocessor on the rising edge of CLK2.
2) Cache Write Hit (CWTH), Buffered — Like in CRDH cycles the 82395DX returns READYO# in T2 so that the cycle runs with zero wait states on the Local Bus. The write cycle is placed in the write buffer and will be performed when the System Bus is available. If the System Bus is on HOLD up to four write cycles can be buffered before introducing any wait states on the Local Bus.
3) CWTH, Non-Buffered — In the case of a non-buffered write hit cycle the write buffers can not be used so the 386 DX Microprocessor must wait until the System Bus is free to do the write. READYO# is returned to the cycle after SRDY# is driven to the 82395DX.

5.4 Local Bus Response to Miss Cycles

In a Cache Read Miss (CRDM) cycle a Line Fill is performed on the System Bus. READYO# is returned to the 386 DX Microprocessor one cycle after SRDY# or SBRDY# for the first DW of the Line Fill is driven into the 82395DX.

5

5.5 Local Bus Control Signals — ADS#, READYI#

ADS# and READYI# are the two bus control inputs used by the 82395DX to determine the status of the Local Bus cycle. ADS# denotes the beginning of a 386 DX Microprocessor cycle and READYI# is the 386 DX Microprocessor cycle terminator.

ADS# active and M/IO# = 1 invokes a look-up request to the 82395DX's cache directory; the look-up is performed in T1 state. The Cache Directory access is simultaneous with all other cycle qualification activities, this Way the hit/miss decision becomes the last in the cycle qualification process. This parallelism enhances performance, and enables the 82395DX to respond to ADS# within one clock period. If the cycle is to a Local Bus device (LBA# asserted) or is non-cacheable, the hit/miss decision is ignored.

5.6 82395's Response to the 386 DX Microprocessor Cycles

Tables 5.2 - 5.4 show the 82395DX's response to the various 386 DX Microprocessor cycles. They depict the activity in the internal cache, cache directory, the System Bus and write buffers in response to various cycle definition signals. Special cycles such as: LOCK, HALT/SHUTDOWN, WP, LBA, NPI are discussed separately below.

5.6.1 LOCKED CYCLES

The 386 DX Microprocessor LOCK#ed cycles are all those cycles in which LOCK# is active. The 82395DX forces all LOCK#ed cycles to run on the System Bus. The 82395DX starts the LOCK#ed cycle after it has emptied its write buffers.

If the LOCK#ed cycle is cacheable the 82395DX will respond as follows (see table 5.2):

Cache Read Miss (CRDM) — handled similar to a non cacheable cycle.

Cache Read Hit (CRDH) — handled similar to a non cacheable cycle (LRU bits are not updated).

Cache Write Miss (CWTM) — the cache is not updated, the write is not buffered.

Cache Write Hit (CWTH) — the cache is updated if the line is not write protected. The write is not buffered. Note that this write is not buffered even though it is cacheable. The LRU mechanism is updated.

If the LOCK#ed cycle is non-cacheable (e.g. IO cycle, INTA cycle) then it will be performed as a common non-cacheable cycle with the addition of asserting SLOCK# on the System Bus.

Conceptually, a LOCK# cycle on the Local Bus is reflected into an SLOCK# cycle on the System Bus. Detailed timing considerations were presented in chapter 3. SLOCK# becomes inactive only after LOCK# has become inactive. If there are idle clocks in between the LOCK#ed cycles but LOCK# is still active - SLOCK# will remain active as well. **A consequence of this is that SLOCK# is negated one clock after LOCK# is negated.**

During LOCK#ed cycles on System Bus (i.e. when SLOCK# signal is active), the 82395DX does not acknowledge hold requests so the whole sequence of LOCK#ed cycles will run without interruption by another master.

Note that when a LOCK#ed LBA# cycle runs on the Local Bus, and the System Bus is idle and not at HLDA state, SLOCK# will be asserted even though the LBA# cycle will not be transferred to the system bus.

5.6.2 I/O, HALT/SHUTDOWN

I/O and HALT/SHUTDOWN cycles are handled as non-cacheable cycles. They are neither cached nor kept in the write buffer. The 386 DX Microprocessor HALT/SHUTDOWN cycles are memory write cycles to code area (i.e. M/IO# = 1, D/C# = 0). The 82395DX completes I/O and HALT/ SHUTDOWN cycles by returning READYO#, after receiving the SRDY#.

5.6.3 LBA# CYCLES

LBA# cycles are all the 386 DX Microprocessor cycles in which LBA# is active, or all cycles in which the 387 DX Math Coprocessor or Weitek 3167 Floating-Point Coprocessor is addressed. A CPU access to I/O space with A31 = 1 is decoded as a 387 DX Math Coprocessor access. A CPU access to memory space C0000000H through C1FFFFFFH is decoded as a Weitek 3167 Floating-Point Coprocessor access, provided that the Weitek decoding is enabled.

When an LBA# cycle is detected all other attributes are ignored. If a 387 DX Math Coprocessor access is decoded, READYO# is activated as described in section 5.6. No other activity takes place.

5.6.4 NPI# CYCLES

NPI# cycles are all the 386 DX Microprocessor memory write cycles in which NPI# is active. In response to a cycle with NPI# active, the 82395DX first executes all pending write cycles in the write buffer (if any), and then executes the current write cycle on the System Bus. READYO# is returned to the CPU only after SRDY# for the current write cycle is returned to the 82395DX.

All NPI# cycles must have at least one wait state on the System Bus or be done to non-cacheable memory.

NPI# is ignored for read cycles, as well as all write cycles that cannot be buffered.

5.6.5 LBA#/NPI# TIMING

These inputs must be valid throughout the 386 DX Microprocessor bus cycle, namely in T1 and all T2 states (See Figure 5.1).

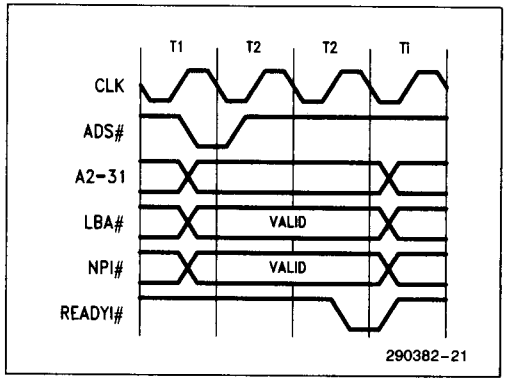


Figure 5.1 - Valid Time of LBA# and NPI#

5.7 82395DX READYO# Generation

The 82395DX READYO# generation rules are listed below:

CRDH cycles (non-LOCK#ed), READYO# is activated during the first T2 state, so the cycle runs with zero wait states.

CRDM cycles - READYO# is returned one clock after the first SRDY# or SBRDY#.

Non cacheable reads - READYO# is returned one clock after SRDY# or SBRDY#.

All cacheable writes (with the exception of LOCK#ed writes) are buffered. These cycles may be divided into two categories:

(a) The first four write cycles — while the write buffer is not fully exploited. READYO# is returned in zero wait states. The address and the data are registered in the write buffer.

(b) When the write buffer is full — READYO# is delayed until one clock after the SRDY# or SBRDY# of the first write cycle in the buffer. In other words the fifth write waits until there is one vacant entry in the write buffer.

Non cacheable writes (plus LOCK#ed writes) — these writes are not buffered. READYO# is returned one clock after SRDY# or SBRDY# of the same cycle.

READYO# activation during SRAM mode is described in Chapter 7. READYO# activation during self configuration is listed in Chapter 4.

In all 387 DX Math Coprocessor accesses, the 82395DX monitors the READYI#. If it wasn't activated immediately after ADS#, READYO# will be activated in the next clock i.e. a one wait state cycle. So, the 82395DX READYO# can be used to terminate any 387 DX Math Coprocessor access.

Note that the timing of the 82395's READYO# generation for 387 DX Math Coprocessor cycles is incompatible with 80287 timing. When activated, READYO# remains active until READYI# is sampled active. This procedure enables adding control logic to control the 386 DX Microprocessor READYI# generation (see Figure 5.2).

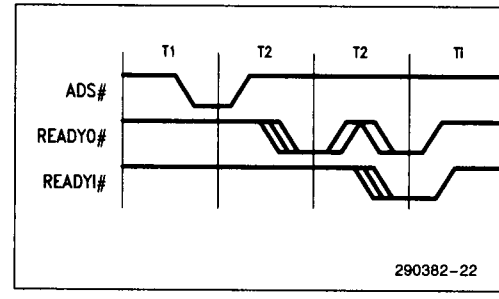


Figure 5.2 - Externally Delayed READY

In a multi-82395DX system, each device on the Local Bus must be able to return READYO#. Therefore, READYO# is wired OR on the Local Bus. READYO# is normally floated, and it is connected to the positive power supply by a pull-up resistor. An external OR gate ORs the 82395DXs' READYO#s with the READYO# of all other Local Bus devices.

5

5.8 A20 Mask Signal

The A20M# signal is provided to allow for emulation of the address wraparound at 1 MByte which occurs on the 8086. A20M# pin is synchronized internally by the 82395DX, then ANDed with the A20 input pin. The product of synchronized A20M# and A20 is presented to the rest of the 82395DX logic, as shown in Figure 5.3.

A20M# must be valid two clock cycles before ADS# is sampled active by the 82395DX, and must remain valid until after READYI# is sampled active (see Figure 5.4).

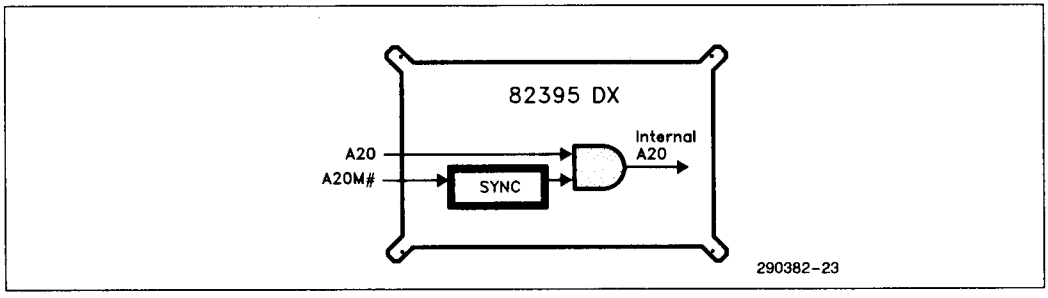


Figure 5.3 - A20 Mask Logic

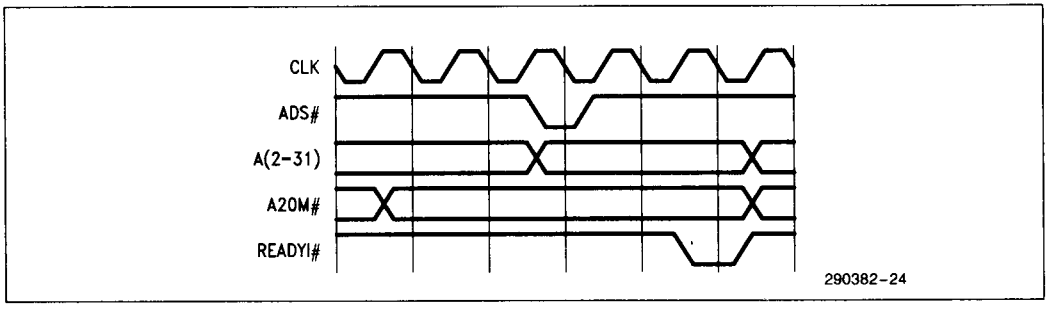


Figure 5.4 - Valid Time of A20M#

5.9 82395DX Cycle Overview

Table 5.1 - 386 DX Microprocessor Bus Cycle Definition

M/IO#	D/C#	W/R#	386 DX Microprocessor Cycle Definition
0	0	0	Interrupt Acknowledge
0	0	1	Undefined
0	1	0	I/O Read
0	1	1	I/O Write
1	0	0	Memory Code Read
1	0	1	Halt/Shutdown
1	1	0	Memory Data Read
1	1	1	Memory Data Write

Table 5.2 describes the activity in the cache, in the Tagram, on the System Bus and in the write buffers. The cycles are defined in table 5.1. Table 5.2 is sorted in a descending order. The more dominant the attribute the higher it is located. For example, if the cycle is both LBA# and I/O it is considered an LBA# cycle. Table 5.2 is for non test modes.

Table 5.2 - Activity by Functional Groupings

Cycle Type	WP	Cache	TAGRAM		System Bus	Posted Write	Comm.
			LRU	TAG			
1. LBA & 387/Weitek Cycles	N/A	—	—	—	—	N/A	
2. I/O Write, I/O Read, Halt/Shutdown, INTA, LOCK#ed Read	N/A	—	—	—	Non Cacheable Cycle	No	2
3. LOCK#ed Write Hit	Yes		Update	—	Memory Write	No	2
4. LOCK#ed Write Hit	No	Cache Write	Update	—	Memory Write	No	2
5. LOCK#ed Write Miss	N/A	—	—	—	Memory Write	No	2
6. Other Read Hit	N/A	Cache Read	Update	—	—	N/A	1
7. Other Read Miss SKEN# Active	N/A	Cache Write	Update	Update	Line Fill	N/A	2
8. Other Read Miss SKEN# Inactive	N/A	—	—	—	Noncacheable Read No Line Fill	N/A	2
9. Other Write Hit NPI# Inactive	Yes	—	Update	—	Memory Write	Yes	1
10. Other Write Hit NPI# Active	Yes	—	Update	—	Memory Write	No	2
11. Other Write Hit NPI# Inactive	No	Cache Write	Update	—	Memory Write	Yes	1
12. Other Write Hit NPI# Active	No	Cache Write	Update	—	Memory Write	No	2
13. Other Write Miss NPI# Inactive	N/A	—	—	—	Memory Write	Yes	1
14. Other Write Miss NPI# Active	N/A	—	—	—	Memory Write	No	2

Table 5.3 describes line buffer hit cycles. Hit/miss here means to the specific DW in the line buffer.

Table 5.3. Activity in Line Buffer Hit Cycles

Cycle Type	WP	Cache	TAGRAM		System Bus	Posted Write	Comm.
			LRU	TAG			
15. LOCK#ed Write	Yes	—	—	—	Memory Write	No	2
16. LOCK#ed Write	No	Cache Write	—	—	Memory Write	No	4
17. Read Hit	N/A	LB Read	—	—	—	N/A	1
18. Read Miss	N/A	LB Read	—	—	—	N/A	3
19. Other Write NPI# Inactive	Yes	—	—	—	Memory Write	Yes	6
20. Other Write NPI# Active	Yes	—	—	—	Memory Write	No	2
21. Other Write NPI# Inactive	No	Cache Write	—	—	Memory Write	Yes	5
22. Other Write NPI# Inactive	No	Cache Write	—	—	Memory Write	No	4

Table 5.4 describes the line buffer hit cycles, when the Line Fill is interrupted (by: FLUSH#, snoop hit to the line buffer or interrupted burst, even if the Line Fill continues on the System Bus in the first two cases). The table includes only the cycles which wait to the end of the Line Fill or to the CPU cache update. Hit/Miss here means to the right DW in the line buffer.

Table 5.4. Activity in the Line Buffer During ALF Cycles

Cycle Type	WP	Cache	TAGRAM		System Bus	Posted Write	Comm.
			LRU	TAG			
23. LOCK#ed Write	N/A	—	—	—	Memory Write	No	2
24. Read Miss (Restart)	N/A	Cache Write	Update	Replace	Line Fill	N/A	2
25. Other Write NPI# Inactive	N/A	—	—	—	Memory Write	Yes	5
26. Other Write NPI# Active	N/A	—	—	—	Memory Write	No	2

Table 5.5 depicts the 82395DX Test Cycles.

Table 5.5. Activity in Test Cycles

Cycle Type	WP	A16	Cache	TAGRAM		System Bus	Posted Write	Comm.
				LRU	TAG			
27. High Impedance	N/A	N/A	—	—	—	—	N/A	
28. SRAM Mode Read Add 256K-512K	N/A	0	—	LRU RD	TAG RD	—	N/A	
29. SRAM Mode Read Add 256K-512K	N/A	1	Cache	—	—	—	N/A	
30. SRAM Mode Write Add 256K-512K	N/A	0	—	LRU WR	TAG WR	—	N/A	
31. SRAM Mode Write Add 256K-512K	N/A	1	Cache Write	—	—	—	N/A	
32. SRAM Mode Read Add < > 256K-512K	N/A	N/A	—	—	—	Noncacheable Cycle	No	2
33. SRAM Mode Write Add < > 256K-512K	N/A	N/A	—	—	—	Noncacheable Cycle	N/A	

Remarks for Tables 5-2 through 5-5:

1. READYO# is active in the first T2. (In read cycles, in write it depends if the write buffer is full).
2. READYO# is active one clock cycle after SRDY#/SBRDY# of this cycle is asserted. In case of Line Fill, READYO# is active one clock cycle after first SRDY#/SBRDY# of this cycle is asserted.
3. READYO# is active immediately after the current line fill is finished.
4. READYO# is active after the previous line fill and the write cycle are terminated by SRDY# or SBRDY#, and the cache is updated.
5. READYO# is active after the cache is updated for the previous Line Fill, or after the Line Fill is aborted.
6. READYO# is active on the third T2 (2 wait states) if the write buffer is not full.
7. "OTHER" means the cycle does not fall within the first five categories.

6.0 SYSTEM BUS INTERFACE

The System Bus (SB) interface is similar to the 386 DX Microprocessor interface. It runs synchronously to the 386 DX Microprocessor clock. In general, the interface is similar to the 82385 in terms of: System Bus pipelining, snooping support and write cycle buffering. In addition, the following enhancements are provided:

1) Line Fill buffer.

2) Optional burst Line Fill.

3) System cacheability attribute, SKEN#.

4) System Write Protection attribute, SWP#.

5) The SBREQ/SHOLD/SHLDA arbitration mechanism to support multi master systems.

6) The SEADS# snooping mechanism to support concurrency on the System Bus and on the general purpose bus.

7) SFHOLD# mechanism to resolve deadlocks in multiprocessing systems.

8) Four Double-Word write buffer (16 bytes).

9) SNENE# (System NExt NEar) function to simplify the design of page mode DRAM system, and save wait states.

The 82395DX System Bus interface has identical bus signals to the 386 DX Microprocessor bus. It has the bus control signals (SADS#, SRDY# and SNA#), the cycle definition signals (SLOCK#, SW/R#, SD/C# and SM/IO#), the address and byte enable signals (SA2–SA31 and SBE0#–SBE3#) and the data signals (SD0–SD31). In addition, the 82395DX has the SBRDY# signal for burst support. The SKEN# signal for the system cacheability attribute. The SWP# signal for the system Write Protection attribute. The SAHOLD and SEADS# signals for snooping support. The SBREQ, SHOLD and SHLDA signals for system arbitration. And SNENE# for DRAM hook-up. Also, the 82395DX provides a signal, SBLAST#, which when asserted, indicates that the current cycle is the last cycle in a burst transfer.

The 82395DX System Bus interface can support any device, non cacheable, I/O or cacheable memory with any number of wait states. However, zero wait state non-posted writes are not allowed. The 82395DX is able to support one clock burst cycles. The 82395's System Bus state machine is similar to the 386 DX Microprocessor bus state machine (refer to the "386 DX Microprocessor data sheet"). Note that during burst Line Fill, the 82395DX remains is ST2 state until SRDY# or SBRDY# is asserted for the fourth cycle of the burst transfer. Figure 6.1 describes the 82395's System Bus state machine.

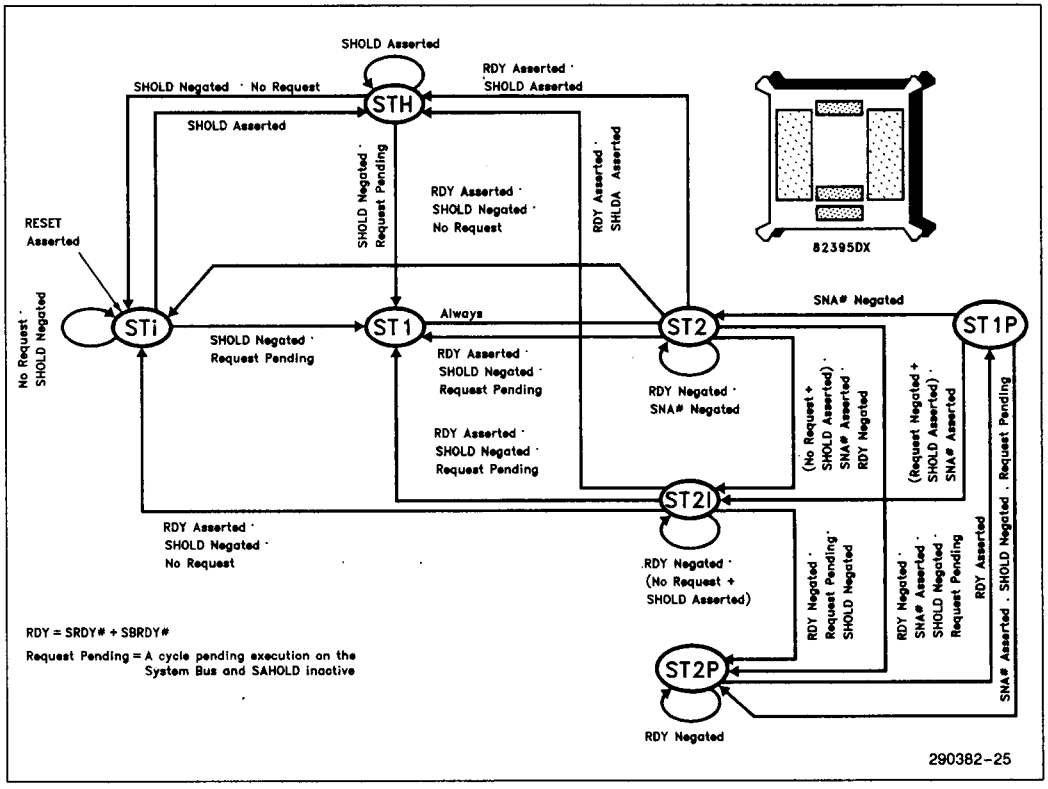


Figure 6.1 - SB State Machine

6.1 System Bus Cycle Types

Following five types of SB cycles are supported:

1) Buffered write cycle
2) Non buffered write cycle
3) Buffered/non-buffered write protected cycles.
4) Non cacheable read cycle
5) Cacheable read cycle

6.1.1 BUFFERED WRITE CYCLE

All the cacheable write cycles, except LOCK#ed write cycles or non-buffered write cycles (as indicated by NPI# pin sampled active), are buffered. These cycles are terminated on the Local Bus before they are terminated on the System Bus.

The following Figures (6.2 - 6.3) include waveforms of several cases of buffered write cycles:

The 82395DX has a four DW deep write buffer but five writes cycles can be buffered if one of the buffered writes is being executed.

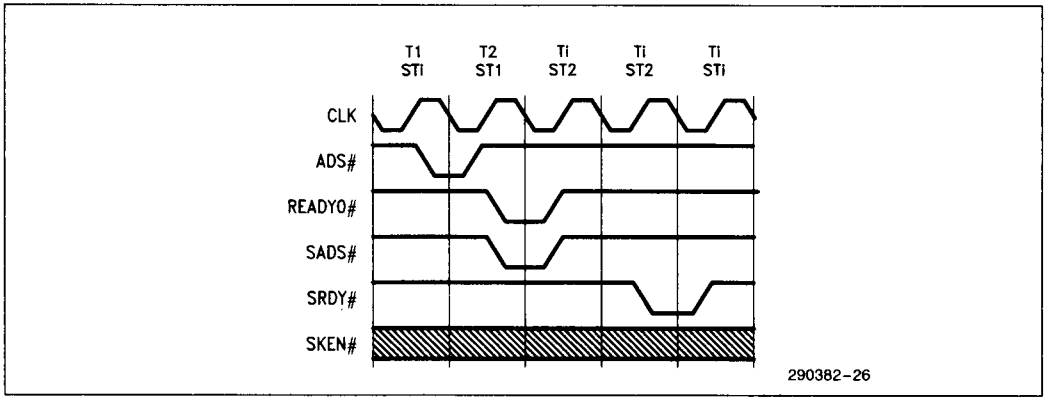
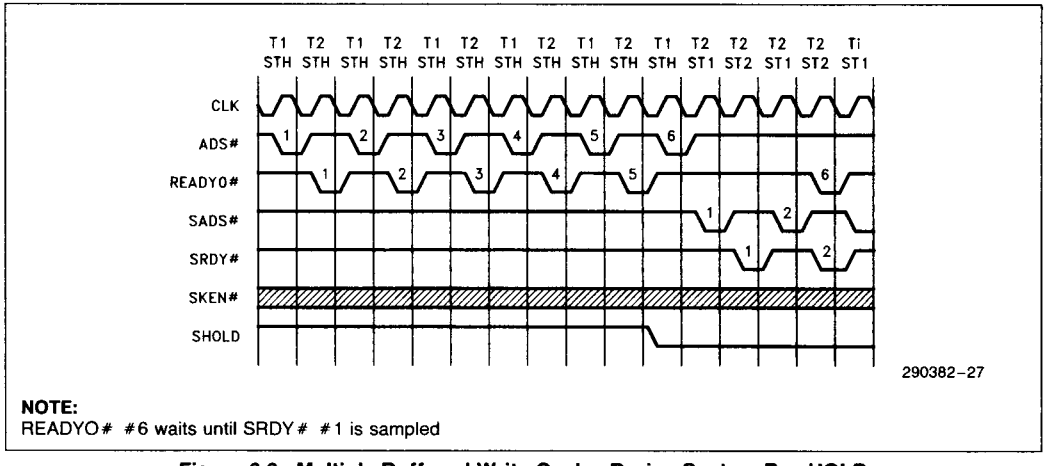


Figure 6.2 - Single Buffered Write Cycle



NOTE:
READYO# #6 waits until SRDY# #1 is sampled

Figure 6.3 - Multiple Buffered Write Cycles During System Bus HOLD

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6.1.2 NON-BUFFERED WRITE CYCLE

These cycles are terminated on the System Bus one clock before they are terminated on the Local Bus.

The following Figures (6.4 - 6.5) include waveforms of several cases of non buffered write cycles.

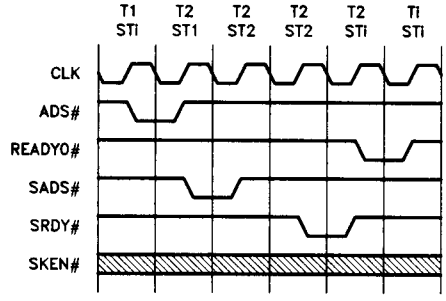
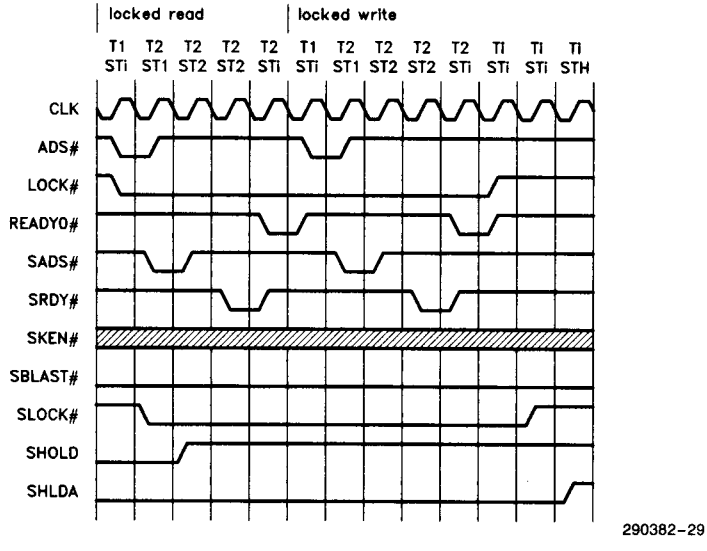


Figure 6.4 - I/O Write Cycle



NOTE:
While SLOCK# is active SHOLD input is ignored

Figure 6.5 - LOCK#ed "Ready Modify Write" cycle

6.1.3 WRITE PROTECTED CYCLES

The Write Protection attribute is provided by the system bus SWP# input. The SWP# is sampled with the first SRDY# or SBRDY# in every Line Fill cycle. The write protection indicator is registered in the Cache Directory together with the TAG address and TAG Valid bit of every line. In every cacheable write cycle, the write protection indicator is read simultaneously with the Hit/Miss decision. If the write cycle is a hit and the write protection indicator is set, the cache will not be updated. In all other cases, the write protection indicator is ignored.

6.1.4 NON-CACHEABLE READ CYCLE

Non cacheable read cycles are terminated on the System Bus one clock before they are terminated on the Local Bus.

The following Figures (6.6 - 6.7) include waveforms of several cases of non cacheable read cycles.

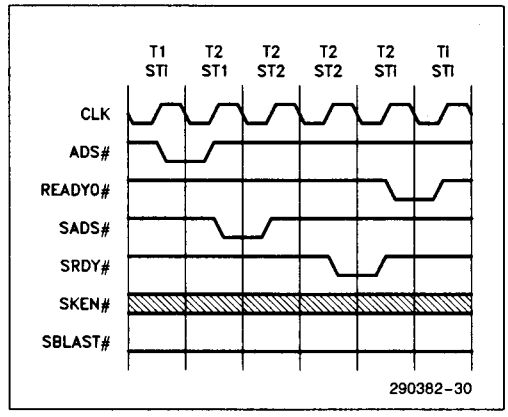
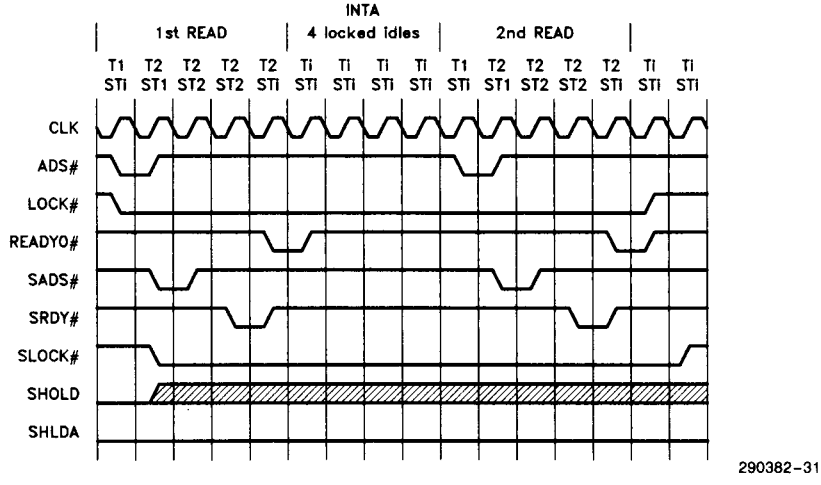


Figure 6.6 - I/O Read Cycle



NOTE:
While SLOCK# is active SHOLD input is ignored
Even if the System Bus is in its idle state, SLOCK# is active because LOCK# is active.

Figure 6.7 - INTA LOCK#ed Cycle

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6.1.5 CACHEABLE READ MISS CYCLES

The 82395DX attempts to start a Line Fill for non LOCK#ed CRDM cycles. However, a Line Fill will be converted into a single read cycle if the access is indicated as non-cacheable by the SKEN# signal.

CRDM cycles start as a System Bus read cycle. READYO# is returned to the 386 DX Microprocessor one clock cycle after the System Bus read cycle is terminated.

One CLK cycle before the first SNA#, SRDY# or SBRDY# of the system read cycle, the SKEN# input is sampled. If active, the read miss cycle continues as a Line Fill cycle, and three additional DWs are read from the memory into the 82395DX. Also, the SWP# input will be sampled with the first SNA#, SRDY# or SBRDY# so the WP flag of the line will be updated in the Cache Directory.

6.1.5.1 Aborted Line Fill (ALF) Cycles

The System Bus can respond that the area of memory included in a particular request is non-cacheable, by returning SKEN# inactive. As soon as the 82395DX samples SKEN# inactive, it converts the cycle from a cache Line Fill, which requires additional read cycles to be completed, to a single cycle.

In this case SBLAST# will stay active. Also, the 82395DX will not generate another system cycle for the same Line Fill, because the cycle has already been finished by the first SBRDY# or SRDY# after SKEN# was sampled inactive.

The following Figure 6.8 includes waveforms of an ALF cycle.

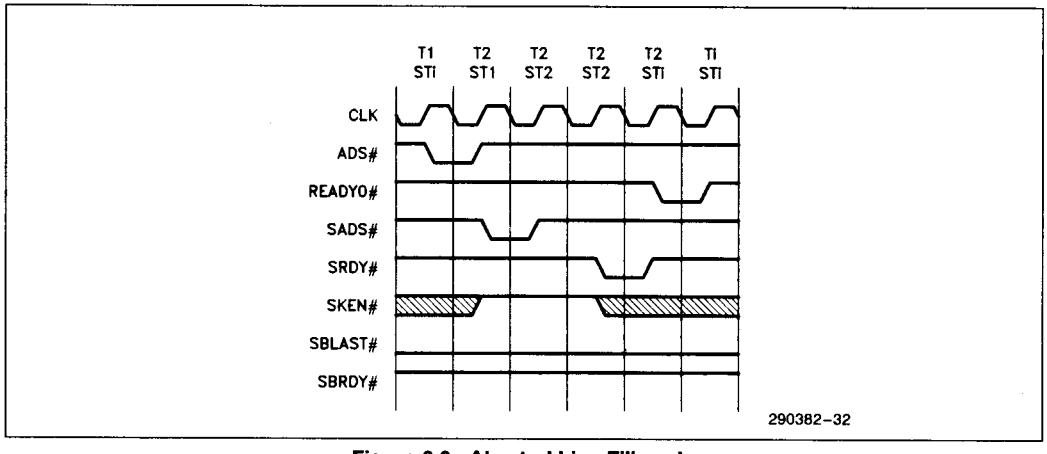

Figure 6.8 - Aborted Line Fill cycle

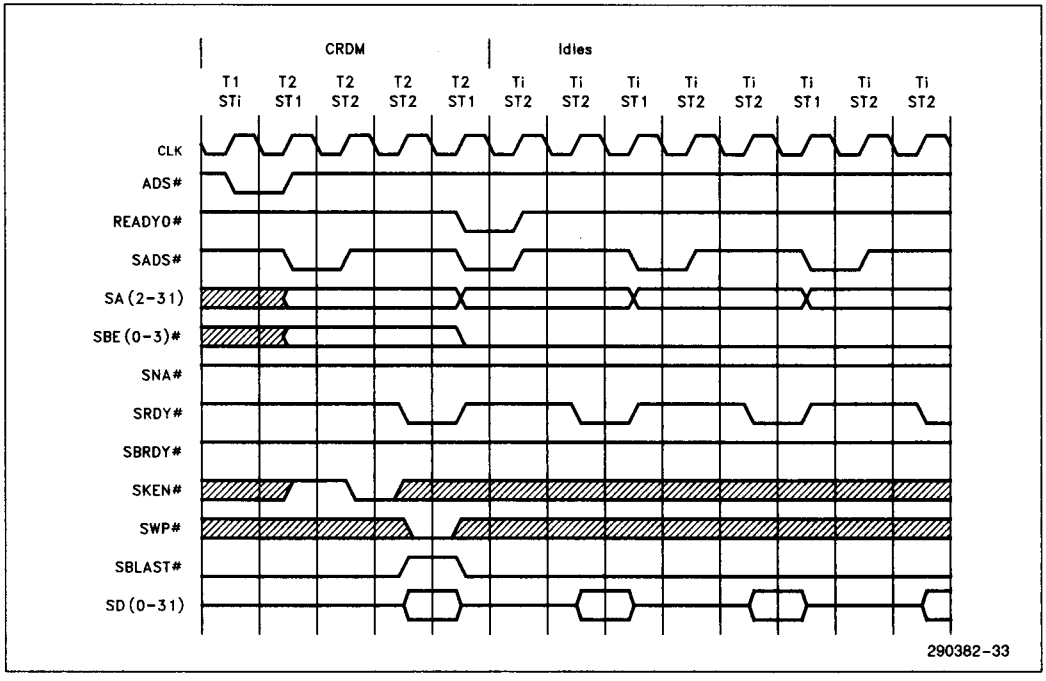

Figure 6.9 - Line Fill Without Burst or Pipeline

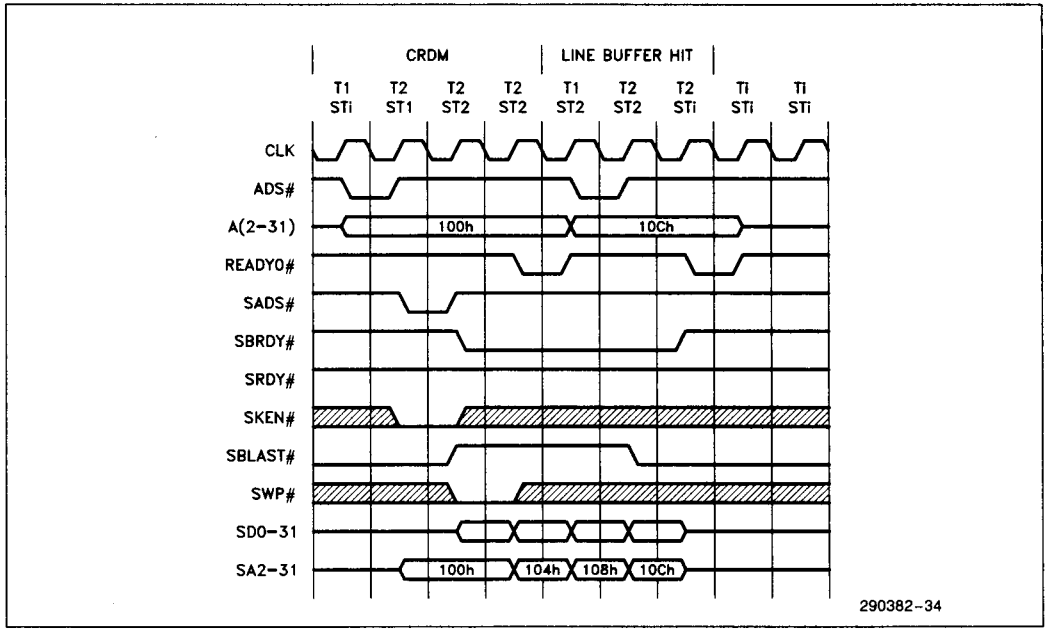

Figure 6.9A - Burst Mode Line Fill followed by a Line Buffer Hit Cycle

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6.1.5.2 Line Fill Cycles

A Line Fill transfer consists of four back to back read cycles. Three types of Line Fill cycles are supported:

1. Non pipeline, Non burst, SNA# inactive.
2. Pipelined, non burst, SNA# active.
3. Burst, non pipelined, SNA# inactive, SRDY# inactive, SBRDY# active.

Note that a pipelined burst cycle is not supported. When SNA# is sampled active, SBRDY# is treated as SRDY#.

The 82395DX supports burst cycles in system Line Fills only. Burst cycles are designed to allow fast line fills by allowing consecutive read cycles to be executed at a rate of one DW per clock cycle. In burst cycles SADS# is pulsed for one clock cycle while the address and control lines are valid until the transfer is completed. SA2–3 are updated every bus cycle during the burst transfer.

The 82395DX starts the Line Fill as a normal read cycle, and waits for SBRDY# or SRDY# to be returned active. If SNA# is sampled active at least one clock cycle before either SBRDY# or SRDY#, the Line Fill will be non burst pipelined. (See Figure 6.10). If SNA# is sampled active at the same clock cycle as SBRDY# or SRDY#, the line fill will be non-burst, non-pipelined.

If SKEN# is sampled inactive one clock before either SNA#, SBRDY# or SRDY#, then the access is considered non-cacheable and Line Fill will not be executed. (See Figure 6.8) Otherwise, if SRDY# is sampled active, the line fill cycle resumes as a non-burst sequence of three more cycles (see Figure 6.9). Finally, if SBRDY# and SKEN# are sampled active (and SNA# and SRDY# are sampled inactive), then the Line Fill cycle will be a burst cycle (see Figures 6.11 - 6.12).

If a system cannot support burst cycles, a non burst line fill must be requested by merely returning SRDY# instead of SBRDY#, in the first read cycle (see Figure 6.9). Once a burst cycle started, it will not be aborted until it's completed, regardless if SKEN# is sampled inactive or SHOLD is sampled active, i.e. all four DWs will be read from memory. However, the system may abort a burst Line Fill transfer before it's completed, by returning SRDY# active (instead of SBRDY#) for the second or third DW in a Line Fill transaction (see Figure 6.13). In this case the cache will not be updated. The first DW will already have been transferred to the CPU.

Note that in the last (fourth) bus cycle in a line fill transfer, SBRDY# or SRDY# has the same effect on the 82395DX. That is to indicate the end of the Line Fill. For all cycles that cannot run in burst mode (non-Line Fill cycles or pipelined Line Fill cycles) SBRDY# has the same effect on the 82395DX as the normal SRDY# pin. SRDY# and SBRDY# are the same apart from their function during burst cycles.

The fastest burst cycle possible requires two clocks for the first data item to be returned to the 82395DX with subsequent data items returned every clock. Such a bus cycle is shown in Figure 6.11. An example of a burst cycle where two clocks are required for every burst item is shown in Figure 6.12. When initiating any read, the 82395DX presents the address for the data item requested. When the 82395DX converts this cycle into a cache Line Fill, the first data item returned must correspond to the address sent out by the 82395DX. This address is the original address that is requested by the 386 DX Microprocessor. The 82395DX updates this address after each SBRDY# according to table 6.1 (SA2 and SA3 are updated). This is also true for non-burst Line Fill cycles. The 82395DX presents each request for data in an order determined by the first address in the transfer. For example, if the first address was 104, the next three addresses in the burst will be 100, 10C, and 108. The burst order used by the 82395DX is shown in Table 6.1. This remains true whether the external system responds with a sequence of normal bus cycles or with a burst cycle. An example of the sequencing of burst addresses is shown in Figure 6.12.

This order was designed to optimize the performance of 64- bit memory systems. The second cycle of a burst reads the DW that forms the other half of an aligned 64-bit block, no matter whether that DW is at a higher or lower address. The third and fourth cycles then read the two DWs which form the other half of an aligned 128-bit block. The order in which the third and fourth DWs are accessed corresponds to the order used for the first and second DWs.

Table 6.1 - Line Fill Address Order

First Address	Second Address	Third Address	Fourth Address
0	4	8	C
4	0	C	8
8	C	0	4
C	8	4	0

In the following cases, a Line Fill cycle will not update the cache:

1. Aborted burst: burst cycle will be aborted if SRDY# is returned active in the second or third bus cycle. The Line Fill will not resume, and the cache will not be updated.
2. Snoop hit to line buffer: If, during a Line Fill transfer, a snoop cycle is initiated after the first SRDY# or SBRDY#, and the address matches the address of the line being retrieved, the Line Fill cycle will continue as usual but the cache will not be updated.
3. FLUSH during Line Fill cycle: the Line Fill cycle will continue as usual, but the cache will not be updated.

Figures (6.9 - 6.13) include waveforms of several cases of Line Fill cycles.

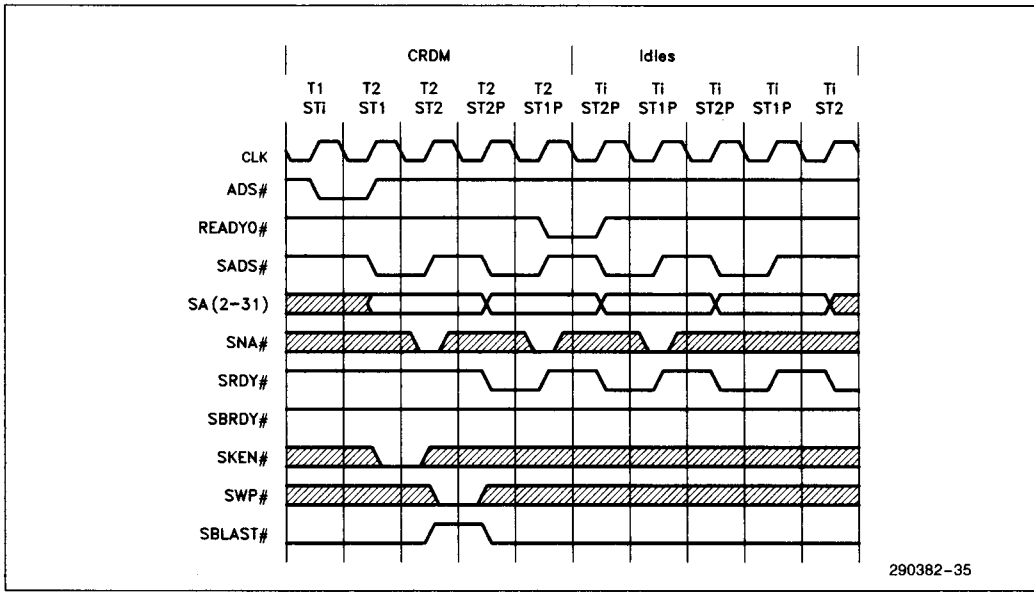

Figure 6.10 - Pipelined Line Fill

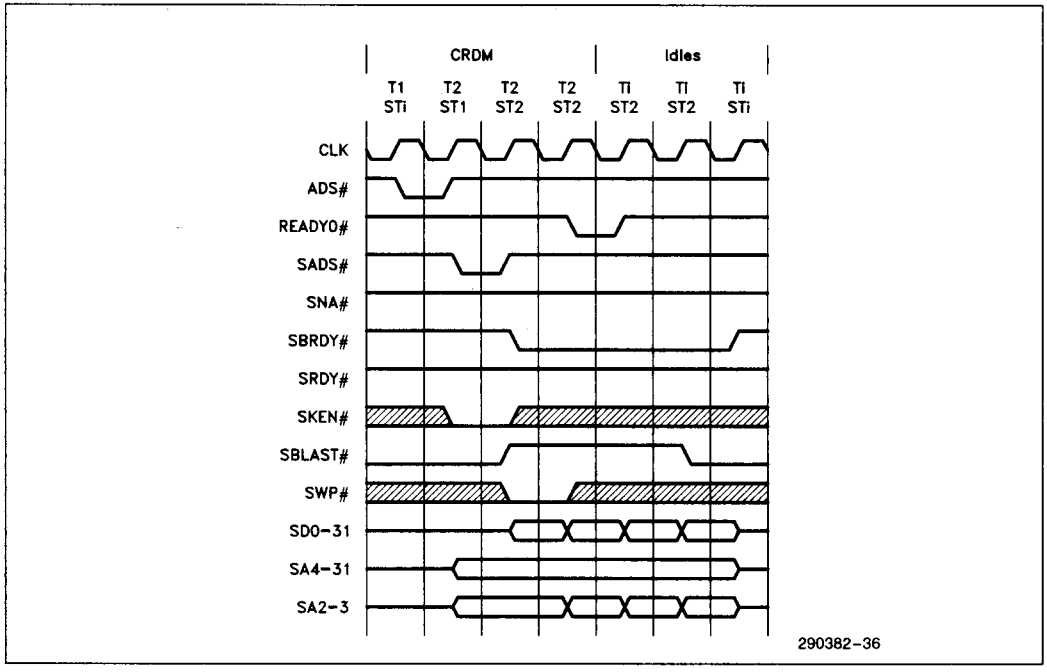

Figure 6.11 - Fastest Burst cycle (one clock burst)

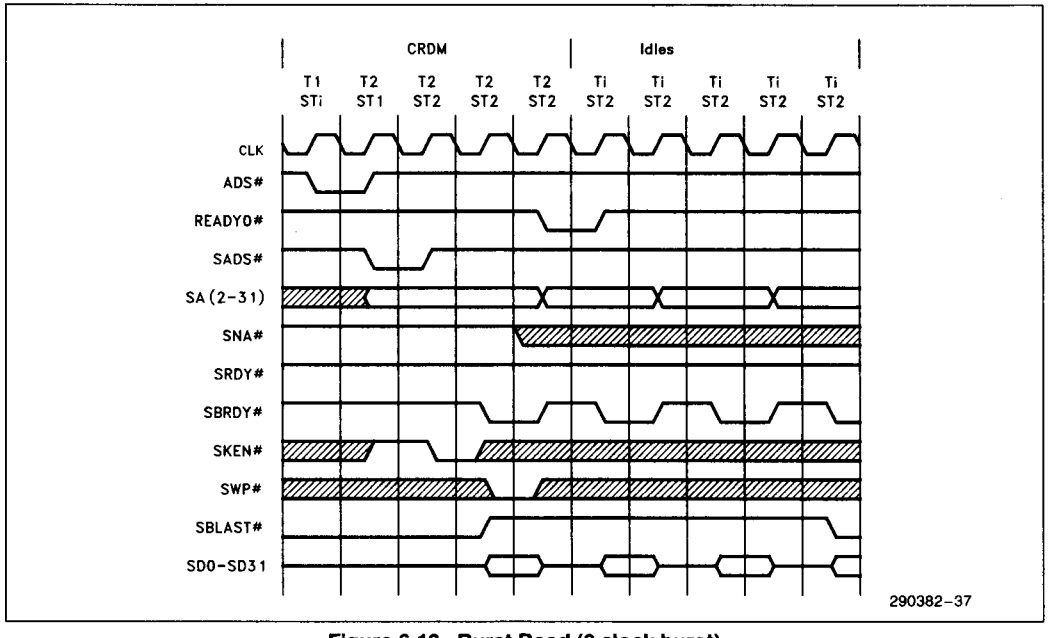

Figure 6.12 - Burst Read (2 clock burst)

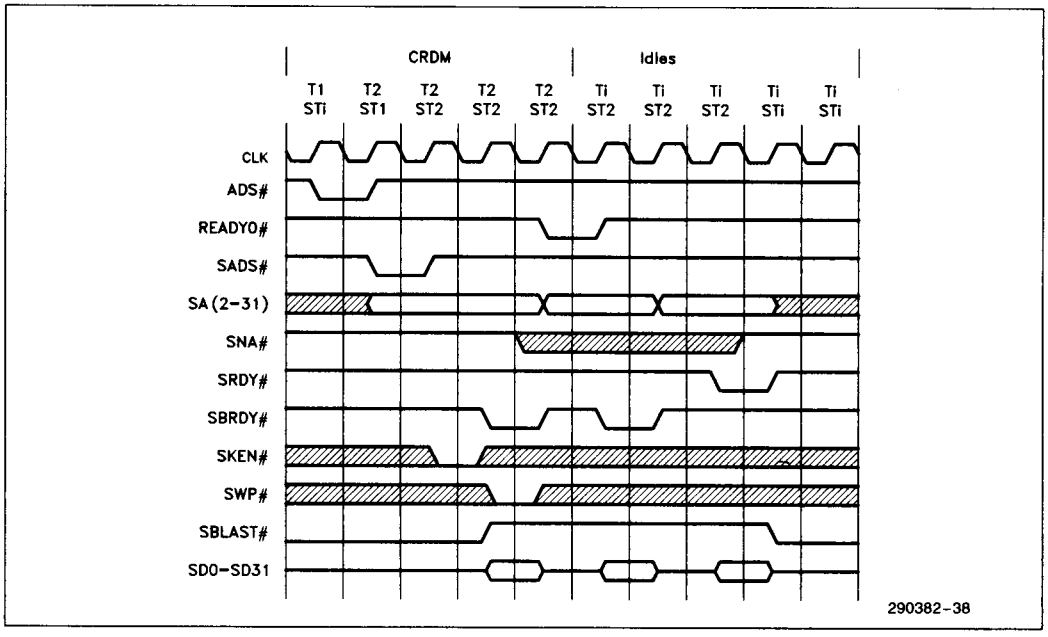

Figure 6.13 - Interrupted Burst Read (2 clock burst)

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6.2 82395DX Latency in System Bus Accesses

The 82395DX acts as a buffer between the 386 DX Microprocessor and the main memory causing some latency in initiating the System Bus cycle (SADS# delay from ADS#) and in completing the cycle (386 READYO# delay from SRDY# or SBRDY#). The 82395DX drives the SADS# one clock after the ADS#. In cacheable cycles, the 82395DX starts driving the SADS# before it decides whether the cycle is a cache hit or miss since the hit/miss decision is valid in the second clock (the first T2 cycle). In case the cycle is a hit, the 82395DX deactivates SADS#. This causes an undesirable glitch on the SADS# signal, and also it causes an SADS# timing incompatibility with the 386 DX Microprocessor i.e. SADS# delay is slightly longer than the ADS# delay. For proper system functionality, SADS# must be sampled by the next clock edge.

At the end of System Bus non- cacheable read cycle, or non- buffered write cycle, the 82395DX drives READYO# active one clock after SRDY#. In a Line Fill cycle, READYO# is activated one clock after the first SBRDY# or SRDY# is sampled active. The set-up timing requirements of SRDY# and system data force one wait state at the end of the cycle.

6.3 SHLDA Latency

For non-LOCK#ed cycles the worst case delay between SHOLD and SHLDA would be when SHOLD is activated during ST2P state, followed by a Line Fill. In this case, the HOLD request will be acknowledged only after the Line Fill is completed. In LOCKed cycles SHLDA will not be asserted until after SLOCK# is negated. The latency would be:

Latency = (Number of ST2Pcycles) + (Number of Line Fill cycles) OR (Number of LOCK#ed cycles)

6.4 Cache Consistency Support

The 82395DX supports snooping using the SEADS# mechanism. Besides insuring the consistency, this mechanism provides multi processing support by having the 82395DX System Bus and the Local Bus running concurrently.

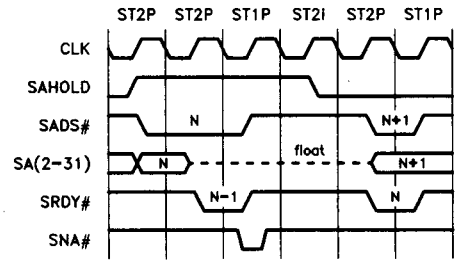
The 82395DX will always float its address bus in the clock immediately following the one in which SAHOLD is received. Thus, no address hold acknowledge is required. When the address bus is floated, the rest of the 82395DX's System Bus will remain active, so that data can be received from a bus cycle that was already underway. Another bus cycle will not begin, and the SADS# signal will not be generated. However, multiple data transfers for burst cycles can occur during address holds.

A companion input to SAHOLD, SEADS# indicates that an external address is actually valid on the address inputs of the 82395DX. When this signal is activated, the 82395DX will read the external address and perform an internal cache invalidation cycle to the address indicated. The internal invalidation cycle occurs one clock after SEADS# is sampled active. In case of contention with 386 DX Microprocessor look up, the invalidation is serviced two clocks after SEADS# was activated. The maximum rate of invalidation cycles is one every other clock. Multiple cache invalidations can occur in a single address hold transfer. SEADS# is not masked by SAHOLD inactive, so cache invalidations can occur during a normal bus cycle. This also means that if SEADS# is driven active when the 82395DX is driving the address bus, the values that are being driven by the 82395DX will be used for a cache invalidation cycle.

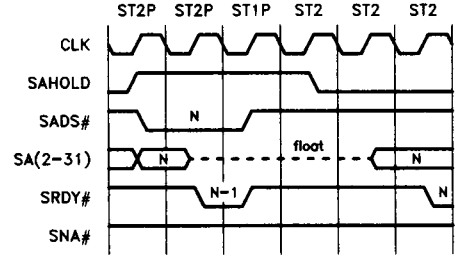
If the 82395DX is running a line fill cycle and an invalidation is driven into the 82395DX in the same clock the first data is returned, or in any subsequent clock, the 82395DX will invalidate that line even if it is the same cache line that the 82395DX is currently filling.

SAHOLD in pipelined cycles: The activation of SAHOLD only causes the system address to be floated in the next clock without changing the behavior of pipelined cycles. If SAHOLD is activated before entering the ST2P state, the 82395DX will move into non-pipeline and drive the SADS# only after the deactivation of SAHOLD. However, if SAHOLD is asserted in the ST2P state and the Nth cycle has already started, the system address is floated but SADS# is kept active until SRDY# (for the N-1 th cycle) is returned. It is the system designers' responsibility to latch the address bus. Note that the address driven on the System Bus after SAHOLD is deasserted (in pipelined cycles) depends on whether SNA# has been sampled active during the SAHOLD state and another cycle is pending. As seen from Figure 6.14, the (N+1)th address will be driven by the 82395DX once SAHOLD was deactivated and SNA# was sampled active, provided there is a cycle pending in the 82395DX. The following figures describe the 82395DX behavior in two cases. First, when SNA# is sampled active and second, in the case of SNA# sampled inactive.

Note that the maximum rate of snooping cycles is every other clock. The first clock edge in which SEADS# is sampled active causes the 82395DX to



(A) - SNA # sampled active



(B) - SNA # sampled inactive

Figure 6.14 - SAHOLD Behavior in Pipelined Cycles

5

latch the system address bus and initiate a cache invalidation cycle. If SEADS# is driven active for more than one clock, only one snooping cycle will be initiated on the first clock edge at which SEADS# is sampled active. The SA4–31 setup and hold timings are specified to the same clock edge in which SEADS# is sampled active.

6.5 Bus Deadlock Resolution Support

In a multi-master system another bus master may require the use of the bus to enable the 82395DX to complete it's current bus request. In this situation, the 82395DX will float it's entire System Bus until the other bus master has completed it's bus transaction.

The 82395DX will float it's System Bus immediately in response to the external system asserting the Fast HOLD (SFHOLD#) signal. The only effect of this signal being sampled active is forcing the 82395DX System Bus pins to float. It is the system designer's responsibility to ensure that no 82395DX cycle is prematurely terminated, and that no new 82395DX cycle is generated during Fast HOLD. When SFHOLD# is deasserted the System Bus address, cycle definition and data are redriven by the 82395DX and the cycle is not restarted. SRDY# and SBRDY# are not recognized during SFHOLD# states. SFHOLD# asserted internally disables SRDY# and SBRDY#.

6.6 Arbitration Mechanism

As more than one device may be connected to the shared system bus, there is a need for arbitration between the devices that wish to utilize the shared resource. The 82395DX supplies the interface signals to an external arbiter (either centralized or distributed) to enable it to perform the task.

The 82395DX provides a normal bus SHOLD/SHLDA handshake protocol, exactly as the 386 DX Microprocessor does on the Local Bus. SHOLD is used to indicate to the 82395DX that another bus master desires control of the 82395DX System Bus. Whenever the 82395DX completes its current bus cycle (a full line transfer if the cycle is a Line Fill), or sequence of LOCK#ed bus cycles, it will grant its external bus to the requesting device by floating it and by driving SHLDA active. The 82395DX will relinquish its System Bus at the end of a bus cycle, even if it has other cycles internally pending. As soon as the 82395DX responds with SHLDA, it tristates all bus control and address outputs. Now, if the System Bus is required by the 82395DX (on behalf of a 386 DX Microprocessor request on the Local Bus) but is not available, processing will cease. Then the 82395DX will have to re-arbitrate on the System Bus by driving SBREQ active.

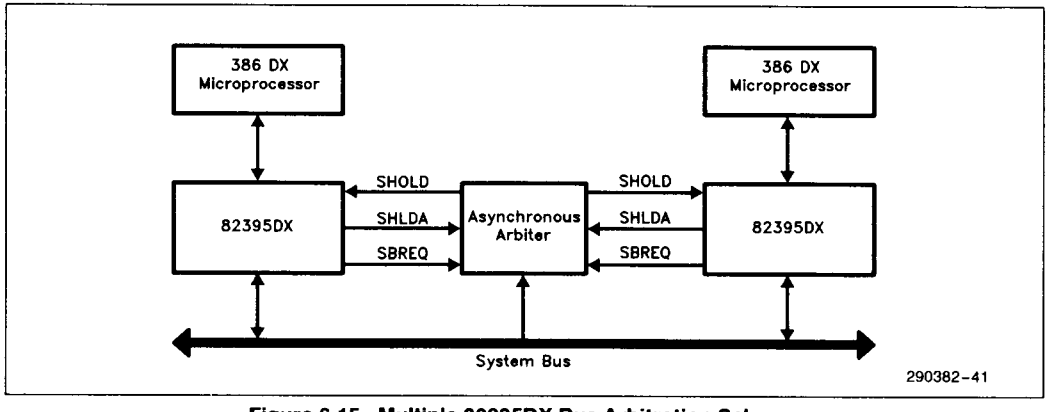


Figure 6.15 - Multiple 82395DX Bus Arbitration Scheme

The SBREQ output is activated whenever the 82395DX has internally generated a bus cycle request. It is inactivated immediately after the 82395DX asserts SADS# of the cycle. By examining this signal, external logic can determine when the 82395DX requires the use of the System Bus and intelligently arbitrate the System Bus among multiple processors. This pin is always driven, regardless of the state of bus hold (See Figure 6.16).

The SHOLD input has higher priority than the pending request. In the case of LOCK#ed System Bus cycles, SHOLD requests will not be acknowledged. Another case is a non-burst Line Fill, where SHOLD is acknowledged after reading the fourth DW, even though SHOLD was activated before.

6.7 Next Near Cycles

For all System Bus cycles, the 82395DX generates a signal, SNENE#, to indicate that the current cycle is in the same 2048 Byte area as the previous memory cycle. Namely, it indicates that address lines A11–A31 of the current System Bus memory cycle are identical to address lines A11–A31 of the previous memory cycle. This signal can be used by an external DRAM system to run CAS# only cycles, therefore increasing the throughput of the memory system. SNENE# timing is identical to system address timing, namely it is valid from SADS# active until SRDY# or SBRDY# is sampled active (non-pipelined cycles) or until SNA# is sampled active (pipelined cycles). SNENE# is valid for all memory cycles, and must be ignored in I/O and idle cycles.

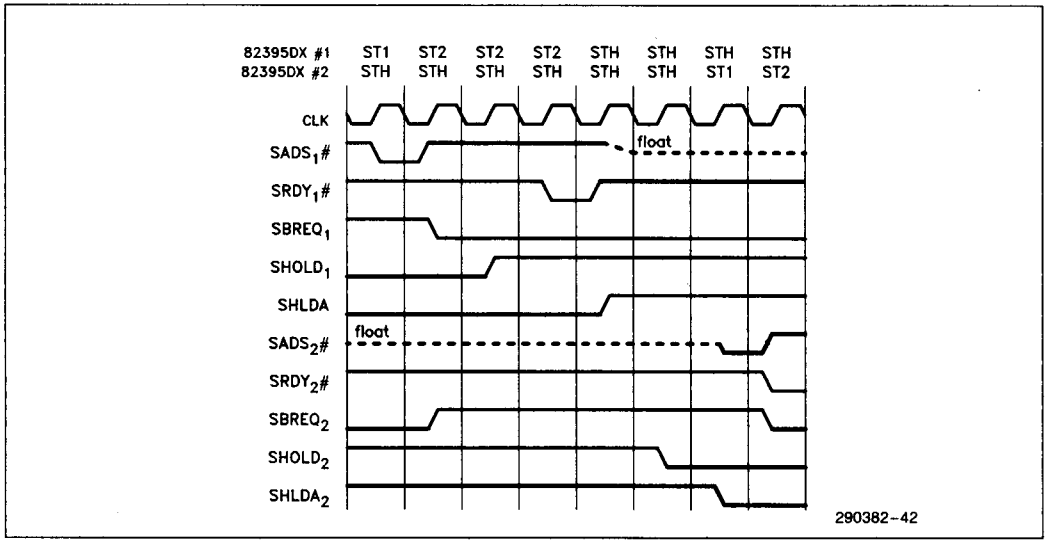


Figure 6.16 - SHOLD/SHLDA/SBREQ Mechanism

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After the 82395DX exits the SHOLD state, SNENE# is always inactive. SNENE# is always inactive in the first memory cycle after a Halt/Shutdown cycle.

If SAHOLD is sampled active while the System Bus is idle, the next 82395DX cycle will have SNENE# inactive. If SAHOLD is sampled active while the 82395DX is running a System Bus cycle, SNENE# will not change until the next SADS# is issued. During SHLDA, SNENE# is floated and the first cycle after SHLDA is deactivated will have SNENE# inactive. SNENE# can run in the pipeline, the same as the system address.

6.8 Write Buffer

The 82395DX is able to internally store up to four write cycles (address, data and status information). All those write cycles will run without wait states on the Local Bus. They will run on the System Bus as soon as the bus is available. In case of a write cycle which cannot be stored since the buffer is full, the 386 DX Microprocessor will be forced to wait until one of the buffered write cycles is completed. READYO# is returned two CLK's after SRDY# or SBRDY# is asserted if the write buffer is full. If the write buffer is not full READYO# is returned one clock after SRDY# or SBRDY# is asserted.

All non cacheable write cycles and LOCK#ed writes are not buffered. In this case, the 82395DX will activate READYO# after getting the SRDY# for the non buffered cycle.

The write buffer maintains the exact original order of appearance of the Local Bus requests. It allows no reordering and no bypassing of any sort.

7.0 TESTABILITY FEATURES

This chapter discusses the requirements for properly testing an 82395DX based system after power up and during normal system operation.

7.1 SRAM Test Mode

This mode is invoked by driving the FLUSH# pin active for less than four clocks during normal operation. SRAM test mode may only be invoked when the 82395DX is in idle state, namely there is no cycle in progress, and no cycle is pending in the 82395DX. The 82395DX exits this mode with subsequent activation of the FLUSH# pin for minimum of 1 clock cycle. If FLUSH# is activated for at least four clock cycles during SRAM test mode, the 82395DX will FLUSH# its cache directory in addition to terminating the SRAM test mode.

SRAM test mode is provided for system diagnostics purposes. In this mode, the 82395DX cache and cache directory are treated as a standard SRAM. The 82395DXs in the system are mapped into address space 256K-512K of the 386 DX Microprocessor memory space, and allows the CPU non-cacheable, non-buffered access to the rest of the memory and address space. Each 82395DX occupies 32KB of address space: 16KB for the cache and 16KB (not fully utilized) for the TAGRAM. The 82395DX, in SRAM mode, will recognize 387 DX Math Coprocessor/Weitek 3167 Floating-Point Coprocessor cycles and Local Bus cycles and handle them the same as it does in its normal mode. This way, the CPU may

Table 7.1 - Entering/Exiting the Various 82395DX Smart Cache Test Modes

Operating Mode	FLUSH#	SAHOLD	Comments
Tristate Test Mode	0	1	Sampled 1 CLK prior to RESET falling. Exit by next activation of RESET with FLUSH# and SAHOLD deactivated.
SRAM Test Mode	0	X	FLUSH# activation for less than four CLKs during normal mode. Exit with activation of FLUSH# for a minimum of one CLK.
Reserved Mode	0	0	Sampled 1 CLK prior to RESET falling.
Normal Mode	1	X	

execute code that tests the 82395DX as a regular memory component, with the only limitation that no code or data may reside in the memory space 256K-512K during this mode. During SRAM test mode, all accesses to memory space other than 256K-512K are handled exactly as in normal mode with the following exceptions:

1. All read cycles are non-cacheable - read hits are not serviced from the cache and read misses don't cause Line Fills.
2. All write cycles are not buffered.
3. All write cycles do not update the cache.
4. Snooping is disabled.

The local address pins indicate the 82395DX internal addresses. The partitioning is as follows:

- A16 = 0 selects the cache directory. A16 = 1 select the cache.
- A15-14 select the "way".
- A12 and A13 select one 82395DX in a multi 82395DX system.
- A11-A4 are the set address.
- A3-2 select a DW in the line. Applicable in cache accesses (A16 = 1).

The user can write to any byte in any line in case of a cache write cycle and write to all the Tagram fields (25 bits) in one Way in one Tagram write cycle. The memory mapping of the SRAM mode is the described in Table 7.2.

As can be seen from Table 7.2, the address space allocated for either Tagram or Cache is 4096 (4K) addresses per way, per 82395DX. The address allocation within each 4K segment is shown in Tables 7.3 and 7.4.

The data presented on the 82395DX local data pins is the SRAM data input. The SRAM data output is also driven on the local data pins. The BE(0-3)# pins indicate the bytes which must be written. During SRAM test mode, all the AC specifications are met. Figures 7.1 and 7.2 depict the SRAM mode read and write cycles respectively. Note that two wait states are inserted during SRAM test mode read cycles and one wait state is inserted in write cycles. The system may extend the number of wait states by gating READYO# for any number of clock cycles (1 clock cycle in Figure 7.1, 0 clock cycles in Figure 7.2).

The user can write to any byte in any line in case of a cache write cycle and write to all the Tagram fields (25 bits) in one way in one Tagram write cycle. The memory mapping of the SRAM test mode described in Table 7.2.

Table 7.2 - SRAM Memory Map

Cache/Tagram	Way	82395DX	Start Address
Cache	3	4	0005F000 h
Cache	3	3	0005E000 h
Cache	3	2	0005D000 h
Cache	3	1	0005C000 h
Cache	2	4	0005B000 h
Cache	2	3	0005A000 h
Cache	2	2	00059000 h
Cache	2	1	00058000 h
Cache	1	4	00057000 h
Cache	1	3	00056000 h
Cache	1	2	00055000 h
Cache	1	1	00054000 h
Cache	0	4	00053000 h
Cache	0	3	00052000 h
Cache	0	2	00051000 h
Cache	0	1	00050000 h
Tagram	3	4	0004F000 h
Tagram	3	3	0004E000 h
Tagram	3	2	0004D000 h
Tagram	3	1	0004C000 h
Tagram	2	4	0004B000 h
Tagram	2	3	0004A000 h
Tagram	2	2	00049000 h
Tagram	2	1	00048000 h
Tagram	1	4	00047000 h
Tagram	1	3	00046000 h
Tagram	1	2	00045000 h
Tagram	1	1	00044000 h
Tagram	0	4	00043000 h
Tagram	0	3	00042000 h
Tagram	0	2	00041000 h
Tagram	0	1	00040000 h

As can be seen from Tables 7.3 and 7.4, the address space allocated for either Tagram or Cache is 4096 (4K) addresses per way, per 82395DX. The address allocation within each 4K segment is shown in Table 7.3 for the Cache and Table 7.4 for the Tagram.

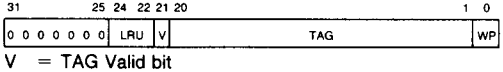
Table 7.3 - Cache Address Allocation

SET	DW	Start Address
255	3	FFC h
255	2	FF8 h
255	1	FF4 h
255	0	FF0 h
.	.	.
.	.	.
.	.	.
.	.	.
1	3	01C h
1	2	018 h
1	1	014 h
1	0	010 h
0	3	00C h
0	2	008 h
0	1	004 h
0	0	000 h

Table 7.4 - TAGRAM Address Allocation

SET	Start Address
255	FFC h
255	FF8 h
255	FF4 h
255	FF0 h
.	.
.	.
.	.
.	.
1	01C h
1	018 h
1	014 h
1	010 h
0	00C h
0	008 h
0	004 h
0	000 h

Double Word format in Tagram read/write:



V = TAG Valid bit
WP = Write Protect bit
"0" = Indicates don't care bits. Writing to these bits will have no effect. When reading the Tagram these bits will have a value of 0.

NOTE:
In Tagram accesses, BE0#-BE3# are ignored in both read and write cycles.

The data presented on the 82395DX D0-D31 pins is the SRAM data input for write cycles and is also the SRAM data output for read cycles during the SRAM test mode. The BE3# - BE0# pins indicate the bytes which will be written to. During SRAM test mode all the AC specifications are met. Figures 7.1 and 7.2 depict the SRAM test mode read and write cycles respectively. The system may extend the number of wait states by gating READYO# for any number of clock cycles (one clock cycle in Figure 7.1, zero in Figure 7.2).

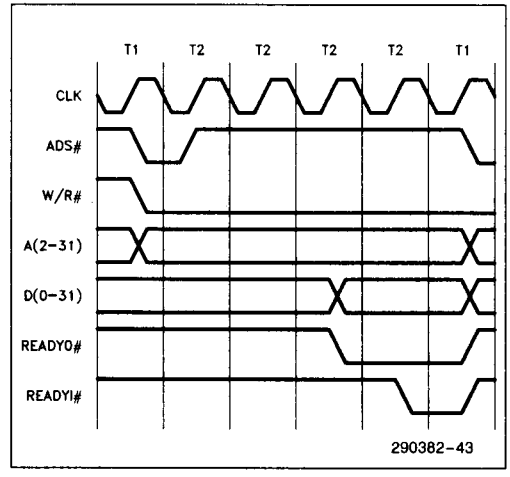


Figure 7.1 - SRAM Mode Read Cycle

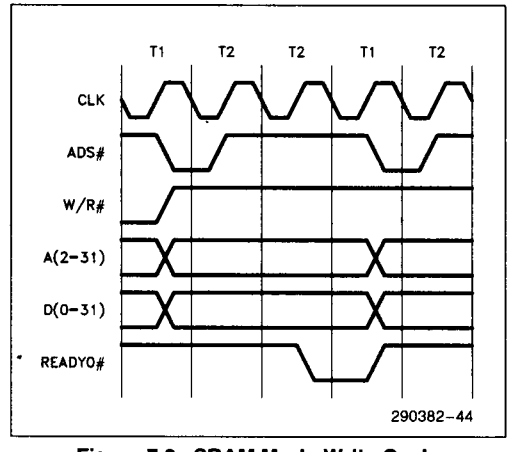


Figure 7.2 - SRAM Mode Write Cycle

7.2 Tristate Output Test Mode

The 82395DX provides the option of isolating itself from other devices on the board for system debugging, by floating all it's outputs. Output tristate mode is invoked by driving the SAHOLD and FLUSH# pins active during RESET. The 82395DX will remain in this mode after RESET is deactivated, if SAHOLD and FLUSH# pins are sampled active in the CLK2 prior to RESET going low (See Figure 7.3). The 82395DX exits this mode with the next activation of RESET with SAHOLD or FLUSH# driven inactive.

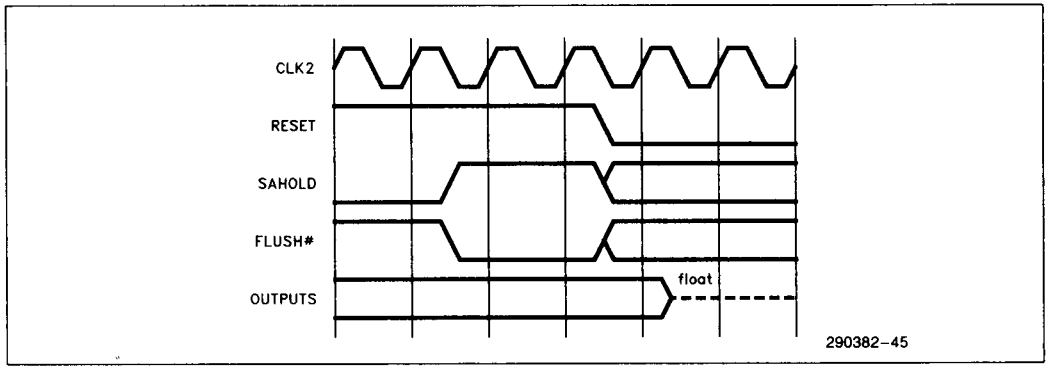


Figure 7.3 - Entering the Tristate Test Mode

8.0 MECHANICAL DATA

8.1 Introduction

This chapter discusses the physical package and its connections.

8.2 Pin Assignment

The 82395DX pinout as viewed from the top side of the component is shown in figure 0.1. V_{CC} and V_{SS} connections must be made to multiple V_{CC} and V_{SS} (GND) planes. Each V_{CC} and V_{SS} pin must be connected to the appropriate voltage level. The circuit board must contain V_{CC} and V_{SS} (GND) planes for power distribution and all V_{CC} and V_{SS} pins must be connected to the appropriate planes.

8.3 Package Dimensions and Mounting

The 82395DX package is a 196 lead plastic quad flat pack (PQFP). For information on dimensions refer to Table 8.1 and Figures 8.1–8.3.

8.4 Package Thermal Specification

The 82395DX is specified for operation when the case temperature is within the range of 0–85 °C. The case temperature may be measured in any environment, to determine whether the 82395DX is within the specified operating range. The case temperature must be measured at the center of the top surface opposite the pins.

196 Pin PQFP Package Key Attributes:

Electrical:

L	6-20	nH	(lead)
L	3-6	nH	(V_{CC}/V_{SS})
C	<2.3	pF	(Loading)
C	<1.6	pF	(Id/Id)
C	130-200	nH	(V_{CC}/V_{SS})

Thermal:

"See Table 8.1".

Lead Stiffness:

In-Plane	17	gm/mil
Transverse	18	gm/mil

Thermal characterization of the 196 lead PQFP package yielded the information contained in Figures 8.4–8.6.

Table 8.1 - 196 Lead PQFP Package Typical Thermal Characteristics

Parameter	Thermal Resistance—°C/Watt							
	Airflow LFM							
	0	50	100	200	400	600	800	1000
θ_{JC}	5	5	5	5	5	5	5	5
θ_{JA}	24	22	21	19	17	15	14	13

NOTES:
1. Table 8.1 applies to the 82395DX Smart Cache PQFP plugged into the socket or soldered directly onto the board.
2. $\theta_{CA} = \theta_{JA} - \theta_{JC}$, where θ_{CA} is the case to ambient thermal resistance, θ_{JA} is the junction to ambient thermal resistance and θ_{JC} is the junction to case thermal resistance.

The ambient temperature must be controlled to prevent T_{CASE} from being violated. The ambient temperature can be calculated from the thermal resistance values with the following equations:

$T_J = T_{CASE} + P * \theta_{JC}$

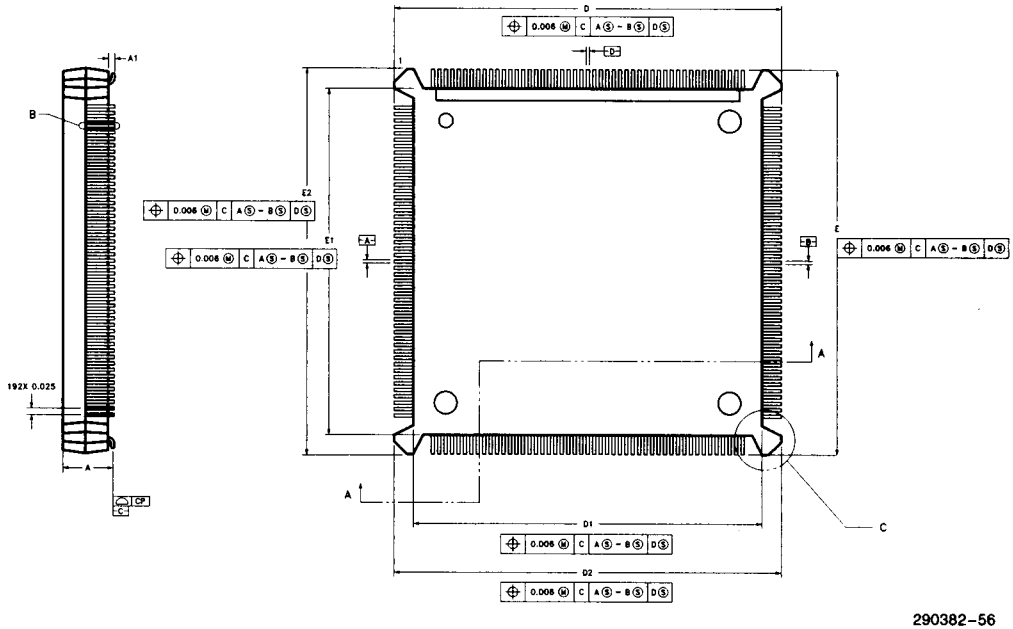
$T_{amb} = T_J - P * \theta_{JA}$

$T_{CASE} = T_{amb} + P * [\theta_{JA} - \theta_{JC}]$

Values for θ_{JA} and θ_{JC} are given in Table 8.1 for the 196 lead PQFP package at various airflow rates. Table 8.2 shows the maximum T_{amb} allowable (without exceding T_{CASE}) at various airflows. Note that T_{amb} can be improved further by attaching "fins" or a "heat sink" to the package.

Table 8.2 - Ambient Temperature Requirements

Using I_{CC2}	Ambient Temperature Not to Exceed T_{CASE} = 85°C							
	Airflow LFM							
	0	50	100	200	400	600	800	1000
T_{amb} @ 33 MHz (°C)	40.4	45.1	47.4	52.1	56.8	61.5	63.9	66.2
T_{amb} @ 25 MHz (°C)	45.1	49.3	51.4	55.6	59.8	64.0	66.1	68.7
T_{amb} @ 20 MHz (°C)	48.0	51.9	53.8	57.7	61.6	65.5	67.5	69.4



NOTES:
1. Interpret dimensions and tolerances in accordance with ANSI Y14.5M-1982.
2. Data enclosed in parentheses is for reference only.

Figure 8.1 - Principal Dimensions and Data

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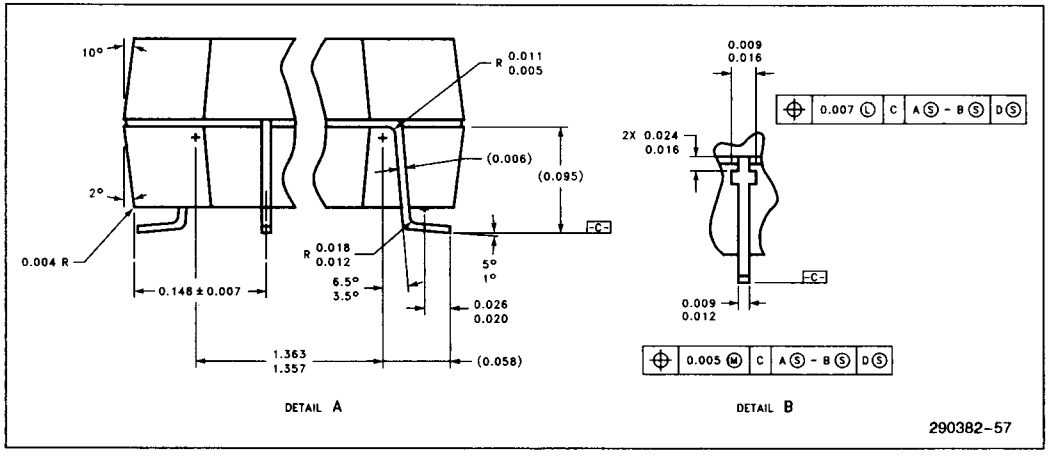

Figure 8.2 - Typical Lead

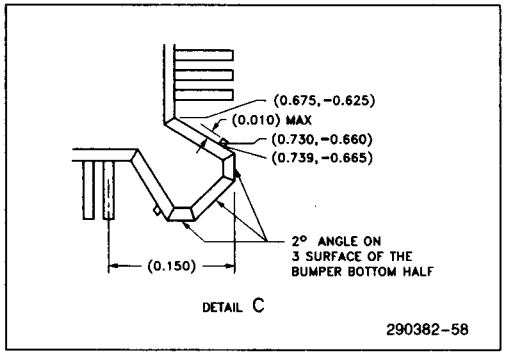

Figure 8.3 - Detail C

Table 8.3 - Symbol List and Dimensions for 196 Lead Plastic Quad Flat Pack Package

Symbol	Description of Dimensions	Min	Max
A	**Package Height:** Distance from the seating plane to the highest point of body.	0.160	0.175
A1	**Standoff:** The distance from the seating plane to the base plane.	0.020	0.035
D, E	**Overall Package Dimension:** Lead tip to lead tip.	1.470	1.485
D1, E1	**Plastic Body Dimension**	1.347	1.353
D2, E2	**Bumper Distance** Without FLASH With FLASH	 1.497 1.497	 1.503 1.510
CP	**Seating Plane Coplanarity**	0.000	0.004

NOTES:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Dimensions are in inches.
3. Data enclosed in parenthesis is for reference only.

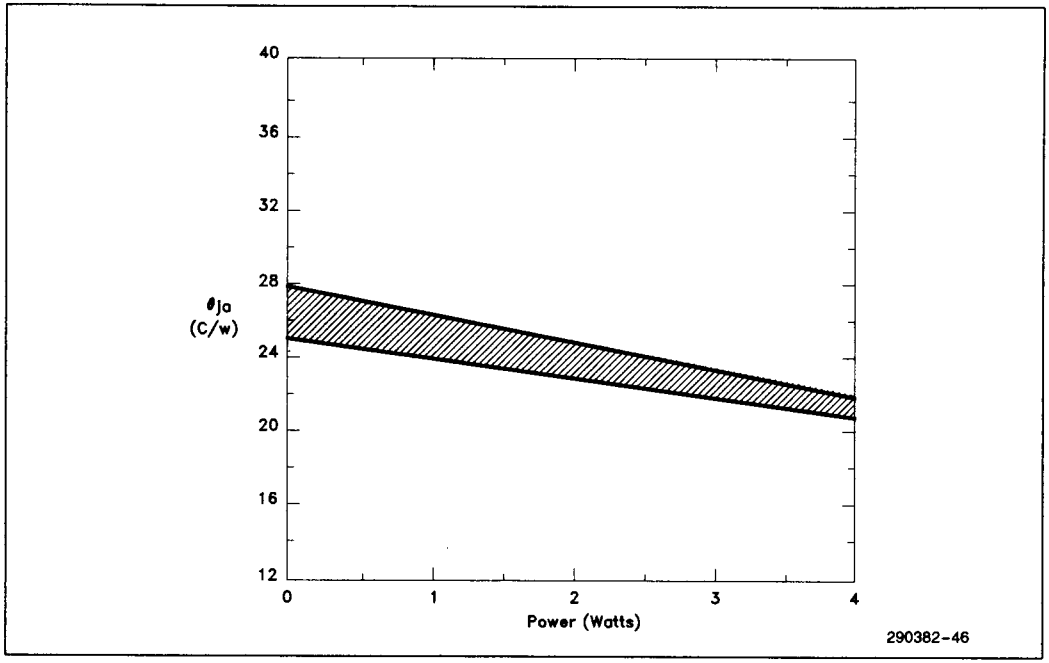

Figure 8.4 - Junction to Ambient Thermal Resistance vs Power

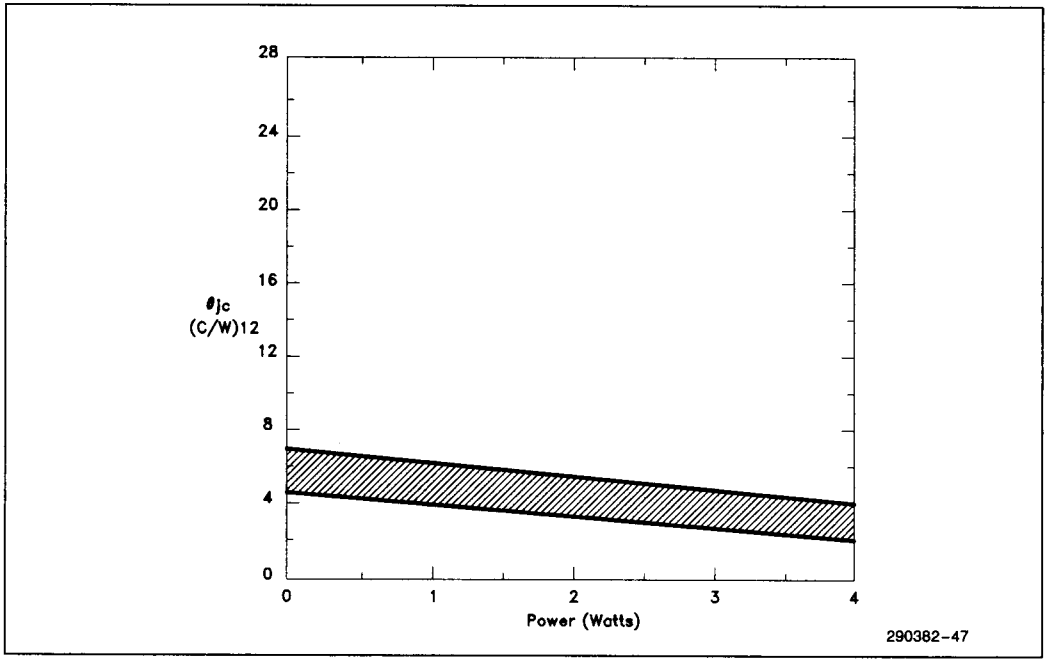

Figure 8.5 - Junction to Case Thermal Resistance vs Power

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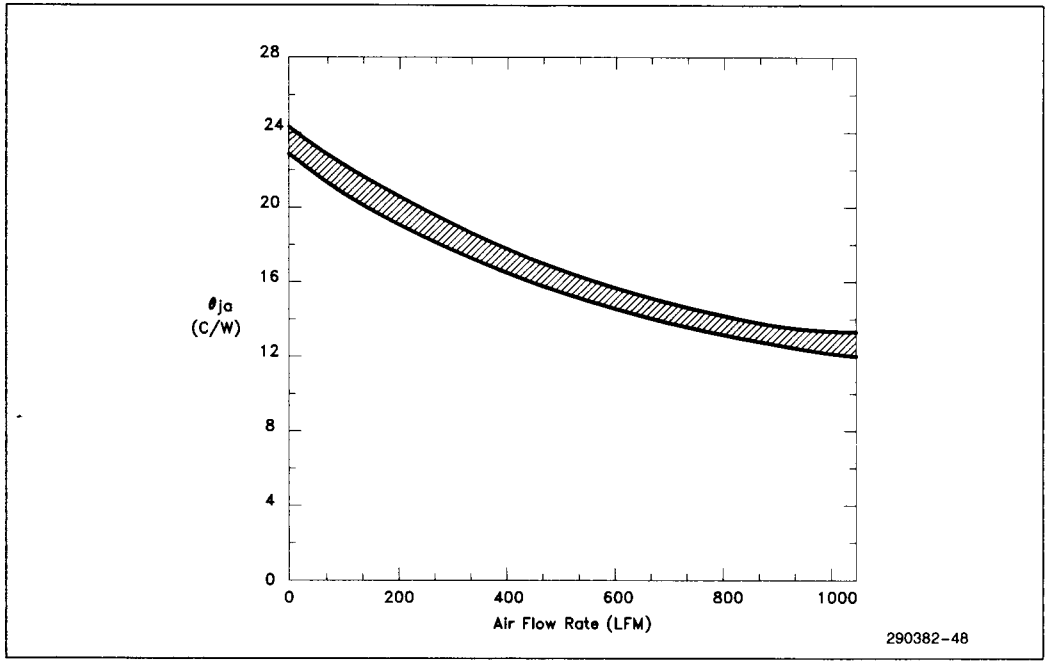

Figure 8.6 - Junction to Ambient Thermal Resistance vs Air Flow Rate

9.0 ELECTRICAL DATA

This chapter presents the A.C. and D.C. specifications for the 82395DX.

9.1 Power and Grounding

The 82395DX has a high clock frequency and 108 output buffers which can cause power surges as multiple output buffers drive new signal levels simultaneously. For clean on-chip power distribution at high frequency, 15 V_{CC} and 17 V_{SS} pins separately feed power to the functional units of the 82395DX.

Power and ground connections must be made to all external V_{CC} and V_{SS} pins of the 82395DX. On the circuit board, all V_{CC} pins must be connected on a V_{CC} plane and all V_{SS} pins must be connected on a GND plane.

9.1.1 POWER DECOUPLING RECOMMENDATIONS

Liberal decoupling capacitors must be placed near the 82395DX. The 82395DX driving it's 32 bit data buses and 30 bit system address bus at high frequency can cause transient power surges, particularly when driving large capacitive loads. Low inductance capacitors and interconnects are recommended for the best high frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the 82395DX and the decoupling capacitors as much as possible.

9.1.2 RESISTOR RECOMMENDATIONS

The 82395DX does not have any internal pullup resistors. All unused inputs must be tied externally to a solid logic level. The outputs that require external pullup resistors are listed in table 9.1. A particular designer may have reason to adjust the resistor values recommended here, or alter the use of pull-up resistors in other ways.

9.2 Absolute Maximum Ratings

Storage Temperature ..... −65 ° C to 150 ° C

Case Temperature under Bias ..... −65 ° C to 110 ° C

Supply voltage with Respect to V_{SS} ..... −0.5V to 6.5V

Voltage on Other Pins ..... −0.5V to V_{CC} +0.5V

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Table 9.1 - Pullup Resistor Recommendations

Signal	Pullup Value	Purpose
READYO#	20K Ohms ±10%	Lightly pull READYO# inactive when the 82345DX is not driving it. Allows the selected 82395DX to drive READYO# while it is inactive for the others.
SADS#	20K Ohms ±10%	Lightly pull SADS# inactive when the 82345DX is not driving it. Allows the selected 82395DX to drive SADS# while it is inactive for the others.
SLOCK#	20K Ohms ±10%	Lightly pull SLOCK# inactive for 82395DX SHOLD states.

9.3 DC SPECIFICATIONS Tcase = 0°C to +85°C, Vcc = 5V ±5%

Table 9.2 - DC Specifications

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
VIL	Input Low Voltage	−0.3	0.8	V	
VIH	Input High Voltage	2.0	Vcc+0.3	V	
VCIL	CMOS Input Low	−0-.3	0.8	V	See Note 6
VCIH	CMOS Input High	Vcc−0.8	Vcc+0.3	V	See Note 6
VOL	Output Low Voltage		0.45	V	See Note 1
VOH	Output High Voltage	2.4		V	See Note 2
VCOL	CMOS Output Low Voltage		0.45	V	See Notes 1,7
VCOH	CMOS Output High Voltage	Vcc−0.45		V	See Notes 2,7
ILI	Input Leakage		±15	uA	OV<Vin<Vcc
ILO	Output Leakage		±15	uA	0.45V<Vout<Vcc
Cin	Cap. Input		10	pF	See Note 4
I_{CC}	Power Supply Current 33 MHz @ T_{CASE} = 0°C		650	mA	See Note 3
	Power Supply Current 25 MHz @ T_{CASE} = 0°C		600	mA	See Note 3
	Power Supply Current 20 MHz @ T_{CASE} = 0°C		550	mA	See Note 3

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9.3 DC SPECIFICATIONS Tcase = 0°C to +85°C, Vcc = 5V ±5% (Continued)

Table 9.2 - DC Specifications (Continued)

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
I_{CC2}	Power Supply Current 33 MHz @ T_{CASE} = 85°C		470	mA	See Note 8
	Power Supply Current 25 MHz @ T_{CASE} = 85°C		420	mA	See Note 8
	Power Supply Current 20 MHz @ T_{CASE} = 85°C		390	mA	See Note 8

NOTES:
1. This parameter is measured at IOL = 4mA for all the outputs.
2. This parameter is measured at IOH = 1mA for all the outputs.
3. Measured with inputs driven to CMOS levels, V_{CC} = 5.25V, T_{CASE} = 0°C, using a test pattern consisting of 33% read, 33% write and 33% idle cycles. Refer to Table 8.2 for the ambient temperature requirements.
4. CLK2 input capacitance is 20pF.
5. No activity on the Local/System Bus.
6. Applies to CLK2, READYO# inputs.
7. Applies to READYO# output.
8. I_{CC2} was measured using V_{CC} of 5.0V at T_{CASE} = 85°C. This I_{CC} measurement is representative of the worst case I_{CC} at T_{CASE} = 85°C with the outputs unloaded. This is not 100% tested.

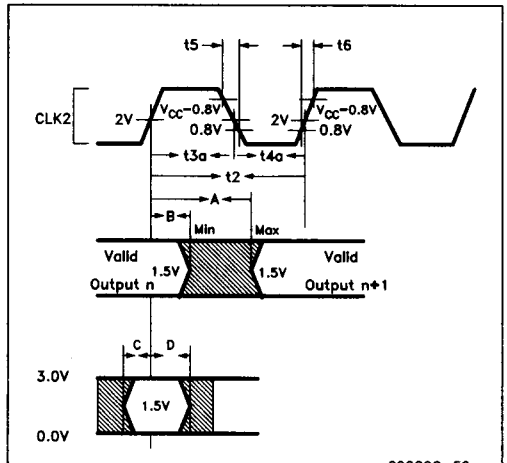
9.4 AC Characteristics

Some of the 82395DX AC parameters are clock-frequency dependent. Thus, while the part functions properly at the entire frequency range specified by the t1 spec, the AC parameters are guaranteed at three distinct frequencies only: 20MHz, 25MHz and 33MHz. Note that, for example, when a 33MHz part operates at 25Mhz CLK frequency, the AC parameters under "25MHz" column must be used.

- Functional operating range: VCC = 5V ±5%, Tcase = 0°C to +85°C.
- All AC parameters are measured relative to 1.5V for falling and rising, CLK2 is at 2V.
- All outputs tested at a 50pF load. In case of overloaded signals, the derating factor is 1ns for every extra 25pF load.
- All parameters are referred to PHI1 unless otherwise noted.
- The reference Figure of CLK2 parameters and AC measurements level is Figure 9.1 and RESET and internal phase is Figure 3.2.
- Dynamic frequency changes are not allowed.

9.4.1 TIMING CONSIDERATIONS FOR CACHE EXTENSIONS

The values listed in Tables 9.3 and 9.4 for the AC parameters are valid for a design using one 82395DX with its 16KB cache or two 82395DXs to extend the cache size to 32KB. For a design using four 82395DXs to extend the cache size to 64KB, some timing adjustments must be made due to the increased capacitive load on the signal traces. The capacitive derating curve (see Figure 9.6) must be used to accurately determine the impact on AC timings.



Legend:
A - Maximum Output Delay
B - Minimum Output Delay
C - Minimum Input Setup Time
D - Minimum Input Hold Time

Figure 9.1 - Drive Levels and Measurement Points for AC Specifications

9.4.2 AC CHARACTERISTICS TABLES Tcase = 0°C to 85°C, Vcc = 5V ±5%

Table 9.3 - Local Bus Signal AC Parameters

Symbol	Parameter	20 MHz		25 MHz		33 MHz		Units	Notes
		Min	Max	Min	Max	Min	Max		
t1	Operating Frequency	15.4	20	15.4	25	15.4	33	MHz	Internal CLK
t2	CLK2 Period	25	32.5	20	32.5	15	32.5	ns	
t3a	CLK2 High Time	8		7		6.25		ns	Measured at 2V
t3b	CLK2 High Time	5		5		4.5		ns	Measured at 3.7V
t4a	CLK2 Low Time	8		7		6.25		ns	Measured at 2V
t4b	CLK2 Low Time	6		5		4.5		ns	Measured at 0.8V
t5	CLK2 Fall Time		7		7		4	ns	Note 1
t6	CLK2 Rise Time		7		7		4	ns	Note 2
t7a	A2–A31 Setup Time	24		17		13		ns	
t7b	LOCK# Setup Time	12		11		9		ns	
t7c	BE0–3# Setup Time	18		14		13		ns	
t8	A2–A31, BE0–3#, LOCK# Hold Time	3		3		3		ns	
t9a	M/IO#, D/C#, W/R# Setup Time	20		17		13		ns	
t9b	ADS# Setup Time	23		17		13.5		ns	
t10	M/IO#, D/C#, W/R#, ADS# Hold Time	3		3		3		ns	
t11	READYI# Setup Time	12		9		7		ns	
t12	READYI# Hold Time	4		4		4		ns	
t13	LBA#, NPI# Setup Time	10		9		5.5		ns	Note 7
t14	RESET Setup Time	12		10		5		ns	
t15a	LBA#, NPI# Hold Time	3		3		3		ns	
t15b	RESET Hold Time	4		3		2		ns	
t16	D0–31 Setup Time	10		11		4		ns	Note 3
t17	D0–31 Hold Time	2		2		2		ns	Note 3
t18	D0–31 Valid Delay	3	38	3	32	3	24	ns	
t19	D0–31 Float Delay		25		20		17	ns	Note 5
t20	READYO# Valid Delay	4	32	4	25	4	17.5	ns	
t21	READYO# Float Delay		25		20		15	ns	Notes 4,5
t22	READYO# Setup Time	16		13		11		ns	
t23	READYO# Hold Time	4		4		4		ns	
t24a	CONF# Setup Time	12		10		5		ns	Note 8
t24b	CONF# Setup Time	16		13		11		ns	Note 9
t25a	CONF# Hold Time	4		3		2		ns	Note 8
t25b	CONF# Hold Time	4		4		4		ns	Note 9

Table 9.4 - System Bus Signal AC Parameters

Symbol	Parameter	20 MHz		25 MHz		33 MHz		Units	Notes
		Min	Max	Min	Max	Min	Max		
t31	SA2–31, SBE0–3#, SLOCK#, SD/C#, SW/R#, SM/IO# Valid Delay	3	28	3	21	3	15	ns	
t32	SA2–31, SBE0–3#, SLOCK#, SD/C#, SW/R#, SM/IO# Float Delay	3	30	3	30	3	20	ns	Note 5
t33	SBLAST#, SHLDA, SBREQ, SNENE# Valid Delay	3	28	3	22	3	20	ns	
t34	SBLAST#, SNENE# Float Delay	3	30	3	25	3	20	ns	Note 5
t35	SD0–31 Write Data Valid Delay	3	38	3	27	3	24	ns	Note 4
t36	SD0–31 Float Delay		27		22	3	17	ns	Notes 4,5
t37	SA4–31 Setup Time	10		9		7		ns	
t38	SA4–31 Hold Time	3		3		3		ns	
t39	SD0–31 Read Setup Time	11		7		5		ns	
t40	SD0–31 Read Hold Time	3		3		3		ns	
t41	SNA# Setup Time	18		13		7		ns	Note 3
t42	SNA# Hold Time	3		3		3		ns	Note 3
t43a	SKEN# Setup Time	17		12		6.5		ns	
t43b	SHOLD, SAHOLD, SFHOLD# Setup Time	18		15		12		ns	
t43c	SWP# Setup Time	17		12		10		ns	
t44	SHOLD, SKEN#, SWP#, SFHOLD#, SAHOLD Hold Time	3		3		3		ns	
t45a	SEADS# Setup Time	14		11		7		ns	
t45b	SRDY#, SBRDY# Setup Time	14		11		9		ns	
t46	SEADS#, SRDY#, SBRDY# Hold Time	4		4		4		ns	
t47	FLUSH#, A20M# Setup Time	18		13		8		ns	Note 6
t48	FLUSH#, A20M# Hold Time	3		3		3		ns	Note 6
t49	SADS# Valid Delay	3	28	3	22	3	16	ns	
t50	SADS# Float Delay		25		20		15	ns	Notes 4,5

NOTES:
1. Tf is Measured at 3.7V to 0.8V. Tf is not 100% tested.
2. Tr is Measured at 0.8V to 3.7V. Tr is not 100% tested.
3. The specification is relative to PHI2 i.e. signal sampled by PHI2.
4. The specification is relative to PHI2 i.e. signal driven by PHI2.
5. Float condition occurs when maximum output current becomes less than ILO in magnitude. Float delay is not 100% tested.
6. The signal is allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
7. The signal is not sampled. It must be valid through the entire cycle (as the Address lines).
8. When tested as the second 82395DX.
9. When tested as the third 82395DX.

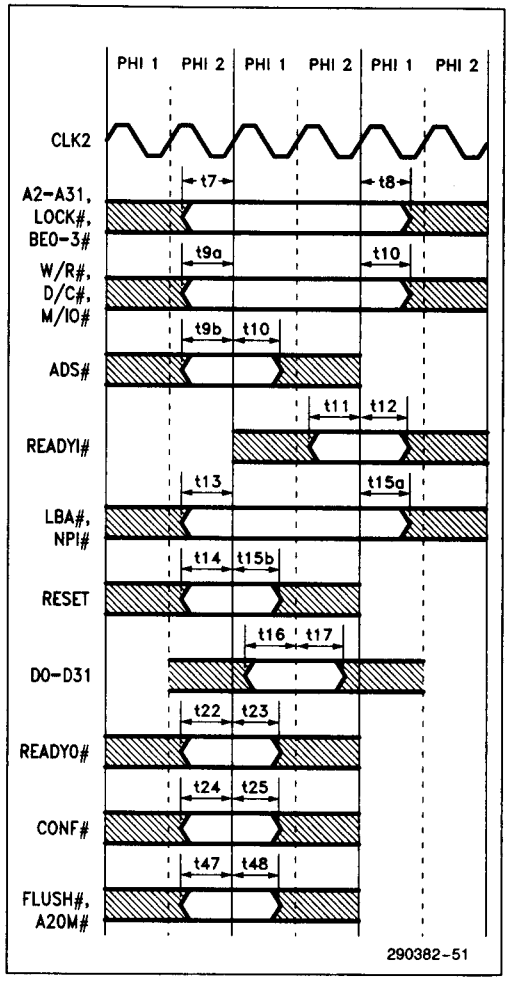


Figure 9.2 - AC Timing Waveforms - Local Bus Input Setup and Hold Timing

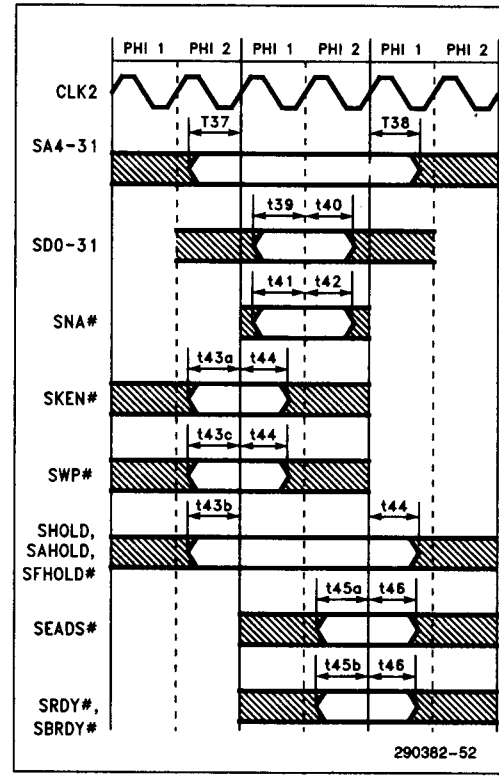


Figure 9.3 - AC Timing Waveforms - System Bus Input Setup and Hold Timing

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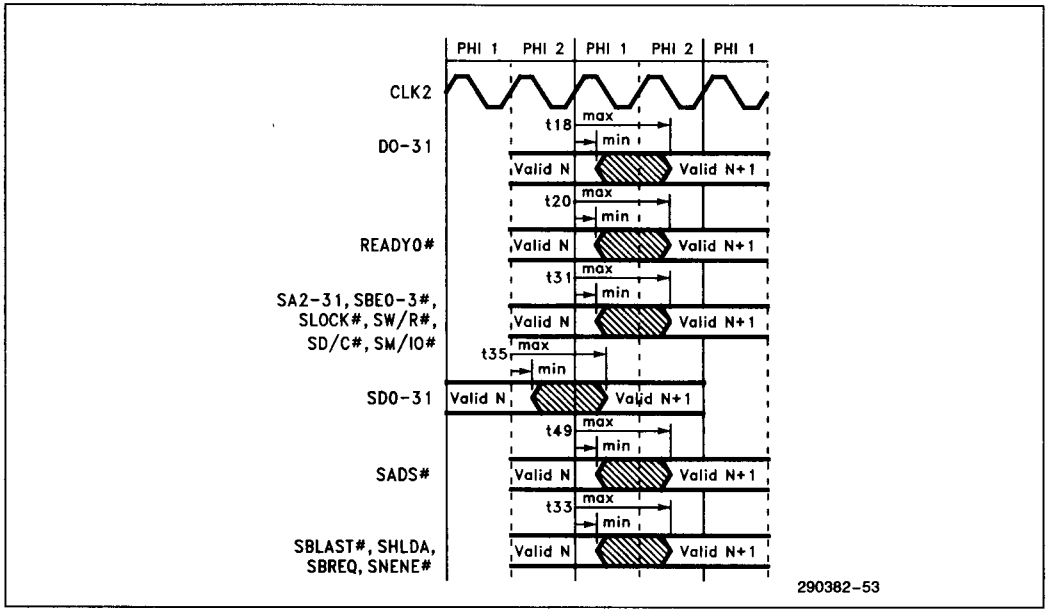

Figure 9.4 - AC Timing Waveforms - Output Valid Delay

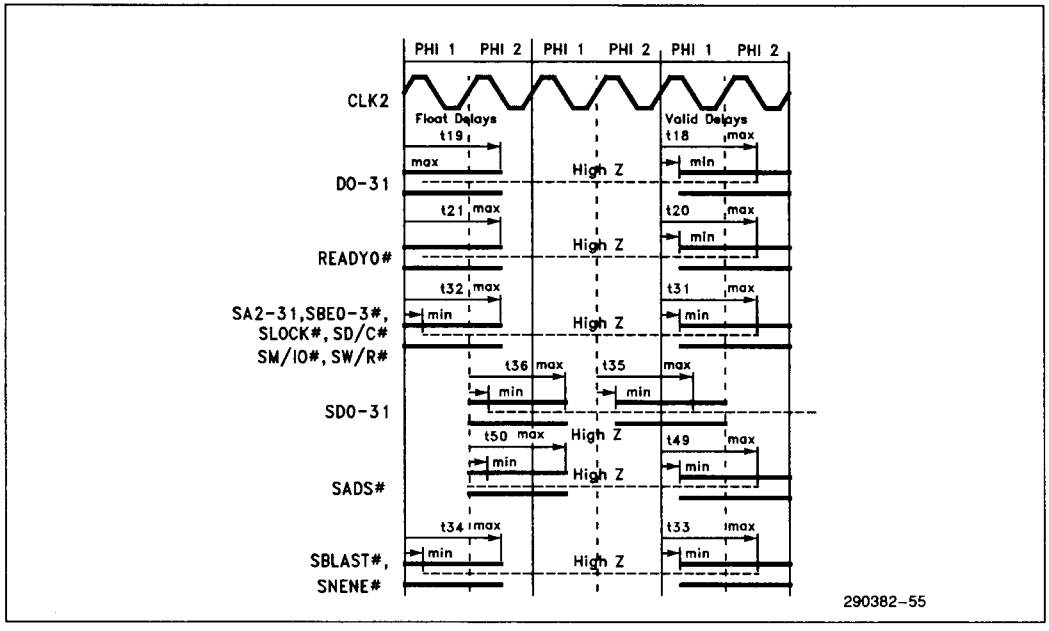

Figure 9.5 - AC Timing Waveforms - Output Float Delays

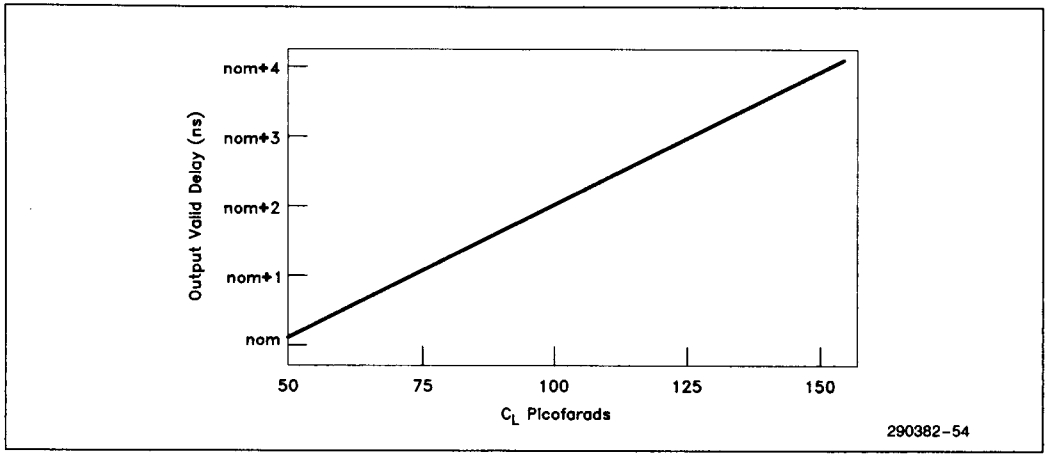

Figure 9.6 - Typical Output Valid Delay vs Load Capacitance at Maximum Operating Temperature (C_L = 50pF)

APPENDIX A

Term	Definition	Term	Definition
AC	Alternating Current	RAM	Random Access Memory
ALF	Aborted Line Fill	SB	System Bus
CDF	Cache Directory FLUSH	TV	Tag Valid
CDL	Cache Directory Lookup	WP	Write Protect
CDS	Cache Directory SNOOP	xxK	xx thousand
CDT	Testability Access	xxKB	xx K Bytes
CDU	Cache Directory Update	xxGB	xx Giga Bytes
CR	Cache Read	xWS	xx Wait States
CW	Cache Write	T1	Local Bus State
CU	Cache Update	T2	Local Bus State
CT	Testability Access	TI	Local Bus State
CPU	Central Processing Unit	TH	Local Bus State
CHMOS	Complimentary High Performance	ST1	System Bus State
	Metal Oxide Semiconductor	ST1P	System Bus State
CRDH	Cache Read Hit	ST2	System Bus State
CRDM	Cache Read Miss	ST2P	System Bus State
CWTH	Cache Write Hit	STI	System Bus State
DC	Direct Current	STH	System Bus State
DRAM	Dynamic Random Access Memory	PHI1	1st CLK2 cycle in a 2 CLK2 CLK cycle
DMA	Direct Memory Access	PHI2	2nd CLK2 cycle in a 2 CLK2 CLK cycle
DW	Double Word	C	Celsius
GND	Ground	V	Volts
I/O	Input/Output	μA	10^{-6} Amps
LB	Local Bus	mA	10^{-3} Amps
LBA	Local Bus Access	pF	10^{-12} Farads
LRU	Least Recently Used	MHz	10^{6} Hertz
PQFP	Plastic Quad Flat Pack	ns	10^{-9} seconds