# BLL6H0514L-130; BLL6H0514LS-130 LDMOS driver transistor Rev. 3 — 1 September 2015

**AMMPLEON** 

Product data sheet

## **Product profile**

#### 1.1 General description

130 W LDMOS transistor intended for pulsed applications in the 0.5 GHz to 1.4 GHz range.

**Application information** Table 1.

Typical RF performance at  $T_{case} = 25$  °C;  $I_{Dq} = 50$  mA; in a class-AB application circuit.

Mode of operation	f	t <sub>p</sub>	δ	V <sub>DS</sub>	PL	Gp	RLin	$\eta_{D}$	P <sub>droop(pulse)</sub>	t <sub>r</sub>	t <sub>f</sub>
	(MHz)	(μs)	(%)	(V)	(W)	(dB)	(dB)	(%)	(dB)	(ns)	(ns)
pulsed RF	960 to 1215	128	10	50	130	19	10	54	0	15	8
	1200 to 1400	300	10	50	130	17	10	50	0	15	8

#### 1.2 Features and benefits

- Easy power control
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (0.5 GHz to 1.4 GHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

#### 1.3 Applications

Amplifiers for pulsed applications in the 0.5 GHz to 1.4 GHz frequency range

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLL6H0514L	-130 (SOT1135A)		
1	drain		,
2	gate	1	لــا
3	source [1]		2 — 3 3 sym112
BLL6H0514L	S-130 (SOT1135B)		
1	drain		4
2	gate	1	نے
3	source [1]	3	2 — 3 3 sym112

## 3. Ordering information

Table 3. Ordering information

Type number	Packag	Package			
	Name	Description	Version		
BLL6H0514L-130	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT1135A		
BLL6H0514LS-130	-	earless flanged ceramic package; 2 leads	SOT1135B		

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol Parameter Conditions	Min	Max	Unit
V <sub>DS</sub> drain-source voltage	-	100	V
V <sub>GS</sub> gate-source voltage	-0.5	+13	V
I <sub>D</sub> drain current	-	18	Α
T <sub>stg</sub> storage temperature	-65	+150	°C
T <sub>j</sub> junction temperature	-	200	°C

<sup>[1]</sup> Connected to flange.

#### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
$Z_{\text{th(j-c)}}$	transient thermal impedance from junction to case	T <sub>case</sub> = 85 °C; P <sub>L</sub> = 130 W		
		$t_p$ = 100 $\mu$ s; $\delta$ = 10 %	0.17	K/W
		$t_p$ = 200 $\mu$ s; $\delta$ = 10 %	0.22	K/W
		$t_p$ = 300 $\mu$ s; $\delta$ = 10 %	0.25	K/W
		$t_p$ = 100 $\mu$ s; $\delta$ = 20 %	0.23	K/W
		$t_p$ = 1 ms; $\delta$ = 10 %	0.36	K/W

#### 6. Characteristics

Table 6. DC characteristics

 $T_i = 25$  °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 630 \text{ mA}$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS}$ = 10 V; $I_{D}$ = 135 mA	1.3	1.8	2.25	V
$I_{DSS}$	drain leakage current	$V_{GS}$ = 0 V; $V_{DS}$ = 50 V	-	-	1.4	μΑ
I <sub>DSX</sub>	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	15.8	18	-	Α
I <sub>GSS</sub>	gate leakage current	$V_{GS} = 11 \text{ V}; V_{DS} = 0 \text{ V}$	-	-	140	nA
9 <sub>fs</sub>	forward transconductance	$V_{DS}$ = 10 V; $I_{D}$ = 135 mA	806	-	1578	mS
R <sub>DS(on)</sub>	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 6.25 \text{ V};$ $I_D = 135 \text{ mA}$	-	200	275	mΩ

#### Table 7. RF characteristics

Mode of operation: pulsed RF;  $t_p$  = 300  $\mu$ s;  $\delta$  = 10 %; RF performance at  $V_{DS}$  = 50 V;  $I_{Dq}$  = 50 mA; f = 1.2 GHz to 1.4 GHz;  $T_{case}$  = 25 °C; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$P_L$	output power		130	-	-	W
V <sub>DS</sub>	drain-source voltage	P <sub>L</sub> = 130 W	-	-	50	V
G <sub>p</sub>	power gain	P <sub>L</sub> = 130 W	15	17	-	dB
RLin	input return loss	P <sub>L</sub> = 130 W	7	10	-	dB
$\eta_{D}$	drain efficiency	P <sub>L</sub> = 130 W	45	50	-	%
P <sub>droop(pulse)</sub>	pulse droop power	P <sub>L</sub> = 130 W	-	0	0.3	dB
t <sub>r</sub>	rise time	P <sub>L</sub> = 130 W	-	20	50	ns
t <sub>f</sub>	fall time	P <sub>L</sub> = 130 W	-	6	50	ns

#### 6.1 Ruggedness in class-AB operation

The BLL6H0514L-130 and BLL6H0514LS-130 are capable of withstanding a load mismatch corresponding to VSWR = 5:1 through all phases under the following conditions:  $V_{DS}$  = 50 V;  $I_{Dq}$  = 50 mA;  $P_L$  = 130 W; f = 1.2 GHz to 1.4 GHz;  $t_p$  = 300  $\mu$ s;  $\delta$  = 10 %.

## 7. Application information

#### 7.1 Impedance information

Table 8. **Typical impedance** 

f	Z <sub>S</sub>	Z <sub>L</sub>
MHz	Ω	Ω
1200	1.21 – j3.44	2.40 – j0.63
1300	1.56 – j4.49	2.30 – j0.87
1400	2.21 – j4.86	2.00 – j1.71

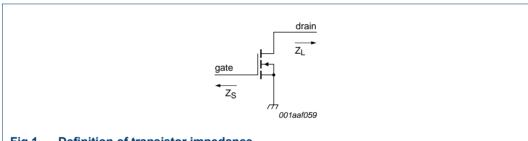
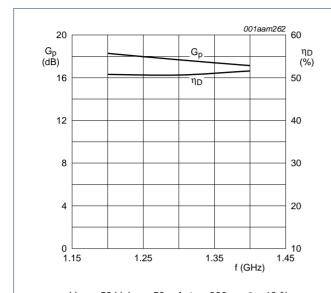


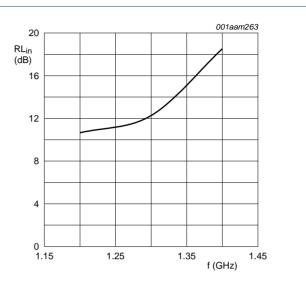
Fig 1. **Definition of transistor impedance** 

#### 7.2 Performance curves



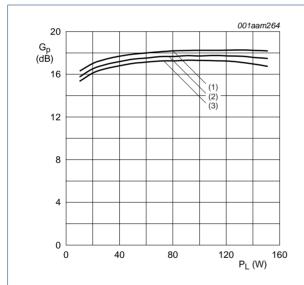
 $V_{DS}$  = 50 V;  $I_{Dq}$  = 50 mA;  $t_p$  = 300  $\mu s$ ;  $\delta$  = 10 %.

Fig 2. Power gain and drain efficiency as function of frequency; typical values



 $V_{DS}$  = 50 V;  $I_{Dq}$  = 50 mA;  $t_p$  = 300  $\mu$ s;  $\delta$  = 10 %.

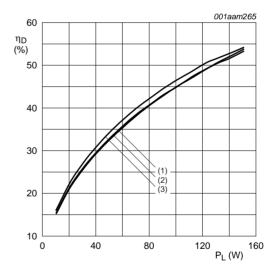
Fig 3. Input return loss as a function of frequency; typical values



 $V_{DS}$  = 50 V;  $I_{Dq}$  = 50 mA;  $t_p$  = 300  $\mu$ s;  $\delta$  = 10 %.

- (1) f = 1.2 GHz
- (2) f = 1.3 GHz
- (3) f = 1.4 GHz

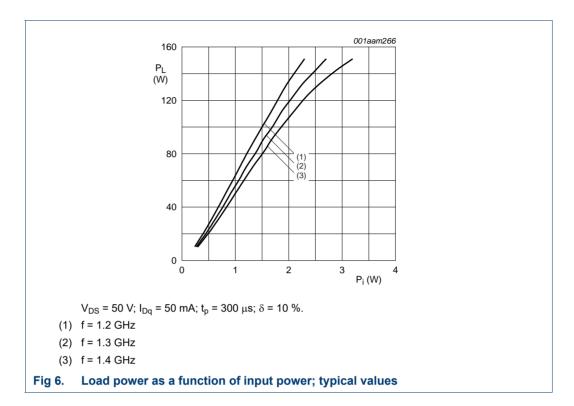
Fig 4. Power gain as a function of load power; typical values



 $V_{DS}$  = 50 V;  $I_{Dq}$  = 50 mA;  $t_p$  = 300  $\mu s;~\delta$  = 10 %.

- (1) f = 1.2 GHz
- (2) f = 1.3 GHz
- (3) f = 1.4 GHz

Fig 5. Drain efficiency as function of load power; typical values



#### 8. Test information

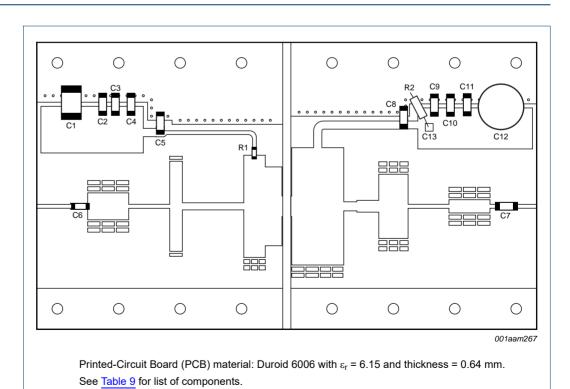


Fig 7. Component layout

**Table 9. List of components** See Figure 7 for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	10 μF; 50 V	
C2, C11	multilayer ceramic chip capacitor	1 nF	[1]
C3, C4, C6, C9, C10	multilayer ceramic chip capacitor	100 pF	[2]
C5, C7, C8	multilayer ceramic chip capacitor	43 pF	[2]
C12	electrolytic capacitor	220 μF; 63 V	
C13	multilayer ceramic chip capacitor	1 nF	fitted vertically in series with R2
R1	SMD resistor	10 Ω	SMD 0603
R2	wirewound lead resistor	2.61 Ω; 0.25 W	fitted in series with C13

<sup>[1]</sup> American Technical Ceramics type 700A or capacitor of same quality.

<sup>[2]</sup> American Technical Ceramics type 100A or capacitor of same quality.

<sup>[3]</sup> American Technical Ceramics type 100B or capacitor of same quality.

## 9. Package outline

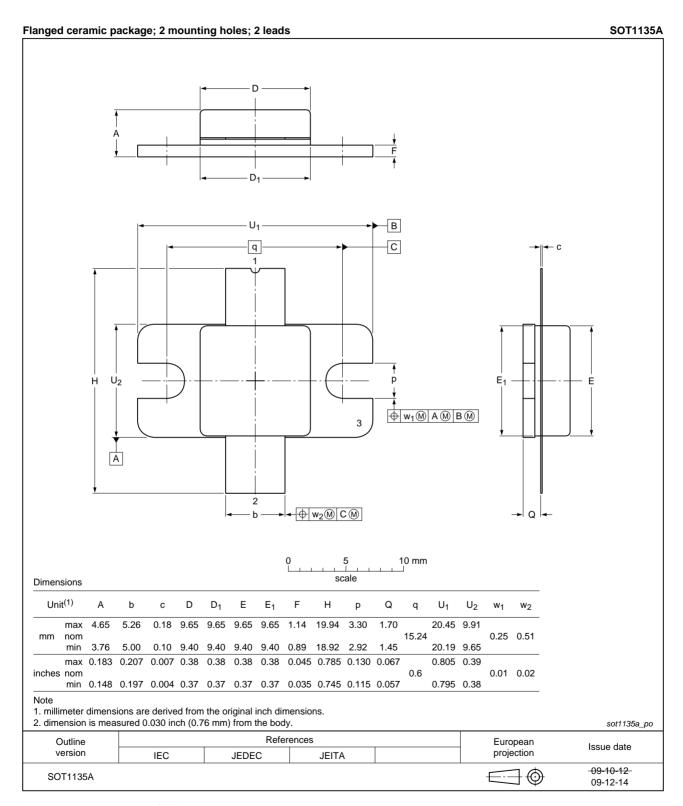


Fig 8. Package outline SOT1135A

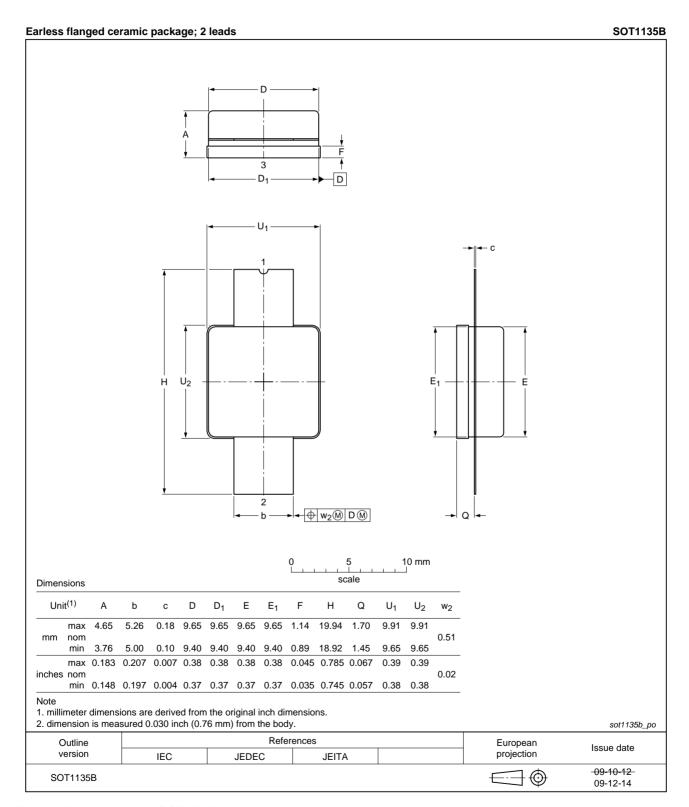


Fig 9. Package outline SOT1135B

## 10. Handling information

#### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 11. Abbreviations

Table 10. Abbreviations

Acronym	Description
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
RF	Radio Frequency
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

## 12. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
BLL6H0514L-130_0514LS-130#3	20150901	Product data sheet		BLL6H0514L-130_0 514LS-130 v.2	
Modifications:	The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.				
<ul> <li>Legal texts have been adapted to the new company name where a</li> </ul>			ne where appropriate.		
BLL6H0514L-130_0514LS-130 v.2	20100913	Product data sheet	-	BLL6H0514L-130_ 0514LS-130 v.1	
BLL6H0514L-130_0514LS-130 v.1	20100809	Preliminary data sheet	-	-	

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#### 13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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BLL6H0514L-130 0514LS-130#3

## BLL6H0514L(S)-130

**LDMOS** driver transistor

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## BLL6H0514L(S)-130

**LDMOS** driver transistor

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