Data Sheet | January 2004 | FN3172.3

Low Voltage Reference

The ICL8069 is a 1.2V temperature-compensated voltage reference. It uses the band-gap principle to achieve excellent stability and low noise at reverse currents down to 50µA. Applications include analog-to-digital converters, digital-to-analog converters, threshold detectors, and voltage regulators. Its low power consumption makes it especially suitable for battery operated equipment.

Ordering Information

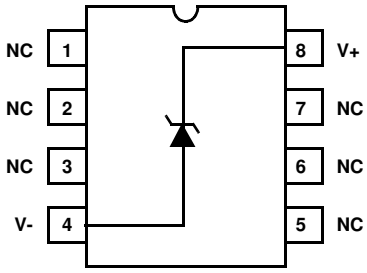
PART NUMBER	MAXIMUM TEMPCO	TEMP. RANGE (^{O}C)	PACKAGE	PKG. DWG. #
ICL8069CCZR	0.005%/^{O}C	0 to 70	SIP Package (TO-92)	Z3.05
ICL8069DCZR	0.01%/^{O}C	0 to 70	SIP Package (TO-92)	Z3.05
ICL8069CCBA	0.005%/^{O}C	0 to 70	8 Ld SOIC	M8.15

Features

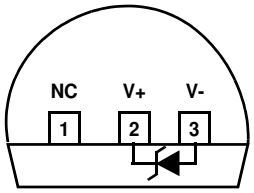
- Low Bias Current (Min) 50µA
- Low Dynamic Impedance
- Low Reverse Voltage
- Low Cost

Pinouts

ICL8069 (SOIC)
TOP VIEW

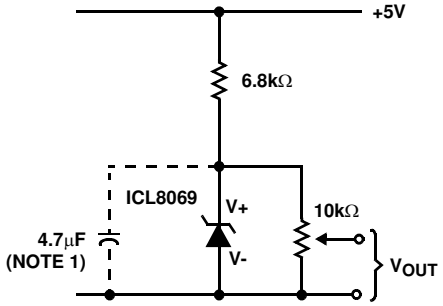


ICL8069 (SIP TO-92)
TOP VIEW

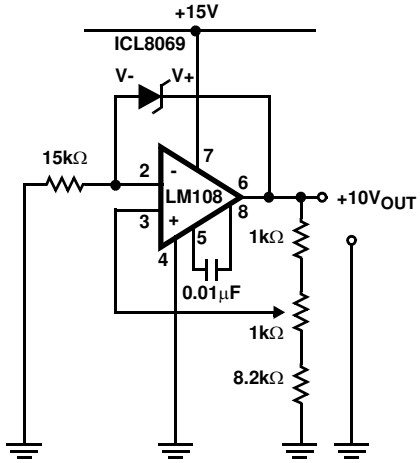


Functional Block Diagrams

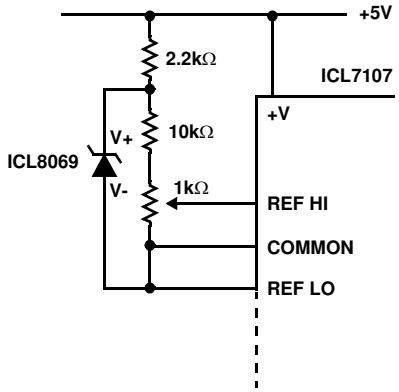
SIMPLE REFERENCE (1.2V OR LESS)



BUFFERED 10V REFERENCE USING A SINGLE SUPPLY



DOUBLE REGULATED 100mV REFERENCE FOR ICL7107 ONE-CHIP DPM CIRCUIT



Absolute Maximum Ratings

Reverse Voltage . . . . . See Note 3
Forward Current. 10mA
Reverse Current. 10mA

Operating Conditions

Temperature Ranges
ICL8069C . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
SOIC Package	170	N/A
SIP (TO-92) Package.	200	N/A

Power Dissipation Limited by MAX Forward/Reverse Current
Maximum Junction Temperature (SOIC Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^oC$ Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage	$I_R = 500\mu A$	1.20	1.23	1.25	V
Reverse Breakdown Voltage Change	$50\mu A \le I_R \le 5mA$	-	15	20	mV
Reverse Dynamic Impedance	$I_R = 50\mu A$	-	1	2	Ω
	$I_R = 500\mu A$	-	1	2	Ω
Forward Voltage Drop	$I_F = 500\mu A$	-	0.7	1	V
RMS Noise Voltage	$10Hz \le F \le 10kHz$, $I_R = 500\mu A$	-	5	-	μV
Long Term Stability	$I_R = 4.75mA$, $T_A = 25^oC$	-	1	-	ppm/kHR
Breakdown Voltage Temperature Coefficient ICL8069C	$I_R = 500\mu A$, T_A = Operating Temperature Range	-	-	0.005	$\%/^oC$
ICL8069D		-	-	0.01	$\%/^oC$
Reverse Current Range	1.18V to 1.27V	0.050	-	5	mA

NOTES:

2. If circuit strays in excess of 200pF are anticipated, a $4.7\mu F$ shunt capacitor will ensure stability under all operating conditions.
3. In normal use, the reverse voltage cannot exceed the reference voltage. However when plugging units into a powered-up test fixture, an instantaneous voltage equal to the compliance of the test circuit will be seen. This should not exceed 20V.

Typical Performance Curves

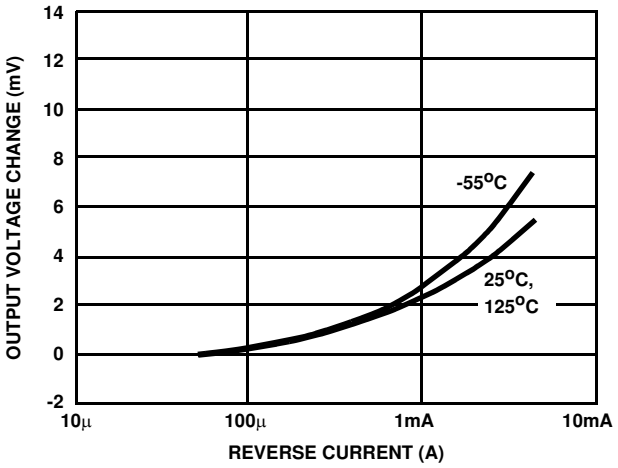


FIGURE 1. VOLTAGE CHANGE AS A FUNCTION OF REVERSE CURRENT

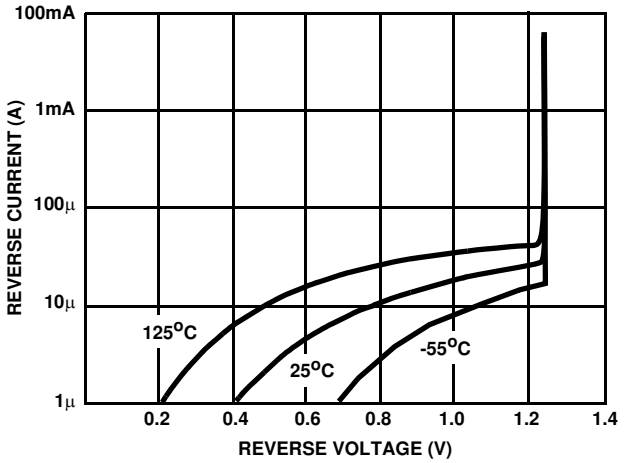


FIGURE 2. REVERSE VOLTAGE AS A FUNCTION OF CURRENT

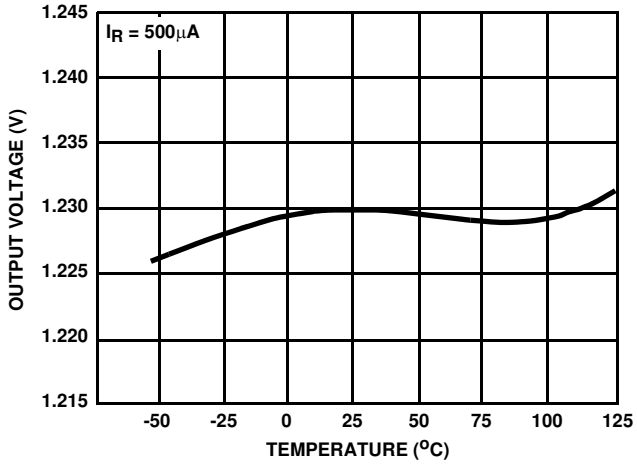
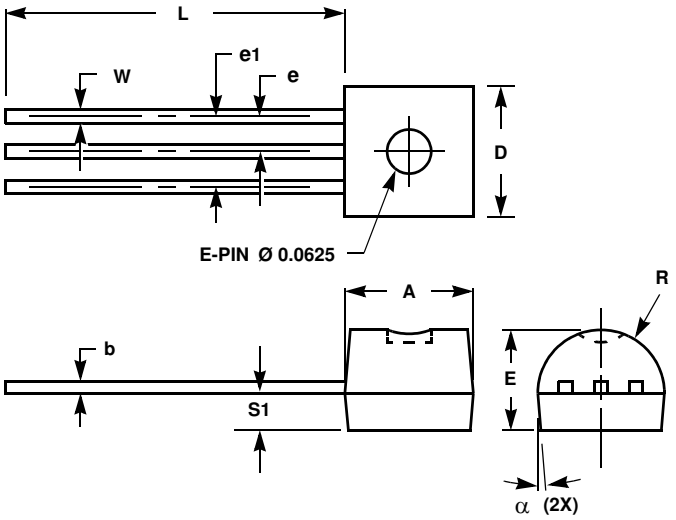


FIGURE 3. REVERSE VOLTAGE AS A FUNCTION OF TEMPERATURE

Single-In-Line Plastic Packages (SIP)



Z3.05 (JEDEC STYLE TO-92 MODIFIED)
3 LEAD PLASTIC SINGLE-IN-LINE PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.195	4.32	4.95	1
b	0.014	0.020	0.36	0.51	2
E	0.130	0.155	3.30	3.94	1
e	0.045	0.055	1.14	1.40	-
e1	0.095	0.105	2.41	2.67	-
L	0.500	0.610	12.70	15.49	-
R	0.085	0.095	2.16	2.41	-
S1	0.045	0.060	1.14	1.52	-
W	0.016	0.022	0.41	0.56	2
D	0.175	0.195	4.45	4.95	1
α	4^o	6^o	4^o	6^o	-

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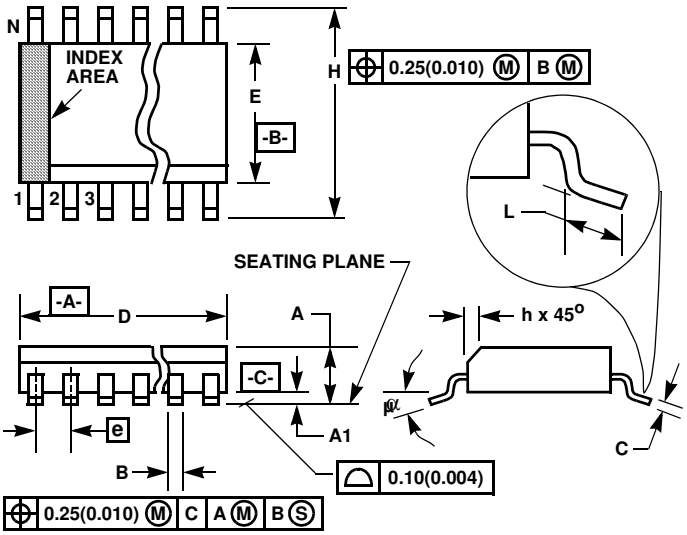
NOTES:

1. Package body dimensions do not include any mold flash or protrusions.
2. Package outline dimensions do not include burrs.
3. Controlling dimension: INCH.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

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