SAM9X60-EK

SAM9X60-EK User's Guide

Scope

This user's guide introduces the SAM9X60 Evaluation Kit (SAM9X60-EK) and describes the development and debugging capabilities running on SAM9 Arm®-based embedded MPUs.

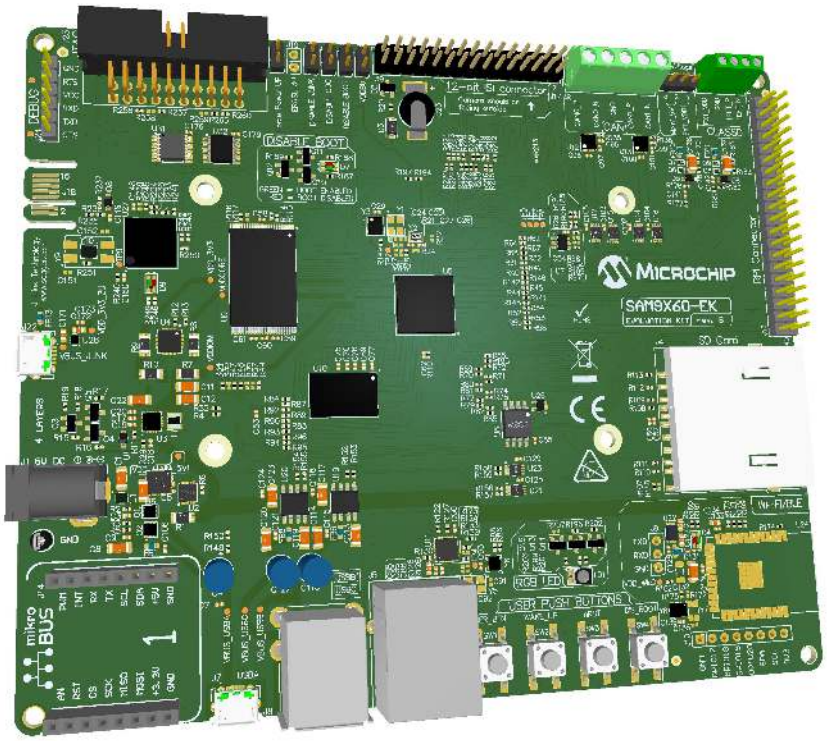


Table of Contents

1. Introduction

1.1 Document Layout

The document is organized as follows:

- Chapter 1. “Introduction”
- Chapter 2. “Product Overview” – Important information about the SAM9X60-EK board
- Chapter 3. “Function Blocks” – Specifications of the SAM9X60-EK and high-level description of the major components and interfaces
- Chapter 4. “Installation and Operation” – Instructions on how to get started with the SAM9X60-EK
- Appendix. “Schematics and Layouts” – SAM9X60-EK schematics and layout diagrams

1.2 Recommended Reading

The following Microchip document is available and recommended as a supplemental reference resource:

- SAM9X60 Datasheet. Lit. Number DS60001579

2. Product Overview

The SAM9X60-EK follows the Microchip MPU strategy for low cost evaluation kits, showcasing all the features that the SAM9X60 MPU can offer.

2.1 SAM9X60-EK Features

Table 2-1. SAM9X60-EK Features

Characteristic	Specification	Featured Components
Processor	228-ball TFBGA, 11x11 mm, 0.65 mm pitch	Microchip SAM9X60
External clock	MPU: 24 MHz, 32.768 KHz Misc. osc.: 25 MHz	DSC1001CI5 DSC6083CE2A
Memory	One 16-bit, 2-Gbit DDR2 One NAND Flash One QSPI Flash One EEPROM	Winbond W972GG6KB-25 Micron MT29F08BA Microchip SST26VF064B Microchip 24AA02E48
SD/MMC	One standard 4-bit SD card interface	–
USB	Two stacked Type-A connectors with power switches One Micro-B USB Device	2 * Microchip MIC2025
CAN	Two CAN interfaces	Microchip MCP2542
Ethernet	One ETH port	Microchip KSZ8081
Wi-Fi/BT	One optional Wi-Fi® /Bluetooth® interface	Slot for Microchip ATWILC3000
Audio	One ClassD audio port	–
Display	One 24-bit LCD interface	–
Camera	One 12-bit Image Sensor Interface	–
IO	One expander IO	Microchip MCP23008
Debug port	One J-Link-OB + CDC One JTAG interface	Embedded J-Link-OB through the CDC interface (ATSAM3U4C TFBGA100)
Board monitor	One RGB (Red, Green, Blue) LED Four push button switches	– –
Expansion	One PIO connector One mikroBUS™ connector	– Hundreds of possible Click™ extensions featuring Microchip functions inside
Power management	Two power regulators Two power consumption measurement devices	Microchip MIC2800, MCP1725 Microchip PAC1934, PAC1710
Board supply	From USB A or from external connector	–
Backup battery	SuperCap	–

2.2 Evaluation Kit Specifications

Table 2-2. Evaluation Kit Specifications

Characteristic	Specification
Board	SAM9X60-EK
Board supply voltage	External or USB-powered
Temperature	Operating: 0°C to +70°C Storage: –40°C to +85°C
Relative humidity	0 to 90% (non-condensing)
Main board dimensions	150 × 125 × 20 mm
RoHS status	Compliant
Board identification	SAM9X60 Evaluation Kit

2.3 Power Sources

Two options are available to power up the SAM9X60-EK board:

- Powering through an external AC to DC +5V wall adapter connector (J1)
- Powering through the USB Micro-B connector on the USBA port (J7 – default choice)

Table 2-3. Electrical Characteristics

Electrical Parameters	Value
Input voltage	5VDC
Maximum input voltage (limits)	6VDC
Maximum 3.3VDC current	300 mA

⚠ CAUTION The SAM9X60-EK board runs at a 3.3V voltage level logic. The maximum voltage that the I/O pins can tolerate is 3.3V. Providing higher voltages (e.g., 5V) to an I/O pin could damage the board.

2.4 Connectors on Board

The fully-featured SAM9X60-EK board integrates multiple peripherals and interface connectors, as shown in the following figures.

Figure 2-1. SAM9X60-EK Top Connectors

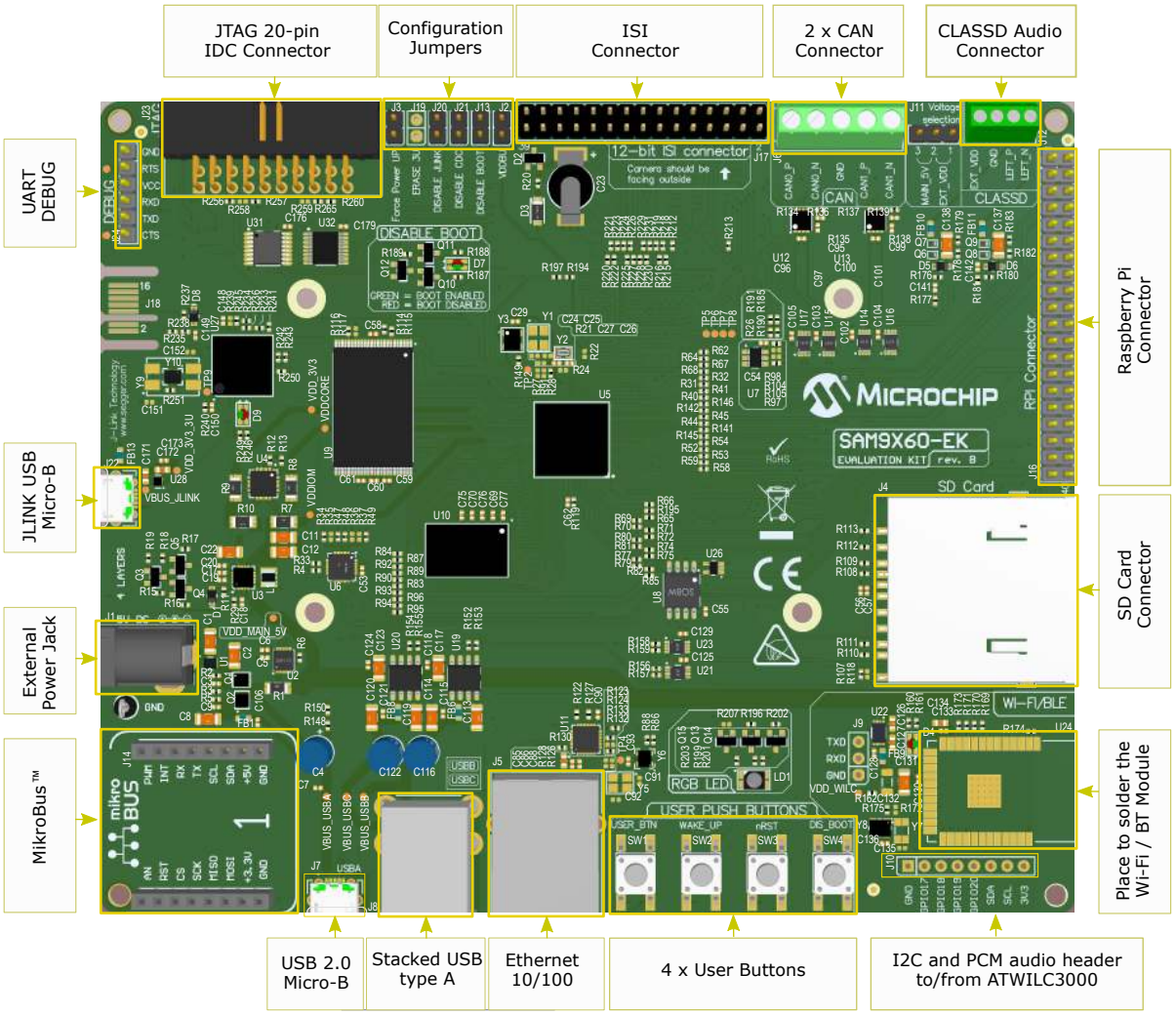


Figure 2-2. SAM9X60-EK Bottom Connectors

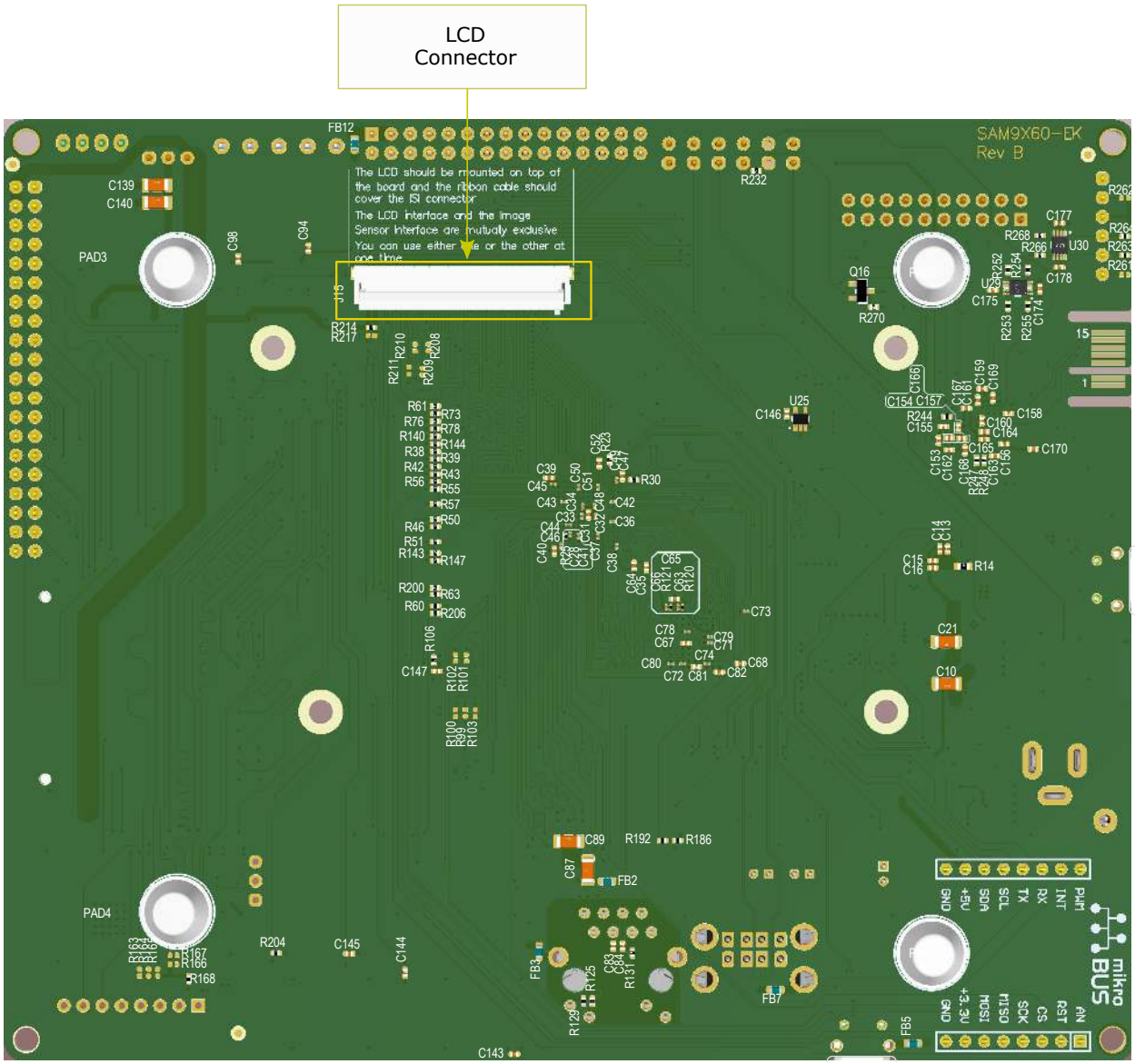


Table 2-4. SAM9X60-EK Board Interface Connectors

Connector	Interfaces to
J1	External power jack
J4	Standard SDMMC connector
J6	Dual CAN
J7	USB 2.0 Micro-B (USB-A)
J8A	Stacked Type-A USB (USB-B)
J8B	Stacked Type-A USB (USB-B)
J10 (not populated)	ATWILC3000 GPIO
J9 (not populated)	ATWILC3000 UART

.....continued	
Connector	**Interfaces to**
J5	Ethernet 10/100 RJ45 (port 1)
J11	Audio external power
J12	ClassD audio output
J14	mikroBUS socket
J15	LCD connector
J16	External GPIO
J17	ISI Camera Connector
J18	PCB connector for factory-programming the SAM3U/J-Link-OB (not to be used by end user)
J22	USB 2.0 Micro-B, J-Link-OB/J-Link-CDC
J23	JTAG, 20-pin IDC
J24	FTDI connector (UART debugger)

2.5 Default Jumper Settings

Table 2-5. SAM9X60-EK Jumper Settings

Jumper	State	Function
J2	Closed	VDDBU current measurement
J3	Closed	Disable the SHDN function and always keep the board powered on
	Open (default)	Normal behavior, the PMIC can be powered down by the MPU
J13	Closed	Booting from on-board memories is permanently disabled
	Open (default)	Booting from on-board memories is disabled only when SW4 is pressed
J19 (not populated)	Closed	Erase SAM3U firmware (not populated, reserved for factory configuration and should never be used by the end user)
	Open (default)	Normal SAM3U operation (runs the J-Link interface)
J20	Closed	J-Link on-board interface is disabled. MPU debugging is done through J23, the 20-pin SAM-ICE™ connector (i.e., an external JTAG interface is required)
	Open (default)	J-Link on-board interface is enabled. MPU debugging is done through it (i.e., using the SAM3U MCU and the micro USB connector J22)
J21	Closed	Disable UART communication (CDC) between MPU and SAM3U
	Open (default)	Enable UART communication (CDC) between MPU and SAM3U (PD20 port must be high as well)

2.6 Kit Content

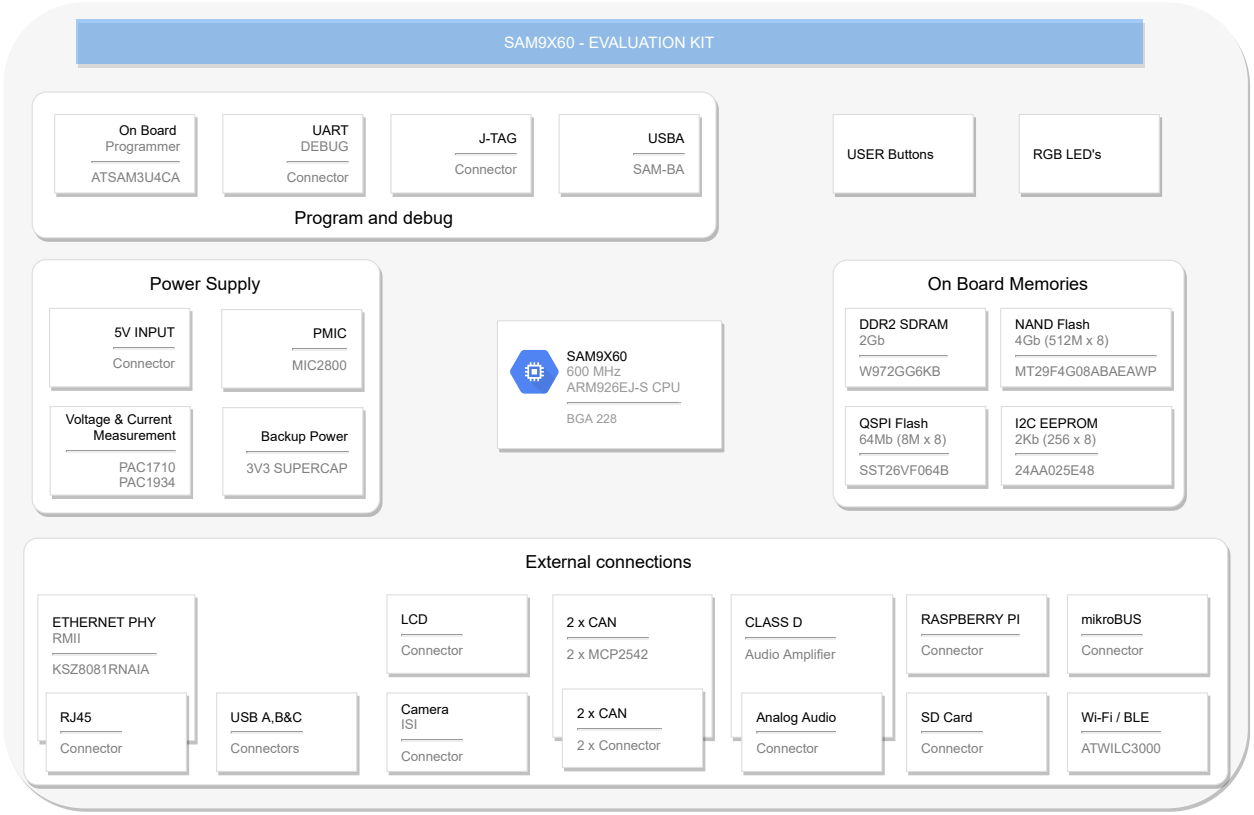
The SAM9X60 evaluation kit includes the following:

- The SAM9X60-EK board
- USB-A to USB Micro-B cable
- 50-position FFC/FPC cable

3. Function Blocks

This section covers the specifications of the SAM9X60-EK and provides a high-level description of the board's major components and interfaces. This document is not intended to provide detailed documentation about the processor or about any other component used on the board. It is expected that the user will refer to the appropriate documents of these devices to access detailed information.

Figure 3-1. SAM9X60-EK Block Diagram



3.1 Power Supply Topology and Power Distribution

This section describes the implementation and the circuitry that ensures adequate voltage stability and current budget for all the devices on the board and a correct power-up sequence for the MPU. The power-up and power-down sequences indicated in the SAM9X60 datasheet must be respected for a reliable operation of the device.

3.1.1 Input Power Options

The SAM9X60-EK board can be powered through:

- an external AC to DC +5V wall adapter connected via a 2.1 mm center-positive plug into the power jack of the board (J1). The recommended output capacity of the power adapter is 2A,
- USB port A (J7).

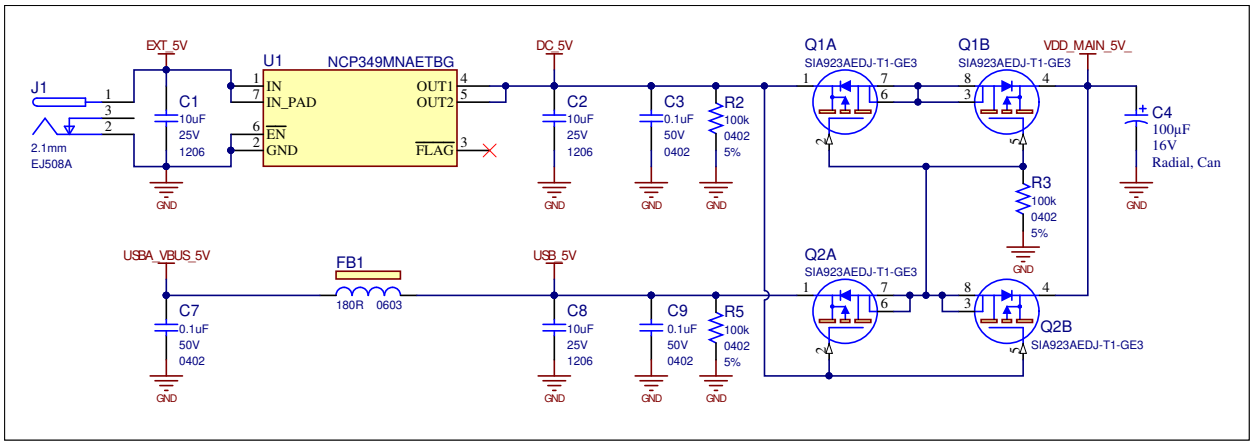
The +5V from the wall adapter is protected through an NCP349 positive overvoltage controller switch. The controller is able to disconnect the system from its output pin when incorrect input operating conditions are detected (5.83V max).

The USB-powered operation comes from the USB device port connected to a PC or a 5VDC supply. The USB supply is enough to power the board in most applications. It is important to note that when the USB supply is used, the USB port has limited power. If USB Host port is required for the application, it is recommended that the external DC supply be used.

The switch between the two powering options is made by four transistors that ensure the separation between the two when both are plugged. The switch prioritizes powering from the wall adapter to maximize power transfer.

The following figure shows the input power supply topology.

Figure 3-2. Input Power Options



Note: USB-powered operation eliminates additional wires and batteries. It is the preferred mode of operation for any project that requires only a 5V source at up to 500 mA.

3.1.2 Power Management Integrated Circuit

The MIC2800 is a high-performance power management IC providing three output voltages with maximum efficiency. Integrating a 2-MHz DC/DC converter with an LDO post-regulator, the MIC2800 gives two high-efficiency outputs with a second, 300 mA LDO for maximum flexibility. The DC-to-DC converter uses small values of L and C to reduce board space while still retaining efficiency over 90% at load currents up to 600 mA. For more information about the MIC2800, refer to the product web page.

Each LDO has an independent Enable (EN) pin thus allowing a proper power-up sequence for the MPU. The 20 KΩ resistor in series and the 0.1 µF capacitor in parallel with the EN1 input make a low-pass filter and introduce the necessary delay between the 3.3V and 1.15V rails needed for the proper operation of the MPU. The diode (D1 in Figure 3-3) ensures that the capacitor fast discharges during the power-down sequence.

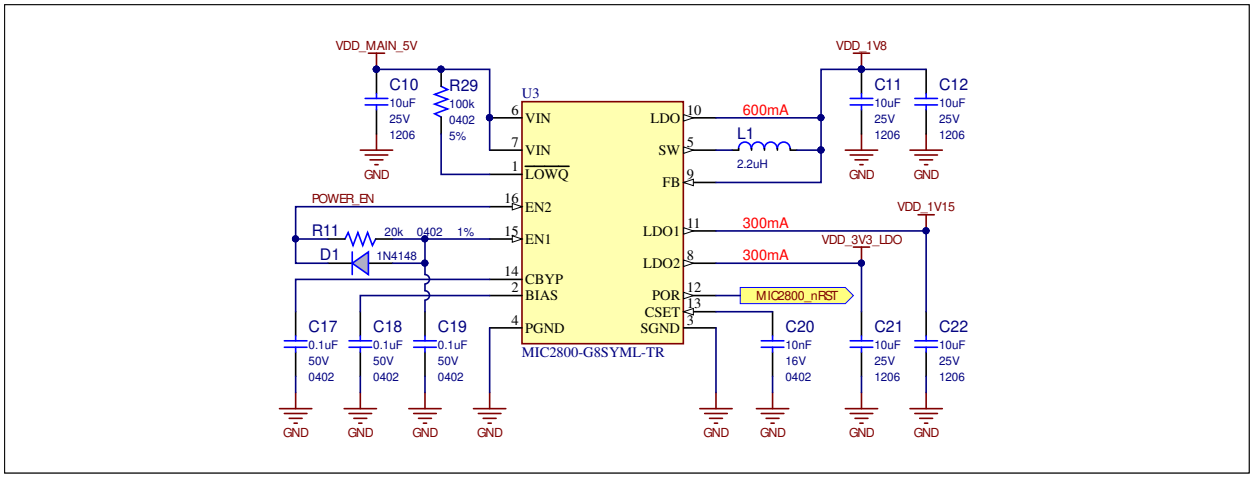
Detailed information on the SAM9X60 MPU power supplies and power-up/down considerations are described in section “Electrical Characteristics” in the SAM9X60 device datasheet (see 1.2 Recommended Reading).

The MIC2800-G8S comes preset to supply all the voltage rails needed by the system:

- 1.8V DC/DC supplies SAM9X60 DDR2 pads (VDDIOM) and devices.
- 1.15V LDO1 supplies SAM9X60 Core (VDDCORE).
- 3.3V LDO2 supplies SAM9X60 I/O pads.

The figure below shows the power management scheme.

Figure 3-3. Power Management Integrated Circuit

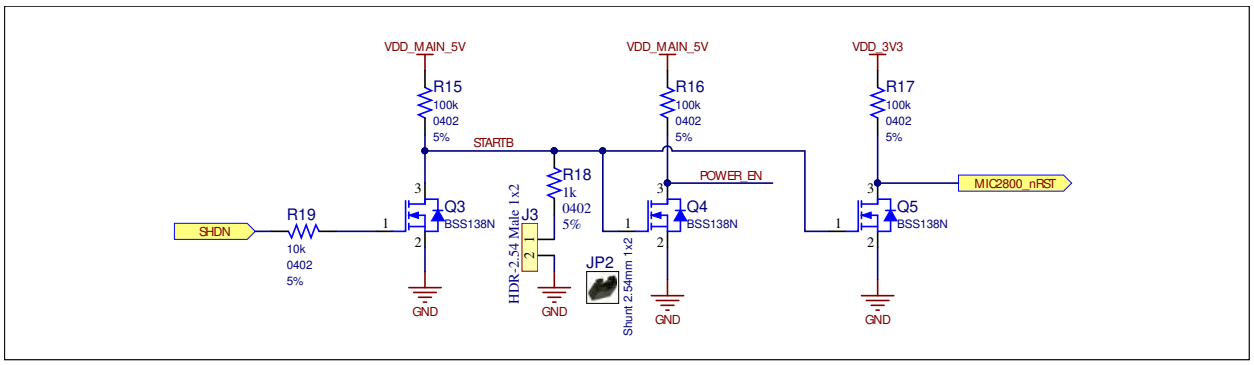


3.1.3 Shutdown Circuitry

The processor can assert the SHDN signal to shut down the PMIC and enter Power-down mode. This is done by pulling both enable pins of the PMIC to GND through a Field Effect Transistor (FET) scheme.

Jumper J3 must not be set to enable this functionality. By setting jumper JP2/J3, the user can shut down the MPU without powering down its power rails.

Figure 3-4. Shutdown Circuitry



3.1.4 Battery Unit

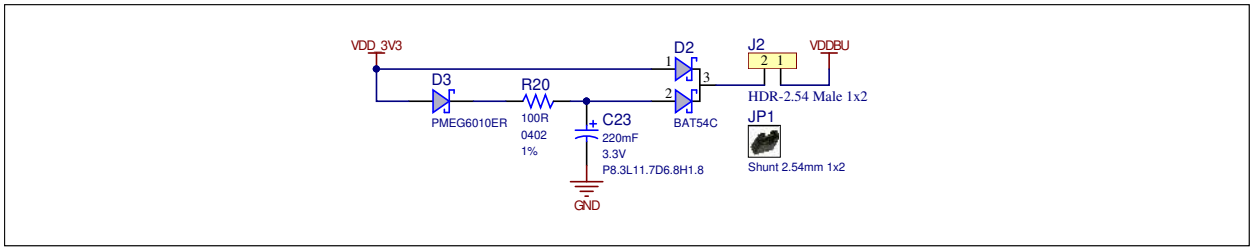
A 3.3V battery (supercapacitor) is implemented to permanently maintain the VDDBU voltage.

This function allows the user to shut down the MPU and the system, thus entering a low power mode, and still keep the custom configuration that was previously set in the MPU backup area. While in Shut-down mode, the board can be woken up by action on the SW2 button (WAKE UP), which signals the MPU to resume operations.

Jumper JP1/J2 must be in place for proper operation of the MPU, and can be removed if the user wants to bring the MPU back to the initial configuration, by resetting the General Purpose Backup Registers (GPBR).

⚠WARNING Make sure the board is powered off before removing the JP1/J2 jumper.

Figure 3-5. Battery Unit



3.1.5 Current Measurement

Two Microchip DC power/energy monitors are embedded on the SAM9X60-EK board:

- one single high-side current sense monitor PAC1710
- one four-channel current sense monitor PAC1934

Both chips communicate with the MPU via a Two-wire Interface (TWI) and both output their ALERT# signal to a port expander.

The PAC1710 is a single high-side bidirectional current sensing monitor with precision voltage measurement capabilities. The power monitor measures the voltage developed across an external sense resistor to represent the high-side current of a battery or voltage regulator. The PAC1710 also measures the SENSE+ pin voltage and calculates average power over the integration period. The PAC1710 can be programmed to assert the ALERT# pin when high and low limits are exceeded for current sense and bus voltage. For more information about the PAC1710, refer to the product web page.

One current sense resistor is populated on board for measuring voltage and current on the main 5V power rail.

Figure 3-6. PAC1710 Current Measurement

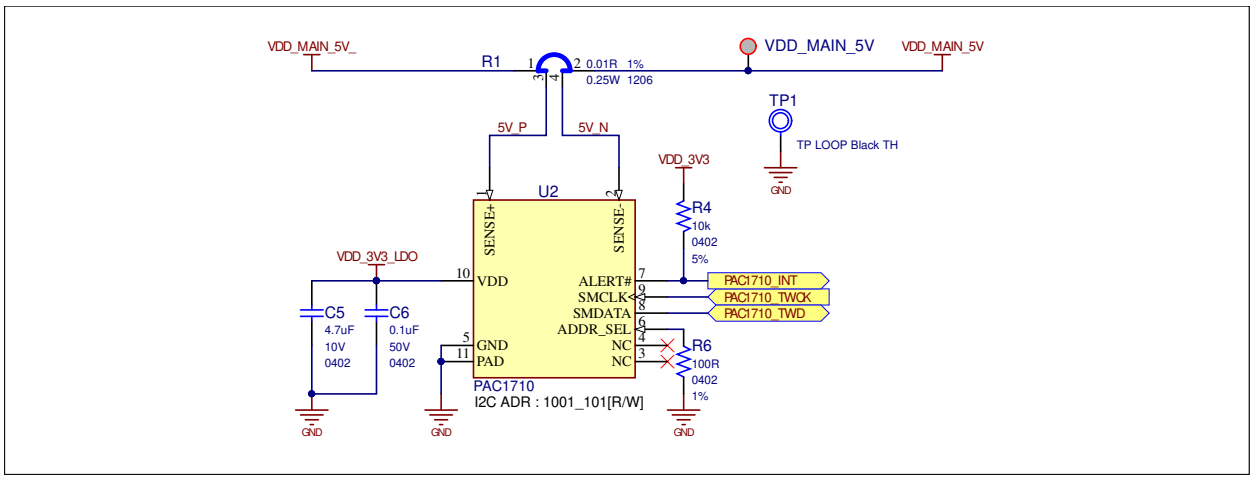


Table 3-1. PAC1710 Signal Descriptions

PIO	Signal Name	Shared PIO	Signal Description
PA31	PAC1710_TWCK	Power TWI	TWI clock
PA30	PAC1710_TWD	Power TWI	TWI data
–	PAC1710_INT	–	Interrupt – to port expander U6

The PAC1934 is a four-channel power/energy monitor with current sensor amplifier and bus voltage monitors that feed high resolution ADCs. Digital circuitry performs power calculations and energy accumulation. The PAC1934 enables energy monitoring with integration periods from 1 ms to up to 36 hours. Bus voltage, sense resistor voltage, and accumulated proportional power are stored in registers for retrieval by the system master or embedded controller. For more information about the PAC1934, refer to the product web page.

Four current sense resistors are populated on board for measuring voltage and current consumption on the power rails:

- 3.3V VDD_3V3_MPU - MPU on the 3.3V rail
- 3.3V VDD_3V3_SYS - rest of the system on the 3.3V rail
- 1.8V VDDIOM - MPU and DDR2 memory
- 1.15V VDDCORE – MPU core

Figure 3-7. PAC1934 Current Measurement

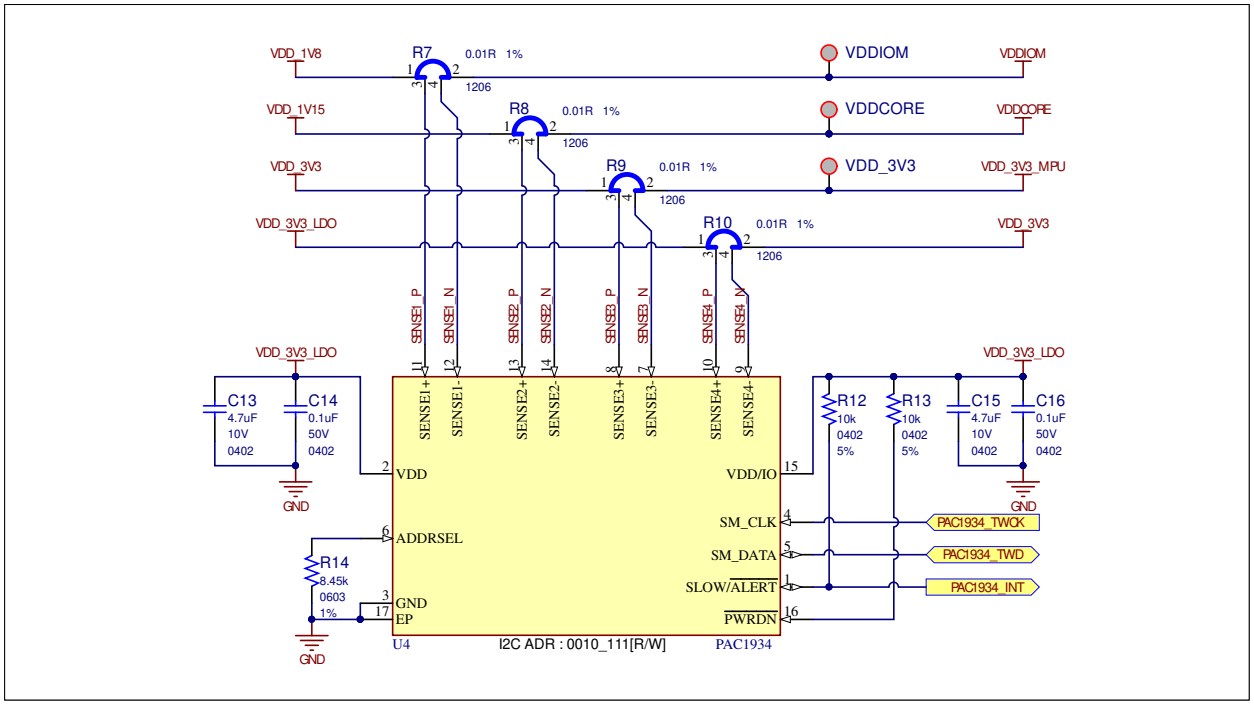


Table 3-2. PAC1934 Signal Descriptions

PIO	Signal Name	Shared PIO	Signal Description
PA31	PAC1934_TWCK	Power TWI	TWI clock
PA30	PAC1934_TWD	Power TWI	TWI data
–	PAC1934_INT	–	Interrupt – to port expander U6

3.2 Processor

The SAM9X60 is a high-performance, ultra-low power ARM926EJ-S CPU-based embedded microprocessor (MPU) running up to 600 MHz, with support for multiple memories such as SDRAM, LPSDRAM, LPDDR, DDR2, QSPI and e.MMC Flash. The device integrates powerful peripherals for connectivity and user interface applications, and offers security functions (tamper detection, etc.), TRNG, as well as high-performance crypto accelerators for AES and SHA.

Refer to the SAM9X60 datasheet for more information (see 1.2 Recommended Reading).

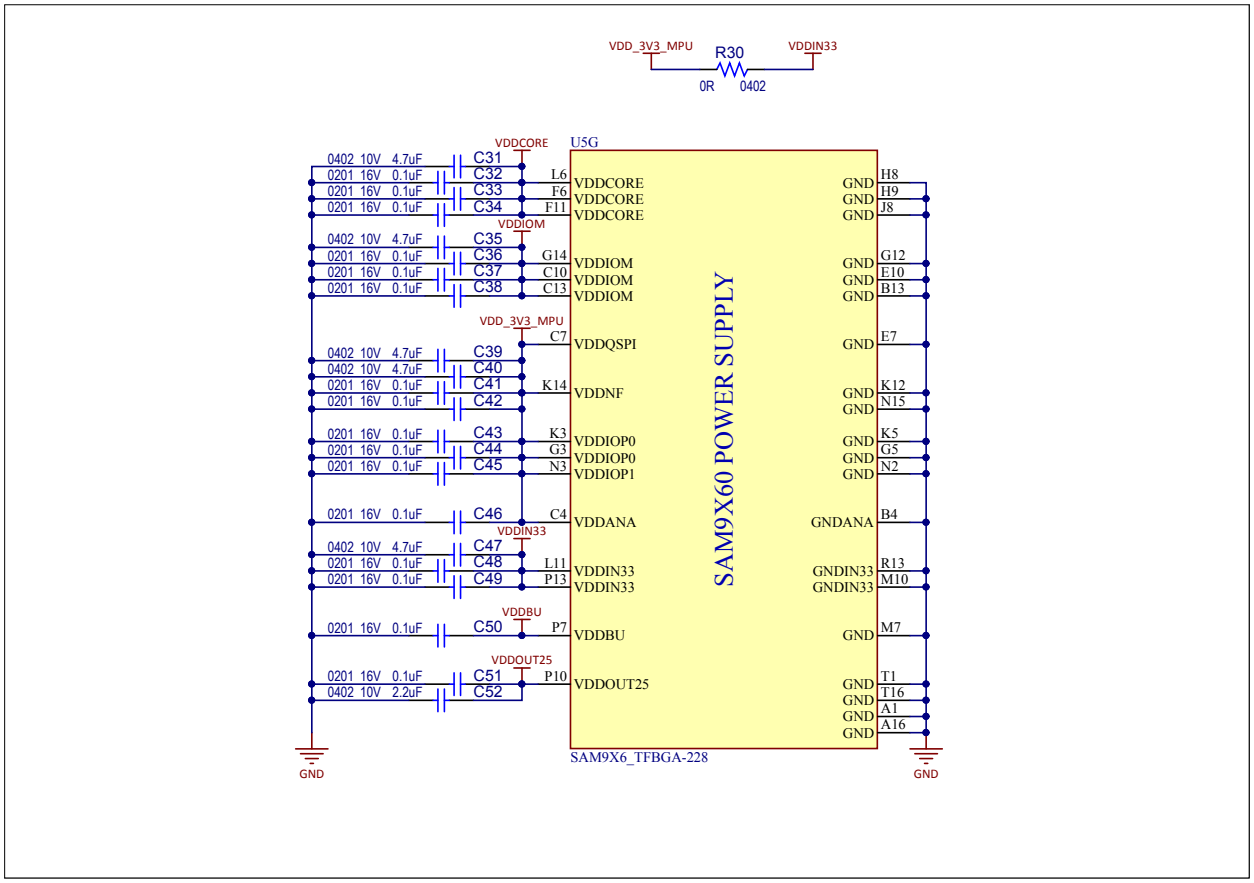
3.2.1 Power Supply

The PMIC (main regulator) provides all power supplies required by the SAM9X60 device:

- 1.15V for VDDCORE
- 1.8V for VDDIOM
- 3.3V for VDDIOP0, VDDIOP1, VDDANA, VDDNF, VDDQSPI, VDDIN33 and VDDBU

Decoupling capacitors are placed close to the MPU power pins to stabilize the voltage rails.

Figure 3-8. Processor Power Supplies

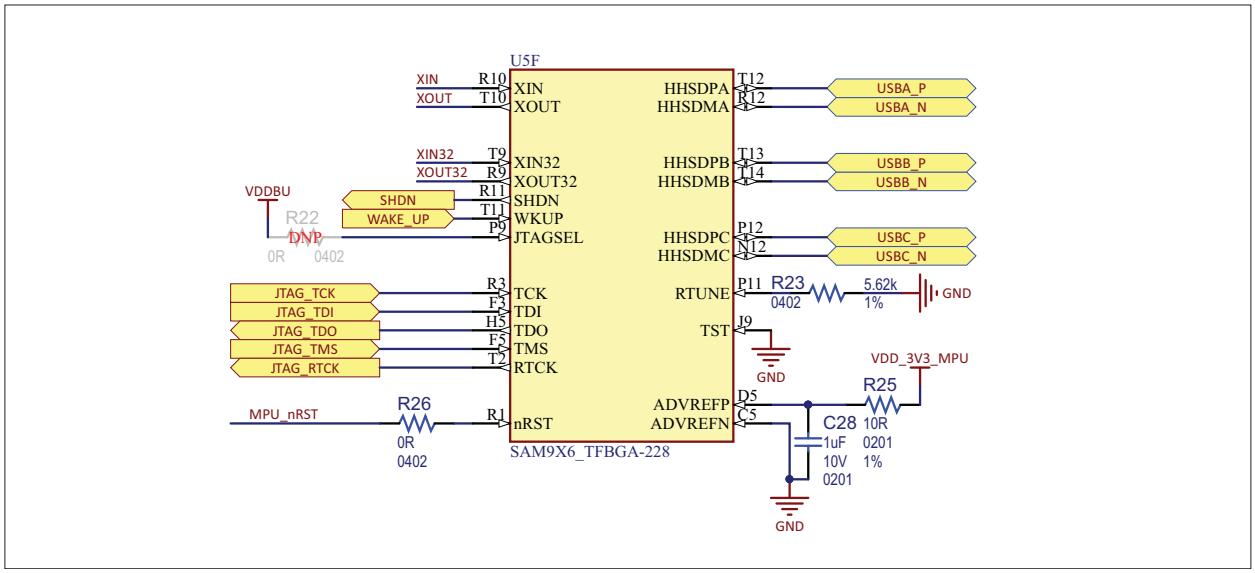


3.2.2 Main Configuration and Control

This block depicts the main block for processor configuration and control:

- XIN and XOUT are the Main Clock Oscillator input/output.
- XIN32 and XOUT32 are the Slow Clock Oscillator input/output.
- SHDN is an output signal used to enable and disable an external power supply circuit.
- WKUP is an event detection input pin used to wake up the processor from Shutdown state.
- JTAGSEL is an input that when pulled high enables the JTAG boundary scan.
- TCK, TDI, TDO, TMS and RTCK are used for JTAG communication.
- nRST is the processor main reset input.
- HHSD_A/B/C are the three USB ports embedded inside the MPU.
- RTUNE is used for USB external tuning.
- TST input is reserved for processor manufacturing tests.
- ADVREFP and ADVREFN are the positive and negative reference points for the embedded analog comparator. A small low-pass filter is placed to reduce the input noise and improve accuracy.

Figure 3-9. Processor Main Configuration and Control



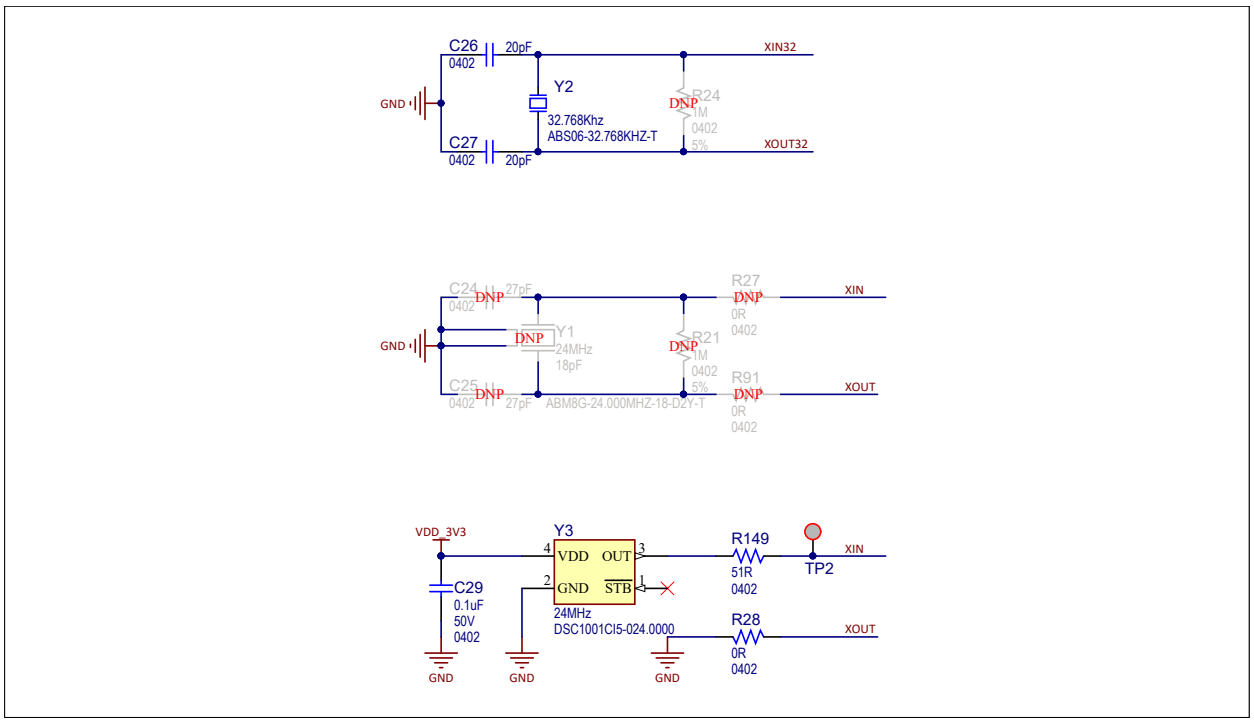
3.2.3 Clock Circuitry

The embedded MPU generates its necessary clocks based on two oscillators: one slow clock (SLCK) oscillator running at 32.768 kHz and one main clock oscillator running at 24 MHz.

The main clock oscillator is implemented with a MEMS (Micro Electro-Mechanical System) device DSC1001.

For evaluation purposes, we leave users the freedom to mount a crystal instead, using the PCB footprint reservation (Y1). In that case, resistors R149 and R28 should be removed, resistors R27 and R91 should be populated and capacitors C24 and C25 should be populated with the appropriate load capacitance for the selected crystal.

Figure 3-10. Processor Clock Circuitry

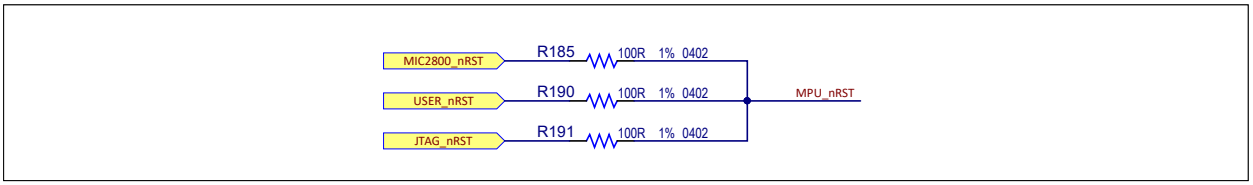


3.2.4 Reset Circuitry

Three reset sources for the SAM9X60 MPU are placed on the board:

- Power-on Reset from the power management unit MIC2800
- User push button reset SW3
- External JTAG or J-Link-OB reset from an in-circuit emulator

Figure 3-11. Processor Reset Circuitry



3.2.5 DDR Controller (MPDDRC)

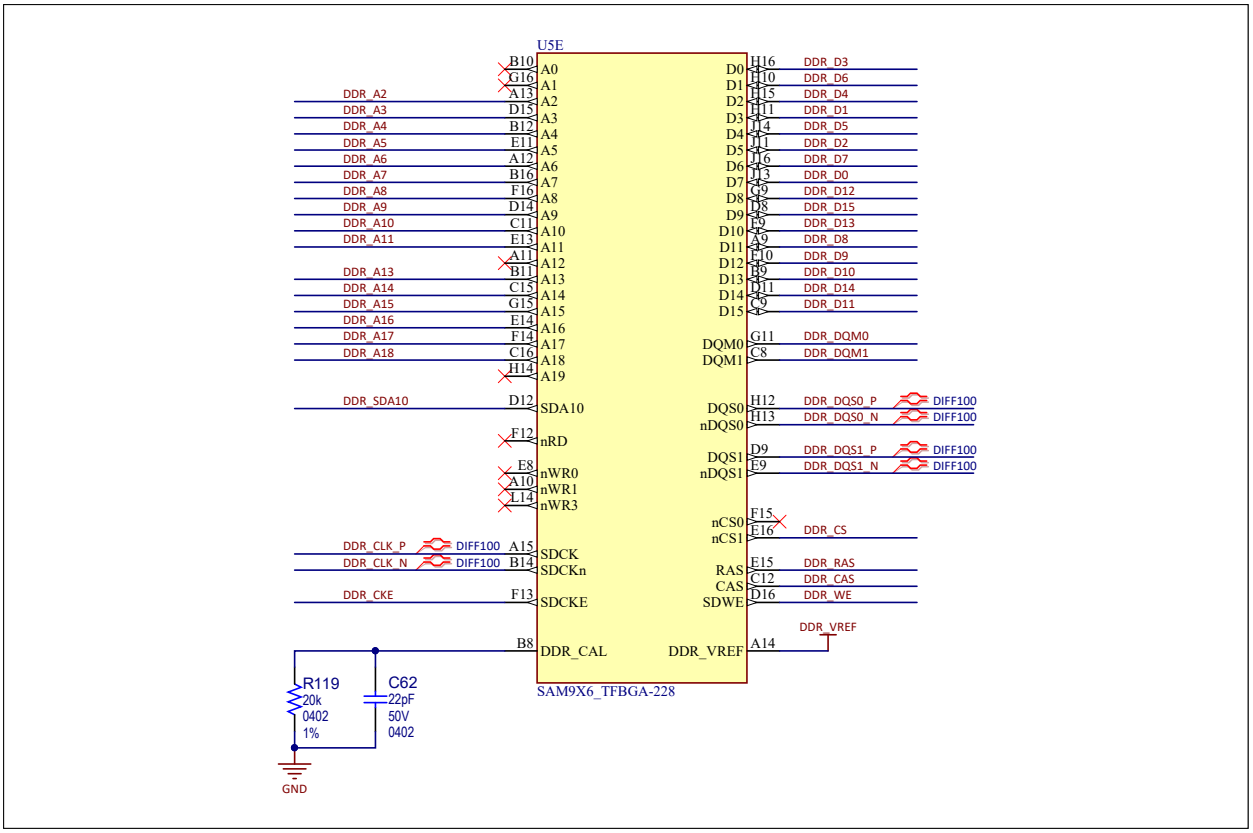
The SAM9X60 embeds a Multi-Port DDR-SDRAM Controller (MPDDRC) to drive DDR2 and LPDDR1 memories.

Note the following regarding the command and control signal connections between the DDR Controller and the DDR Memory:

- Addresses A0, A1 and A12 are not used on the controller side.
- Addresses A2 to A11 are connected to A0 to A9 on the memory side.
- Signal SDA10 must be connected to A10.
- Addresses A13 to A15 are connected to the last three addresses on the memory side.
- A16 to A18 are connected to BA0 to BA2.

It is recommended to double-check the design schematic against the information provided in the datasheet.

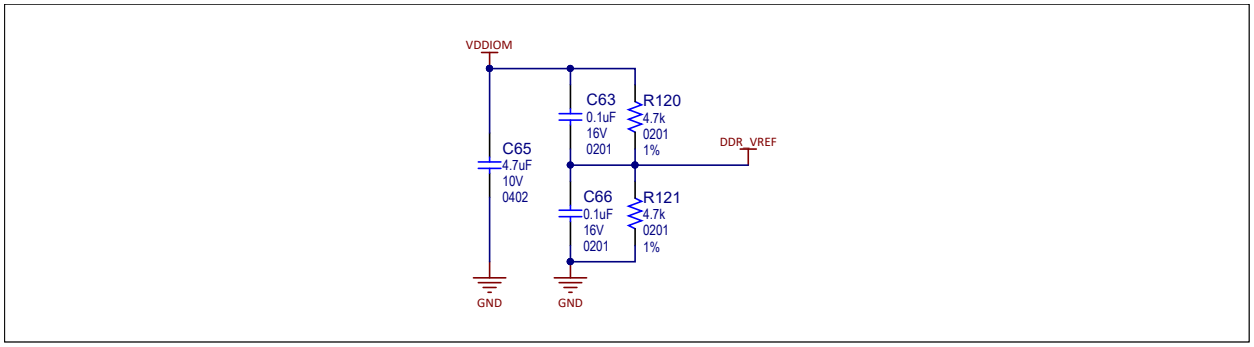
Figure 3-12. Processor DDR Controller



The MPDDRC I/Os embed an automatic impedance matching control to avoid overshoots and to reach the best performance levels depending on the bus load and external memories. A serial termination connection scheme, where the driver has an output impedance matched to the characteristic impedance of the line, is used to improve signal quality and reduce EMI. This is done using the ZQ calibration procedure to calibrate the SAM9X60 DDR I/O drive strength. The pin name where the ZQ resistor must be connected is DDR_CAL and, as indicated in the SAM9X60 datasheet for DDR2 case, the resistor value is 20 KOhms.

The DDR_VREF pin serves as a voltage reference input for the DDR I/Os when DDR2 or LPDDR external SDRAM memories are used.

Figure 3-13. DDR Reference Voltage



3.2.6 PIOs

The following sections depict all the signals connected to the SAM9X60 MPU ports.

See Table 3-3 for details about each port's functions.

Figure 3-14. Processor PIOs PA and PC

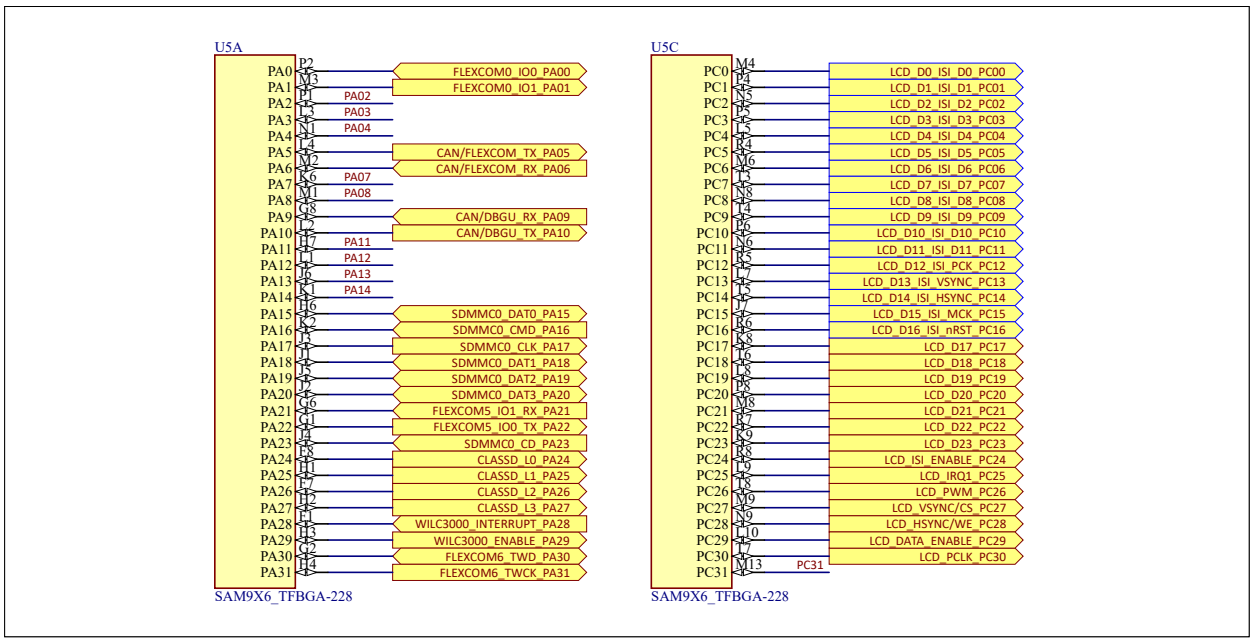
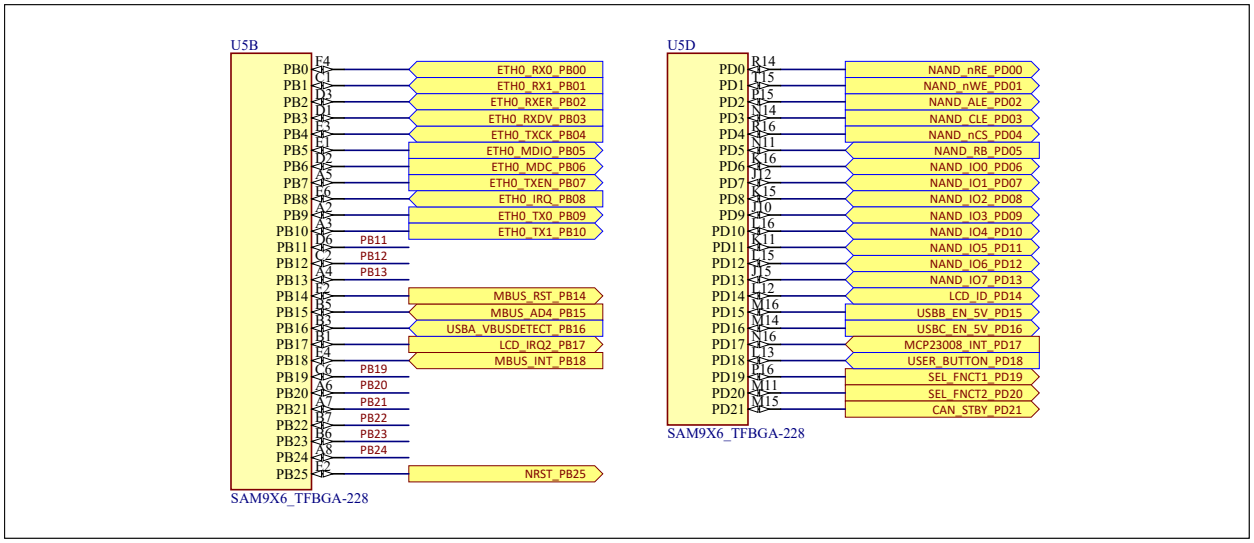


Figure 3-15. Processor PIOs PB and PD



Some of the ports were multiplexed to accommodate more devices on the evaluation kit and to showcase all the functions the SAM9X60 MPU can address off a single PIO wire.

Most of the ports that share multiple functions are split through passive resistors placed on the board as close to the MPU as possible, therefore no other hardware change must be made. In most cases, the user can use only one of their functions at a time, or can develop a composite driver enabling the use of multiple functions at the same time.

Figure 3-16. Processor PIO Muxing

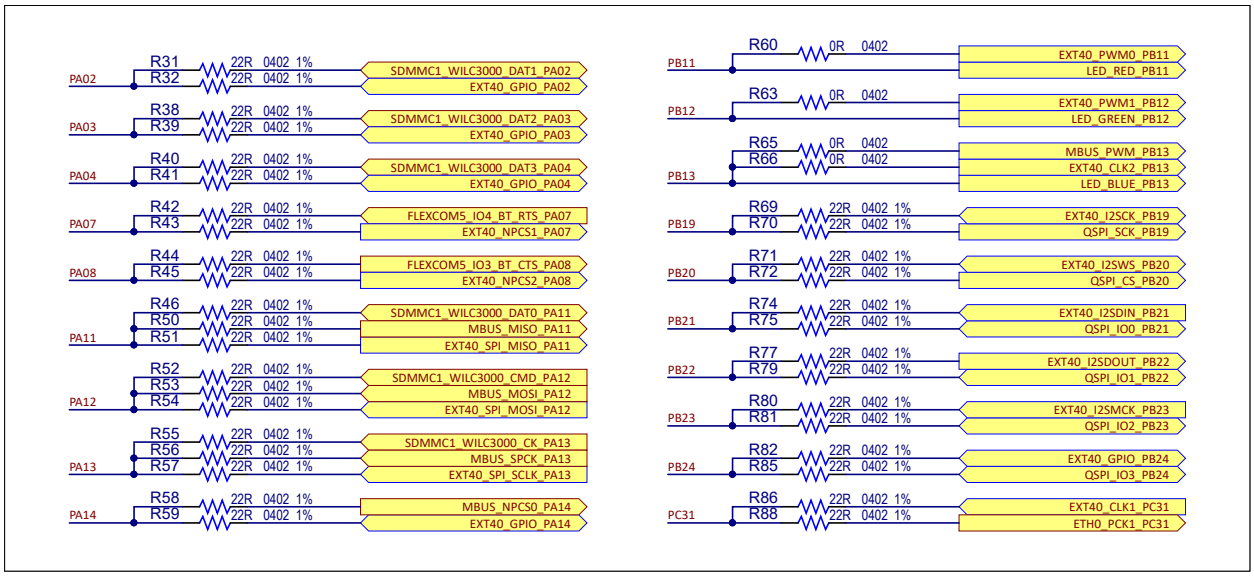


Table 3-3. Processor PIOs Pin Assignment and Signal Description

Pad	Power Rail	Function	I/O Type
PA0	VDDIOP0 (3.3V)	FLEXCOM0_IO0	TWI Data (TWD) bidirectional line shared between the LCD, EEPROMs and external 40-pin header
PA1	VDDIOP0 (3.3V)	FLEXCOM0_IO1	TWI Clock (TWCK) output line shared between the LCD, EEPROMs and external 40-pin header

.....continued

Pad	Power Rail	Function	I/O Type
PA2	VDDIOP0 (3.3V)	SDMMC1_DAT1	SDIO Data 1 (I/O1) bidirectional line for the ATWILC3000 Wi-Fi/BT module
		GPIO	GPIO going to the external 40-pin header
PA3	VDDIOP0 (3.3V)	FLEXCOM0_IO3	SDIO Data 2 (I/O2) bidirectional line for the ATWILC3000 Wi-Fi/BT module
		GPIO	GPIO going to the external 40-pin header
PA4	VDDIOP0 (3.3V)	FLEXCOM0_IO2	SDIO Data 3 (I/O3) bidirectional line for the ATWILC3000 Wi-Fi/BT module
		GPIO	GPIO going to the external 40-pin header
PA5[1]	VDDIOP0 (3.3V)	FLEXCOM1_IO0	UART Transmit (TX) output line going to the external 40-pin header
		CANTX1	CAN Transmit (CANTX) output line going to the second CAN transceiver MCP2542
PA6[1]	VDDIOP0 (3.3V)	FLEXCOM1_IO1	UART Receive (RX) input line going to the external 40-pin header
		CANRX1	CAN Receive (CANRX) input line going to the second CAN transceiver MCP2542
PA7	VDDIOP0 (3.3V)	FLEXCOM4_IO4	First SPI Chip Select (nCS) output line for the external 40-pin header
		FLEXCOM5_IO4	SPI Request to Send (RTS) output line for the BT module
PA8	VDDIOP0 (3.3V)	FLEXCOM4_IO5	Second SPI Chip Select (nCS) output line for the external 40-pin header
		FLEXCOM5_IO3	SPI Clear to Send (CTS) input line for the BT module
PA9[2]	VDDIOP0 (3.3V)	DRXD	DEBUG UART Receive (DRX) input line
		CANRX0	CAN Receive (CANRX) input line going to the first CAN transceiver MCP2542
PA10[2]	VDDIOP0 (3.3V)	DTXD	DEBUG UART Transmit (DTX) input line
		CANTX0	CAN Transmit (CANTX) output line going to the first CAN transceiver MCP2542
PA11	VDDIOP0 (3.3V)	FLEXCOM4_IO1	SPI Master Input Slave Output (MISO) input line shared between the mikroBUS and external 40-pin connectors
		SDMMC1_DAT0	SDIO Data 0 (I/O0) bidirectional line going to the ATWILC3000 Wi-Fi/BT module
PA12	VDDIOP0 (3.3V)	FLEXCOM4_IO0	SPI Master Output Slave Input (MOSI) output line shared between the mikroBUS and external 40-pin connectors
		SDMMC1_CMD	SDIO Command (CMD) bidirectional line going to the ATWILC3000 Wi-Fi/BT module
PA13	VDDIOP0 (3.3V)	FLEXCOM4_IO2	SPI Source Clock (SCLK) output line shared between the mikroBUS and external 40-pin connectors
		SDMMC1_CK	SDIO Data 0 (I/O0) bidirectional line going to the ATWILC3000 Wi-Fi/BT module
PA14	VDDIOP0 (3.3V)	FLEXCOM4_IO3	SPI Chip Select (nCS) output line for the mikroBUS connector
		GPIO	GPIO going to the external 40-pin header

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Pad	Power Rail	Function	I/O Type
PA15	VDDIOP0 (3.3V)	SDMMC0_DAT0	SDIO Data 0 (I/O0) bidirectional line going to the SD card connector
PA16	VDDIOP0 (3.3V)	SDMMC0_CMD	SDIO Command (CMD) bidirectional line going to the SD card connector
PA17	VDDIOP0 (3.3V)	SDMMC0_CK	SDIO Clock (CLK) output line going to the SD card connector
PA18	VDDIOP0 (3.3V)	SDMMC0_DAT1	SDIO Data 1 (I/O1) bidirectional line going to the SD card connector
PA19	VDDIOP0 (3.3V)	SDMMC0_DAT2	SDIO Data 2 (I/O2) bidirectional line going to the SD card connector
PA20	VDDIOP0 (3.3V)	SDMMC0_DAT3	SDIO Data 3 (I/O3) bidirectional line going to the SD card connector
PA21	VDDIOP0 (3.3V)	FLEXCOM5_IO1	UART Receive (RX) input line shared between the mikroBUS connector and the BT transceiver on the ATWILC3000 module
PA22	VDDIOP0 (3.3V)	FLEXCOM5_IO0	UART Transmit (TX) output line shared between the mikroBUS connector and the BT transceiver on the ATWILC3000 module
PA23	VDDIOP0 (3.3V)	GPIO	GPIO used as input to detect when an SD card has been inserted in the SD connector
PA24	VDDIOP0 (3.3V)	CLASSD_L0	CLASSD Left Output L0
PA25	VDDIOP0 (3.3V)	CLASSD_L1	CLASSD Left Output L1
PA26	VDDIOP0 (3.3V)	CLASSD_L2	CLASSD Left Output L2
PA27	VDDIOP0 (3.3V)	CLASSD_L3	CLASSD Left Output L3
PA28	VDDIOP0 (3.3V)	GPIO / WKUP4	GPIO Input used to signal any interrupt coming from the WILC300 Wi-Fi/BT module
PA29	VDDIOP0 (3.3V)	GPIO	GPIO Output used to enable the WILC300 Wi-Fi/BT module by enabling its power supply
PA30	VDDIOP0 (3.3V)	FLEXCOM6_IO0	TWI Data (TWD) bidirectional signal shared between PAC1934, PAC1710, MPC23008 and the mikroBUS connector
PA31	VDDIOP0 (3.3V)	FLEXCOM6_IO1	TWI Clock (TWCK) Bidirectional signal shared between PAC1934, PAC1710, MPC23008 and the mikroBUS connector
PB0	VDDANA (3.3V)	E0_RX0	RMII Ethernet Receive Data 0 signal going to KSZ8081
PB1	VDDANA (3.3V)	E0_RX1	RMII Ethernet Receive Data 1 signal going to KSZ8081
PB2	VDDANA (3.3V)	E0_RXER	RMII Ethernet Receive Error signal going to KSZ8081
PB3	VDDANA (3.3V)	E0_RXDV	RMII Ethernet Receive Data Valid signal going to KSZ8081
PB4	VDDANA (3.3V)	E0_TXCK	RMII Ethernet Transmit Clock signal going to KSZ8081
PB5	VDDANA (3.3V)	E0_MDIO	RMII Ethernet Management Data I/O signal going to KSZ8081
PB6	VDDANA (3.3V)	E0_MDC	RMII Ethernet Management Data Clock signal going to KSZ8081
PB7	VDDANA (3.3V)	E0_TXEN	RMII Ethernet Receive Data Valid signal going to KSZ8081
PB8	VDDANA (3.3V)	E0_TXER	RMII Ethernet Transmit Coding Error signal going to KSZ8081
PB9	VDDANA (3.3V)	E0_TX0	RMII Ethernet Transmit Data 0 signal going to KSZ8081
PB10	VDDANA (3.3V)	E0_TX1	RMII Ethernet Transmit Data 1 signal going to KSZ8081
PB11	VDDANA (3.3V)	PWM0	PWM signal shared between the LD1 red LED and the 40-pin connector

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Pad	Power Rail	Function	I/O Type
PB12	VDDANA (3.3V)	PWM1	PWM signal shared between the LD1 green LED and the 40-pin connector
PB13	VDDANA (3.3V)	PWM2	PWM signal shared between the LD1 blue LED, the mikroBUS and the 40-pin connectors
PB14	VDDANA (3.3V)	GPIO	GPIO output used as the reset signal for the mikroBUS connector
PB15	VDDANA (3.3V)	AD4	Analog input for the mikroBUS connector
PB16	VDDANA (3.3V)	GPIO	GPIO input used to detect if the board has been connected to a host on the USBA port
PB17	VDDANA (3.3V)	GPIO	GPIO input used to signal any interrupt request from the LCD
PB18	VDDANA (3.3V)	GPIO	GPIO input used to signal any interrupt request from the mikroBUS connector
PB19	VDDQSPI (3.3V)	QSCK	QSPI Serial Clock (SCK) signal going to SST26VF064B
		I2SMCC_CK	I2S Bit Clock (CK) signal going to the 40-pin connector
PB20	VDDQSPI (3.3V)	QCS	QSPI Chip Select (CS) signal going to SST26VF064B
		I2SMCC_WS	I2S Word Select (WS) signal going to the 40-pin connector
PB21	VDDQSPI (3.3V)	QIO0	QSPI Data I/O 0 (IO0) signal going to SST26VF064B
		I2SMCC_DIN0	I2S Data IN 0 (DIN0) signal going to the 40-pin connector
PB22	VDDQSPI (3.3V)	QIO1	QSPI Data I/O 1 (IO1) signal going to SST26VF064B
		I2SMCC_DOUT0	I2S Data Out 0 (DOUT0) signal going to the 40-pin connector
PB23	VDDQSPI (3.3V)	QIO2	QSPI Data I/O 2 (IO2) signal going to SST26VF064B
		I2SMCC_MCK	I2S Master Clock (MCK) signal going to the 40-pin connector
PB24	VDDQSPI (3.3V)	QIO3	QSPI Data I/O 3 (IO3) signal going to SST26VF064B
		GPIO	GPIO signal going to the 40-pin connector
PB25	VDDIOP0 (3.3V)	NRST_OUT	Output signal used to reset all the devices on the board
PC0	VDDIOP1 (3.3V)	LCDDAT0	LCD Data Output 0 (DAT0) signal going to the LCD connector
		ISI_D0	Image Sensor Interface (ISI) Data Input 0 (D0) signal going to the ISI connector
PC1	VDDIOP1 (3.3V)	LCDDAT1	LCD Data Output 1 (DAT1) signal going to the LCD connector
		ISI_D1	Image Sensor Interface (ISI) Data Input 1 (D1) signal going to the ISI connector
PC2	VDDIOP1 (3.3V)	LCDDAT2	LCD Data Output 2 (DAT2) signal going to the LCD connector
		ISI_D2	Image Sensor Interface (ISI) Data Input 2 (D2) signal going to the ISI connector
PC3	VDDIOP1 (3.3V)	LCDDAT3	LCD Data Output 3 (DAT3) signal going to the LCD connector
		ISI_D3	Image Sensor Interface (ISI) Data Input 3 (D3) signal going to the ISI connector

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Pad	Power Rail	Function	I/O Type
PC4	VDDIOP1 (3.3V)	LCDDAT4	LCD Data Output 4 (DAT4) signal going to the LCD connector
		ISI_D4	Image Sensor Interface (ISI) Data Input 4 (D4) signal going to the ISI connector
PC5	VDDIOP1 (3.3V)	LCDDAT5	LCD Data Output 5 (DAT5) signal going to the LCD connector
		ISI_D5	Image Sensor Interface (ISI) Data Input 5 (D5) signal going to the ISI connector
PC6	VDDIOP1 (3.3V)	LCDDAT6	LCD Data Output 6 (DAT6) signal going to the LCD connector
		ISI_D6	Image Sensor Interface (ISI) Data Input 6 (D6) signal going to the ISI connector
PC7	VDDIOP1 (3.3V)	LCDDAT7	LCD Data Output 7 (DAT7) signal going to the LCD connector
		ISI_D7	Image Sensor Interface (ISI) Data Input 7 (D7) signal going to the ISI connector
PC8	VDDIOP1 (3.3V)	LCDDAT8	LCD Data Output 8 (DAT8) signal going to the LCD connector
		ISI_D8	Image Sensor Interface (ISI) Data Input 8 (D8) signal going to the ISI connector
PC9	VDDIOP1 (3.3V)	LCDDAT9	LCD Data Output 9 (DAT9) signal going to the LCD connector
		ISI_D9	Image Sensor Interface (ISI) Data Input 9 (D9) signal going to the ISI connector
PC10	VDDIOP1 (3.3V)	LCDDAT10	LCD Data Output 10 (DAT10) signal going to the LCD connector
		ISI_D10	Image Sensor Interface (ISI) Data Input 10 (D10) signal going to the ISI connector
PC11	VDDIOP1 (3.3V)	LCDDAT11	LCD Data Output 11 (DAT11) signal going to the LCD connector
		ISI_D11	Image Sensor Interface (ISI) Data Input 11 (D11) signal going to the ISI connector
PC12	VDDIOP1 (3.3V)	LCDDAT12	LCD Data Output 12 (DAT12) signal going to the LCD connector
		ISI_PCK	Image Sensor Interface (ISI) Data Input 12 (D12) signal going to the ISI connector
PC13	VDDIOP1 (3.3V)	LCDDAT13	LCD Data Output 13 (DAT13) signal going to the LCD connector
		ISI_VSYNC	Image Sensor Interface (ISI) Vertical Synchronization (VSYNC) signal going to the ISI connector
PC14	VDDIOP1 (3.3V)	LCDDAT14	LCD Data Output 14 (DAT14) signal going to the LCD connector
		ISI_HSYNC	Image Sensor Interface (ISI) Horizontal Synchronization (HSYNC) signal going to the ISI connector
PC15	VDDIOP1 (3.3V)	LCDDAT15	LCD Data Output 15 (DAT15) signal going to the LCD connector
		ISI_MCK	Image Sensor Interface (ISI) Main Clock (MCK) signal going to the ISI connector
PC16	VDDIOP1 (3.3V)	LCDDAT16	LCD Data Output 16 (DAT16) signal going to the LCD connector
PC17	VDDIOP1 (3.3V)	LCDDAT17	LCD Data Output 17 (DAT17) signal going to the LCD connector
PC18	VDDIOP1 (3.3V)	LCDDAT18	LCD Data Output 18 (DAT18) signal going to the LCD connector

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Pad	Power Rail	Function	I/O Type
PC19	VDDIOP1 (3.3V)	LCDDAT19	LCD Data Output 19 (DAT19) signal going to the LCD connector
PC20	VDDIOP1 (3.3V)	LCDDAT20	LCD Data Output 20 (DAT20) signal going to the LCD connector
PC21	VDDIOP1 (3.3V)	LCDDAT21	LCD Data Output 21 (DAT21) signal going to the LCD connector
PC22	VDDIOP1 (3.3V)	LCDDAT22	LCD Data Output 22 (DAT22) signal going to the LCD connector
PC23	VDDIOP1 (3.3V)	LCDDAT23	LCD Data Output 23 (DAT23) signal going to the LCD connector
PC24	VDDIOP1 (3.3V)	LCDDISP	LCD Display ON/OFF (DISP) output signal going to the LCD connector
PC25	VDDIOP1 (3.3V)	GPIO	GPIO input used to signal any interrupt request from the LCD connector
PC26	VDDIOP1 (3.3V)	LCDPWM	LCD PWM for Contrast Control (PWM) output signal going to the LCD connector
PC27	VDDIOP1 (3.3V)	LCDVSYNC	LCD Vertical Synchronization (VSYNC) output signal going to the LCD connector
PC28	VDDIOP1 (3.3V)	LCDHSYNC	LCD Horizontal Synchronization (HSYNC) output signal going to the LCD connector
PC29	VDDIOP1 (3.3V)	LCDDEN	LCD Data Enable (EN) output signal going to the LCD connector
PC30	VDDIOP1 (3.3V)	LCDPCK	LCD Pixel Clock (PCK) output signal going to the LCD connector
PC31	VDDIOP1 (3.3V)	PCK1	Programmable Clock Output that can be used as a clock source for either the RMII Ethernet PHY KSZ8081 or the 40-pin connector
PD0	VDDNF (3.3V)	NANDOE	NAND Flash Output Enable (OE) output signal going to MT29F4G08ABAEA
PD1	VDDNF (3.3V)	NANDWE	NAND Flash Write Enable (OE) output signal going to MT29F4G08ABAEA
PD2	VDDNF (3.3V)	A21/NANDALE	NAND Flash Address Latch Enable (ALE) output signal going to MT29F4G08ABAEA
PD3	VDDNF (3.3V)	A22/NANDCLE	NAND Flash Command Latch Enable (CLE) output signal going to MT29F4G08ABAEA
PD4	VDDNF (3.3V)	NCS3	NAND Flash Chip Select (CLE) output signal going to MT29F4G08ABAEA
PD5	VDDNF (3.3V)	NWAIT	NAND Flash Ready/busy# (R/B#) input pin provides a hardware method of detecting PROGRAM or ERASE cycle completion from MT29F4G08ABAEA
PD6	VDDNF (3.3V)	D16	NAND Flash Data 0 (D0) Bidirectional signal going to MT29F4G08ABAEA
PD7	VDDNF (3.3V)	D17	NAND Flash Data 1 (D1) Bidirectional signal going to MT29F4G08ABAEA
PD8	VDDNF (3.3V)	D18	NAND Flash Data 2 (D2) Bidirectional signal going to MT29F4G08ABAEA
PD9	VDDNF (3.3V)	D19	NAND Flash Data 3 (D3) Bidirectional signal going to MT29F4G08ABAEA
PD10	VDDNF (3.3V)	D20	NAND Flash Data 4 (D4) Bidirectional signal going to MT29F4G08ABAEA

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Pad	Power Rail	Function	I/O Type
PD11	VDDNF (3.3V)	D21	NAND Flash Data 5 (D5) Bidirectional signal going to MT29F4G08ABAEA
PD12	VDDNF (3.3V)	D22	NAND Flash Data 6 (D6) Bidirectional signal going to MT29F4G08ABAEA
PD13	VDDNF (3.3V)	D23	NAND Flash Data 7 (D7) Bidirectional signal going to MT29F4G08ABAEA
PD14	VDDNF (3.3V)	GPIO	GPIO used to identify the type of LCD connected by reading the information stored on an EEPROM placed on the LCD through the OneWire interface
PD15	VDDNF (3.3V)	GPIO	GPIO used as output for enabling the 5V supply on the USBB port
PD16	VDDNF (3.3V)	GPIO	GPIO used as output for enabling the 5V supply on the USBC port
PD17	VDDNF (3.3V)	GPIO	GPIO used as input to signal any interrupt request from the MCP23008 GPIO expander
PD18	VDDNF (3.3V)	GPIO	GPIO used as input to probe the changes of the user button
PD19	VDDNF (3.3V)	GPIO	GPIO used as output for selecting between the functions of PA05 and PA06(1) HIGH = UART to 40-pin connector LOW = CAN1 communication
PD20	VDDNF (3.3V)	GPIO	GPIO used as output for selecting between the functions of PA10 and PA09(2) HIGH = Enable DEBUG UART LOW = CAN0 communication
PD21	VDDNF (3.3V)	D31	GPIO used as output to place the CAN transceivers in or out of standby

Note:

1. The selection of the functions of ports PA5 and PA6 must also comply with the state of PD19 as this signal commands an analog switch placed on the board.
2. The selection of the functions of ports PA9 and PA10 must also comply with the state of PD20 as this signal commands an analog switch placed on the board.

3.2.7 Dedicated Two-wire Interfaces

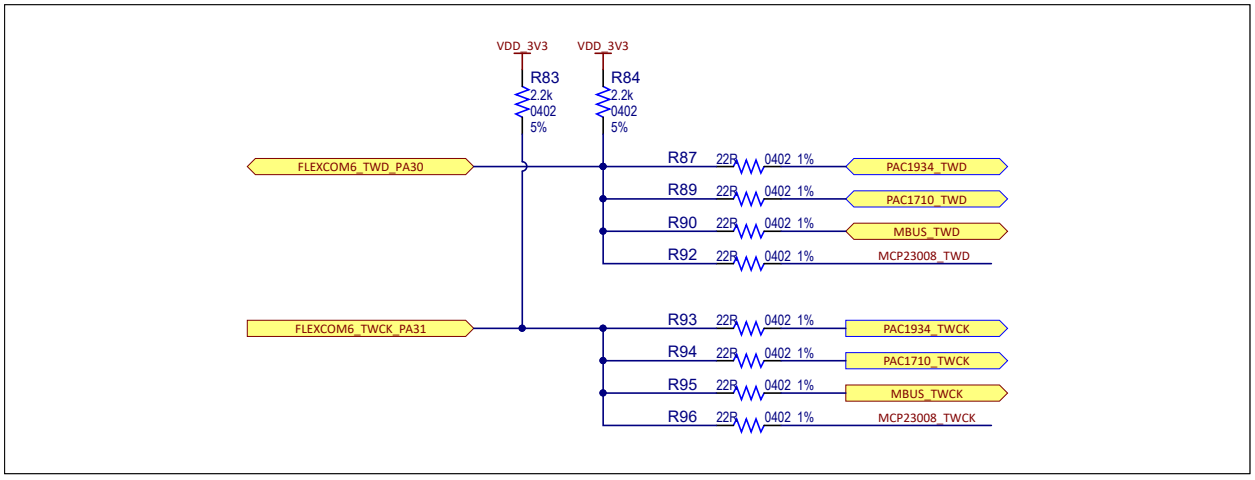
The SAM9X60-EK features two dedicated TWIs to access the devices present on board.

The TWI interface uses only two lines, namely serial data (TWD) and serial clock (TWCK). According to the standard, the TWI clock rate is limited to 400 kHz in Fast mode and 100 kHz in Normal mode, but a configurable baud rate generator permits the output data rate to be adapted to a wide range of core clock frequencies. The TWI supports both Master and Slave modes.

One interface is used to access the devices placed in the lower left side of the board:

- The PAC1934 voltage monitor (address: 0010_111[R/W])
- The PAC1710 voltage monitor (address: 1001_101[R/W])
- The MCP23008 Port Expander (address: 0100_000[R/W])
- And any device placed on the mikroBUS connector

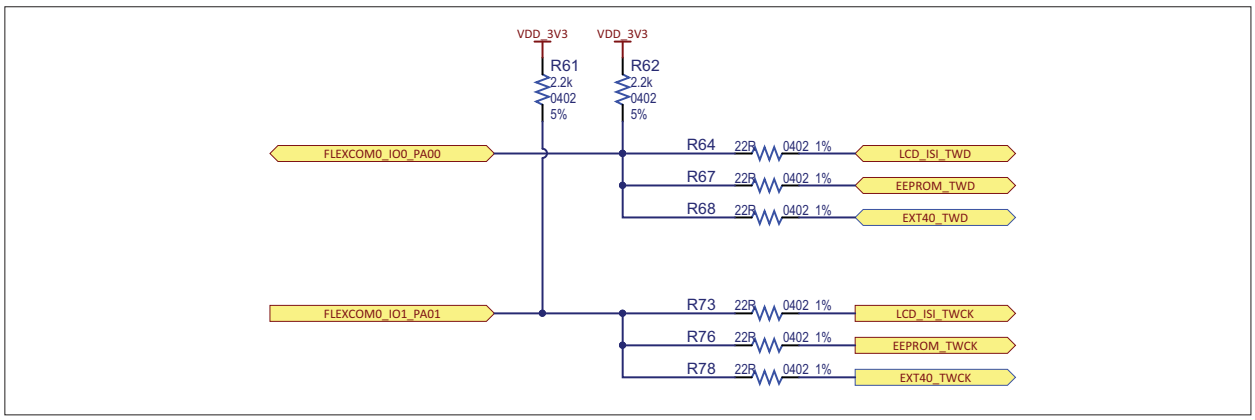
Figure 3-17. Board Lower Left TWI Interface



The second interface is used to access the devices placed in the upper right side of the board:

- The 24AA025E48 serial EEPROM (address: 1010_011[R/W])
- The LCD or camera connected on the ISI connector
- And any device connected on the external 40-pin connector

Figure 3-18. Board Upper Right TWI Interface



3.2.8 I/O Expander

The SAM9X60-EK features an 8-bit I/O expander with serial TWI interface MCP23008.

The MCP23008 consists of multiple 8-bit configuration registers for input, output and polarity selection. The system master can enable the I/Os as either inputs or outputs by writing the I/O configuration bits.

The data for each input or output is kept in the corresponding input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The interrupt output can be configured to activate under two (mutually exclusive) conditions:

- When any input state differs from its corresponding input port register state (indicating to the system master that an input state has changed)
- When an input state differs from a preconfigured register value

The Interrupt Capture register captures port values at the time of the interrupt, thereby saving the condition that caused the interrupt.

The Power-on Reset (POR) sets the registers to their default values and initializes the device state machine.

The MCP23008 communicates with the MPU via a TWI bus.

Figure 3-19. Processor IO Expander

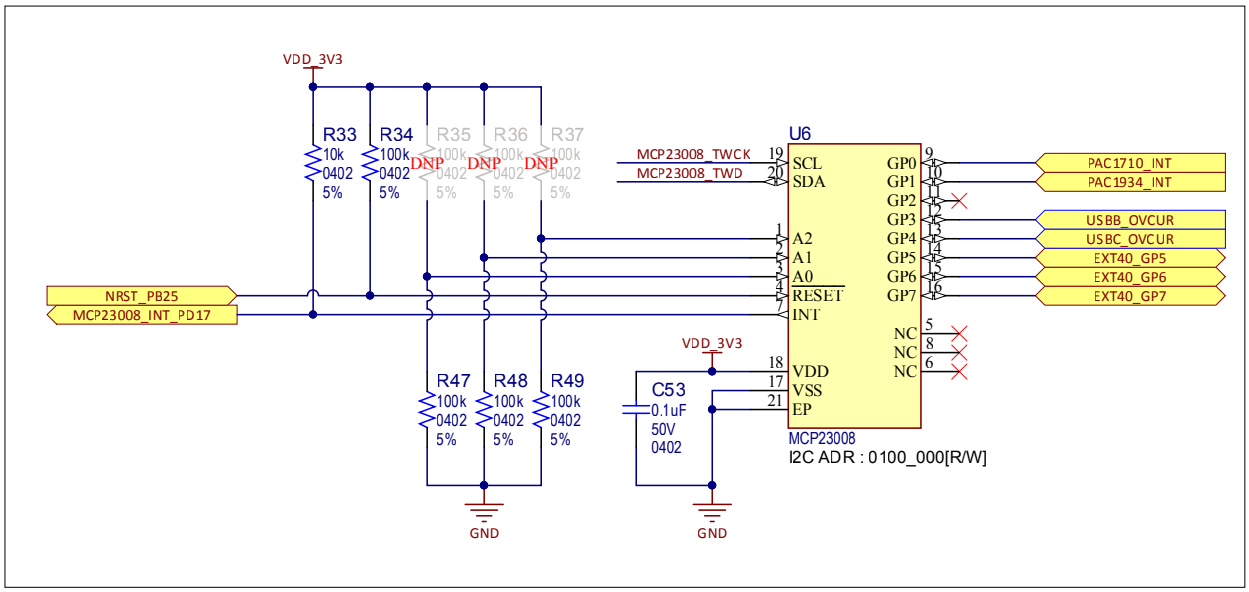


Table 3-4. I/O Expander Signal Descriptions

PIO	Signal Name	Signal Description
GP0	PAC1710_INT	PAC1710 interrupt to MPU
GP1	PAC1934_INT	PAC1934 interrupt to MPU
GP2	–	–
GP3	USBB_OVCUR	USB B overcurrent indicator
GP4	USBC_OVCUR	USB C overcurrent indicator
GP5	EXT40_GP5	Free use GPIO
GP6	EXT40_GP6	Free use GPIO
GP7	EXT40_GP7	Free use GPIO
INT	MCP23008_INT_PD17	MCP23008 Interrupt to MPU
RESET	–	nRST
SCL	MCP23008_TWCK	MCP23008 TWI clock
SDA	MCP23008_TWD	MCP23008 TWI data

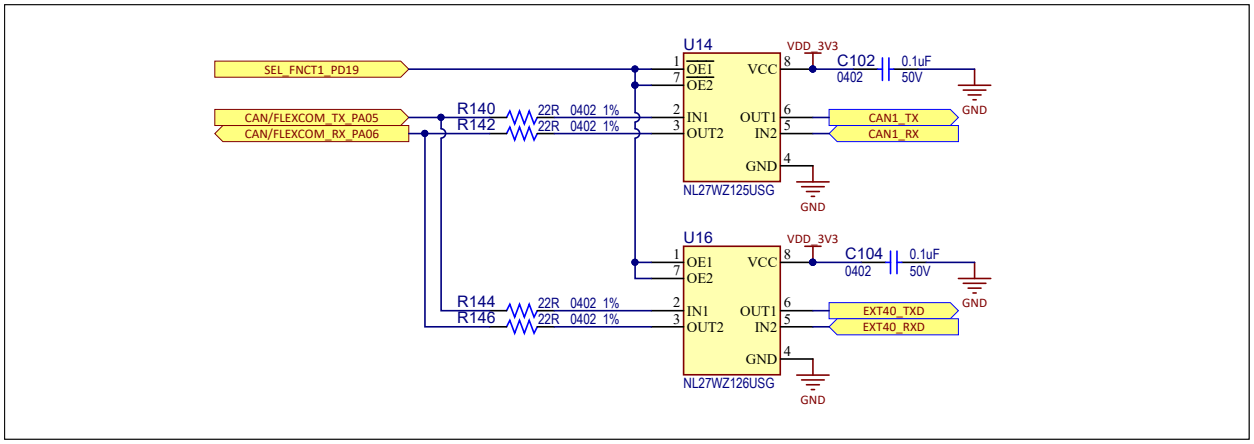
3.2.9 Special Function Selectors

Some ports shared between different interfaces are separated using dedicated signal buffers to avoid any possible interference on the lines.

Ports PA05 and PA06 are shared between the CAN1 transceiver and a UART interface going to the 40-pin connector. The selection is done using port PD19:

- HIGH = UART to 40-pin connector
- LOW = CAN1 communication

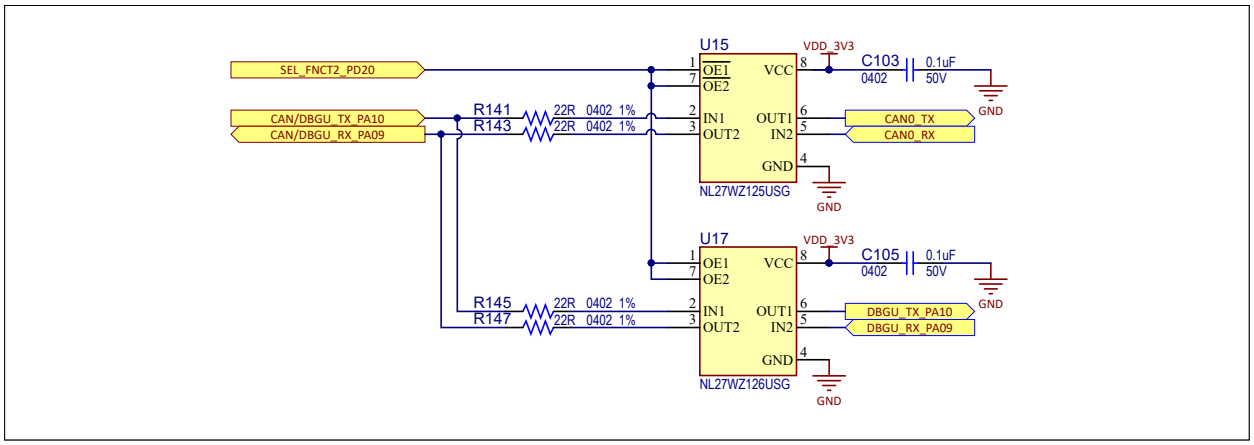
Figure 3-20. Selection between CAN1 or EXT40 UART



Ports PA09 and PA10 are shared between the CAN0 transceiver and the DEBUG UART interface going to the DEBUG connector. The selection is done using port PD20:

- HIGH = DEBUG UART communication
- LOW = CAN0 communication

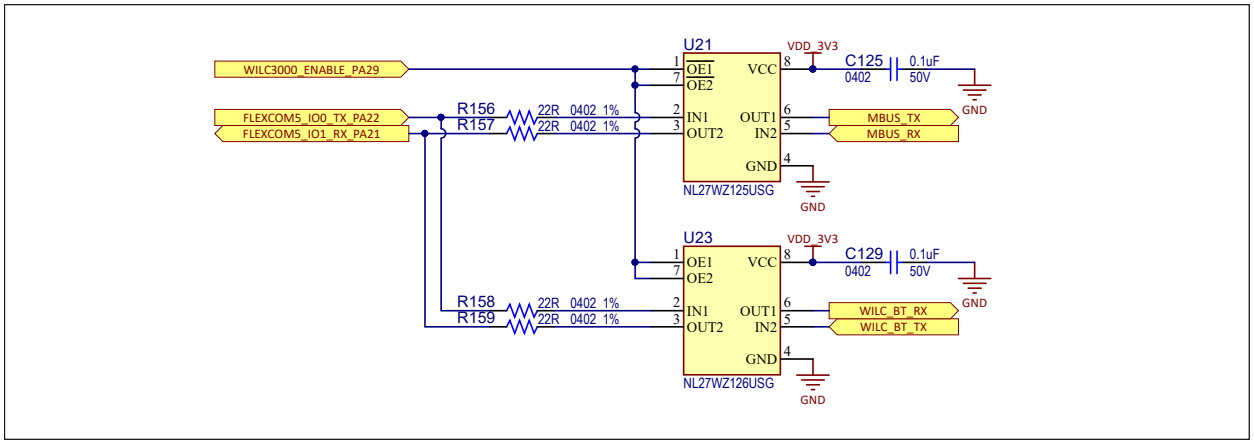
Figure 3-21. Selection between CAN0 or DBGU UART



Ports PA21 and PA22 are shared between a UART interface going to the mikroBUS connector and the UART interface used to access and configure the Bluetooth functions of the ATWILC3000 module. The selection is done using port PA29:

- HIGH = ATWILC3000 UART communication
- LOW = MikroBUS CAN communication

Figure 3-22. Selection between mikroBUS UART or ATWILC3000 Bluetooth UART



When developing an application, the designer must keep in mind to first configure the values for the selection ports (PA29, PD19 and PD20) to ensure the signal takes the desired path.

3.3 On-board Memories

The SAM9X60 features a DDR/SDR memory interface and an External Bus Interface (EBI) to enable interfacing to a wide range of external memories and to almost any type of parallel peripheral.

This section describes the memory devices mounted on the SAM9X60-EK board:

- One DDR2 SDRAM
- One NAND Flash
- One QSPI Flash
- One serial EEPROM

Additional memory can be added to the board by:

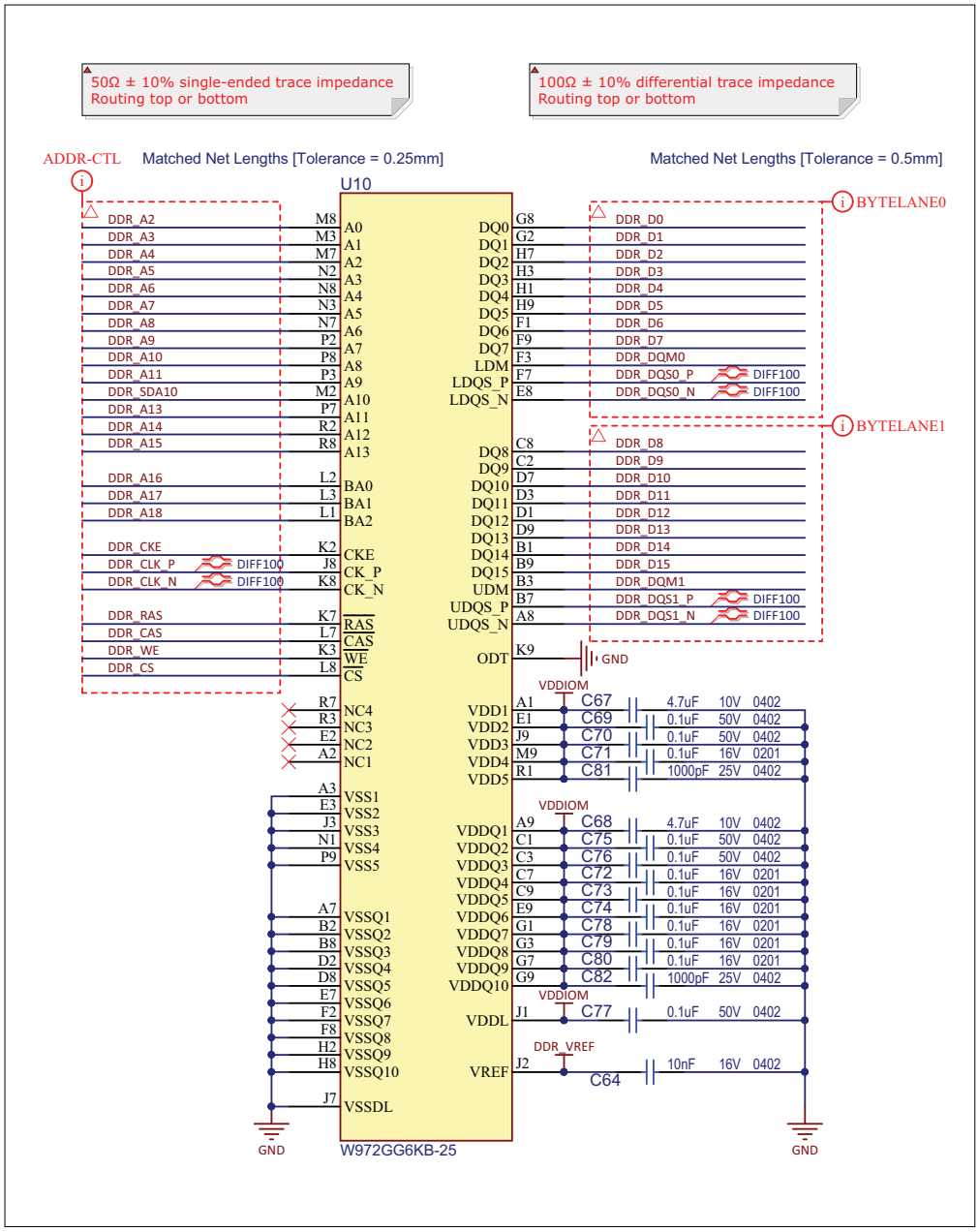
- Installing an SD or MMC card in the SD/MMC slot,
- Using the USB ports.

Support is dependent upon driver support in the OS.

3.3.1 DDR2/SDRAM

One DDR2/SDRAM (2-Gbit W972GG6KB = 16 Mwords x 16 bits x 8 banks) is used as main system memory, totaling 256 KBytes of SDRAM on the board. The memory bus is 16 bits wide and operates with a frequency of up to 200 MHz.

Figure 3-23. DDR2/SDRAM



3.3.2 NAND FLASH

The SAM9X60-EK has native support for NAND Flash memory through its NAND Flash Controller. The board implements one MT29F4G08ABA 4Gb x 8 NAND Flash connected to Chip Select three (NCS3) of the microcontroller. That makes a 512-Mbyte memory space.

Figure 3-24. NAND Flash

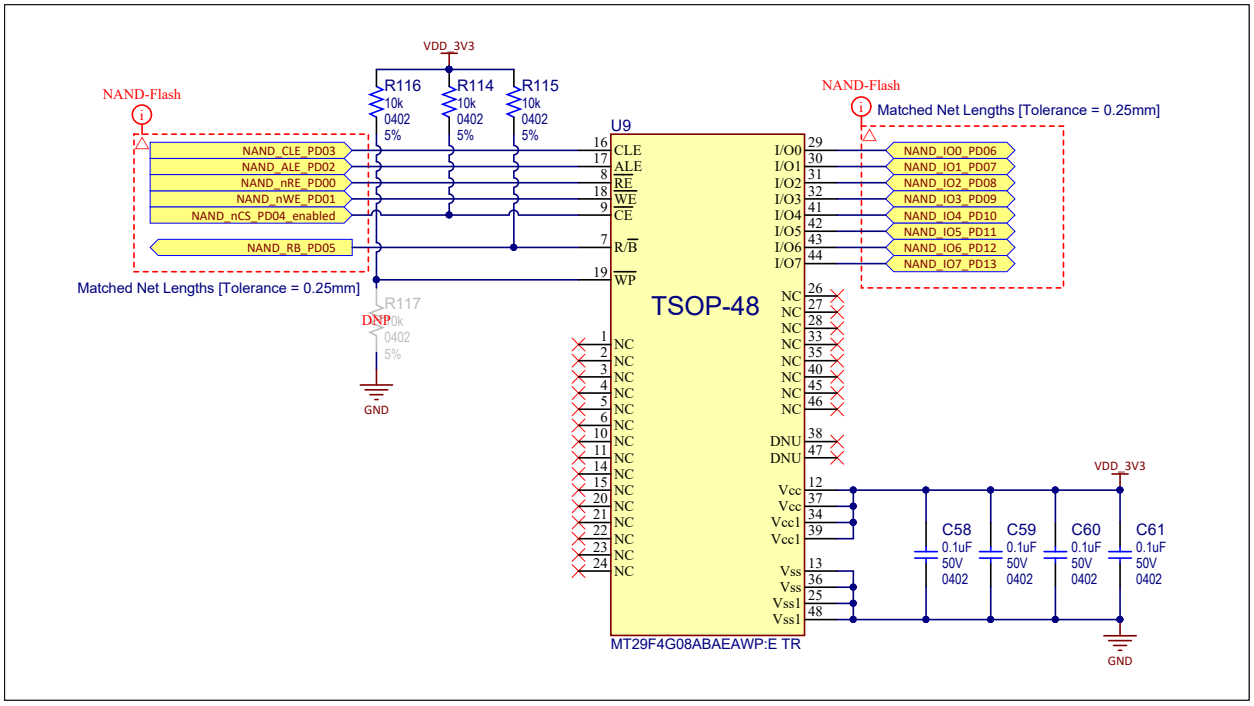


Table 3-5. NAND Flash Signal Descriptions

PIO	Signal Name	Shared PIO	Signal Description
PD6	NAND_IO0_PD06	–	Data 0
PD7	NAND_IO0_PD07	–	Data 1
PD8	NAND_IO0_PD08	–	Data 2
PD9	NAND_IO0_PD09	–	Data 3
PD10	NAND_IO0_PD10	–	Data 4
PD11	NAND_IO0_PD11	–	Data 5
PD12	NAND_IO0_PD12	–	Data 6
PD13	NAND_IO0_PD13	–	Data 7
PD1	NAND_nWE_PD01	–	Write Enable
PD4	NAND_nCS_PD04_enabled	–	Chip Select (through a Disable Boot control buffer – see 3.5.5 Disable Boot)
PD2	NAND_ALE_PD02	–	Address Latch Enable
PD3	NAND_CLE_PD03	–	Command Latch Enable
PD0	NAND_nRE_PD00	–	Output Enable
PD5	NAND_RB_PD05	–	Ready/Busy#

3.3.3 QSPI Serial Flash

The SAM9X60-EK board features one Quad Serial Peripheral Interface (QSPI) memory SST26VF064B.

A QSPI bus is a synchronous serial data link that provides communication with external devices in Master mode.

The QSPI can be used in SPI mode to interface with serial peripherals (such as ADCs, DACs, LCD controllers, CAN controllers and sensors), or in Serial Memory mode to interface with serial Flash memories.

The QSPI allows the system to execute code directly from a serial Flash memory (XIP, or Execute In Place, technology) without code shadowing to RAM. The Flash memory communication protocol is serial, however it is seen in the system as a conventional parallel memory (ROM, SRAM, DRAM, embedded Flash memory, etc.).

With the support of the Quad SPI protocol, the QSPI allows the system to use high-performance serial Flash memories which are small and inexpensive, instead of larger and more expensive parallel Flash memories.

Figure 3-25. QSPI Serial Flash

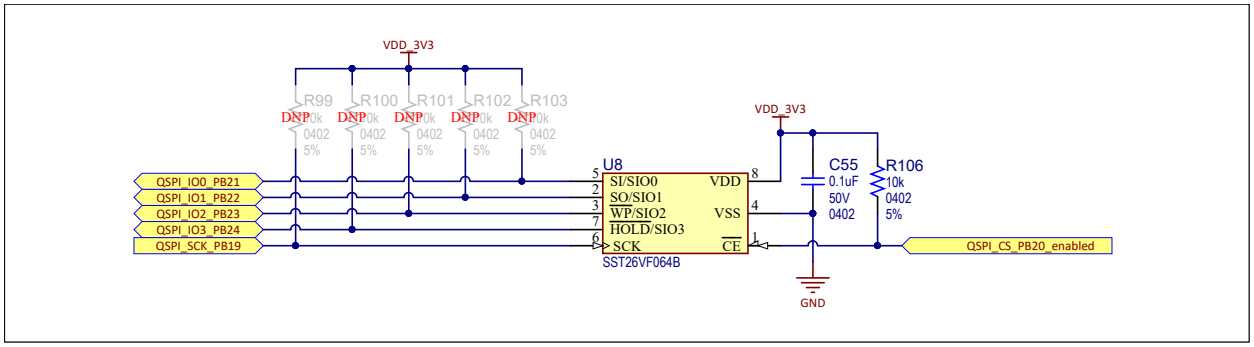


Table 3-6. QSPI Signal Descriptions

PIO	Signal Name	Shared PIO	Signal Description
PB19	QSPI0_SCK_PB19	I2SMCC_CK	QSPI Clock
PB20	QSPI0_CS_PB20_enabled	I2SMCC_WS	Chip Select (through a Disable Boot control buffer – see 3.5.5 Disable Boot)
PB21	QSPI0_IO0_PB21	I2SMCC_DIN0	Data0
PB22	QSPI0_IO1_PB22	I2SMCC_DOUT0	Data1
PB23	QSPI0_IO2_PB23	I2SMCC_MCL	Data2
PB24	QSPI0_IO3_PB24	–	Data3

3.3.4 Serial EEPROM with Unique MAC Address

The SAM9X60-EK board embeds one Microchip 24AA025E48 serial EEPROM. The 24AA025E48 features 2048 bits of serial Electrically-Erasable Programmable Read-Only Memory (EEPROM) organized as 256 words of eight bits each and is accessed via an I^2C-compatible (2-wire) serial interface. In addition, the 24AA025E48 incorporates an easy and inexpensive method to obtain a globally unique MAC or EUI address (EUI-48™). For more information about the 24AA025E48, refer to the product web page.

The EUI-48 addresses can be assigned as the actual physical address of a system hardware device or node, or it can be assigned to a software instance. These addresses are factory-programmed by Microchip and unique. They are permanently write-protected in an extended memory block located outside the standard 2-Kbit memory array.

Figure 3-26. EEPROM 24AA02E48

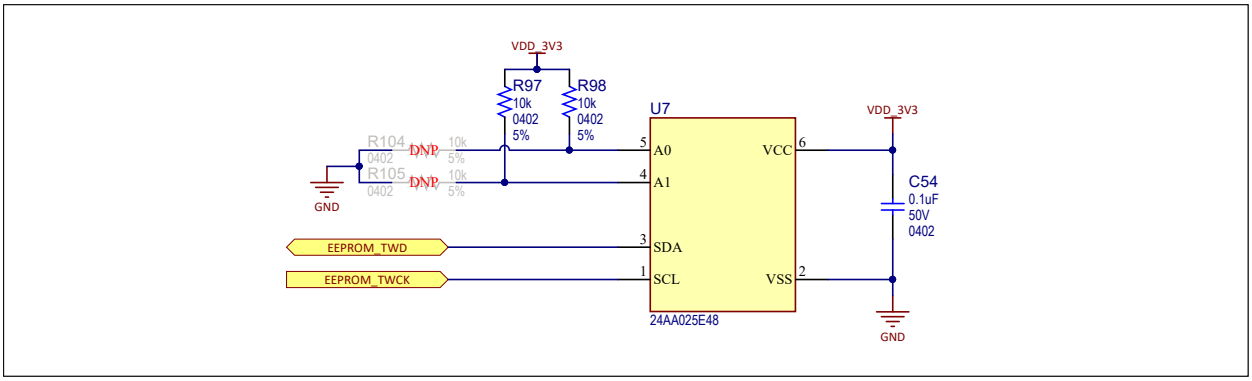


Table 3-7. EEPROM PIO Signal Descriptions

PIO	Signal Name	Shared PIO	Signal Description
PA00	EEPROM_TWD	TWI and SPI	TWI data
PA01	EEPROM_TWCK	TWI and SPI	TWI clock

In the SAM9X60-EK usage context, the EEPROM device is used as a “software label” to store board information such as chip type, manufacturer name and production date, using the last two 16-byte blocks in memory. The information contained in these blocks should not be modified.

3.4 Peripherals

Several interfaces and connectors are implemented in the SAM9X60-EK with the purpose of enabling the user to test all the features that the MPU can offer and to facilitate a reference design for future customer applications.

This section describes the following peripherals mounted on the SAM9X60-EK board:

- Ethernet 10/100 port (GMAC)
- USB host/device
- Wi-Fi/Bluetooth module (optional)
- Controller Area Network (CAN) interface
- Liquid Crystal Display (LCD) interface
- Image Sensor Interface (ISI)
- Audio Class D (CLASSD) amplifier
- Secure Digital Multimedia Card (SDMMC)
- mikroBUS interface
- GPIO interface

3.4.1 Ethernet 10/100 Port (GMAC)

The KSZ8081 is a single-supply 10Base-T/100Base-TX Ethernet physical-layer transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable. The KSZ8081 is a highly-integrated PHY solution. It reduces board cost and simplifies board layout by using on-chip termination resistors for the differential pairs and by integrating a low-noise regulator to supply the 1.2V core, and by offering 1.8/2.5/3.3V digital I/O interface support.

The KSZ8081RNA is connected over the Reduced Media Independent Interface (RMII) directly to the RMII-compliant MAC inside the SAM9X60 MPU. As the power-up default, the KSZ8081RNA uses a 25 MHz MEMS oscillator to generate all required clocks, including the 50-MHz RMII reference clock output for the MAC. For more information about the KSZ8081RNx, refer to the product web page.

An individual unique 48-bit MAC address (Ethernet hardware address) is allocated to this product and is stored in the Microchip 24AA025E48 TWI serial EEPROM described in 3.3.4 Serial EEPROM with Unique MAC Address.

Additionally, for monitoring and control purposes, a LED functionality is carried on the RJ45 connectors to indicate activity, link, and speed status.

Figure 3-27. Ethernet Interface

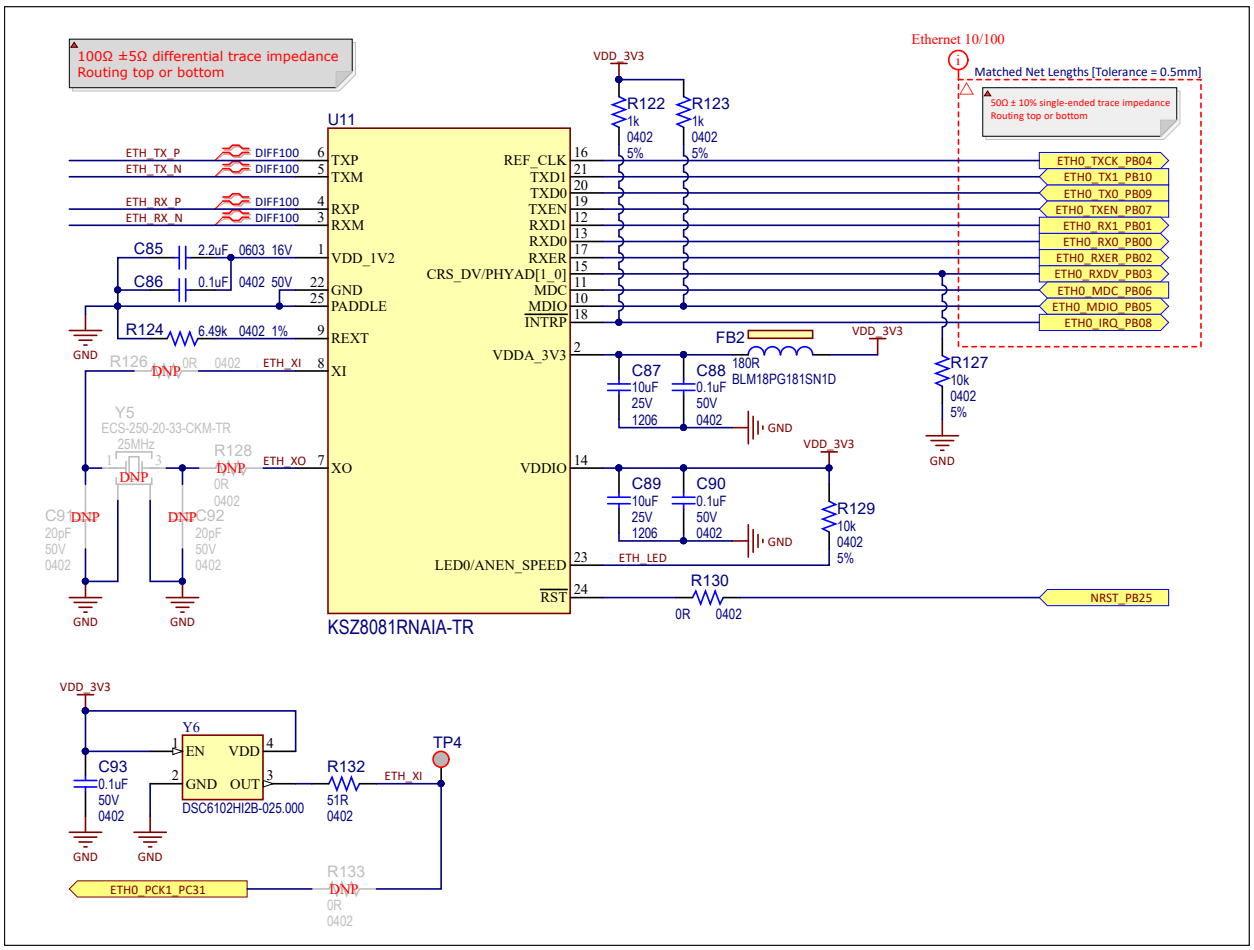


Table 3-8. Ethernet PHY 10/100 Signal Descriptions

PIO	Signal Name	Shared	Signal Description
PB04	ETH_TXCK_PB24	–	Transmit clock
PB07	ETH_TXEN_PB10	–	Transmit enable
PB03	ETH_RXDV_PB03	–	Receive data valid
PB02	ETH_RXER_PB02	–	Receive error
PB00	ETH_RX0_PB00	–	Receive data 0
PB01	ETH_RX1_PB01	–	Receive data 1
PB09	ETH_TX0_PB09	–	Transmit data 0
PB10	ETH_TX1_PB10	–	Transmit data 1
PB06	ETH_MDC_PB06	–	Management data clock
PB05	ETH_MDIO_PB05	–	Management data in/out
PB08	ETH_IRQ_PB08	–	Interrupt

Figure 3-28. Ethernet PHY Connector

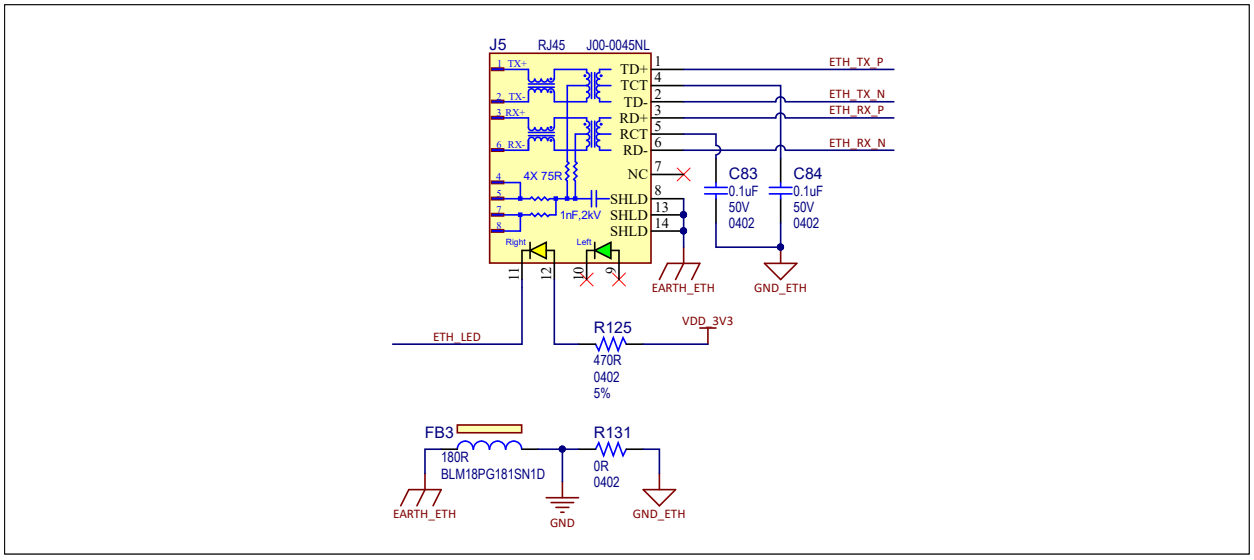


Table 3-9. Ethernet RJ45 Connector J5 Pin Assignment

Pin No	Signal Name	Signal Description
1	TD+	Transmit
2	TD-	Transmit
3	RD+	Receive
4	Decoupling capacitor	–
5	Decoupling capacitor	–
6	RD-	Receive
7	NC	–
8	EARTH / GND	Common ground
9	ACT LED	LED activity
10	ACT LED	LED activity
11	LINK LED	LED link connection
12	LINK LED	LED link connection
13	EARTH / GND	Common ground
14	EARTH / GND	Common ground
15	NC	–
16	NC	–

3.4.2 USB Host/Device

The USB (Universal Serial Bus) is a hot-pluggable general-purpose high-speed I/O standard for computer peripherals. The standard defines connector types, cabling, and communication protocols for interconnecting a wide variety of electronic devices. The USB 2.0 Specification defines data transfer rates as high as 480 Mbps (also known as High Speed USB). A USB host bus connector uses four pins: a power supply pin (5V), a differential pair (D+ and D- pins) and a ground pin.

The SAM9X60-EK board features three USB communication ports named USB-A to USB-C™.

The USB-A port can act only as a USB device interface and can be accessed via the USB Micro-B connector (J7).

Two resistors are placed on its power rail to form a voltage divider, converting 5V into 3.3V that is then used to signal the presence of a USB host to the MPU.

In the case of board bring-up, USB-A is the default port used to connect to the MPU over SAM-BA (SAM Boot Assistance). For more information, refer to the product web page.

The USB-A port is also used as a secondary power source, as mentioned in 3.1 Power Supply Topology and Power Distribution. In most cases, this port is limited to 500 mA.

Figure 3-29. USB-A Port

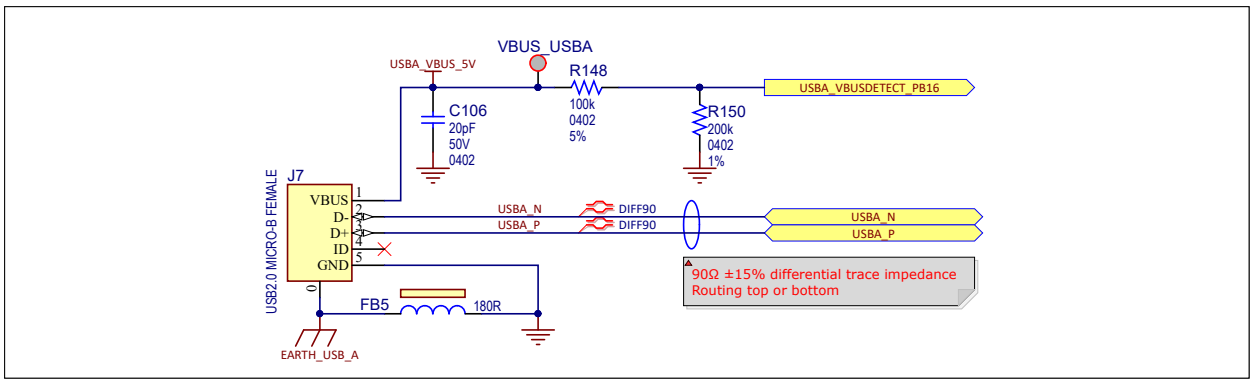


Table 3-10. USB-A Connector Signal Descriptions

Pin No	Signal Name	Signal Description
1	USBA_VBUS_5V	First port 5V power
2	USBA_N	First port data minus
3	USBA_P	First port data plus
4	ID	– (not used)
5	GND	First port ground

Table 3-11. USB-A PIO Signal Descriptions

PIO	Signal Name	Shared	Signal Description
PB16	USBA_VBUSDETECT_PB16	–	VBUS detection

The USB-B and USB-C ports are connected to the stacked USB Type-A connector (J8) and each port can act both as device and as host.

Figure 3-30. USB-B and USB-C Ports

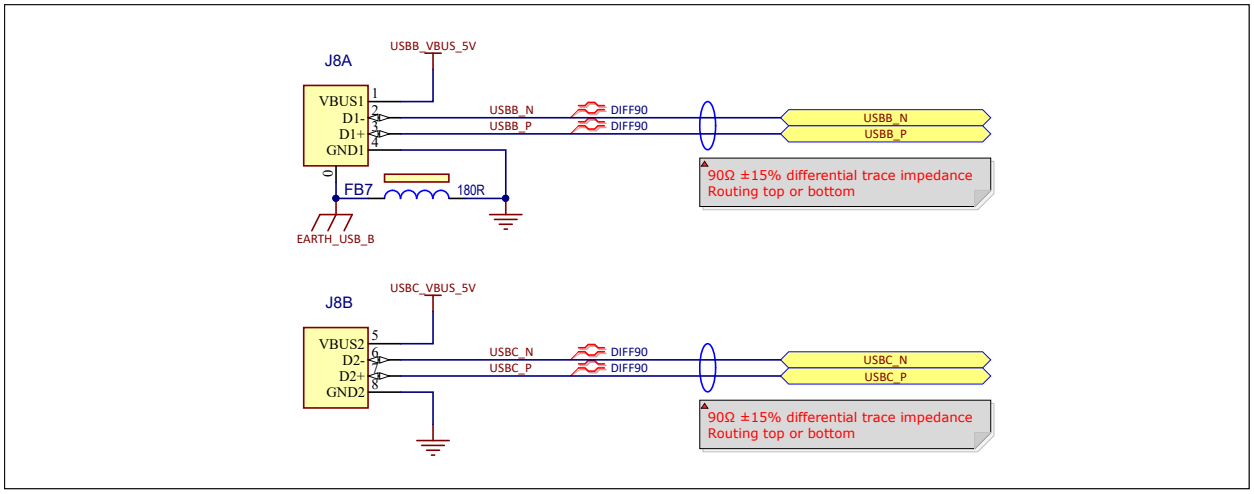


Table 3-12. USB-B and USB-C Connector Signal Descriptions

Pin No	Signal Name	Signal Description
0	EARTH_USB_B	Connector chassis connected to ground
1	USBB_VBUS_5V	Second port 5V power
2	USBB_N	Second port data minus
3	USBB_P	Second port data plus
4	GND	Second port ground
5	USBC_VBUS_5V	Third port 5V power
6	USBC_N	Third port data minus
7	USBC_P	Third port data plus
8	GND	Third port ground

In Host mode, the USB Host ports B and C are equipped with 500-mA high-side power switches to enable self-powered and bus-powered applications. The USBx_EN_5V_PDxx signal controls the current limiting power switch MIC2025, which in turn supplies power to a client device. Per the USB specification, bus-powered USB 2.0 devices are limited to a maximum of 500 mA, therefore the MIC2025 limits the current and indicates an overcurrent with the USBx_OVCUR signal. For more information about the MIC2025, refer to the product web page.

Figure 3-31. USB Power Switches

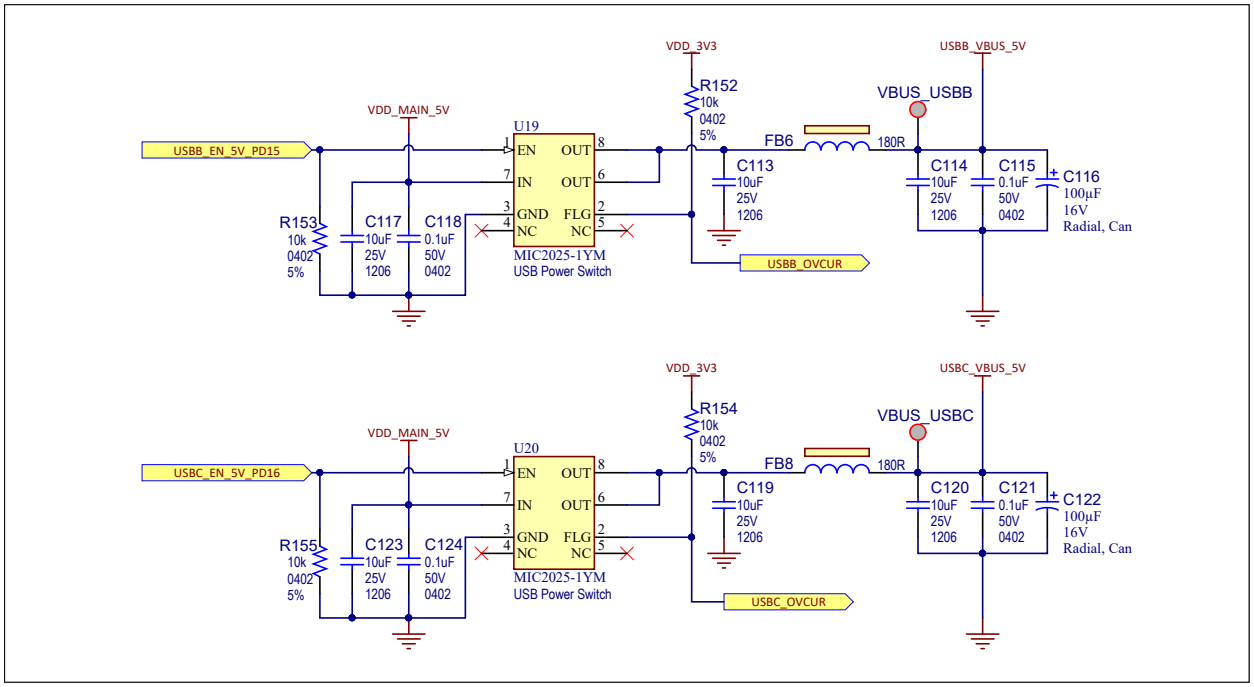


Table 3-13. USB Power Switch PIO Signal Descriptions

PIO	Signal Name	Shared	Signal Description
PD14	USBA_EN_5V_PD14	–	Power switch enable (active high)
GP2 expander	USBA_OVCUR	–	Indicates overcurrent (open drain)
PD15	USBA_EN_5V_PD15	–	Power switch enable (active high)
GP3 expander	USBB_OVCUR	–	Indicates overcurrent (open drain)
PD16	USBC_EN_5V_PD16	–	Power switch enable (active high)
GP4 expander	USBC_OVCUR	–	Indicates overcurrent (open drain)

3.4.3 Wi-Fi/Bluetooth Module (Optional)

The user has the option to solder an ATWILC3000-MR110CA Wi-Fi/BT module with a chip antenna.

The ATWILC3000-MR110PA WLAN PHY is designed to achieve a reliable and power-efficient physical layer communication as specified by IEEE® 802.11 b/g/n in Single Stream mode with a 20-MHz bandwidth. Advanced algorithms are used to achieve maximum throughput in a real-world communication environment with impairments and interference. The PHY implements all required functions such as FFT, filtering, FEC (Viterbi decoder), frequency and timing acquisition and tracking, channel estimation and equalization, carrier sensing and clear channel assessment, as well as automatic gain control. The module is available in a fully certified, 22.428 x 17.732 mm, 36-pin module package. For more information about the ATWILC3000, refer to the product web page.

Figure 3-32. Wi-Fi/Bluetooth Interface

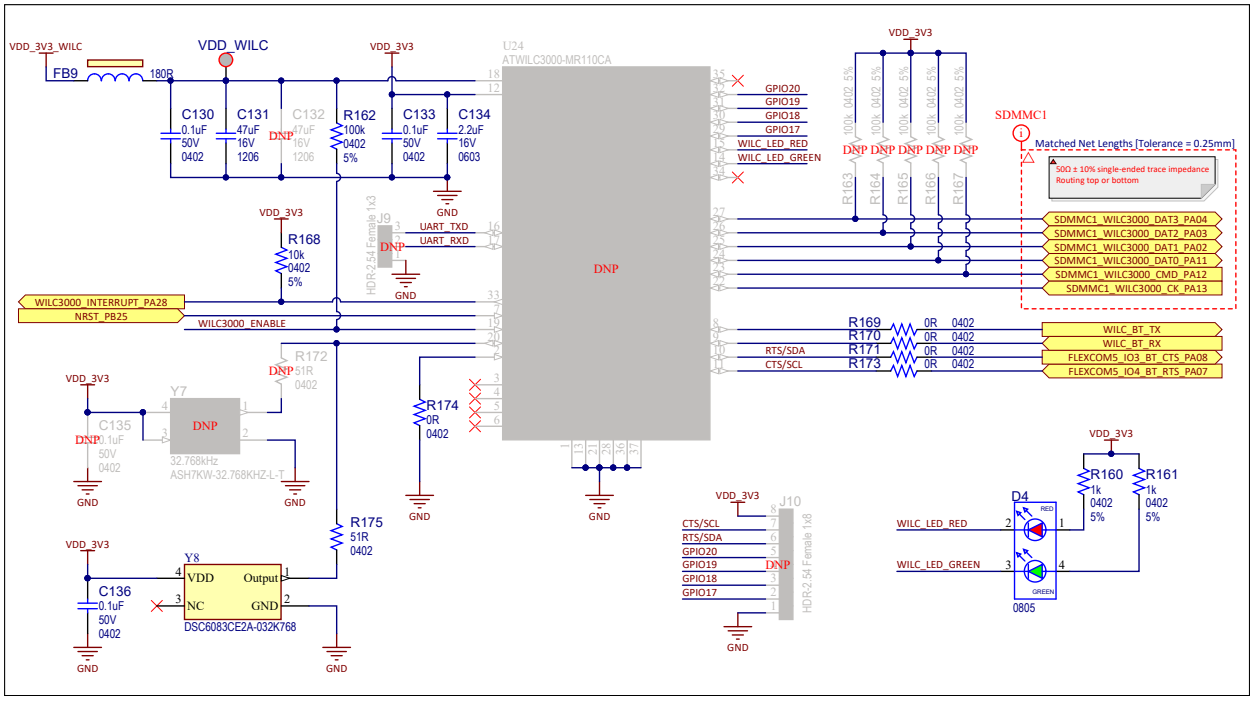


Table 3-14. Wi-Fi/Bluetooth Signal Descriptions

PIO	Signal Name	Shared	Signal Description
PA11	SDMMC1_WILC3000_DAT0_PA11	–	SDIO data
PA02	SDMMC1_WILC3000_DAT1_PA02	–	SDIO data
PA03	SDMMC1_WILC3000_DAT2_PA03	–	SDIO data
PA04	SDMMC1_WILC3000_DAT3_PA04	–	SDIO data
PA12	SDMMC1_WILC3000_CMD_PA12	–	SDIO command
PA13	SDMMC1_WILC3000_CK_PA13	–	SDIO clock
PA21	FLEXCOM1_IO1_RX_PA21	–	Bluetooth serial TX (RX into SAM9X60)
PA22	FLEXCOM1_IO0_TX_PA22	–	Bluetooth serial RX (TX from SAM9X60)
PA07	FLEXCOM1_IO1_RTS_PA07	–	Bluetooth serial RTS
PA08	FLEXCOM1_IO1_CTS_PA08	–	Bluetooth serial CTS
PB25	NRST_PB25	–	Module reset
PA28	WILC3000_INTERUPT_PA28	–	Interrupt
PA29	WILC3000_ENABLE_PA29	–	Chip enable

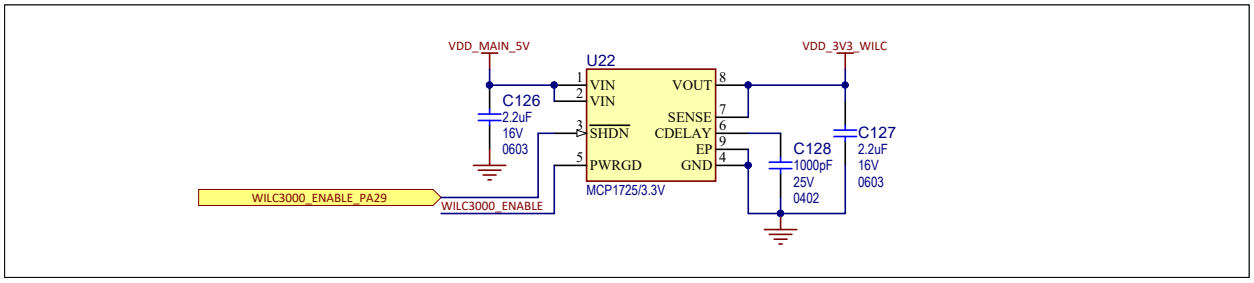
Special care must be taken when powering the ATWILC3000 wireless module. Due to the nature of the wireless transmission, the module draws a lot of current from its supply rail. In the worst-case scenario, the module can draw up to 300 mA. The main PMIC on the board, the MIC2800, has a maximum output capacity of 300 mA on its 3.3V rail, therefore it is not fit to power this module alongside the other components on the board.

To address this issue, the module is fitted with its own separate power supply, the MCP1725, which is a 500-mA Low Dropout (LDO) linear regulator that provides high current and low output voltages in a very small package. For more information about the MCP1725, refer to the product web page.

The MCP1725 was chosen because it can supply the current required by the module, and because it features a shutdown input pin (SHDN) and a Power Good output pin (PWRGD):

- The SHDN input allows to shut down the wireless module if it is unused, therefore saving power.
- The PWRGD output ensures that the ATWILC3000 wireless module is kept in reset until its power rails are stable.

Figure 3-33. Wi-Fi/Bluetooth Enable



Note: Enabling the ATWILC3000 module prevents the Flexcom UART from being used with the mikroBUS connector (this is switched by U23).

3.4.4 Controller Area Network (CAN) Interface

Two MCP2542 transceivers are placed on the SAM9X60-EK.

The MCP2542 is a high-speed CAN transceiver that provides the interface between the Controller Area Network (CAN) protocol controller and the physical two-wire bus. For more information about the MCP2542, refer to the product web page.

Figure 3-34. Dual CAN Interface

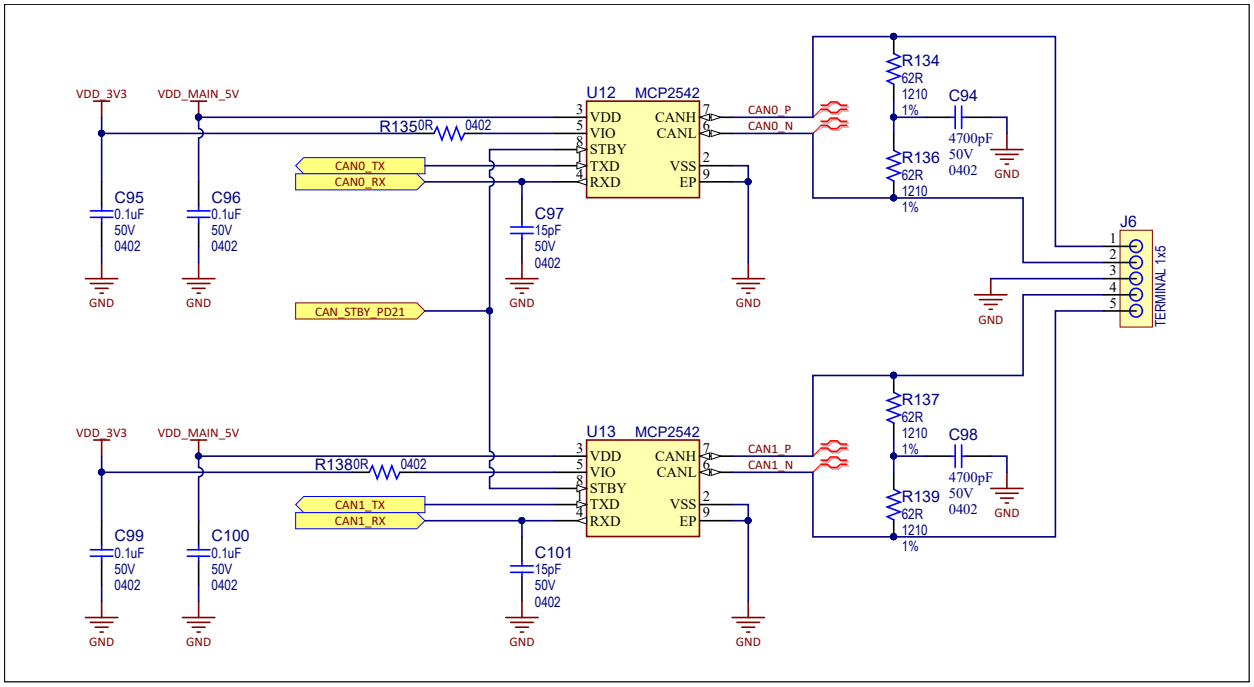


Table 3-15. CAN Signal Descriptions

PIO	Signal Name	Shared	Signal Description
PD21	CAN_STBY_PD21	–	Dual CAN standby
PA10	CAN0_TX_PA10	–	CAN transmit port 0
PA09	CAN0_RX_PA09	–	CAN receive port 0
PA05	CAN1_TX_PA05	–	CAN transmit port 1
PA06	CAN1_RX_PA06	–	CAN receive port 1

Table 3-16. CAN Connector J6 Signal Description

Pin No	Signal Name	Signal Description
1	CANH	Differential positive port 0
2	CANL	Differential negative port 0
3	GND	Common ground
4	CANH	Differential positive port 1
5	CANL	Differential negative port 1

CAN1 function and UART on the external 40-pin connector are shared and selectable through the SEL_FNCT1_PD19 PIO.

CAN0 function and Debug UART are shared and selectable through the SEL_FNCT2_PD20 PIO.

3.4.5 Liquid Crystal Display (LCD) Interface

The SAM9X60-EK board provides a connector with 24 bits of data and control signals to the LCD interface.

Optional displays such as AC320005-5 (refer to the product web page) can be connected to the board.

In order to operate correctly with various LCD modules, two voltage lines are available: 3.3V and 5VDC (default). The selection is made with 0R resistors.

J15 is a 1.27-mm pitch, 50-pin header. It gives access to the LCD signals.

Figure 3-35. LCD Connector

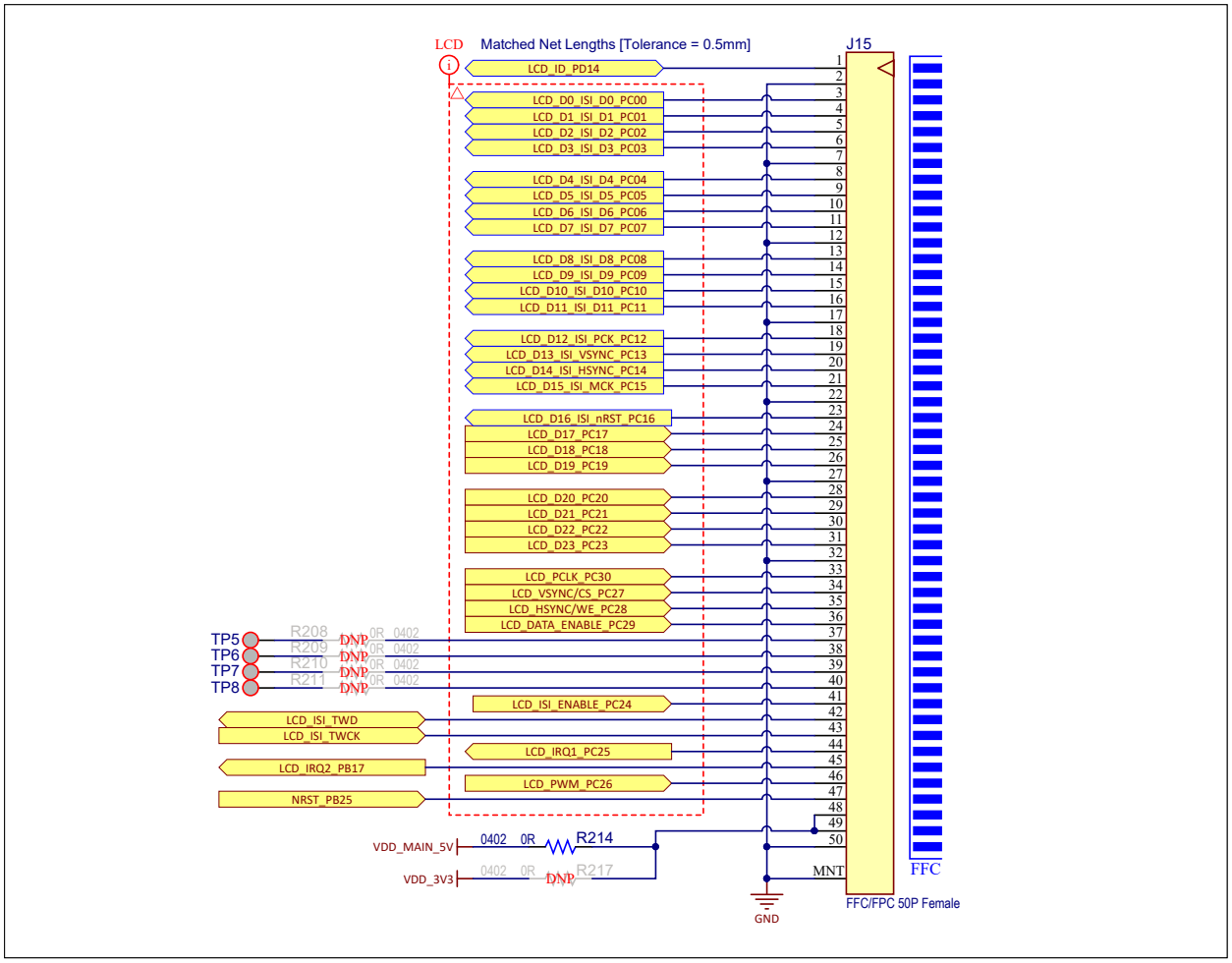


Table 3-17. LCD Connector J15 Signal Descriptions

Pin No	LCD pin	PIO	Signal	Function
1	ID	PD18	LCDID_PD18	ID LCD module
2	GND	–	GND	Ground
3	LCDDAT0	PC0	LCD_D0_ISI_D0_PC00	Data line
4	LCDDAT1	PC1	LCD_D1_ISI_D1_PC01	Data line
5	LCDDAT2	PC2	LCD_D2_ISI_D2_PC02	Data line
6	LCDDAT3	PC3	LCD_D3_ISI_D3_PC03	Data line
7	GND	–	GND	Ground
8	LCDDAT4	PC4	LCD_D4_ISI_D4_PC04	Data line
9	LCDDAT5	PC5	LCD_D5_ISI_D5_PC05	Data line
10	LCDDAT6	PC6	LCD_D6_ISI_D6_PC06	Data line
11	LCDDAT7	PC7	LCD_D7_ISI_D7_PC07	Data line
12	GND	–	GND	Ground
13	LCDDAT8	PC8	LCD_D8_ISI_D8_PC08	Data line

.....continued

Pin No	LCD pin	PIO	Signal	Function
14	LCDDAT9	PC9	LCD_D9_ISI_D9_PC09	Data line
15	LCDDAT10	PC10	LCD_D10_ISI_D10_PC10	Data line
16	LCDDAT11	PC11	LCD_D11_ISI_D11_PC11	Data line
17	GND	–	GND	Ground
18	LCDDAT12	PC12	LCD_D12_ISI_PCK_PC12	Data line
19	LCDDAT13	PC13	LCD_D13_ISI_VSYNC_PC13	Data line
20	LCDDAT14	PC14	LCD_D14_ISI_HSYNC_PC14	Data line
21	LCDDAT15	PC15	LCD_D15_ISI_MCK_PC15	Data line
22	GND	–	GND	Ground
23	LCDDAT16	PC16	LCD_D16_PC16	Data line
24	LCDDAT17	PC17	LCD_D17_PC17	Data line
25	LCDDAT18	PC18	LCD_D18_PC18	Data line
26	LCDDAT19	PC19	LCD_D19_PC19	Data line
27	GND	–	GND	Ground
28	LCDDAT20	PC20	LCD_D20_PC20	Data line
29	LCDDAT21	PC21	LCD_D21_PC21	Data line
30	LCDDAT22	PC22	LCD_D22_PC22	Data line
31	LCDDAT23	PC23	LCD_D23_PC23	Data line
32	GND	–	GND	Ground
33	LCDPCK	PC30	LCD_PCLK_PC30	Pixel clock
34	LCDVSYNC	PC27	LCD_VSYNC/CS_PC27	Vertical synchronization
35	LCDHSYNC	PC28	LCD_HSYNC/WE_PC28	Horizontal synchronization
36	LCDDEN	PC29	LCD_DATA_ENABLE_PC29	Data enable
37	SPI_SPCK	–	NC	Test point to access the SPI interface via DNP resistor (see Figure 3-35)
38	SPI_MOSI	–	NC	Test point to access the SPI interface via DNP resistor (see Figure 3-35)
39	SPI_MISO	–	NC	Test point to access the SPI interface via DNP resistor (see Figure 3-35)
40	SPI_NPCS0	–	NC	Test point to access the SPI interface via DNP resistor (see Figure 3-35)
41	LCDDISP	PC24	LCD_ISI_ENABLE_PC24	Display enable signal
42	TWD	PA00	LCD_TWD	I^2C data line (maXTouch)
43	TWCK	PA01	LCD_TWCK	I^2C clock line (maXTouch)
44	GPIO	PC25	LCD_IRQ1_PC25	maXTouch interrupt line
45	GPIO	PB17	LCD_IRQ2_PB17	Interrupt line for other I^2C devices

.....continued				
Pin No	**LCD pin**	**PIO**	**Signal**	**Function**
46	LCDPWM	PC26	LCD_PWM_PC26	Backlight control
47	RESET	PB25	NRST_PB25	Reset for both display and maXTouch
48	Main_5V/3.3V	VCC	VCC	3.3V or 5V supply (0R)
49	Main_5V/3.3V	VCC	VCC	3.3V or 5V supply (0R)
50	GND	_	GND	Ground

3.4.6 Image Sensor Interface (ISI)

The SAM9X60-EK board provides a connector (J17) for connecting a 12-bit external camera. A TWI connection is also included for controlling the camera.

WARNING The ISI interface and LCD interface are mutually exclusive and should be used one at a time.

J17 is a 30-pin, 2.54-mm pitch header. It gives access to the ISI signals.

Figure 3-36. ISI Expansion Header

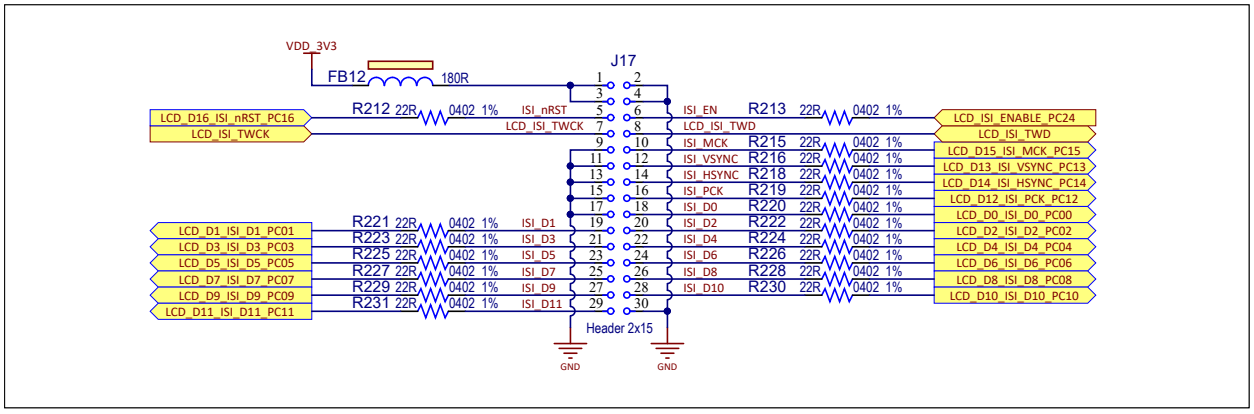


Table 3-18. ISI Connector J17 Signal Descriptions

Pin No	ISI Pin	PIO	Signal	Function
1	Main_3V3	VCC	VCC	3.3V supply
2	GND	–	GND	Ground
3	Main_3V3	VCC	VCC	3.3V supply
4	GND	–	GND	Ground
5	ISI_nRST	PC16	LCD_RESET_PC16	Camera reset line
6	ISI_EN	PC24	LCD_ISI_ENABLE_PC24	Camera enable
7	ISI_TWCK	PA00	LCD_TCKD	TWI interface clock line
8	ISI_TWD	PA01	LCD_TWD	TWI interface data line
9	GND	–	GND	Ground
10	ISI_MCK	PC15	LCD_D15_ISI_MCK_PC15	Master clock line
11	GND	–	GND	Ground

.....continued

Pin No	ISI Pin	PIO	Signal	Function
12	ISI_VSYNC	PC13	LCD_D13_ISI_VSYNC_PC13	Vertical synchronization
13	GND	–	GND	Ground
14	ISI_HSYNC	PC14	LCD_D14_ISI_HSYNC_PC14	Horizontal synchronization
15	GND	–	GND	Ground
16	ISI_PCK	PC12	LCD_D12_ISI_PCK_PC12	Clock line
17	GND	–	GND	Ground
18	ISI_D0	PC00	LCD_D0_ISI_D0_PC00	Data line
19	ISI_D1	PC01	LCD_D1_ISI_D1_PC01	Data line
20	ISI_D2	PC02	LCD_D2_ISI_D2_PC02	Data line
21	ISI_D3	PC03	LCD_D3_ISI_D3_PC03	Data line
22	ISI_D4	PC04	LCD_D4_ISI_D4_PC04	Data line
23	ISI_D5	PC05	LCD_D5_ISI_D5_PC05	Data line
24	ISI_D6	PC06	LCD_D6_ISI_D6_PC06	Data line
25	ISI_D7	PC07	LCD_D7_ISI_D7_PC07	Data line
26	ISI_D8	PC08	LCD_D8_ISI_D8_PC08	Data line
27	ISI_D9	PC09	LCD_D9_ISI_D9_PC09	Data line
28	ISI_D10	PC10	LCD_D10_ISI_D10_PC10	Data line
29	ISI_D11	PC11	LCD_D11_ISI_D11_PC11	Data line
30	GND	–	GND	Ground

3.4.7 Audio Class D (CLASSD) Amplifier

The Audio Class D (CLASSD) Amplifier is a digital input, Pulse Width Modulated (PWM) output stereo Class D amplifier. CLASSD features a high-quality interpolation filter embedding a digitally-controlled gain, an equalizer and a de-emphasis filter.

On its input side, CLASSD is compatible with most common audio data rates. On the output side, its PWM output can drive either:

- high-impedance single-ended or differential output loads (Audio DAC application), or
- external MOSFETs through an integrated non-overlapping circuit (Class D power amplifier application).

For more information, refer to the SAM9X60 datasheet (see 1.2 Recommended Reading).

The output stage of the CLASSD amplifier featured on the SAM9X60-EK can be powered either from the on-board 5V power rail or an outside power supply. The selection is made by changing the jumper (JP3) position on J11:

- 2-3 shorted = on-board 5V power supply
- 1-2 shorted = external power supply

Figure 3-37. Audio Class D Mono Amplifier

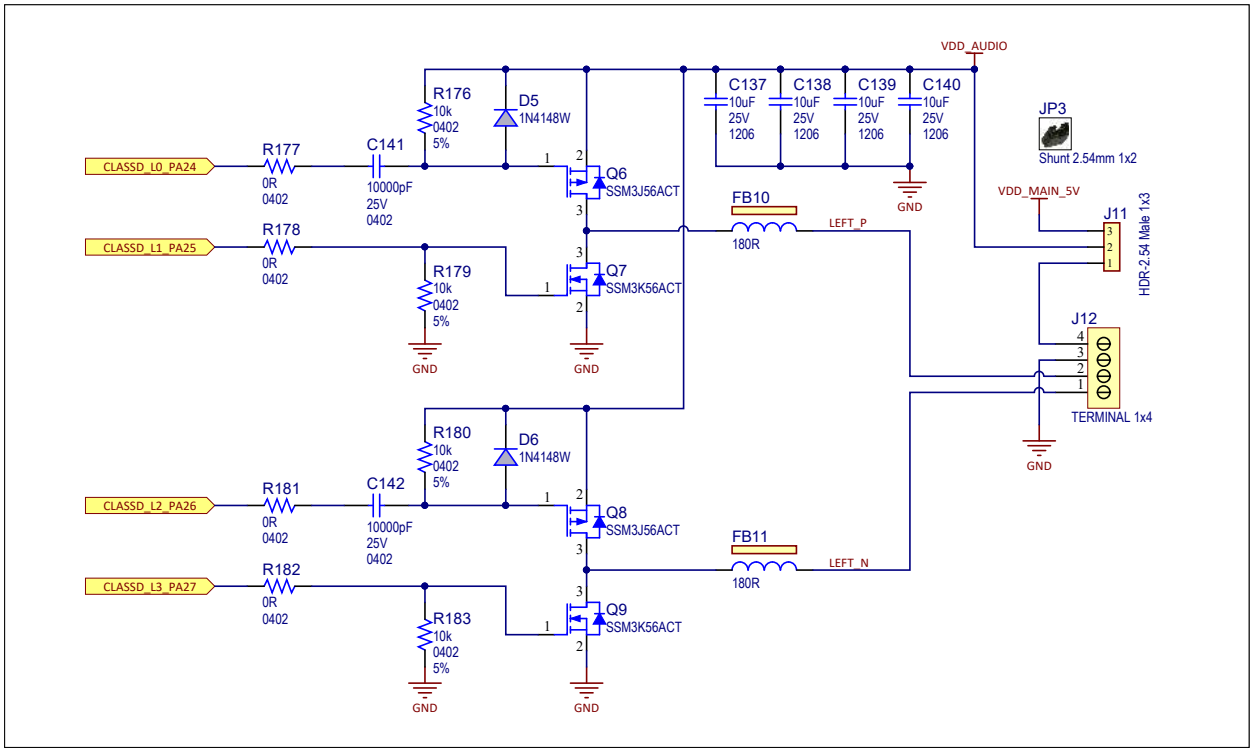


Table 3-19. Class D Output Connector J12 Signal Description

Pin No	Signal Name	Signal Description
1	LEFT_N	Negative level
2	LEFT_P	Positive level
3	GND	Ground
4	External power	Input external power

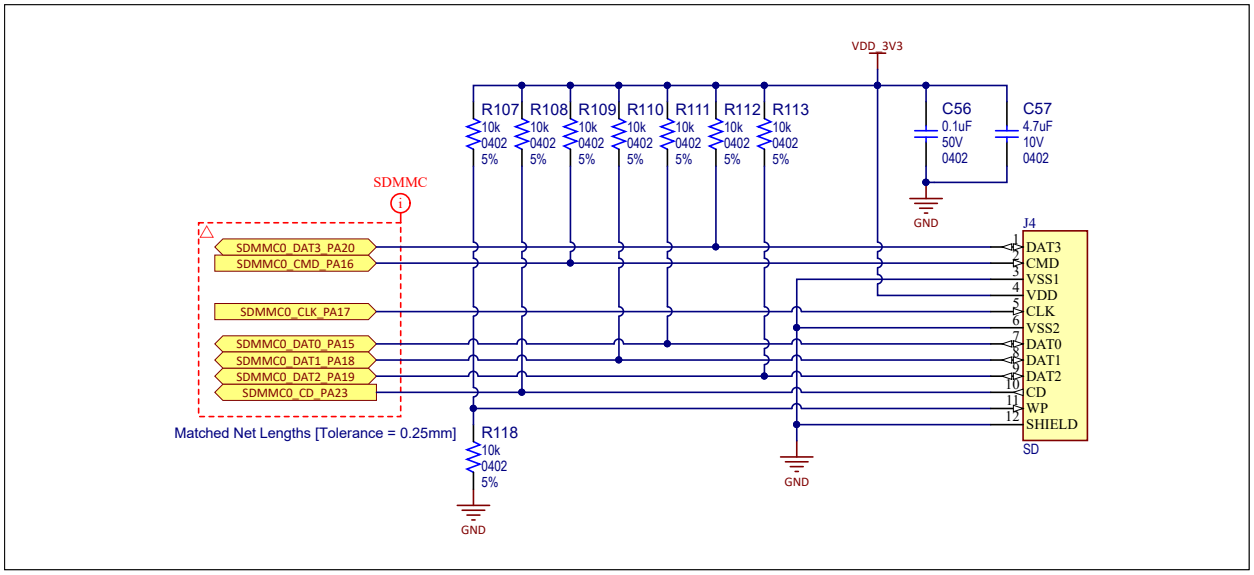
3.4.8 Secure Digital Multimedia Card (SDMMC)

The SD (Secure Digital) card is a non-volatile memory card format used as a mass storage memory in mobile devices.

The SAM9X60 has one Secure Digital Multimedia Card (SDMMC) interface that supports the MultiMedia Card (e.MMC) Specification V4.51, the SD Memory Card Specification V3.0, and the SDIO V3.0 specification. It is compliant with the SD Host Controller Standard V3.0 Specification.

A standard MMC/SD card connector, connected to the SDMMC interface, is mounted on the top side of the board. The SDMMC0 communication is based on an 8-pin interface (clock, command, four data and power lines). It includes a card detection switch.

Figure 3-38. SDMMC Connector



3.4.9 mikroBUS Interface

The SAM9X60-EK hosts a pair of 8-pin female headers (J14) implementing a mikroBUS socket. For details, refer to the mikroBUS documentation on https://www.mikroe.com/mikrobus.

Figure 3-39. mikroBUS Interface

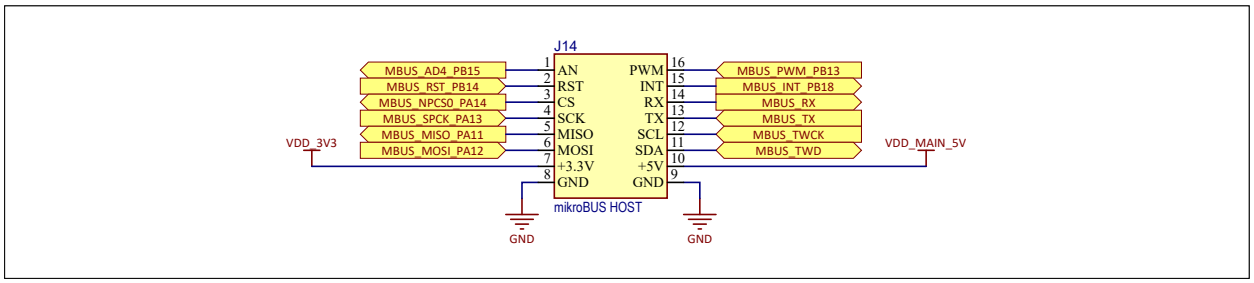


Table 3-20. mikroBUS Connector J14 Pin Assignment

Function	PIO	Mbus Signal	Pin #	Pin #	Mbus Signal	PIO	Function
Analog input	PB15	AN	1	16	PWM	PB13	PWM
Reset	PB14	RST	2	15	INT	PB18	Interrupt
SPI Chip Select	PA14	SPI_NPCS	3	14	UART_RX	PA21	UART receive (output from Mbus into SAM)
SPI clock	PA13	SPI_SPCK	4	13	UART_TX	PA22	UART transmit (input from SAM into Mbus)
SPI MISO	PA11	SPI_MISO	5	12	TWI_SCL	PA31	TWI clock
SPI MOSI	PA12	SPI_MOSI	6	11	TWI_SDA	PA30	TWI data
VCC	_	3V3 Supply	7	10	5V Supply	_	VDD
GROUND	_	GND	8	9	GND	_	Ground

Note: Enabling the ATWILC3000 interface prevents the UART functionality from being used with the mikroBUS connector. See 3.4.3 Wi-Fi/Bluetooth Module (Optional).

3.4.10 GPIO Interface

The SAM9X60-EK board features a 40-pin connector (Raspberry Pi® compatible) for free use.

Figure 3-40. GPIO Connector

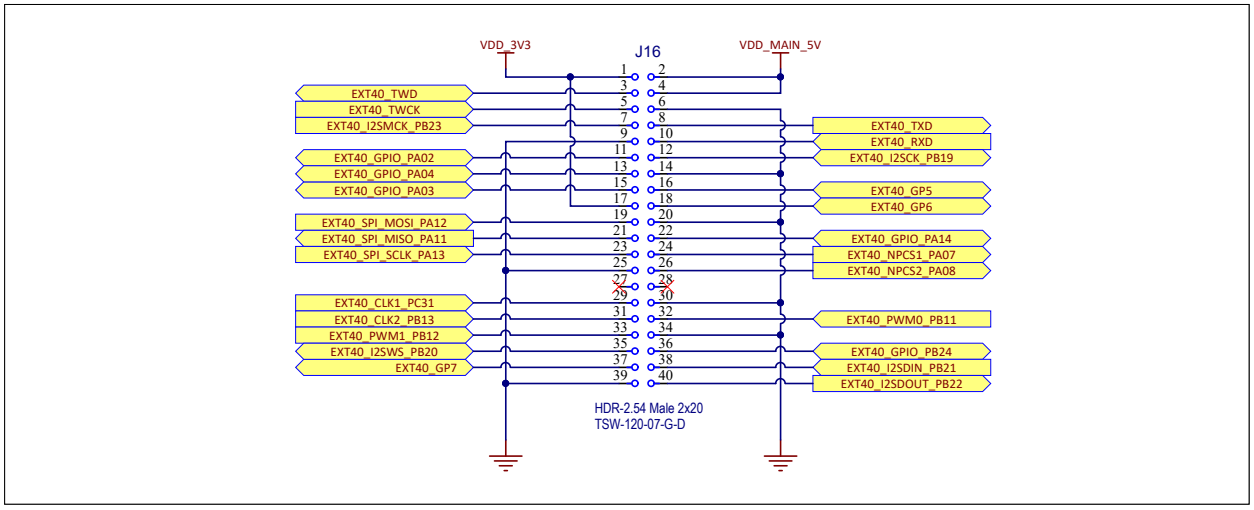


Table 3-21. GPIO Connector J16 Pin Assignment

Signal	Pin No	Pin No	Signal
+3V3	1	2	+5V
EXT40_TWD	3	4	+5V
EXT40_TWCK	5	6	Ground
EXT40_I2SMCK_PB23	7	8	EXT40_TXD
GND	9	10	EXT40_RXD
EXT40_GPIO_PA02	11	12	EXT40_I2SCK_PB19
EXT40_GPIO_PA03	13	14	Ground
EXT40_GPIO_PA04	15	16	EXT40_GP5
+3V3	17	18	EXT40_GP6
EXT40_SPI_MOSI_PA12	19	20	Ground
EXT40_SPI_MISO_PA11	21	22	EXT40_GPIO_PA14
EXT40_SPI_SCLK_PA13	23	24	EXT40_NPCS1_PA07
GND	25	26	EXT40_NPCS2_PA08
NC	27	28	NC
EXT40_CLK1_PC31	29	30	Ground
EXT40_CLK2_PB13	31	32	EXT40_PWM0_PB11
EXT40_PWM1_PB12	33	34	Ground
EXT40_I2SWS_PB20	35	36	EXT40_GPIO_PB24
EXT40_GP7	37	38	EXT40_I2SDIN_PB21
GND	39	40	EXT40_I2SDOUT_PB22

3.5 User Interaction and Debugging

The SAM9X60-EK includes two main debugging interfaces to provide debug-level access to the SAM9X60-EK:

- One UART through the USB/J-Link-OB CDC feature
- Two JTAG interfaces, one connected directly to the MPU using connector J23 and one through the J-Link-OB interface USB port J21

3.5.1 Serial Debug Com Port (FTDI)

The SAM9X60-EK board features a dedicated serial port for debugging, accessible through header J24. Various interfaces can be used as a USB/Serial DBGU port bridge, such as the FTDI TTL-232R USB-to-TTL serial cable.

Figure 3-41. Serial Debug Com Port

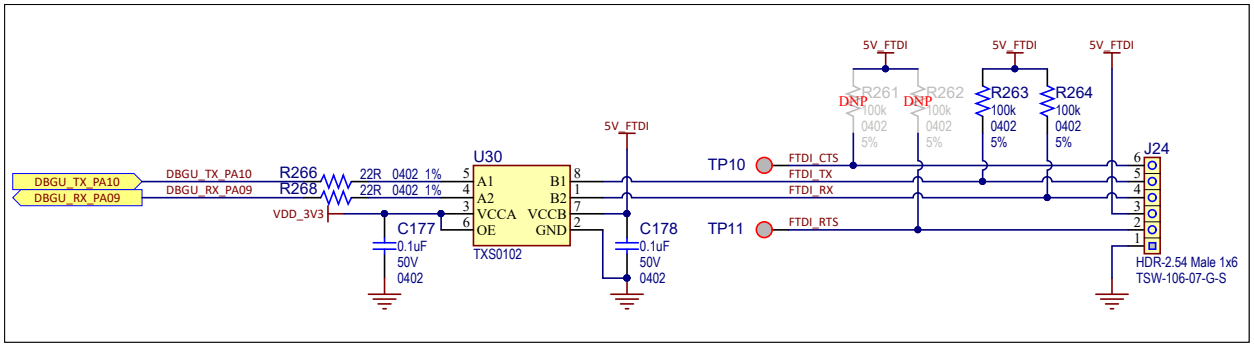


Table 3-22. Debug Com Port Signal Descriptions

PIO	Signal Name	Shared	Signal Description
PA09	DBGU_RX_PA09	DEBUG	Receive data
PA10	DBGU_TX_PA10	DEBUG	Transmit data

3.5.2 Debug JTAG

A 20-pin JTAG header (J23) is provided on the SAM9X60-EK board to facilitate software development and debugging using various JTAG emulators. The interface signals have a voltage level of 3.3V.

Figure 3-42. JTAG Connector

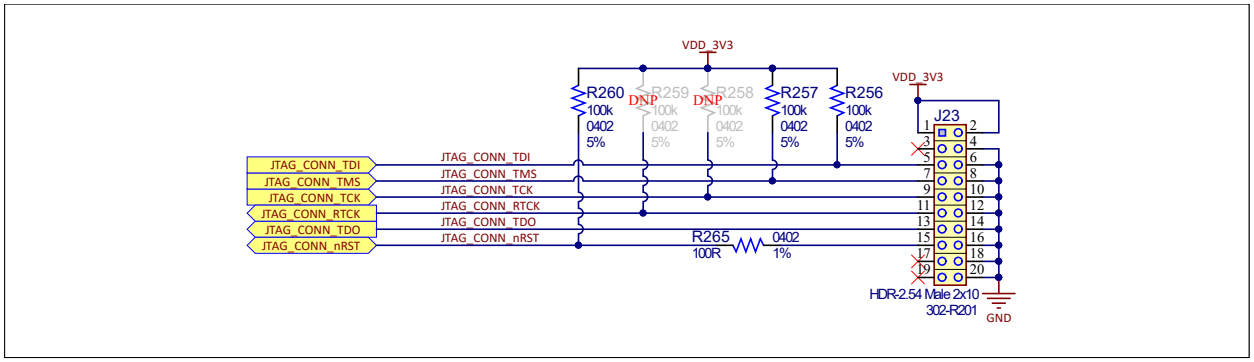


Table 3-23. JTAG/ICE Connector J23 Pin Assignment

Signal	Pin No	Pin No	Signal
+3.3V	2	1	+3V3
GND	4	3	NC
GND	5	5	TDI
GND	8	7	TMS
GND	10	9	TCK
GND	12	11	RTCK
GND	14	13	TDO
GND	16	15	nRST
GND	18	17	NC
GND	20	19	NC

3.5.3 Embedded Debugger (J-Link-OB) Interface

The SAM9X60-EK includes a built-in SEGGER J-Link-On-Board (J-Link-OB) device. The functionality is implemented with an ATSAM3U4C microcontroller in an LFBGA100 package. The ATSAM3U4C provides the functions of the JTAG interface and a bridge from USB to Serial debug port (known as CDC, or communication class device). The bi-colored LED (D9) shows the status of the J-Link-On-Board device.

The J-Link-OB device is designed to provide an efficient, low-cost, on-board alternative to the standard J-Link or SAM-ICE.

Its own dedicated USB port acts as a power source for this block (which is separated from the rest of the system) and provides the communication link to program and debug the MPU.

Figure 3-43. J-Link-OB with J-Link-CDC Interface

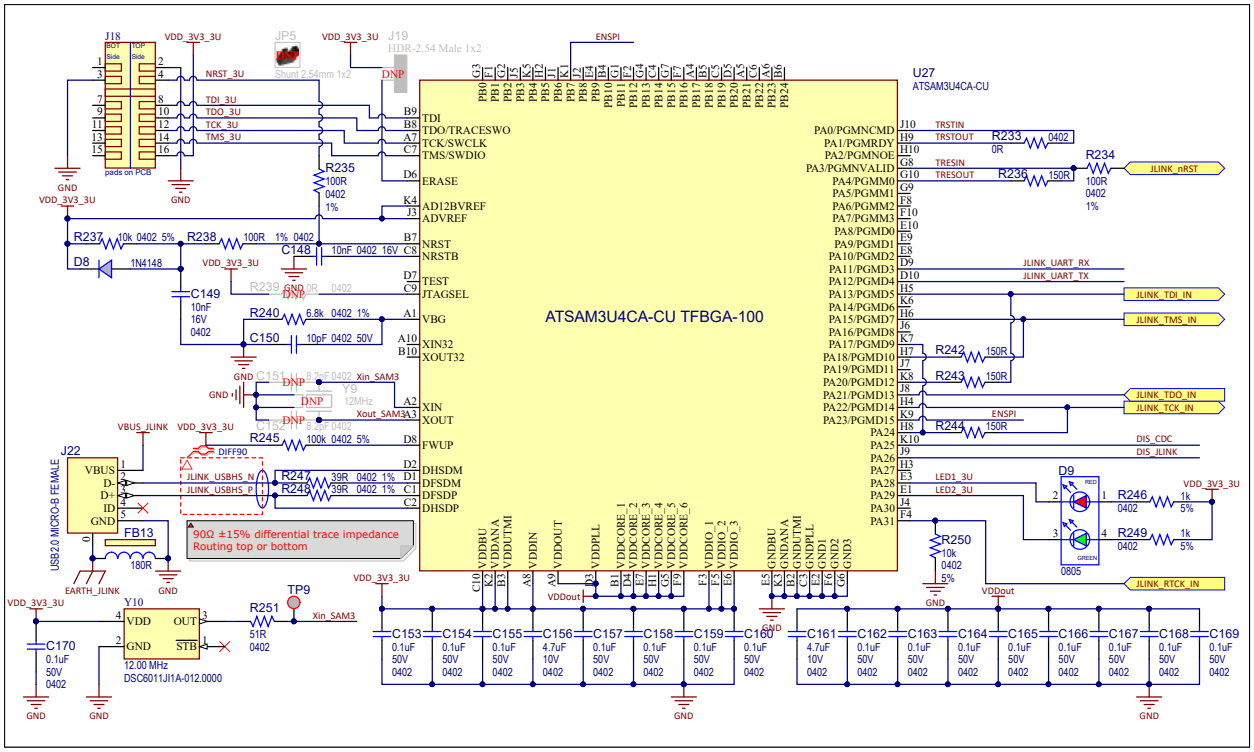


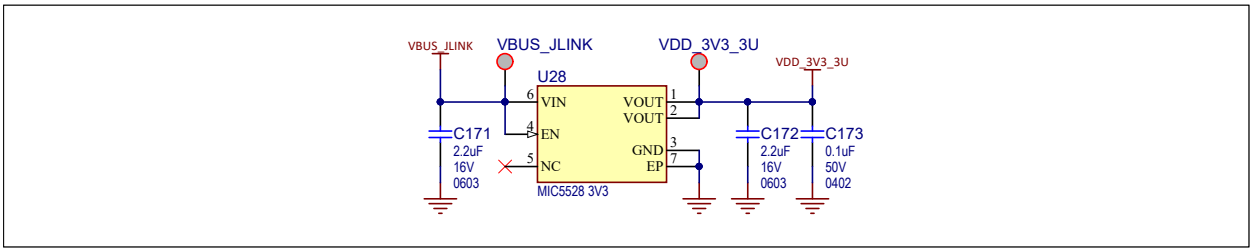
Table 3-24. J-Link-OB and J-Link-CDC LED D9 Status

LED D9	State	Description
Red and Green	Off	J-Link (SAM3U device) is not programmed, or J20 and J21 are installed.
Red	On	J-Link (SAM3U device) is programmed but J-Link is disabled (J20 installed).
Green	Flashing	J-Link is operational but the USB port is not connected.
Green	On	J-Link-OB is connected and ready.

The ATSAM3U microcontroller is powered only through the J-Link USB connector. This way, the programmer IC is separated from the rest of the system and the user can have a better reading of the power that the system is drawing when interrogating the power measurement devices placed on the board.

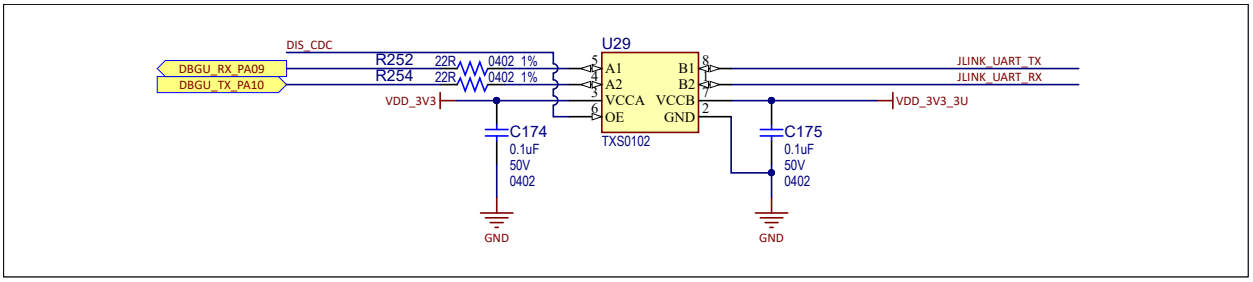
The MIC5528 has been selected to convert the 5V coming from the USB connector into the 3.3V rail needed by the microcontroller. The MIC5528 is a simple low-power, low dropout regulator designed for optimal performance in a very small footprint. It is capable of sourcing up to 500 mA of output current while only drawing 38 µA of operating current. For more information about the MIC5528, refer to the product web page.

Figure 3-44. J-Link-OB Power Supply



If the user does not require the on-board programming feature, this section can be left unpowered, with no impact on the rest of the system. A level shifter has been placed on the DEBUG UART line between the SAM9X60 MPU and the on-board programmer to properly separate the two voltage domains.

Figure 3-45. J-Link-OB Level Shifter



Jumper JP6/J20 disables the J-Link-OB JTAG functionality. When installed (J20 shorted), a quad analog switch (U31/U32) routes the JTAG interface of the SAM9X60 to the 20-pin header J23.

- Jumper JP6/J20 not installed: J-Link-OB-ATSAM3U4C is enabled and fully functional.
- Jumper JP6/J20 installed: J-Link-OB-ATSAM3U4C is disabled and an external JTAG controller can be used through the 20-pin JTAG port J23.

Figure 3-46. Disable J-Link CDC

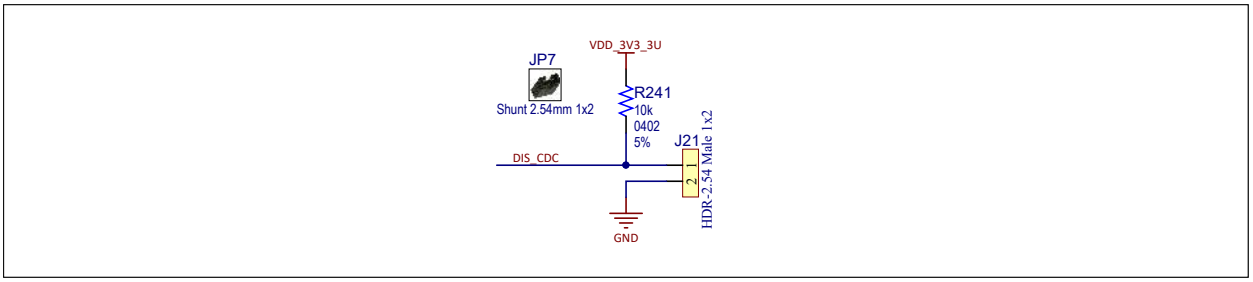
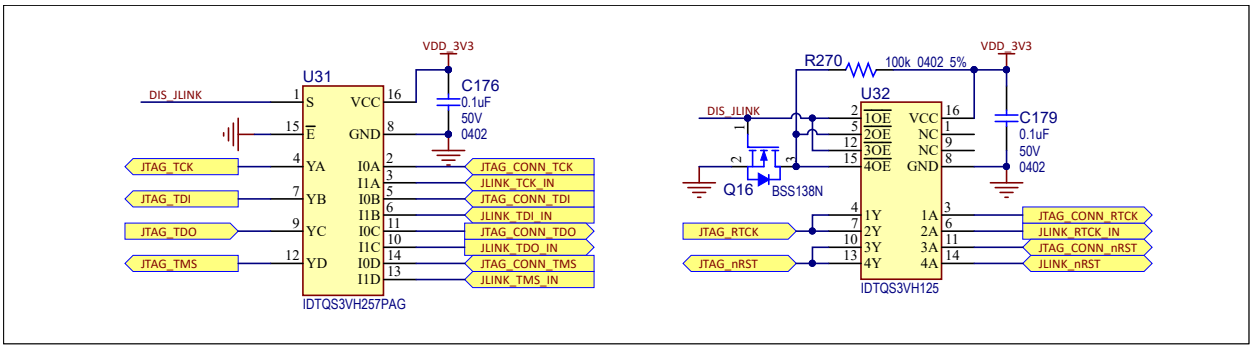


Figure 3-47. JTAG Switch



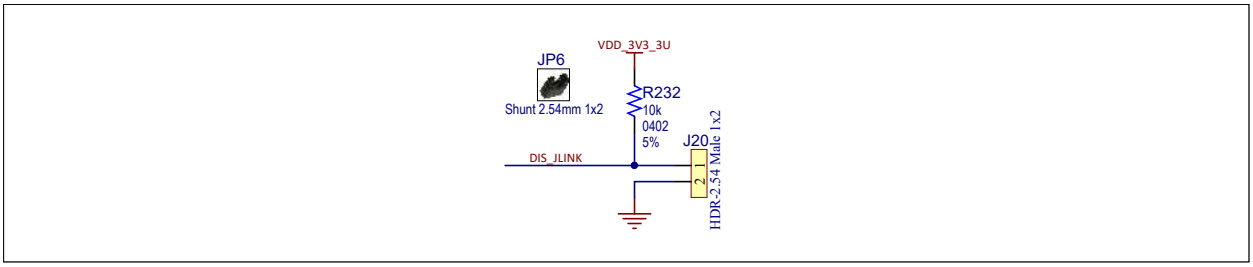
In addition to the J-Link-OB functionality, the ATSAM3U4C microcontroller provides a bridge to a debug serial port (DBGU) of the main board processor. The port is made accessible over the same USB connection used by JTAG by implementing a Communication Device Class (CDC), which allows a terminal communication with the target device.

This feature is enabled/disabled by jumper J21.

- Jumper J21 not installed: the J-Link-OB CDC function is enabled and fully functional.
- Jumper J21 installed: the J-Link-OB CDC function is disabled.

The USB CDC converts the USB device into a serial communication device. The target device running the CDC is recognized by the host as a serial interface (USB2COM, virtual COM port) without the need of installing a special host driver (the CDC is standard). All PC software using a COM port work without modifications with this virtual COM port. Under Microsoft® Windows®, the device shows up as a COM port; under Linux®, as a /dev/ACMx device. This enables the user to use host software which was not designed to be used with USB, such as a terminal program.

Figure 3-48. Disable J-Link JTAG



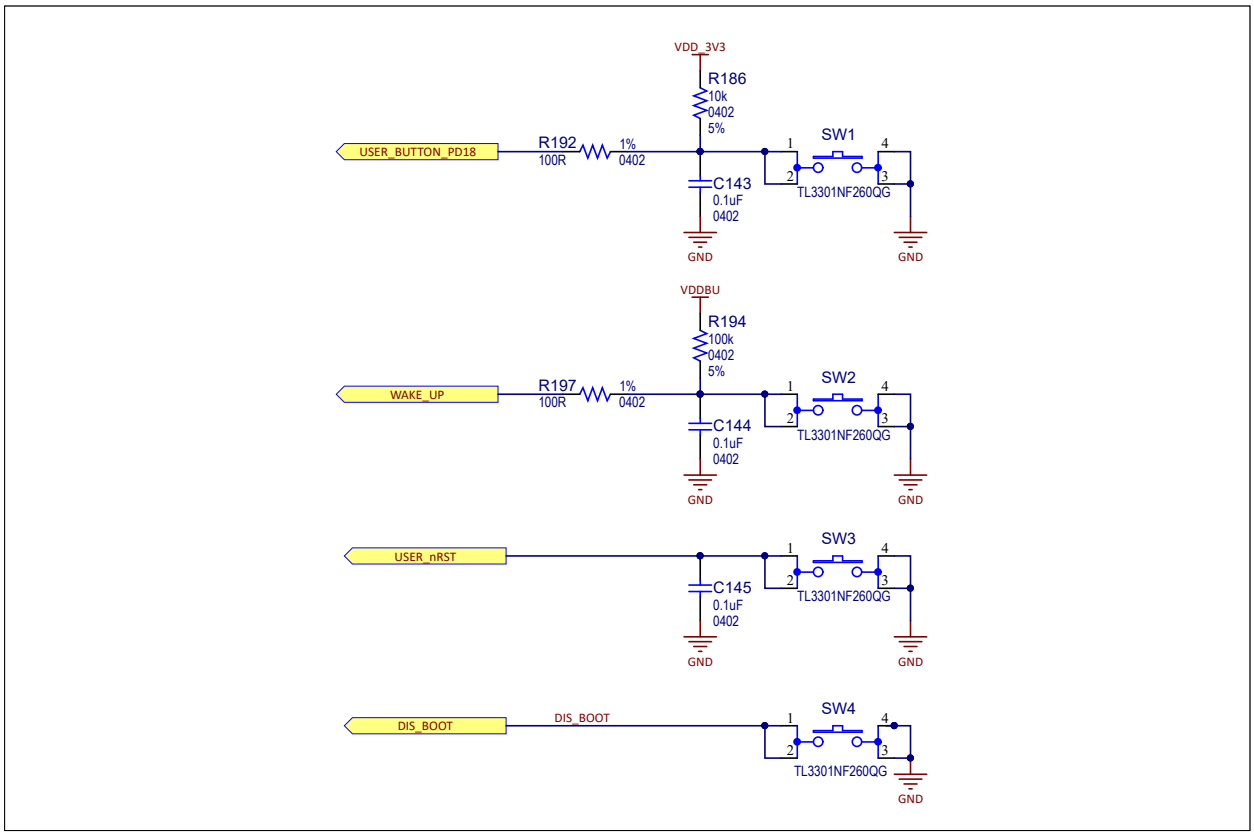
3.5.4 Push Button Switches

The SAM9X60-EK features four push buttons:

- One User push button (SW1) connected to PIO_PD18. This is left at user usage.
- One Wake-up push button (SW2) connected to the SAM9X60 WKUP pin; when pressed, the processor recovers from shutdown.
- One Board Reset push button (SW3); when pressed, the processor is reset.

- One Disable Boot push button (SW4); if kept pressed during power-up, the processor is prevented from booting off the on-board memories (QSPI and NAND Flash), thereby enabling booting from other sources or into ROM Code.

Figure 3-49. User Push Buttons



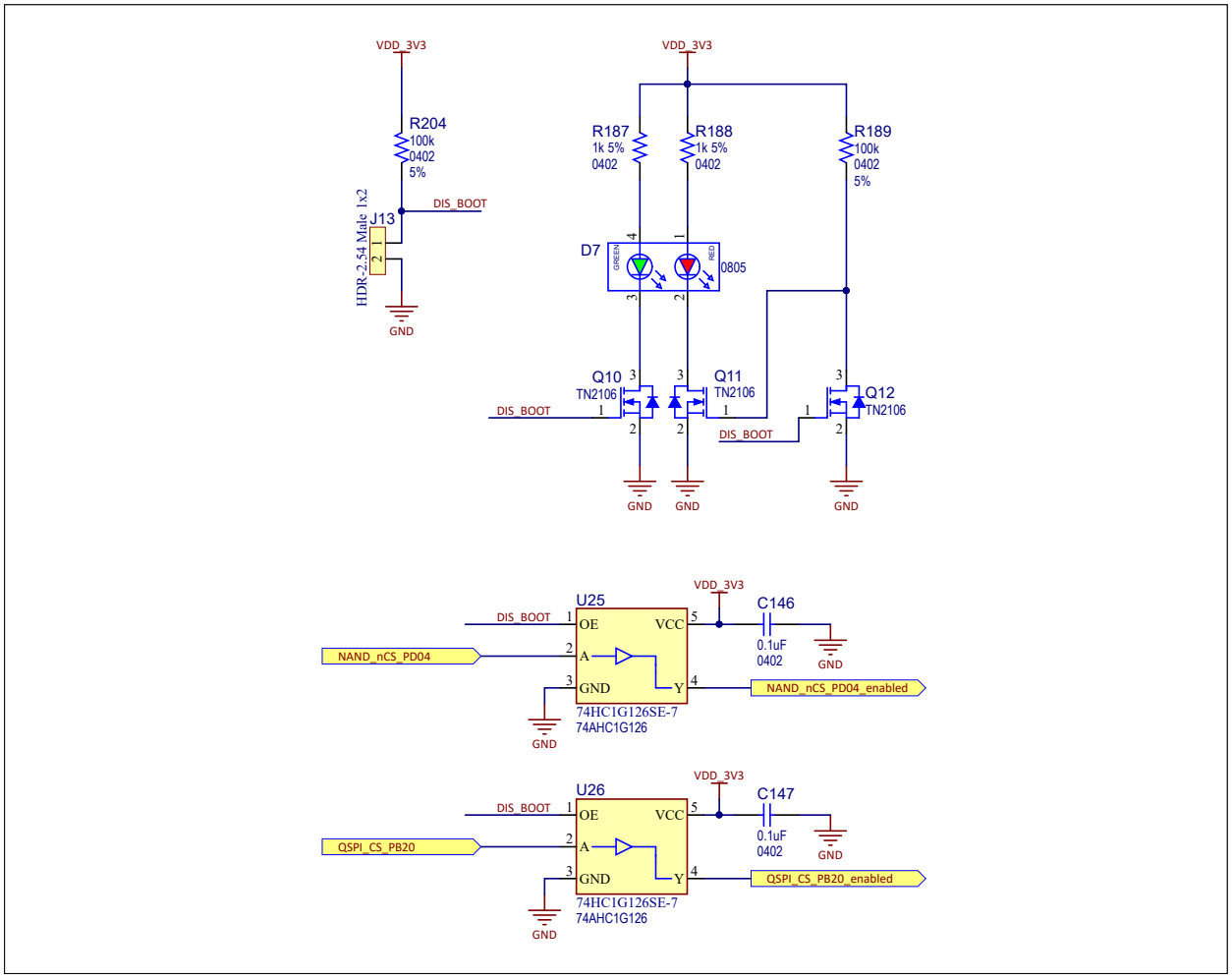
3.5.5 Disable Boot

On-board push button SW4 and/or jumper J13 control the selection (CS#) of the bootable memory components (QSPI and NAND FLASH) using a non-inverting 3-state buffer.

The rule of operation is:

- SW4 (DISABLE_BOOT) or J13 shorted = booting from QSPI and NAND FLASH is disabled.
- LED D6 indicates the state of the DIS_BOOT signal.
  - Red = on-board boot memories are disabled.
  - Green = on-board boot memories are enabled.

Figure 3-50. Disable Boot



Note: The “Disable Boot” mechanism does not disable booting from the SD card connector. The user must remove the SD card in order to disable booting from it.

3.5.6 RGB LED

The SAM9X60-EK board features one RGB LED. The three LED cathodes are controlled via GPIO PWM pins.

Figure 3-51. User LEDs

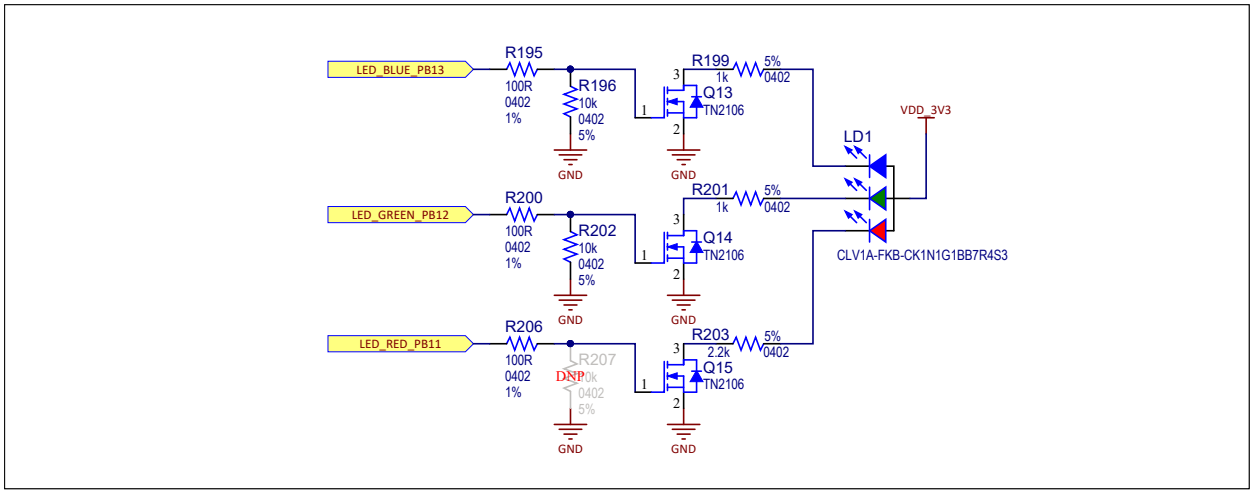


Table 3-25. RGB LED PIOs

Signal	PIO	Function
LED_RED_PB11	PB11	PWMH1
LED_GREEN_PB12	PB12	PWML1
LED_BLUE_PB13	PB13	PWML0

4. Installation and Operation

4.1 System and Configuration Requirements

The SAM9X60-EK requires the following:

- Personal Computer
- USB cable (provided in the kit box)

4.2 Board Setup

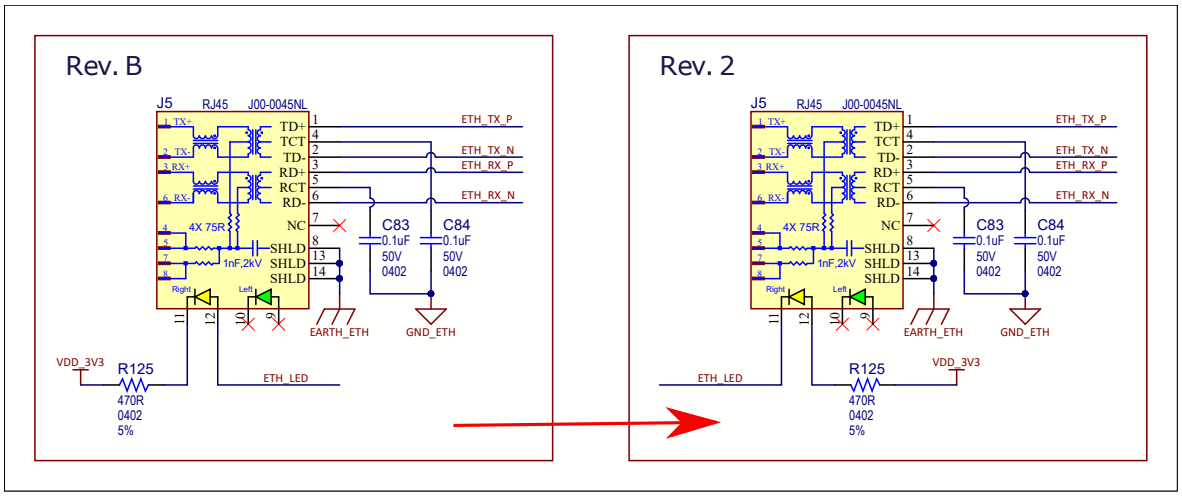
Follow these steps before using the SAM9X60-EK:

1. Unpack the board, taking care to avoid electrostatic discharge.
2. Check the default jumper settings (see 2.5 Default Jumper Settings).
3. Connect the Micro-USB cable to connector J7 (USB-A port).
4. Connect the other end of the cable to a free port on your PC.
5. Open a terminal (console 115200, N, 8, 1) on your PC.
6. Reset the board. A startup message appears on the console.

5. Erratum

1. On SAM9X60-EK Rev. B, the Ethernet activity LED on RJ45 connector J5 is inoperative due to an incorrect LED connection. This issue is solved in Rev. 2, as shown in the following picture. Nevertheless, the Ethernet port is perfectly operational on Rev. B boards.

Figure 5-1. RJ45 Connector Right LED Connection Change from Rev. B to Rev. 2



2. SAM9X60-EK Rev. B has the DSC1001DI5-025.0000 in the place of Y6 while SAM9X60-EK Rev. 2 features the new DSC6102HI2B-025.000.

6. Appendix. Schematics and Layouts

This appendix contains the following schematics and layouts for the SAM9X60-EK board:

- Block Diagram
- Power Supply
- SAM9X60 Processor
- Processor I/Os
- Processor I/O Expansions
- On-board Memories
- USB Interfaces
- Ethernet MAC
- Wi-Fi/Bluetooth
- SDMMC, CAN and CLASSD
- Expansion Connectors
- User Interaction
- On-board J-Link

Figure 6-1. Block Diagram

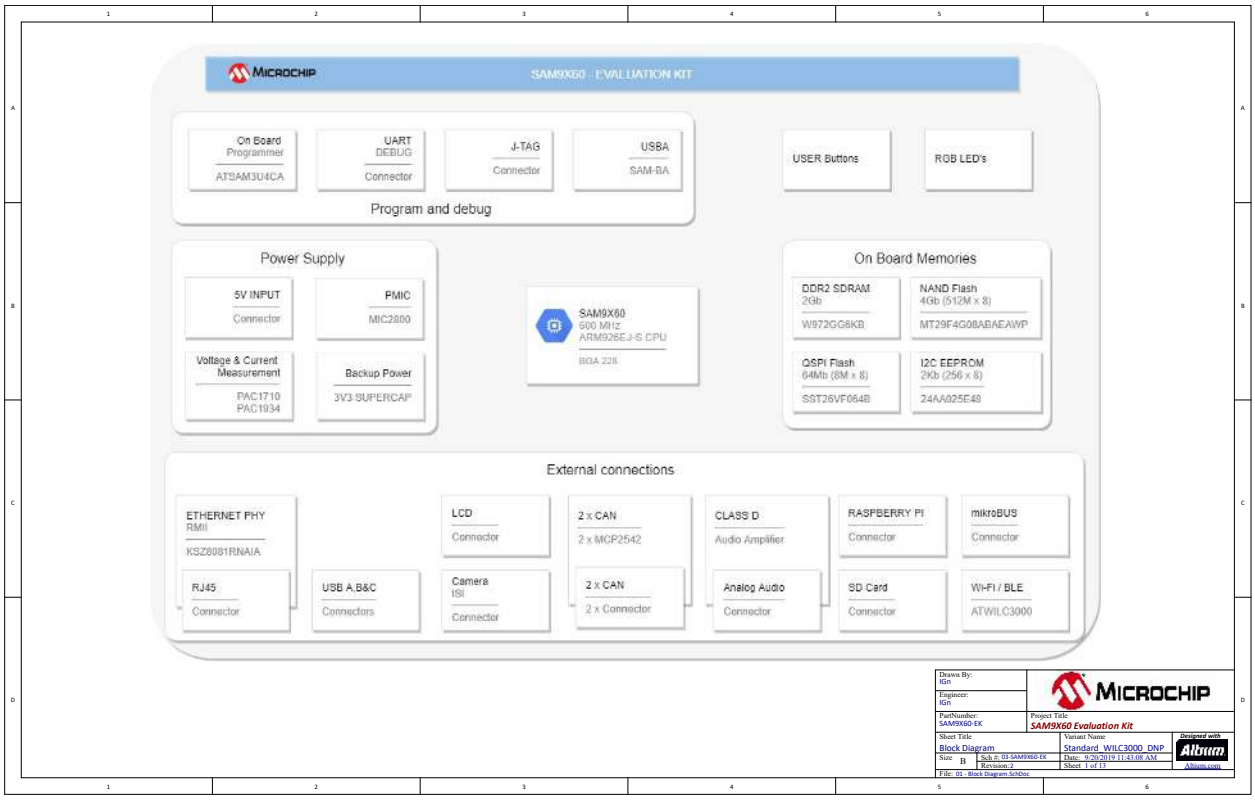


Figure 6-2. Power Supply

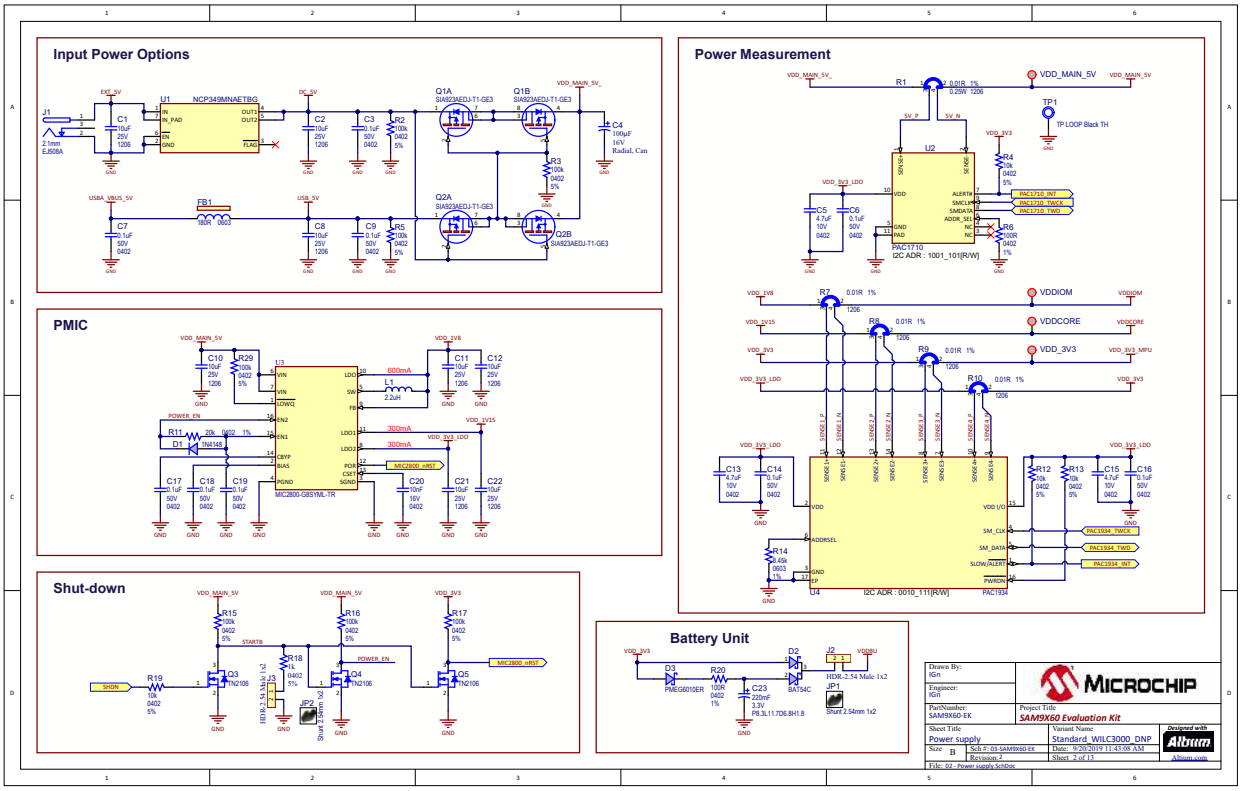


Figure 6-3. SAM9X60 Processor

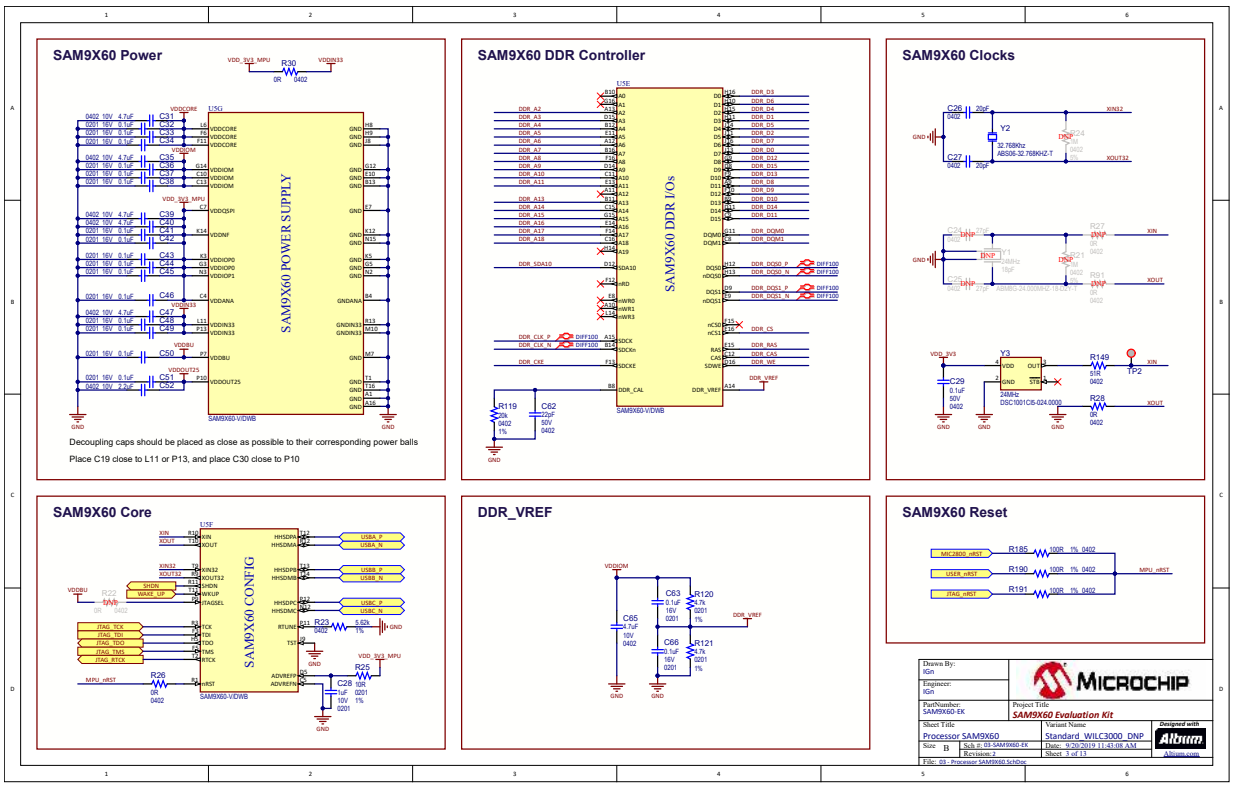


Figure 6-4. Processor I/Os

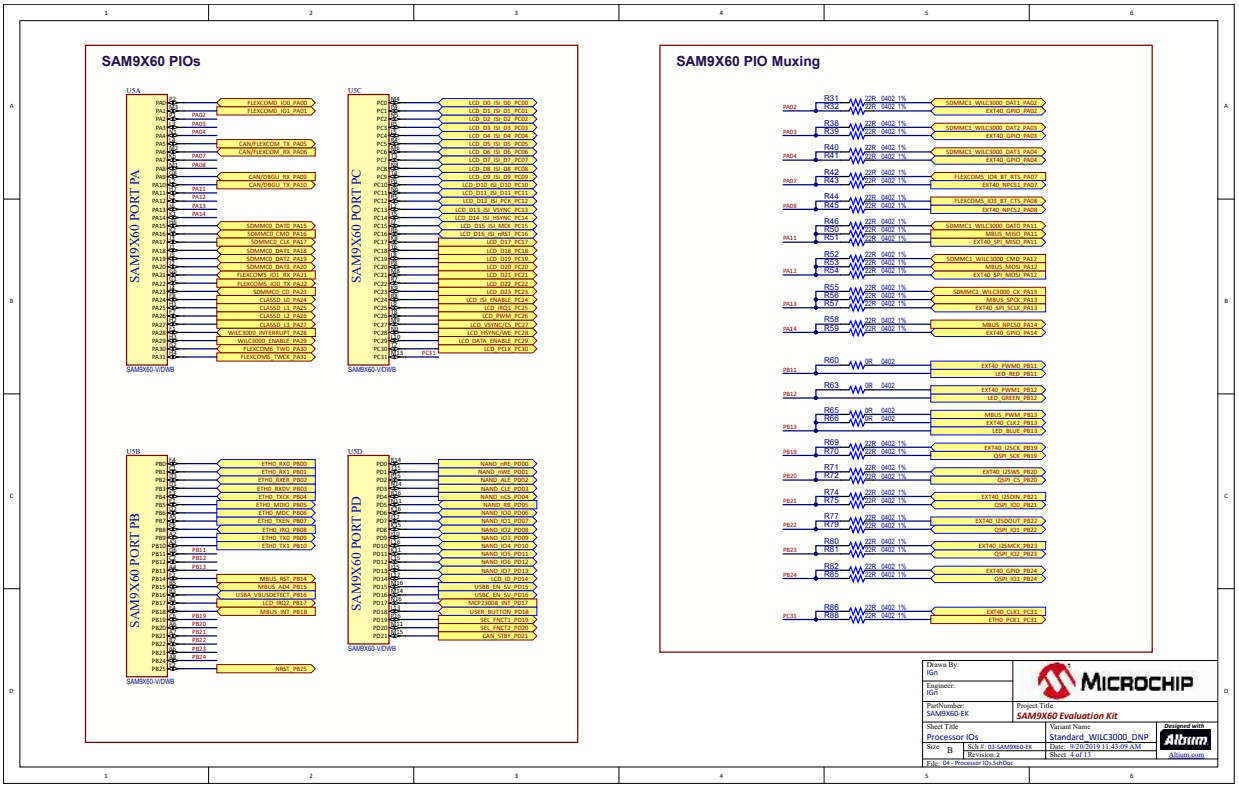


Figure 6-5. Processor I/O Expansions

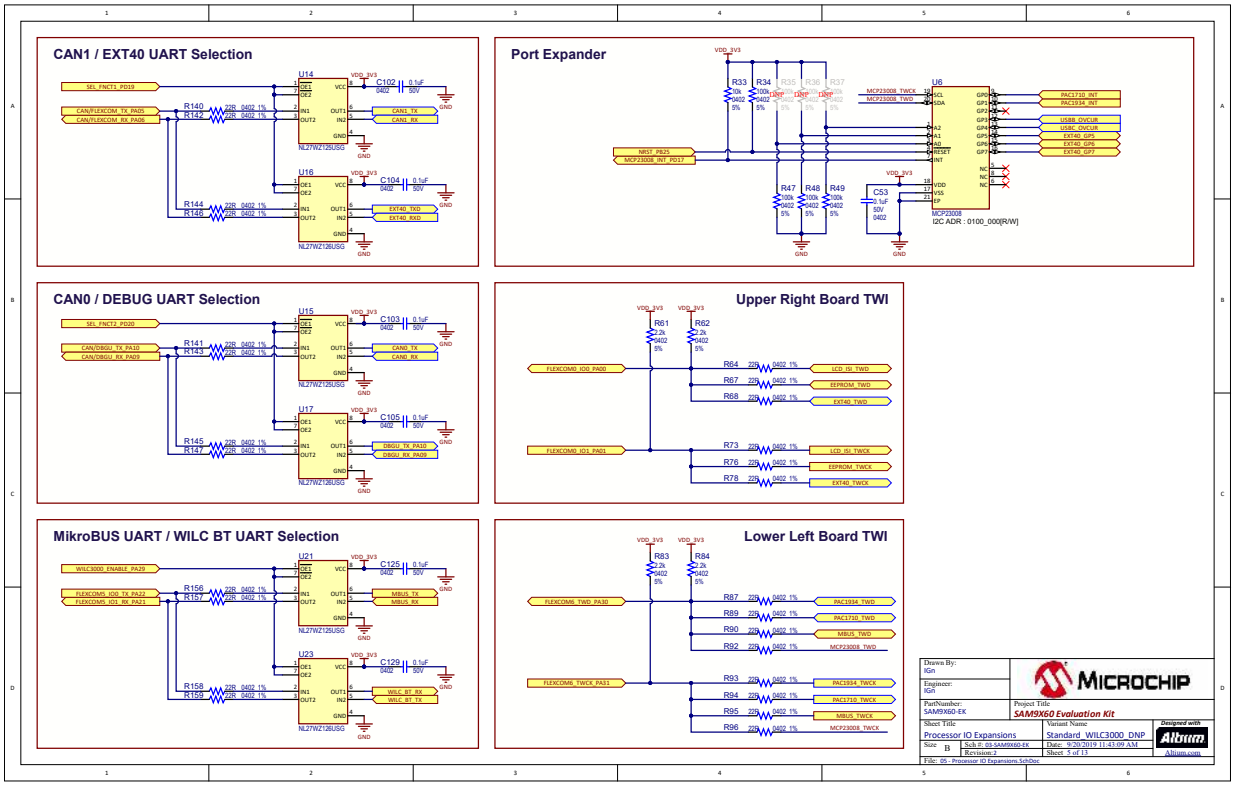


Figure 6-6. On-board Memories

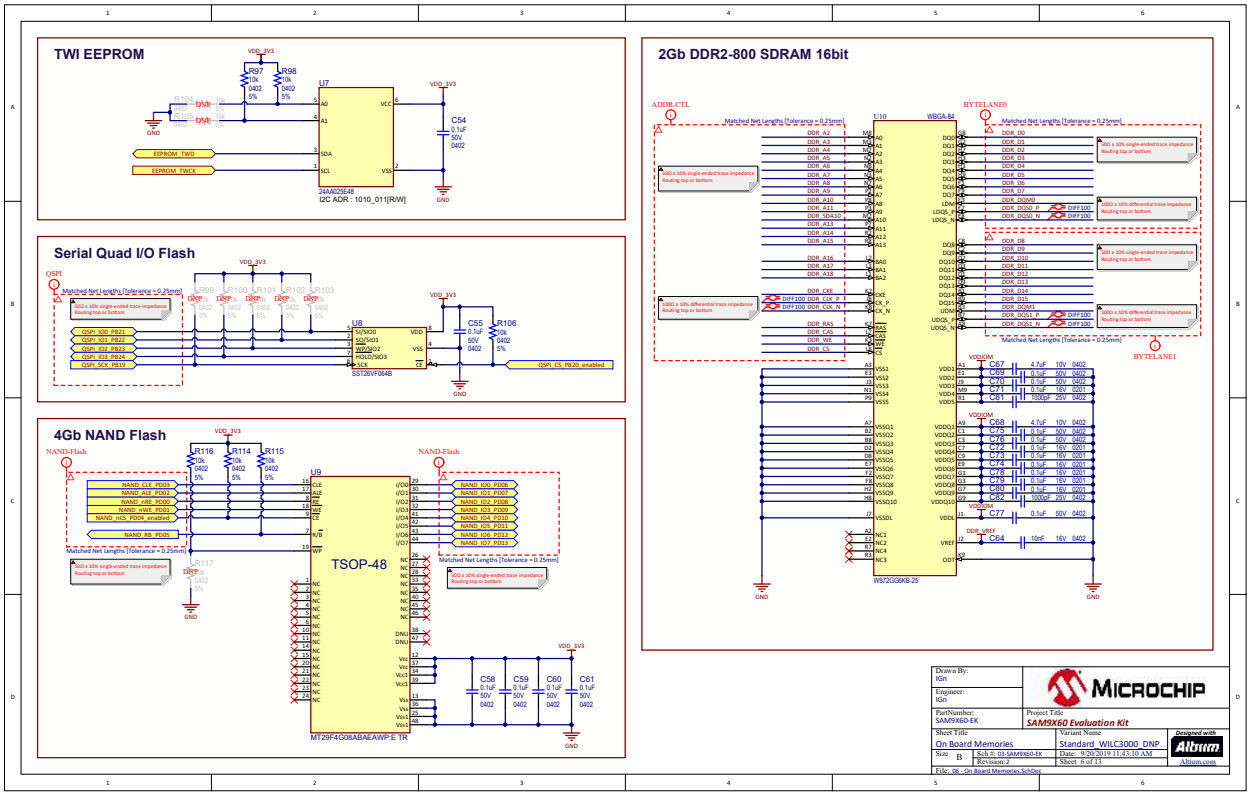


Figure 6-7. USB Interfaces

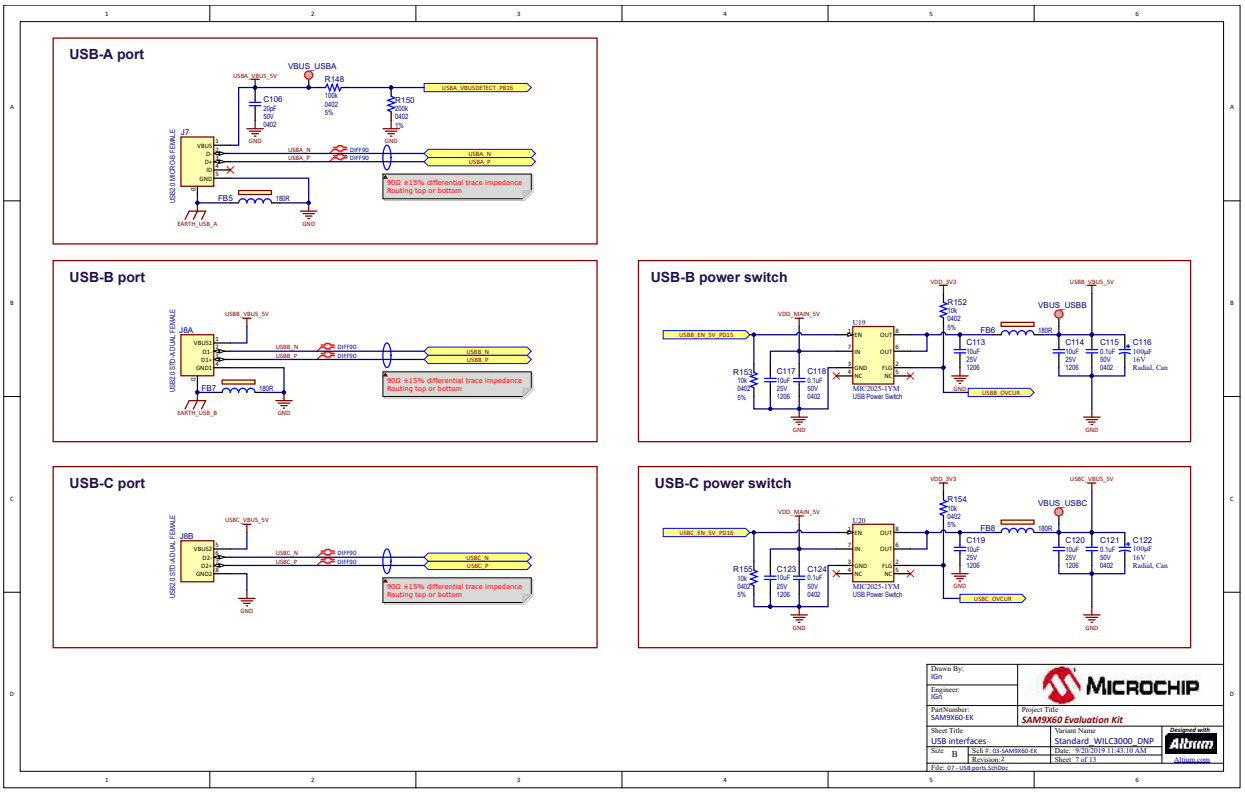


Figure 6-8. Ethernet MAC

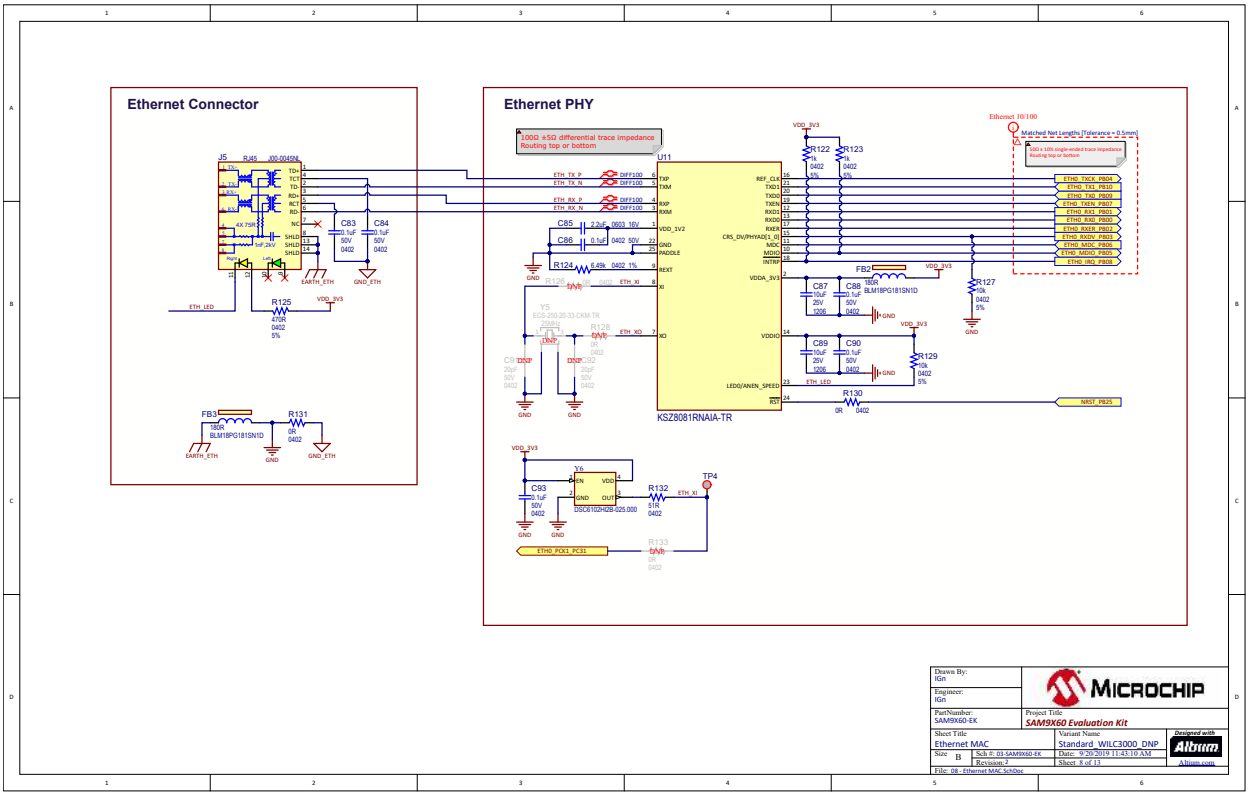


Figure 6-9. Wi-Fi/Bluetooth

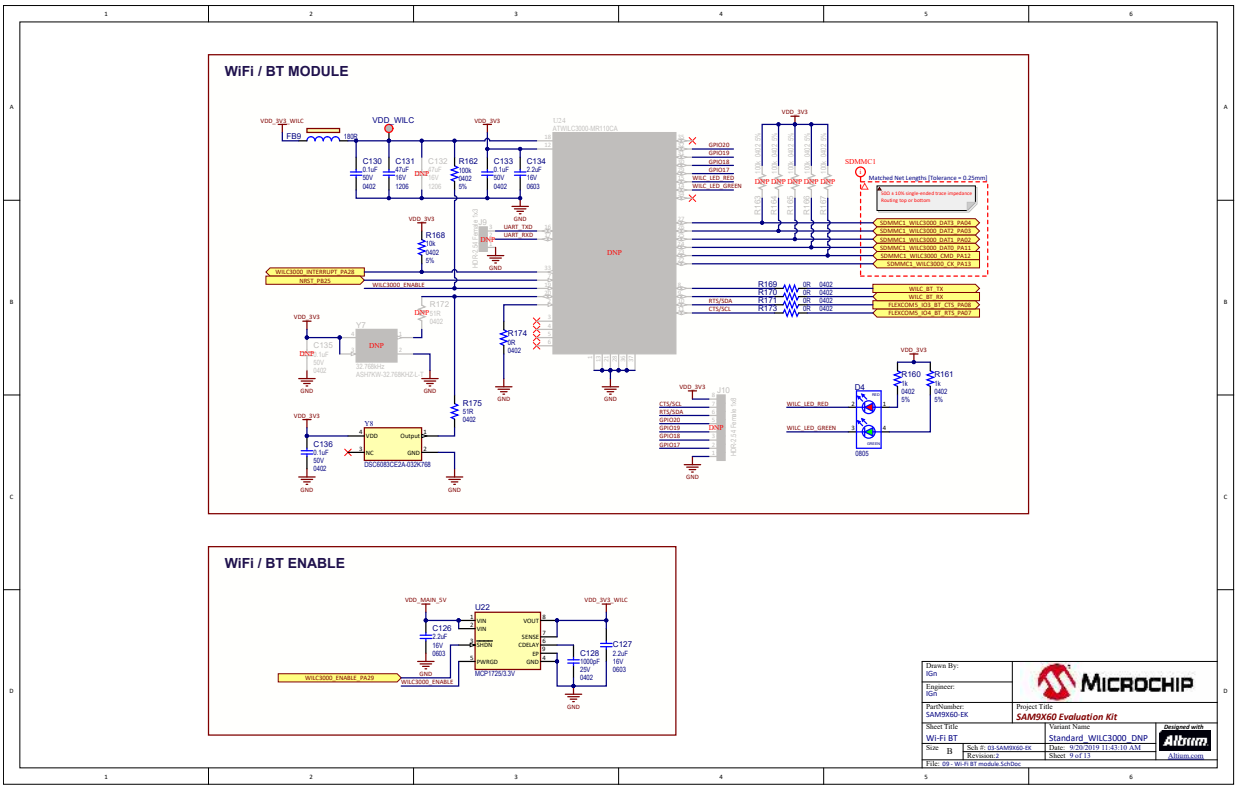


Figure 6-10. SDMMC, CAN and CLASSD

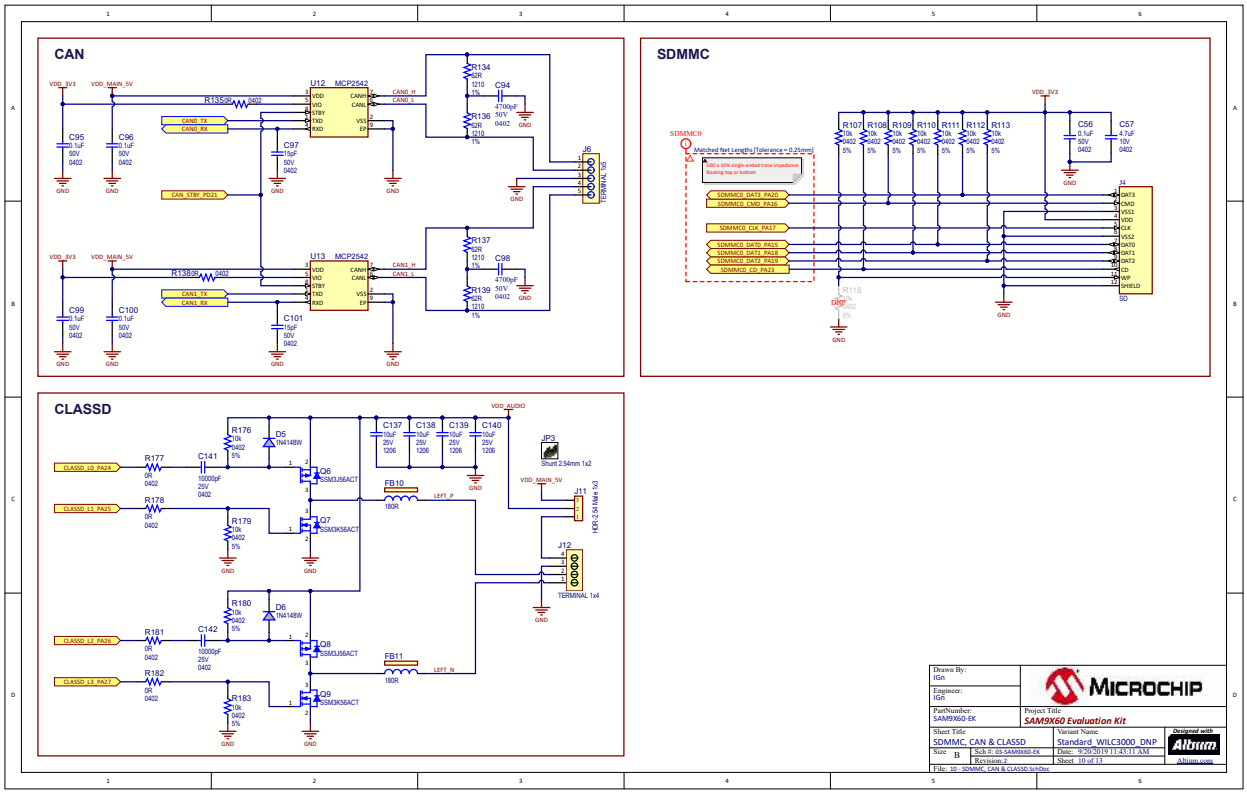


Figure 6-11. Expansion Connectors

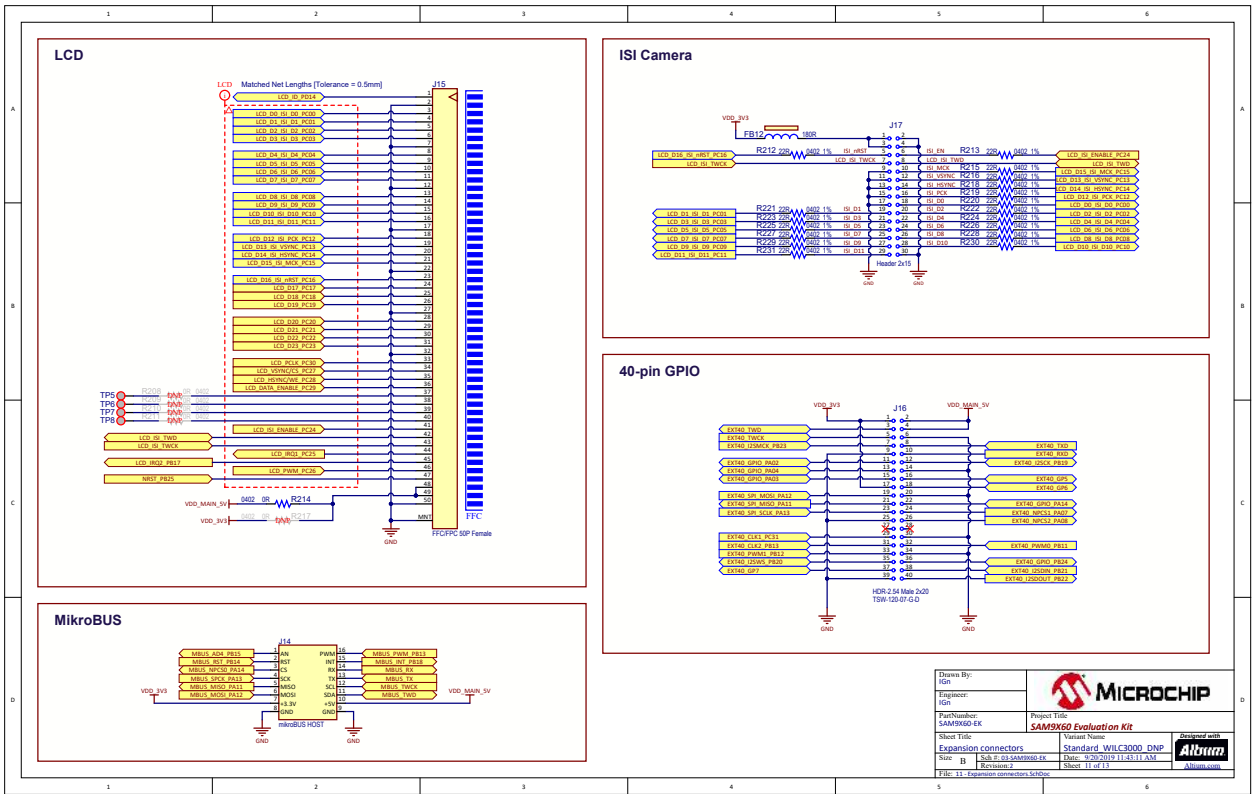


Figure 6-12. User Interaction

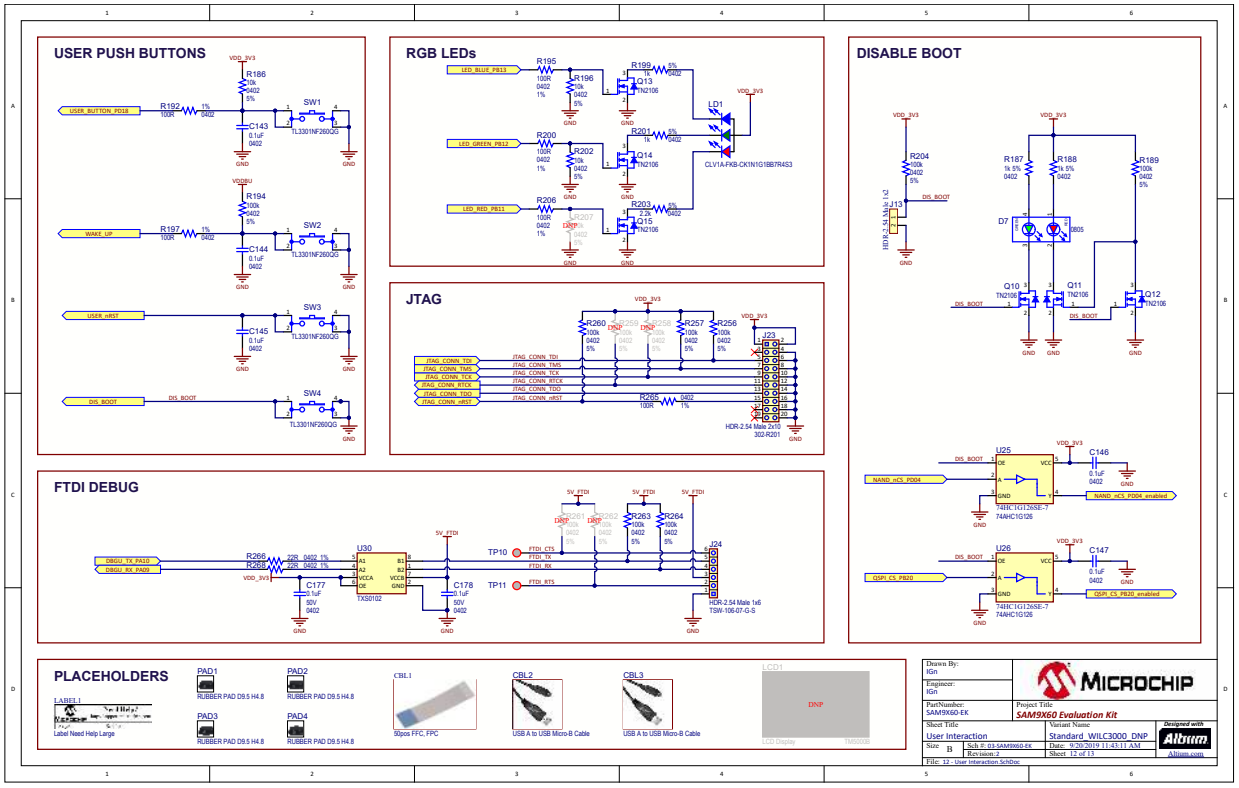
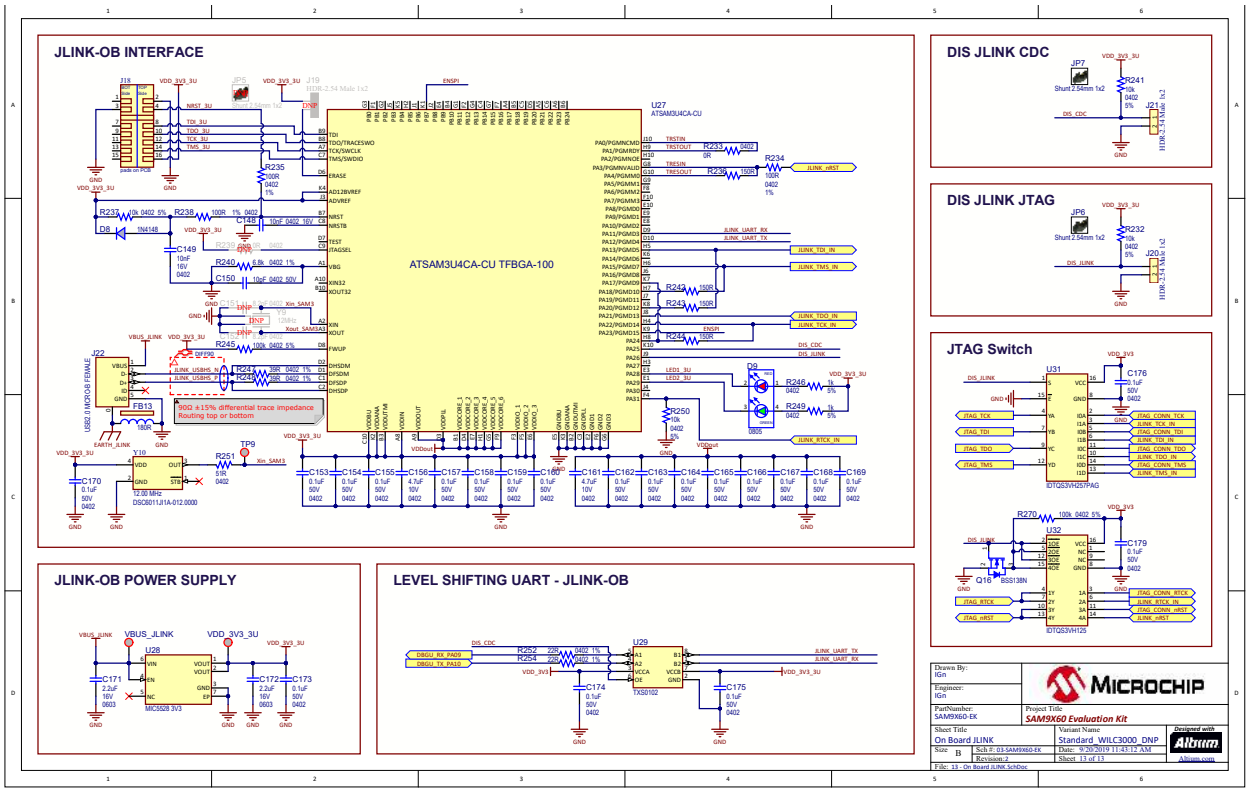


Figure 6-13. On-board J-Link



7. Revision History

7.1 DS50002907A - 10/2019

First issue.

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