SBAS452A – SEPTEMBER 2008 – REVISED JANUARY 2016

PCM3168A 24-Bit, 96-kHz/192-kHz, 6-In/8-Out Audio Codec With Differential Input/Output

1 Features

- 24-Bit ΔΣ ADC and DAC
- Six-ChanneL ADC:
  - High Performance: Differential and Single-Ended, f_S = 48 kHz
  - THD+N: –93 dB (Differential and Single-Ended)
  - SNR: 107 dB (Differential), 104 dB (Single-Ended)
  - Dynamic Range: 107 dB (Differential), 104 dB (Single-Ended)
  - Sampling Rate: 8 kHz to 96 kHz
  - System Clock: 256 f_S, 384 f_S, 512 f_S, 768 f_S
  - Differential Voltage Input: 2 V_{RMS}
  - Single-Ended Voltage Input: 1 V_{RMS}
  - Decimation Filter:
    - Passband Ripple: ±0.035 dB
    - Stop Band Attenuation: –75 dB
  - On-Chip, Highpass Filter: 0.96 Hz at f_S = 48 kHz
  - Overflow Flag
- Eight-Channel DAC:
  - High Performance: Differential, f_S = 48 kHz
  - THD+N: –94 dB
  - SNR: 112 dB
  - Dynamic Range: 112 dB
  - Sampling Rate: 8 kHz to 192 kHz
  - System Clock: 128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, 768 f_S
  - Differential Voltage Output: 8 V_{PP}
  - Analog Lowpass Filter Included
  - 4x/8x Oversampling Digital Filter:
    - Passband Ripple: ±0.0018 dB
    - Stop Band Attenuation: –75 dB
  - Zero Flag
- Flexible Mode Control:
  - Four-Wire SPI™, Two-Wire I²C™ Compatible Serial Control Interface or Hardware Control
- Multi Functions Through SPI or I2C I/F:
  - Audio I/F Mode and Format Select for ADC and DAC
  - Digital Attenuation and Soft Mute for ADC and DAC
  - Digital De-Emphasis: 32, 44.1, and 48 kHz for DAC
- Multi Functions Through H/W Control:
  - Audio I/F Mode/Format Select
  - Digital De-Emphasis Filter: 44.1 kHz for DAC
- External Reset Pin:
  - ADC/DAC Simultaneous
- Audio Interface Mode:
  - ADC/DAC Independent Master and Slave
- Audio Data Format:
  - ADC/DAC Independent I²S™, Left-Justified, Right-Justified, DSP, TDM
- Power Supplies: 5 V for Analog and 3.3 V for Digital
- Package: HTQFP-64
- Operating Temperature Range:
  - Consumer Grade: –40°C to 85°C
  - Automotive Audio Grade: –40°C to 105°C

2 Applications

- Car Audio External Amplifiers
- Car Audio AVN Applications
- Home Theaters
- AV Receivers

3 Description

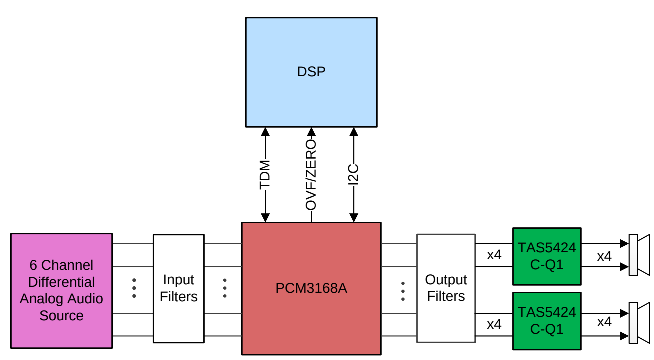
The PCM3168A device is a high-performance, single-chip, 24-bit, 6-in/8-out, audio coder and decoder (codecs) with single-ended and differential-selectable analog inputs and differential outputs.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCM3168A	HTQFP (64)	10.00 mm x 10.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2008) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

5 Description (continued)

The six-channel, 24-bit analog-to-digital converter (ADC) employs a delta-sigma (ΔΣ) modulator and supports 8-kHz to 96-kHz sampling rates and a 16-bit/24-bit width digital audio output word on the audio interface.

The eight-channel, 24-bit digital-to-analog converter (DAC) employs a ΔΣ modulator and supports 8-kHz to 192-kHz sampling rates and a 16-bit/24-bit width digital audio input word on the audio interface. Each audio interface supports I^2S, left-justified, right-justified, and DSP formats with 16-bit/24-bit word width. In addition, the PCM3168A device supports the time-division-multiplexed (TDM) format.

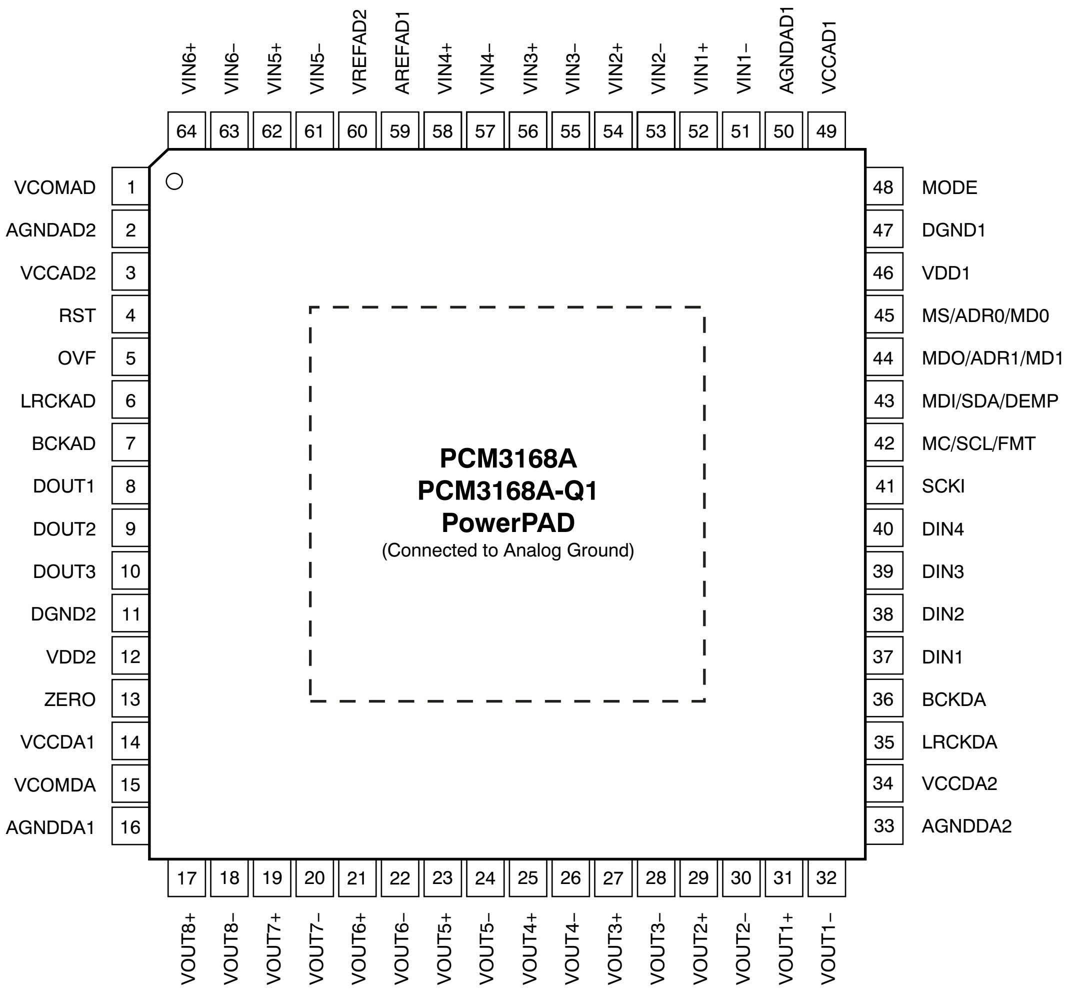
The PCM3168A device can be controlled through a four-wire, SPI-compatible interface, or two-wire, I^2C-compatible serial interface in software, which provides access to all functions including digital attenuation, soft mute, de-emphasis, and so forth. Also, hardware control mode provides a subset of user-programmable functions through four control pins. The PCM3168A device is available in a 12-mm × 12-mm (10-mm × 10-mm body) HTQFP-64 PowerPAD™ package.

6 Device Comparison Table

PART	ADCs	DACs	CONTROL	AUTOMOTIVE GRADE
PCM3168A	6	8	SPI, I^2C	No
PCM3168A-Q1	6	8	SPI, I^2C	Yes

7 Pin Configuration and Functions

PAP Package
64-Pin HTQFP With PowerPAD
Top View



Pin Functions

PIN		I/O	PULL-DOWN	5-V TOLERANT	DESCRIPTION
NO.	NAME				
1	VCOMAD	—	No	No	ADC analog common voltage decoupling
2	AGNDAD2	—	No	No	Analog ground 2 for ADC
3	VCCAD2	—	No	No	ADC analog power supply 2, 5 V
4	RST	I	Yes	Yes	Reset and power-down control input with active low
5	OVF	O	No	No	Overflow flag output for ADC
6	LRCKAD	I/O	Yes	No	Audio data word clock input/output for ADC
7	BCKAD	I/O	Yes	No	Audio data bit clock input/output for ADC
8	DOUT1	O	No	No	Audio data digital output for ADC1 and ADC2
9	DOUT2	O	No	No	Audio data digital output for ADC3 and ADC4
10	DOUT3	O	No	No	Audio data digital output for ADC5 and ADC6
11	DGND2	—	No	No	Digital ground 2
12	VDD2	—	No	No	Digital power supply 2, 3.3 V
13	ZERO	O	No	No	Zero detect flag output for DAC
14	VCCDA1	—	No	No	DAC analog power supply 1, 5 V
15	VCOMDA	—	No	No	DAC voltage common decoupling
16	AGNDDA1	—	No	No	Analog ground 1 for DAC
17	VOUT8+	O	No	No	Positive analog output from DAC8
18	VOUT8–	O	No	No	Negative analog output from DAC8
19	VOUT7+	O	No	No	Positive analog output from DAC7
20	VOUT7–	O	No	No	Negative analog output from DAC7
21	VOUT6+	O	No	No	Positive analog output from DAC6
22	VOUT6–	O	No	No	Negative analog output from DAC6
23	VOUT5+	O	No	No	Positive analog output from DAC5
24	VOUT5–	O	No	No	Negative analog output from DAC5
25	VOUT4+	O	No	No	Positive analog output from DAC4
26	VOUT4–	O	No	No	Negative analog output from DAC4
27	VOUT3+	O	No	No	Positive analog output from DAC3
28	VOUT3–	O	No	No	Negative analog output from DAC3
29	VOUT2+	O	No	No	Positive analog output from DAC2
30	VOUT2–	O	No	No	Negative analog output from DAC2
31	VOUT1+	O	No	No	Positive analog output from DAC1
32	VOUT1–	O	No	No	Negative analog output from DAC1
33	AGNDDA2	—	No	No	Analog ground 2 for DAC
34	VCCDA2	—	No	No	DAC analog power supply 2, 5 V
35	LRCKDA	I/O	Yes	No	Audio data word clock input/output for DAC
36	BCKDA	I/O	Yes	No	Audio data bit clock input/output for DAC
37	DIN1	I	No	No	Audio data input for DAC1 and DAC2
38	DIN2	I	No	No	Audio data input for DAC3 and DAC4
39	DIN3	I	No	No	Audio data input for DAC5 and DAC6
40	DIN4	I	No	No	Audio data Input for DAC7 and DAC8
41	SCKI	I	No	Yes	System clock input
42	MC/SCL/FMT	I	No	Yes	Clock for SPI, clock for I^2C, format select for hardware control mode
43	MDI/SDA/DEMP	I/O	No	Yes	Input data for SPI, data for I^2C (1), de-emphasis control for hardware control mode

(1) Open-drain configuration in I^2C.

Pin Functions (continued)

PIN		I/O	PULL-DOWN	5-V TOLERANT	DESCRIPTION
NO.	NAME				
44	MDO/ADR1/MD1	I/O	No	No	Output data for SPI(2), address select 1 for I²C, mode select 1 for hardware control mode
45	MS/ADR0/MD0	I	Yes	Yes	Chip select for SPI, address select 0 for I²C, mode select 0 for hardware control mode
46	VDD1	—	No	No	Digital power supply 1, 3.3 V
47	DGND1	—	No	No	Digital ground 1
48	MODE	I	No	No	Control port mode selection. Tied to V_{DD}: SPI, pull-up: H/W single-ended input, pull-down: H/W and differential input, tied to DGND: I²C
49	VCCAD1	—	No	No	ADC analog power supply 1, 5 V
50	AGNDAD1	—	No	No	Analog ground 1 for ADC
51	VIN1–	I	No	No	Negative analog input to ADC1
52	VIN1+	I	No	No	Positive analog input to ADC1
53	VIN2–	I	No	No	Negative analog input to ADC2
54	VIN2+	I	No	No	Positive analog input to ADC2
55	VIN3–	I	No	No	Negative analog input to ADC3
56	VIN3+	I	No	No	Positive analog input to ADC3
57	VIN4–	I	No	No	Negative analog input to ADC4
58	VIN4+	I	No	No	Positive analog input to ADC4
59	VREFAD1	—	No	No	ADC analog reference voltage 1 decoupling
60	VREFAD2	—	No	No	ADC analog reference voltage 2 decoupling
61	VIN5–	I	No	No	Negative analog input to ADC5
62	VIN5+	I	No	No	Positive analog input to ADC5
63	VIN6–	I	No	No	Negative analog input to ADC6
64	VIN6+	I	No	No	Positive analog input to ADC6

(2) 3-state (Hi-Z) operation in SPI.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted).[1]

		MIN	MAX	UNIT
Supply voltage	VCCAD1	–0.3	6.5	V
	VCCAD2	–0.3	6.5	
	VCCDA1	–0.3	6.5	
	VCCDA2	–0.3	6.5	
	VDD1	–0.3	4	
	VDD2	–0.3	4	
Ground voltage differences	AGNDAD1	–0.1	0.1	V
	AGNDAD2	–0.1	0.1	
	AGNDDA1	–0.1	0.1	
	AGNDDA2	–0.1	0.1	
	DGND1	–0.1	0.1	
	DGND2	–0.1	0.1	
Supply voltage differences	VCCAD1	–0.1	0.1	V
	VCCAD2	–0.1	0.1	
	VCCDA1	–0.1	0.1	
	VCCDA2	–0.1	0.1	
	VDD1	–0.1	0.1	
	VDD2	–0.1	0.1	
Digital input voltage	RST	–0.3	6.5	V
	MS	–0.3	6.5	
	MC	–0.3	6.5	
	MDI	–0.3	6.5	
	SCK	–0.3	6.5	
	BCKAD/DA	–0.3	$(V_{DD} + 0.3) < +4.0$	
	LRCKAD/DA	–0.3	$(V_{DD} + 0.3) < +4.0$	
	DIN1/2/3/4	–0.3	$(V_{DD} + 0.3) < +4.0$	
	DOUT1/2/3	–0.3	$(V_{DD} + 0.3) < +4.0$	
	MODE	–0.3	$(V_{DD} + 0.3) < +4.0$	
	OVF	–0.3	$(V_{DD} + 0.3) < +4.0$	
	ZERO	–0.3	$(V_{DD} + 0.3) < +4.0$	
	MDO	–0.3	$(V_{DD} + 0.3) < +4.0$	
Analog input voltage	VIN1-6±	–0.3	$(V_{CC} + 0.3) < +6.5$	V
	VCOMAD/DA	–0.3	$(V_{CC} + 0.3) < +6.5$	
	VOUT1-8±	–0.3	$(V_{CC} + 0.3) < +6.5$	
	VREFAD1/2	–0.3	$(V_{CC} + 0.3) < +6.5$	
Input current (all pins except supplies)		–10	10	mA
Ambient temperature range (under bias)		–40	125	°C
Junction temperature			150	°C
Lead temperature (soldering, 5s)			260	°C
Package temperature (IR reflow, peak)			260	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [2]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

			MIN	NOM	MAX	UNIT
V_{CC}	Analog supply voltage		4.5	5.0	5.5	V
V_{DD}	Digital supply voltage		3.0	3.3	3.6	V
Digital Interface				LVTTL compatible		
Digital input clock frequency		Sampling frequency, LRCKAD/LRCKDA [1]	8		96/192 [1]	kHz
		System clock frequency, SCKI	2.048		36.864	MHz
V_I	Analog input level	Single-ended		1		V_{RMS}
		Differential		2		V_{RMS}
V_O	Analog output voltage	Differential		8		V_{PP}
V_{OLR}	Analog output load resistance	To AC-coupled GND	5			kΩ
		To DC-coupled GND	15			kΩ
V_{OLC}	Analog output load capacitance				50	pF
D_{OLC}	Digital output load capacitance				20	pF
T_A	Operating free-air temperature	PCM3168A Consumer grade	–40	25	85	°C

(1) 192 kHz is supported only for DAC.

8.4 Thermal Information

THERMAL METRIC [1]		PCM3168A PAP (HTQFP) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

At T_A = 25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DATA FORMAT						
	Audio data interface format			I^2S, LJ, RJ, DSP, TDM		
	Audio data word length			16, 24		Bits
	Audio data format			MSB first, twos complement		
f_S	Sampling frequency, ADC		8	48	96	kHz
f_S	Sampling frequency, DAC		8	48	192	kHz
	System clock frequency	128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, 768 f_S	2.048		36.864	MHz
INPUT LOGIC						
V_{IH} (1) (2)	Input logic level		2		V_{DD}	VDC
V_{IL} (1) (2)	Input logic level				0.8	VDC
V_{IH} (3) (4)	Input logic level		2		5.5	VDC
V_{IL} (3) (4)	Input logic level				0.8	VDC
I_{IH} (2) (3)	Input logic level	V_{IN} = V_{DD}			±10	µA
I_{IL} (2) (3)	Input logic level	V_{IN} = 0 V			±10	µA
I_{IH} (1) (4)	Input logic level	V_{IN} = V_{DD}		65	100	µA
I_{IL} (1) (4)	Input logic level	V_{IN} = 0 V			±10	µA
OUTPUT LOGIC						
V_{OH} (5)	Output logic level	I_{OUT} = –4 mA	2.4			VDC
V_{OL} (5) (6)	Output logic level	I_{OUT} = 4 mA			0.4	VDC
REFERENCE INPUT/OUTPUT						
	VREFAD1 output voltage			VCCAD1		V
	VREFAD2 output voltage			AGNDAD1		V
	VCOMAD output voltage			0.5 × VCCAD1		V
	VCOMAD output impedance			10		kΩ
	Allowable VCOMAD output source/sink current				1	µA
	VCOMDA output voltage			0.5 × VCCDA1		V
	VCOMDA output impedance			7.5		kΩ
	Allowable VCOMDA output source/sink current				1	µA
ADC CHARACTERISTICS						
	Resolution		16	24		Bits
	Full-scale input voltage	V_{IN} = 0 dB, Single-ended		0.2 × VCCAD1		V_{RMS}
	Full-scale input voltage	V_{IN} = 0 dB, Differential		0.4 × VCCAD1		V_{RMS}
	Center voltage			0.5 × VCCAD1		V
	Input impedance			45		kΩ
	Common-mode rejection ratio			80		dB
DC ACCURACY						
	Gain mismatch channel-to-channel	Full-scale input, V_{IN}		±2.0	±6	% of FSR
	Gain error	Full-scale input, V_{IN}		±2.0	±6	% of FSR
	Bipolar zero error	Highpass filter bypass, V_{IN}		±1.0		% of FSR

(1) BCKAD, BCKDA, LRCKAD, and LRCKDA (in slave mode, Schmitt trigger input with 50-kΩ typical internal pulldown resistor).
(2) DIN1/2/3/4 and MDO/ADR1/MD1. (Except SPI mode, Schmitt trigger input).
(3) SCKI, MDI/SDA/DEMP, and MC/SCL/FMT (Schmitt trigger input, 5-V tolerant).
(4) RST and MS/ADR0/MD0 (Schmitt trigger input with 50-kΩ typical internal pulldown resistor, 5-V tolerant).
(5) BCKAD, BCKDA, LRCKAD, and LRCKDA (in master mode), DOUT1/2/3, ZERO, OVF, and MDO/ADR1/MD1 (in SPI mode).
(6) SDA (in I^2C mode, open-drain low output).

Electrical Characteristics (continued)

At T_A = 25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE(7)(8)					
THD+N, V_{IN} = –1 dB	f_S = 48 kHz, Differential		–93	–87	dB
	f_S = 96 kHz, Differential		–93		
	f_S = 48 kHz, Single-ended		–93		
	f_S = 96 kHz, Single-ended		–93		
Dynamic range	f_S = 48 kHz, A-weighted, differential	100	107		dB
	f_S = 96 kHz, A-weighted, differential		107		
	f_S = 48 kHz, A-weighted, single-ended		104		
	f_S = 96 kHz, A-weighted, single-ended		104		
S/N ratio	f_S = 48 kHz, A-weighted, differential	100	107		dB
	f_S = 96 kHz, A-weighted, differential		107		
	f_S = 48 kHz, A-weighted, single-ended		104		
	f_S = 96 kHz, A-weighted, single-ended		104		
Channel separation (between one channel and others)	f_S = 48 kHz, Differential	98	104		dB
	f_S = 96 kHz, Differential		104		
	f_S = 48 kHz, Single-ended		101		
	f_S = 96 kHz, Single-ended		101		
DIGITAL FILTER PERFORMANCE					
Passband (single)				0.454 × f_S	Hz
Passband (dual)				0.454 × f_S	Hz
Stop band (single)		0.555 × f_S			Hz
Stop band (dual)		0.597 × f_S			Hz
Passband ripple	< 0.454 × f_S, 0.454 × f_S			±0.035	dB
Stop band attenuation	> 0.555 × f_S, 0.597 × f_S	–75			dB
Group delay time (single)			27 / f_S		sec
Group delay time (dual)			17 / f_S		sec
Highpass filter frequency response	–3 dB		0.02 × f_S / 1000		Hz
DAC CHARACTERISTICS					
Resolution		16	24		Bits
DC ACCURACY					
Gain mismatch channel-to-channel			±2.0	±6	% of FSR
Gain error			±2.0	±6	% of FSR
Bipolar zero error			±1.0		% of FSR

(7) In differential mode at VINx± pin, f_{IN} = 1 kHz, using Audio Precision System II, RMS mode with 20-kHz lowpass filter and 400-Hz highpass filter.
(8) f_S = 48 kHz : SCKI = 512 f_S (single), f_S = 96 kHz : SCKI = 256 f_S (dual), f_S = 192 kHz : SCKI = 128 f_S (quad).

Electrical Characteristics (continued)

At T_A = 25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE(9)(10)					
THD+N, V_{OUT} = 0 dB	f_S = 48 kHz		–94	–88	dB
	f_S = 96 kHz		–94		
	f_S = 192 kHz		–94		
Dynamic range	f_S = 48 kHz, EIAJ, A-weighted	105	112		dB
	f_S = 96 kHz, EIAJ, A-weighted		112		
	f_S = 192 kHz, EIAJ, A-weighted		112		
S/N ratio	f_S = 48 kHz, EIAJ, A-weighted	105	112		dB
	f_S = 96 kHz, EIAJ, A-weighted		112		
	f_S = 192 kHz, EIAJ, A-weighted		112		
Channel separation (between one channel and others)	f_S = 48 kHz	102	108		dB
	f_S = 96 kHz		108		
	f_S = 192 kHz		108		
ANALOG OUTPUT					
Output voltage	Differential		1.6 × VCCDA1		V_{PP}
Center voltage			0.5 × VCCDA1		V
Load impedance	To AC-coupled GND(11)	5			kΩ
	To DC-coupled GND(11)	15			
Lowpass filter frequency response	f = 20 kHz		–0.04		dB
	f = 44 kHz		–0.18		
DIGITAL FILTER PERFORMANCE(12)	Slow roll-off				
Passband (single, dual)				0.454 × f_S	Hz
Passband (quad)				0.432 × f_S	Hz
Stop band (single, dual)		0.546 × f_S			Hz
Stop band (quad)		0.569 × f_S			Hz
Passband ripple	≤ 0.454 × f_S			±0.0018	dB
Stop band attenuation	> 0.546 × f_S, 0.569 × f_S	–75			dB
DIGITAL FILTER PERFORMANCE	**Slow roll-off**				
Passband				0.328 × f_S	Hz
Stop band		0.673 × f_S			Hz
Passband ripple	< 0.328 × f_S			±0.0013	dB
Stop band attenuation	> 0.673 × f_S	–75			dB

(9) In differential mode at VOUTx± pin, f_{OUT} = 1 kHz, using Audio Precision System II, RMS mode with 20-kHz lowpass filter and 400-Hz highpass filter.
(10) f_S = 48 kHz : SCKI = 512 f_S (single), f_S = 96 kHz : SCKI = 256 f_S (dual), f_S = 192 kHz : SCKI = 128 f_S (quad).
(11) Allowable minimum input resistance of differential to single-ended converter with D to S Gain = G is calculated as (1 + 2G)/(1 + G) × 5k for AC-coupled and (1+ 0.9G)/(1 + G) × 15k for DC-coupled connection, refer to Figure 61 and Figure 62 of the *Application Information* section.
(12) Exclude single and dual at 128 f_S, 192 f_S system clock and quad at 256 f_S to 768 f_S system clock, and specifications for quad, single, and dual are respectively applied in reverse for them.

Electrical Characteristics (continued)

At T_A = 25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL FILTER PERFORMANCE(12)						
	Group delay time (single, dual)			$28/f_S$		sec
	Group delay time (quad)			$19/f_S$		sec
	De-emphasis error			±0.1		dB
POWER-SUPPLY REQUIREMENTS						
VCCxx1/2	Voltage range		4.5	5.0	5.5	VDC
VDD1/2	Voltage range		3.0	3.3	3.6	VDC
I_{CC}	Supply current	f_S = 48 kHz/ADC, f_S = 48 kHz/DAC		162	210	mA
I_{CC}	Supply current	f_S = 96 kHz/ADC, f_S = 192 kHz/DAC		162		mA
I_{CC}	Supply current	Full power-down(13)		300		µA
I_{DD}	Supply current	f_S = 48 kHz/ADC, f_S = 48 kHz/DAC		106	130	mA
I_{DD}	Supply current	f_S = 96 kHz/ADC, f_S = 192 kHz/DAC		127		mA
I_{DD}	Supply current	Full power-down(13)		50		µA
	Power dissipation	f_S = 48 kHz/ADC, f_S = 48 kHz/DAC		1160	1480	mW
	Power dissipation	f_S = 96 kHz/ADC, f_S = 192 kHz/DAC		1230		mW
	Power dissipation	f_S = 48 kHz/ADC, Power-down/DAC		660		mW
	Power dissipation	Power-down/ADC, f_S = 48 kHz/DAC		633		mW
	Power dissipation	Full power-down(13)		1.67		mW
TEMPERATURE RANGE						
	Operating temperature	PCM3168A Consumer grade	–40		85	°C
θ_{JA}	Thermal resistance	HTQFP-64		21		°C/W

(13) Halt SCKI, BCKAD, BCKDA, LRCKAD, and LRCKDA.

8.6 Timing Requirements: System Clock

Refer to Figure 1.

		MIN	MAX	UNIT
t_{SCY}	System clock pulse cycle time	27		ns
t_{SCH}	System clock pulse width high	10		ns
t_{SCL}	System clock pulse width low	10		ns
t_{DTY}	System clock pulse duty cycle	40%	60%	

8.7 Timing Requirements: Power-On Reset

Refer to Figure 2.

		SINGLE	DUAL	QUAD	UNIT
$t_{DACDLY1}$	DAC delay time internal reset release to VOUT start	3600	7200	14400	Period of LRCKDA
$t_{DACDLY2}$	DAC fade-in/fade-out time	2048	4096	8192	Period of LRCKDA
$t_{ADCDLY1}$	ADC delay time internal reset release to DOUT start	4800	9600	N/A	Period of LRCKAD
$t_{ADCDLY2}$	ADC fade-in/fade-out time	2048	4096	N/A	Period of LRCKAD

8.8 Timing Requirements: Audio Interface for Left-Justified, Right-Justified, and I^{2}S (Slave Mode)(1)

Refer to Figure 3.

		MIN	NOM	MAX	UNIT
t_{BCY}	BCKAD/DA cycle time	75			ns
t_{BCH}	BCKAD/DA pulse width high	35			ns
t_{BCL}	BCKAD/DA pulse width low	35			ns
t_{LRS}	LRCKAD/DA setup time to BCKAD/DA rising edge	10			ns
t_{LRH}	LRCKAD/DA hold time to BCKAD/DA rising edge	10			ns
t_{DIS}	DIN1/2/3/4 setup time to BCKDA rising edge	10			ns
t_{DIH}	DIN1/2/3/4 hold time to BCKDA rising edge	10			ns
t_{DOD}	DOUT1/2/3 delay time from BCKAD falling edge	0		30	ns

(1) Load capacitance of output is 20 pF.

8.9 Timing Requirements: Audio Interface for Left-Justified, Right-Justified, and I^{2}S (Master Mode)(1)

Refer to Figure 4.

		MIN	TYP	MAX	UNIT
t_{BCY}	BCKAD/DA cycle time		1 / (64 × f_S)		
t_{BCH}	BCKAD/DA pulse width high	0.4 × t_{BCY}	0.5 × t_{BCY}	0.6 × t_{BCY}	
t_{BCL}	BCKAD/DA pulse width low	0.4 × t_{BCY}	0.5 × t_{BCY}	0.6 × t_{BCY}	
t_{LRD}	LRCKAD/DA delay time from BCKAD/DA falling edge	–10		20	ns
t_{DIS}	DIN1/2/3/4 setup time to BCKDA rising edge	10			ns
t_{DIH}	DIN1/2/3/4 hold time to BCKDA rising edge	10			ns
t_{DOD}	DOUT1/2/3 delay time from BCKAD falling edge	–10		20	ns

(1) Load capacitance of output is 20 pF.

8.10 Timing Requirements: Audio Interface for DSP and TDM (Slave Mode)[1]

Refer to Figure 5.

		MIN	TYP	MAX	UNIT
t_{BCY}	BCKAD cycle time	75			ns
	BCKDA cycle time	40			ns
t_{BCH}	BCKAD pulse width high	35			ns
	BCKDA pulse width high	15			ns
t_{BCL}	BCKAD pulse width low	35			ns
	BCKDA pulse width low	15			ns
t_{LRW}	LRCKAD/DA pulse width high (DSP format)	t_{BCY}			
	LRCKAD/DA pulse width high (TDM format)	t_{BCY}		$1 / f_S – t_{BCY}$	
t_{LRS}	LRCKAD/DA setup time to BCKAD/DA rising edge	10			ns
t_{LRH}	LRCKAD/DA hold time to BCKAD/DA rising edge	10			ns
t_{DIS}	DIN1/2/3/4 setup time to BCKDA rising edge	10			ns
t_{DIH}	DIN1/2/3/4 hold time to BCKDA rising edge	10			ns
t_{DOD}	DOUT1/2/3 delay time from BCKAD falling edge	0		30	ns

(1) Load capacitance of output is 20 pF.

8.11 Timing Requirements: Audio Interface for DSP and TDM (Master Mode)[1]

Refer to Figure 6.

		MIN	TYP	MAX	UNIT
t_{BCY}	BCKAD/DA cycle time (DSP format)		$1 / (64 \times f_S)$		
	BCKAD/DA cycle time (TDM format, single rate)		$1 / (256 \times f_S)$		
	BCKAD/DA cycle time (TDM format, dual rate)		$1 / (128 \times f_S)$		
t_{BCH}	BCKAD/DA pulse width high	$0.4 \times t_{BCY}$	$0.5 \times t_{BCY}$	$0.6 \times t_{BCY}$	
t_{BCL}	BCKAD/DA pulse width low	$0.4 \times t_{BCY}$	$0.5 \times t_{BCY}$	$0.6 \times t_{BCY}$	
t_{LRW}	LRCKAD/DA pulse width high (DSP format)		t_{BCY}		
	LRCKAD/DA pulse width high (TDM format)		$1 / (2 \times f_S)$		
t_{LRD}	LRCKAD/DA delay time from BCKAD/DA falling edge	–10		20	ns
t_{DIS}	DIN1/2/3/4 setup time to BCKDA rising edge	10			ns
t_{DIH}	DIN1/2/3/4 hold time to BCKDA rising edge	10			ns
t_{DOD}	DOUT1/2/3 delay time from BCKAD falling edge	–10		20	ns

(1) Load capacitance of output is 20 pF.

8.12 Timing Requirements: DAC Outputs and ADC Outputs

Refer to Figure 7.

		SINGLE	DUAL	QUAD	UNIT
$t_{DACDLY3}$	DAC delay synchronization detect to normal data	38	38	29	Period of LRCKDA
$t_{ADCDLY3}$	ADC delay synchronization detect to normal data	60	60	N/A	Period of LRCKAD

8.13 Timing Requirements: Four-Wire Serial Control Interface[1]

Refer to Figure 8.

		MIN	MAX	UNIT
t_{MCY}	MC pulse cycle time	100		ns
t_{MCL}	MC low-level time	40		ns
t_{MCH}	MC high-level time	40		ns
t_{MHH}	MS high-level time	t_{MCY}		ns
t_{MSS}	MS falling edge to MC rising edge	30		ns
t_{MSH}	MS rising edge from MC rising edge for LSB	15		ns
t_{MDH}	MDI hold time	15		ns
t_{MDS}	MDI setup time	15		ns
t_{MDD}	MDO enable or delay time from MC falling edge	0	30	ns
t_{MDR}	MDO disable time from MS rising edge	0	30	ns

(1) These timing parameters are critical for proper control port operation.

8.14 Timing Requirements: SCL and SDA Control Interface

Refer to Figure 9.

		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency		100		400	kHz
t_{BUF}	Bus free time between STOP and START condition	4.7		1.3		μs
t_{LOW}	Low period of the SCL clock	4.7		1.3		μs
t_{HI}	High period of the SCL clock	4.0		0.6		μs
t_{S-SU}	Setup time for START/Repeated START condition	4.7		0.6		μs
t_{S-HD}	Hold time for START/Repeated START condition	4.0		0.6		μs
t_{D-SU}	Data setup time	250		100		ns
t_{D-HD}	Data hold time	0	3450	0	900	ns
t_{SCL-R}	Rise time of SCL signal		1000	20 + (0.1 × C_B)	300	ns
t_{SCL-F}	Fall time of SCL signal		1000	20 + (0.1 × C_B)	300	ns
t_{SDA-R}	Rise time of SDA signal		1000	20 + (0.1 × C_B)	300	ns
t_{SDA-F}	Fall time of SDA signal		1000	20 + (0.1 × C_B)	300	ns
t_{P-SU}	Setup time for STOP condition	4.0		0.6		μs
t_{GW}	Allowable glitch width		N/A		50	
C_B	Capacitive load for SDA and SCL line		400		100	pF
V_{NH}	Noise margin at high level for each connected device (including hysteresis)	0.2 × V_{DD}		0.2 × V_{DD}		V
V_{NL}	Noise margin at low level for each connected device (including hysteresis)	0.1 × V_{DD}		0.1 × V_{DD}		V
V_{HYS}	Hysteresis of Schmitt-trigger input	N/A		0.05 × V_{DD}		V

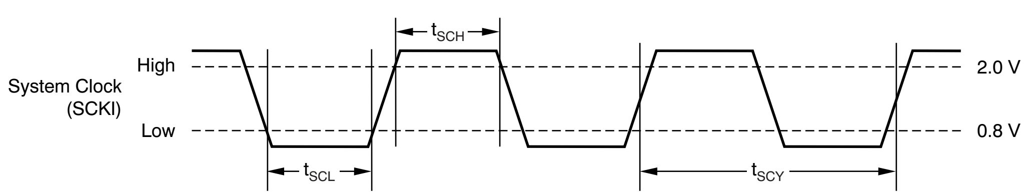


Figure 1. System Clock Timing Requirements

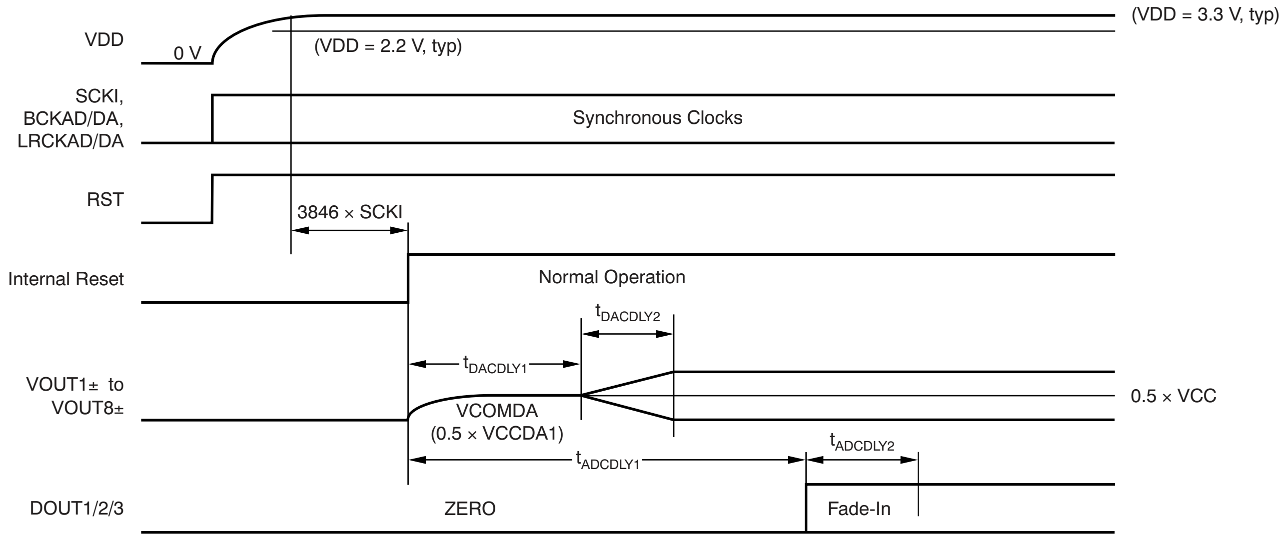


Figure 2. Power-On Reset Timing Requirements

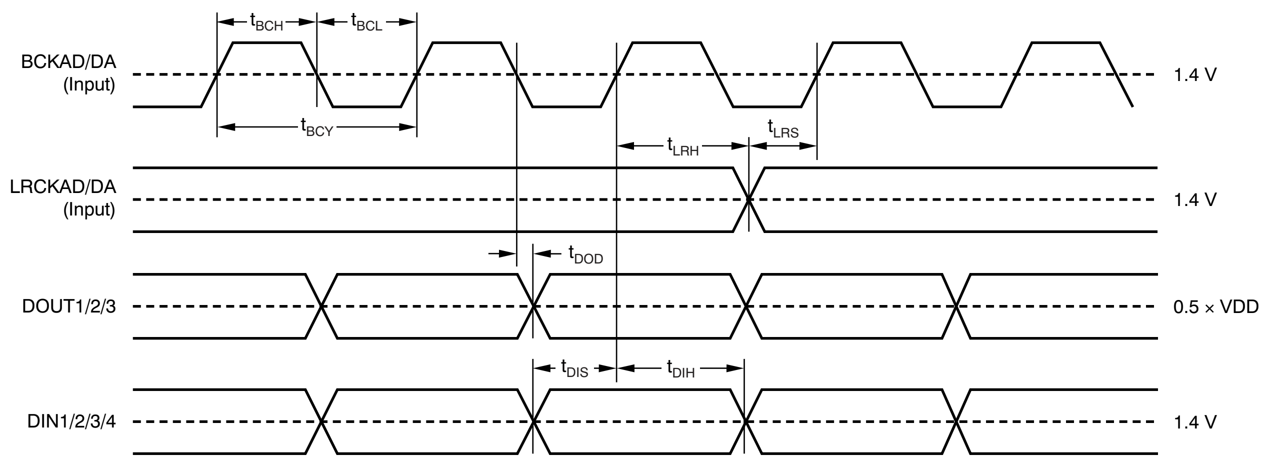


Figure 3. Audio Interface Timing Requirements for Left-Justified, Right-Justified, and I^{2}S Data Formats (Slave Mode)

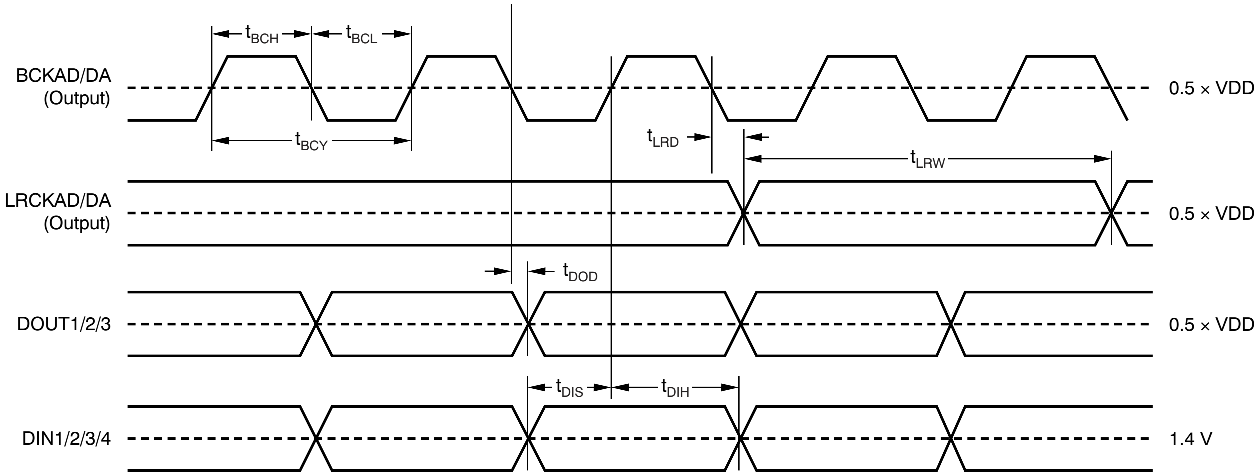


Figure 4. Audio Interface Timing Requirements for Left-Justified, Right-Justified, and I²S Data Formats (Master Mode)

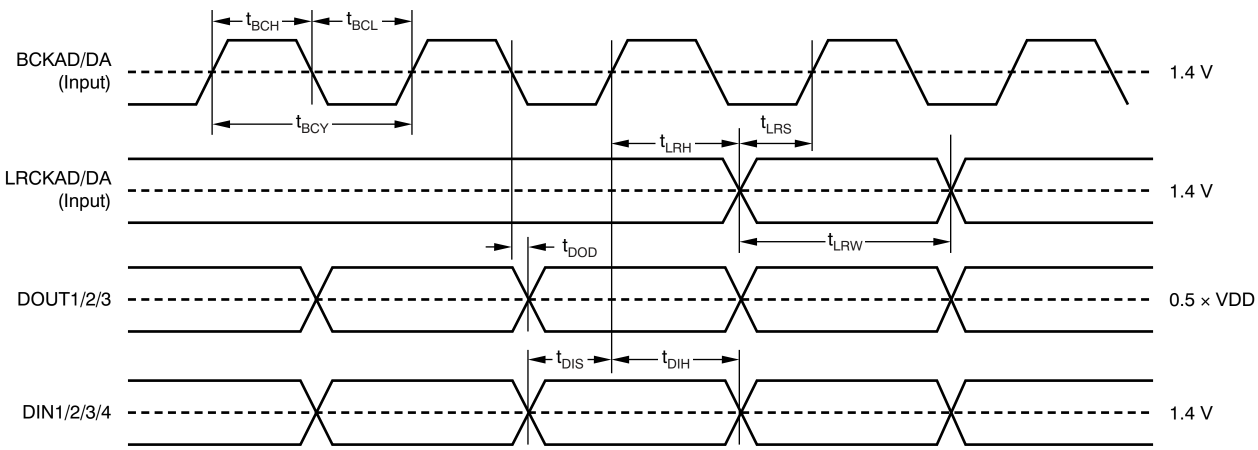


Figure 5. Audio Interface Timing Requirements for DSP and TDM Data Formats (Slave Mode)

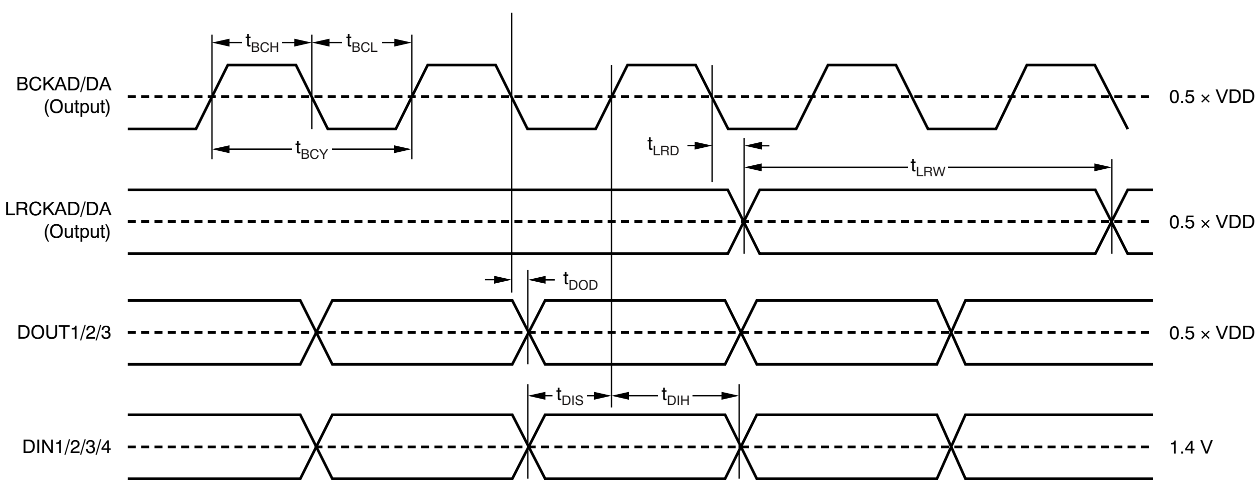


Figure 6. Audio Interface Timing Requirements for DSP and TDM Data Formats (Master Mode)

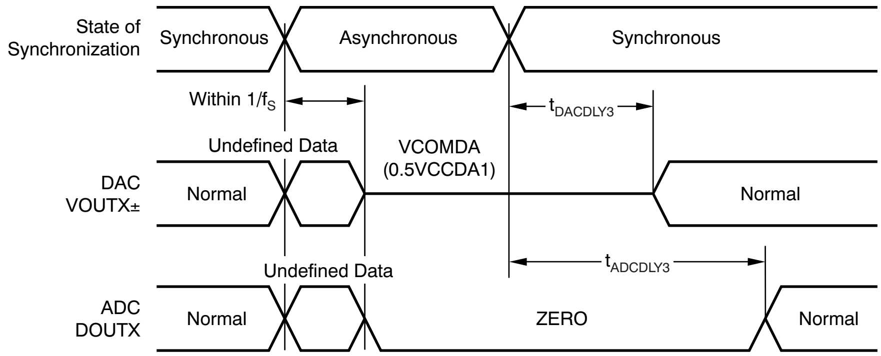
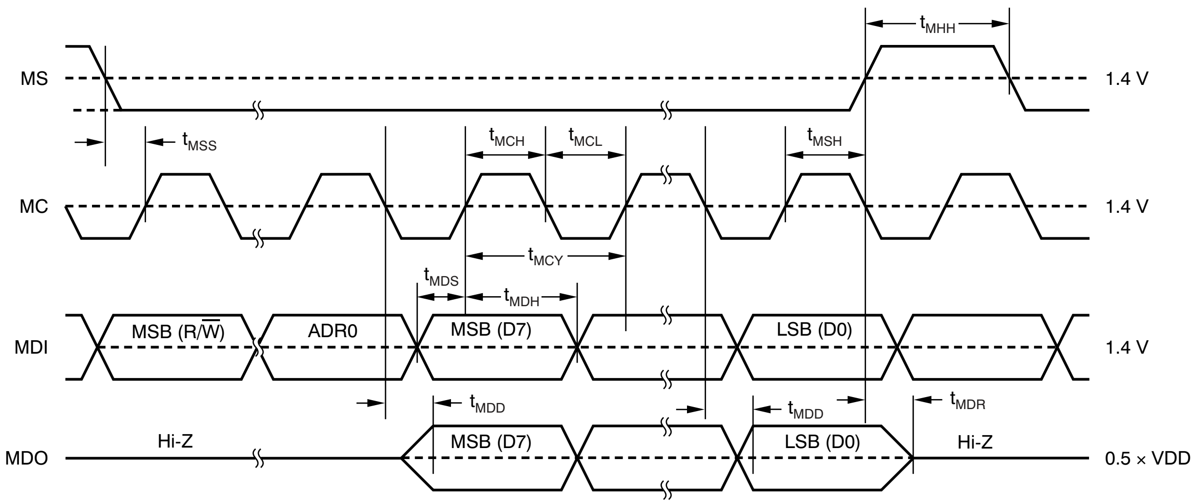


Figure 7. DAC Outputs and ADC Outputs for Loss of Synchronization



(1) These timing parameters are critical for proper control port operation.

Figure 8. Four-Wire Serial Control Interface Timing

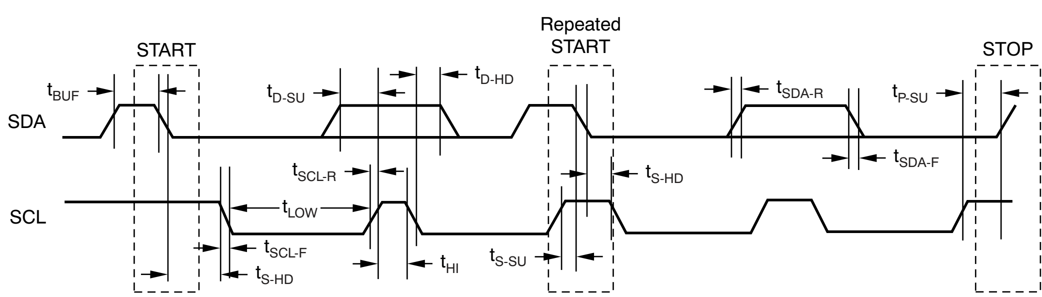


Figure 9. SCL and SDA Control Interface Timing

8.15 Typical Characteristics

8.15.1 ADC Digital Filter

At T_A = 25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.

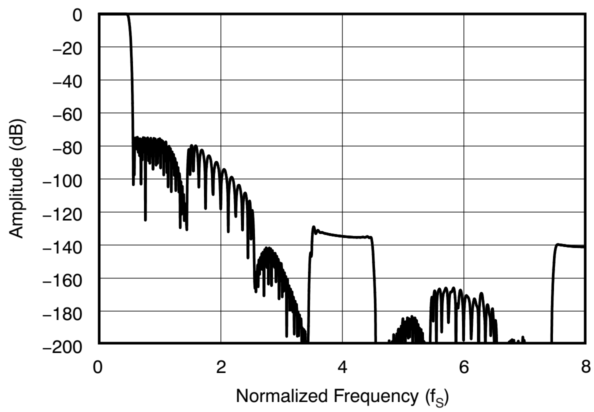


Figure 10. Frequency Response (Single Rate)

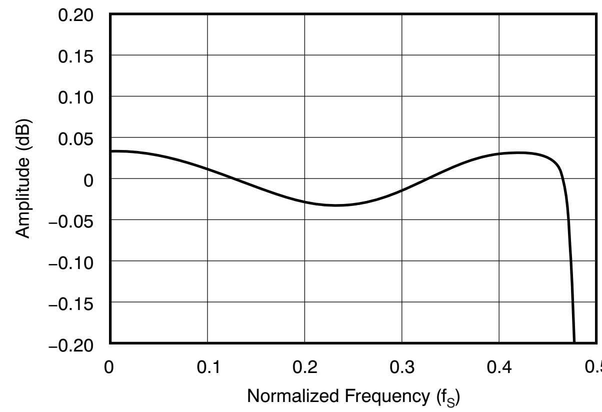


Figure 11. Frequency Response Passband (Single Rate)

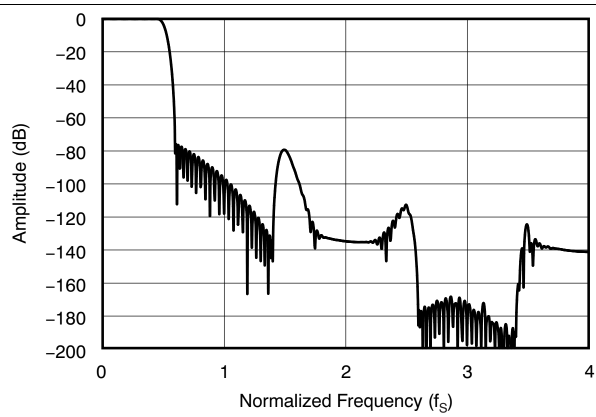


Figure 12. Frequency Response (Dual Rate)

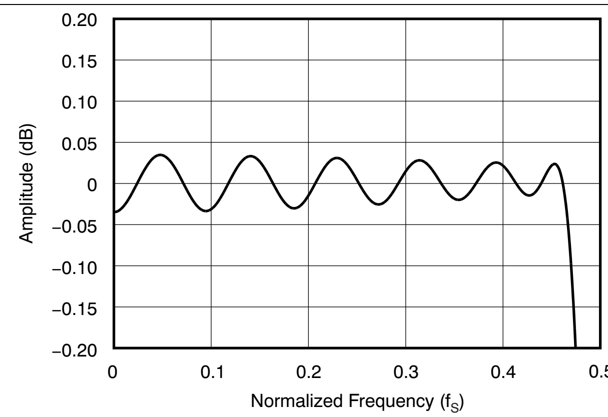


Figure 13. Frequency Response Passband (Dual Rate)

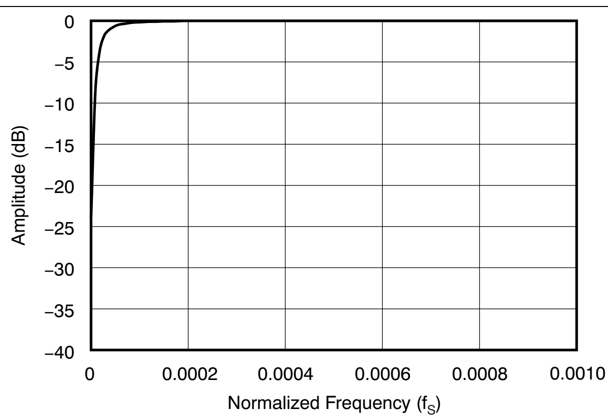


Figure 14. HPF Frequency Response

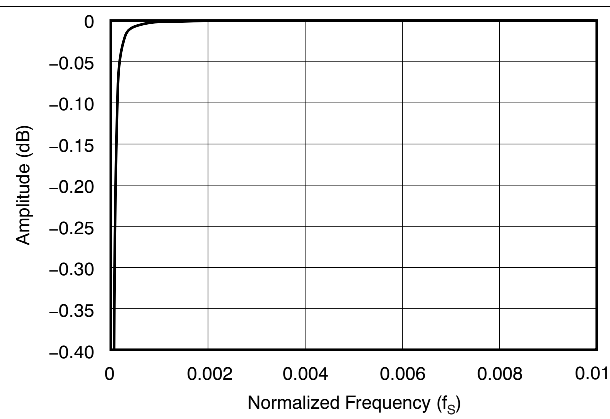


Figure 15. HPF Frequency Response Passband

8.15.2 DAC Digital Filter

At T_A = 25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.

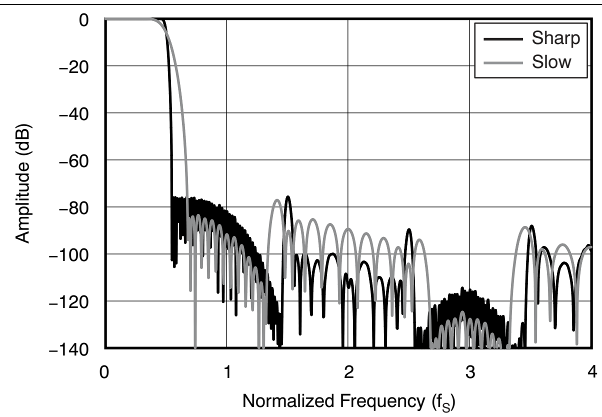


Figure 16. Frequency Response (Single Rate)

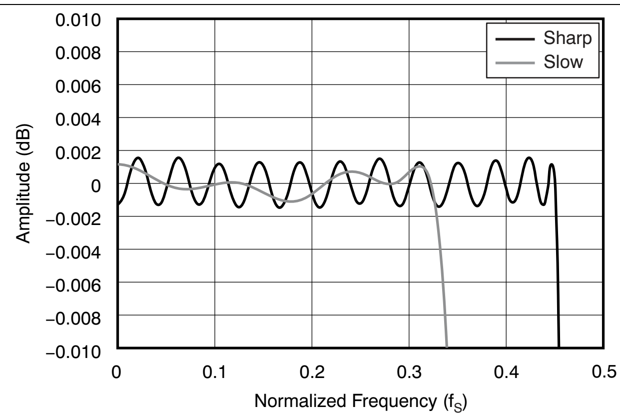


Figure 17. Frequency Response Passband (Single Rate)

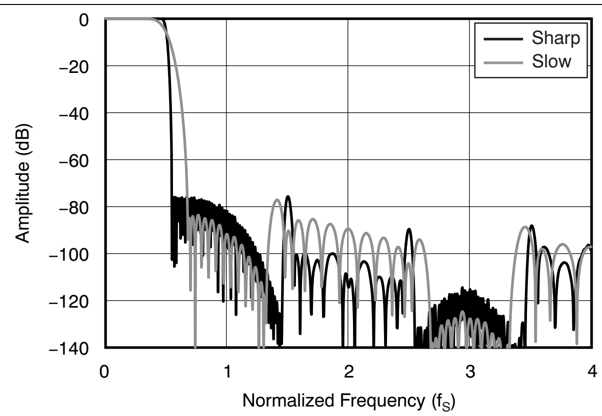


Figure 18. Frequency Response (Dual Rate)

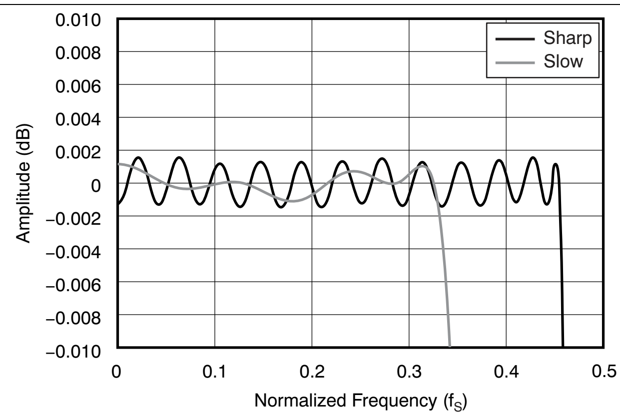


Figure 19. Frequency Response Passband (Dual Rate)

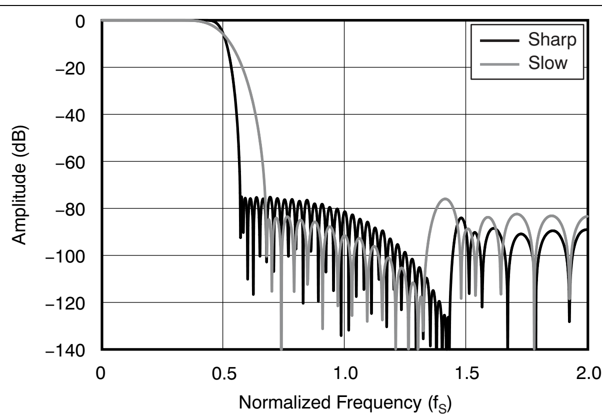


Figure 20. Frequency Response (Quad Rate)

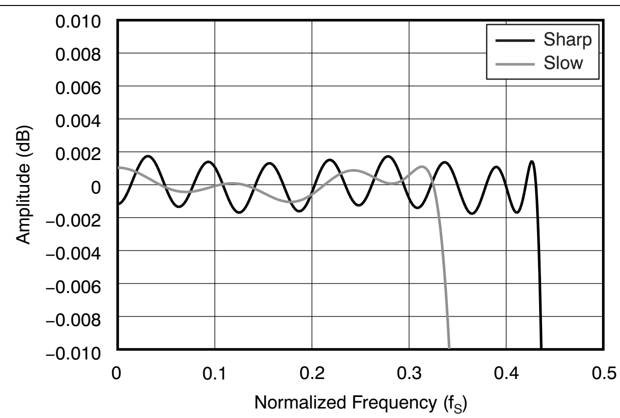


Figure 21. Frequency Response Passband (Quad Rate)

DAC Digital Filter (continued)

At T_A = 25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.

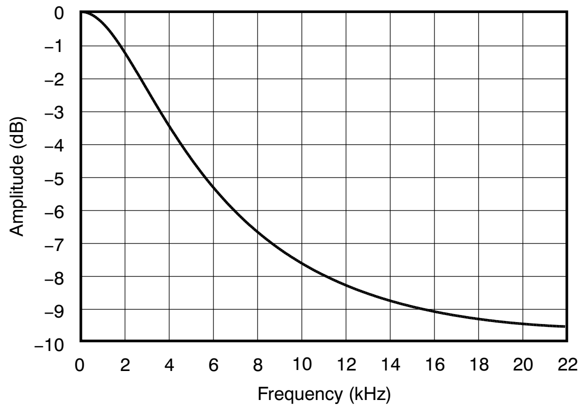


Figure 22. De-Emphasis Characteristic (F_S = 48 kHz)

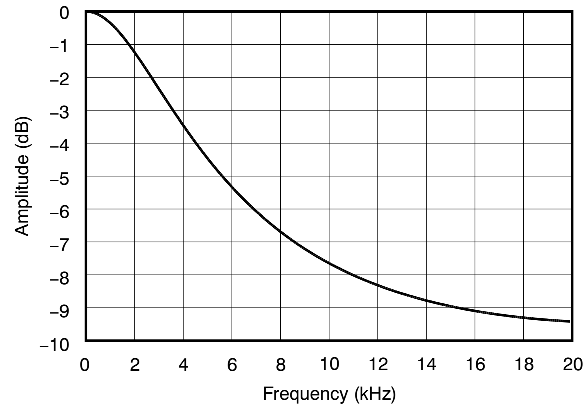


Figure 23. De-Emphasis Characteristic (F_S = 44 kHz)

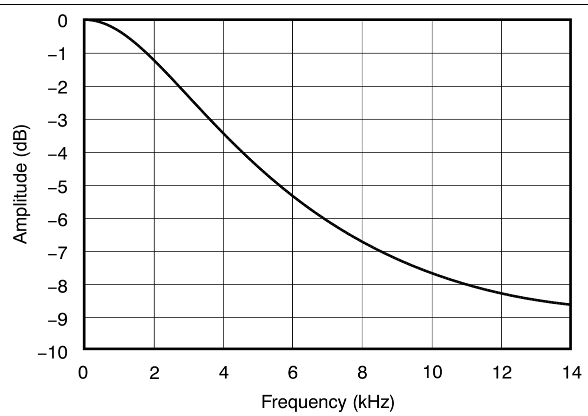


Figure 24. De-Emphasis Characteristic (F_S = 32 kHz)

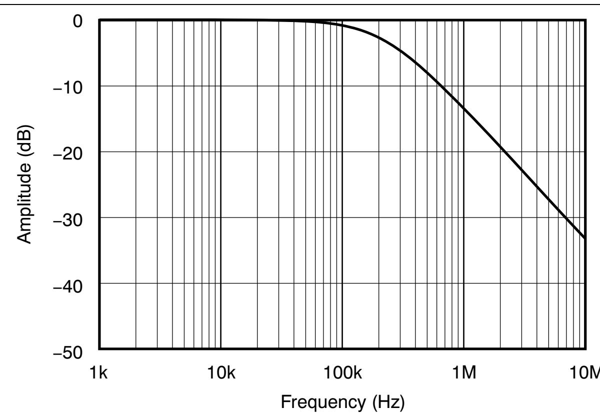


Figure 25. Analog Filter Characteristic

8.15.3 ADC Performance

At T_A = 25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.

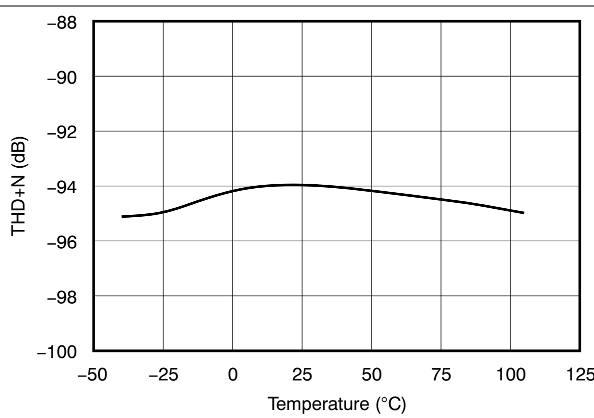


Figure 26. THD+N At –1 dB vs Temperature

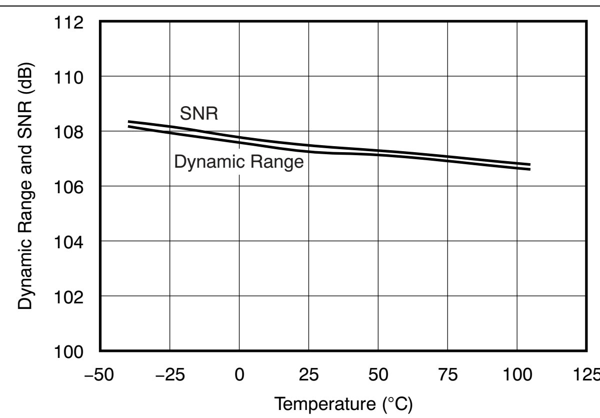


Figure 27. Dynamic Range and SNR vs Temperature

ADC Performance (continued)

At T_A = 25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.

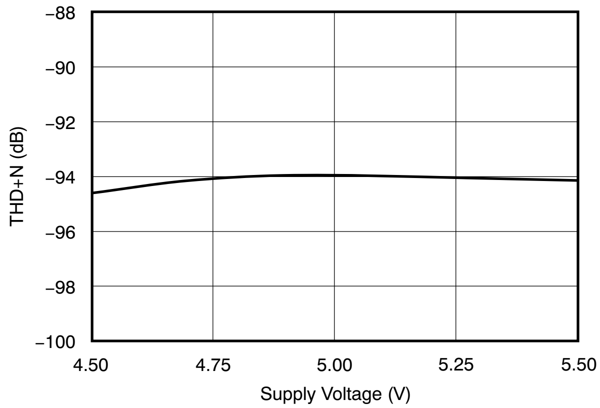


Figure 28. THD+N At –1 dB vs Supply Voltage

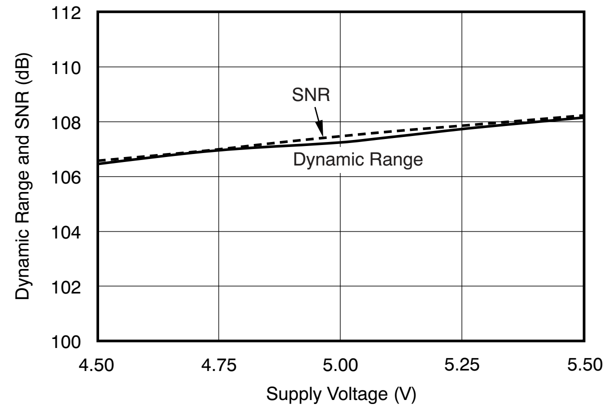


Figure 29. Dynamic Range and SNR vs Supply Voltage

8.15.4 DAC Performance

At T_A = 25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.

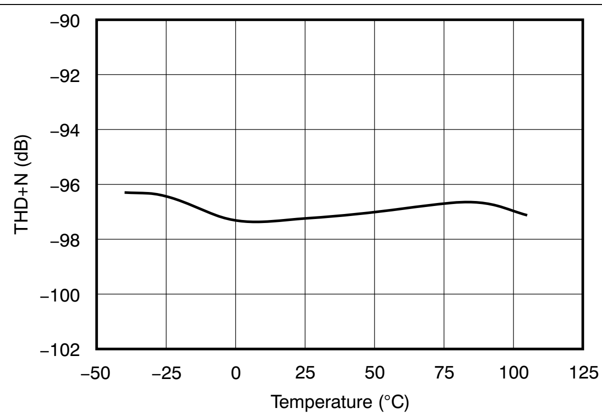


Figure 30. THD+N vs Temperature

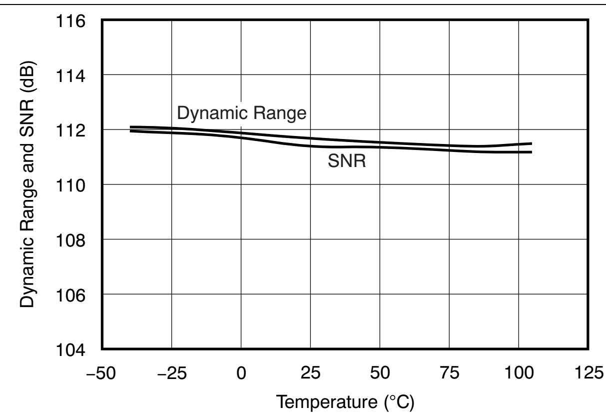


Figure 31. Dynamic Range and SNR vs Temperature

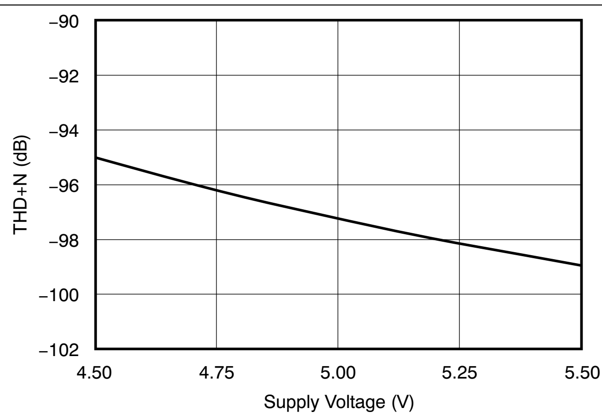


Figure 32. THD+N vs Supply Voltage

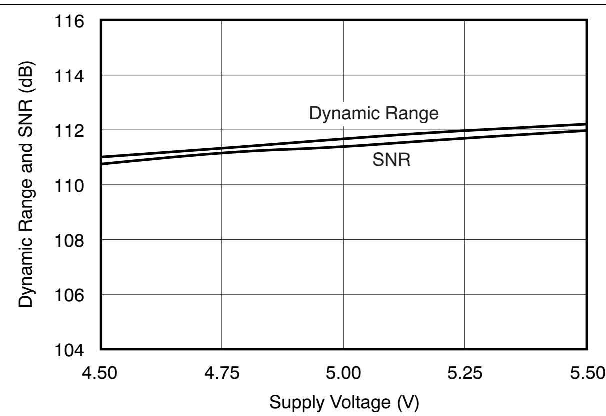


Figure 33. Dynamic Range and SNR vs Supply Voltage

8.15.5 Output Spectrum

At T_A = 25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.

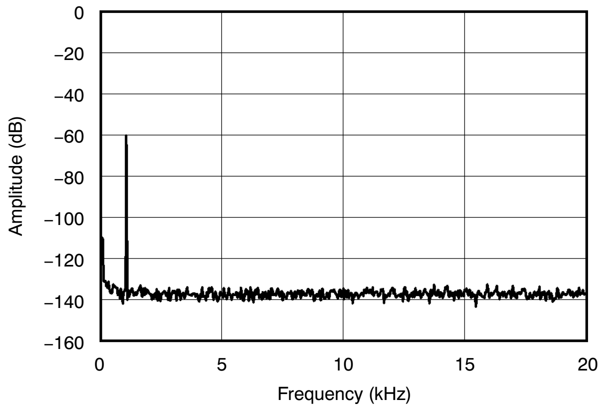


Figure 34. ADC Output Spectrum (–60 dB, N = 32768)

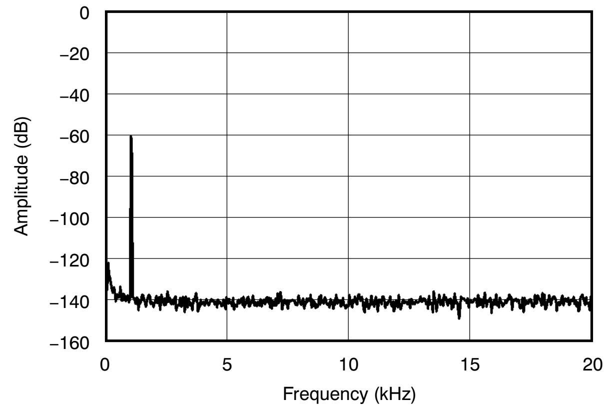


Figure 35. DAC Output Spectrum (–60 dB, N = 32768)

8.15.6 Power-Supply

At T_A = 25°C, VCCAD1 = VCCAD2 = VCCDA1 = VCCDA2 = 5 V, VDD1 = VDD2 = 3.3 V, f_S = 48 kHz, SCKI = 512 f_S, 24-bit data, Sampling Mode = Auto for ADC and DAC, and Interface Mode = Slave for ADC and DAC, unless otherwise noted.

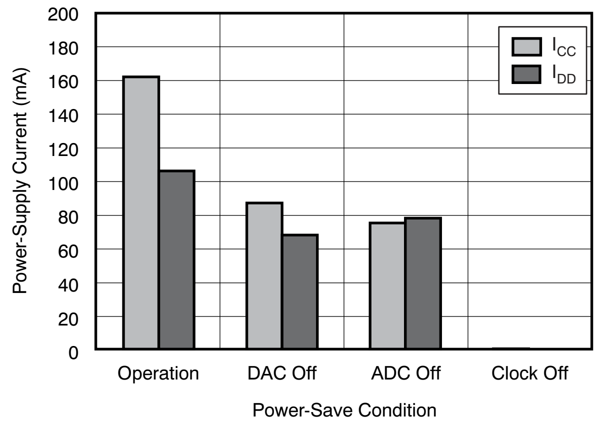


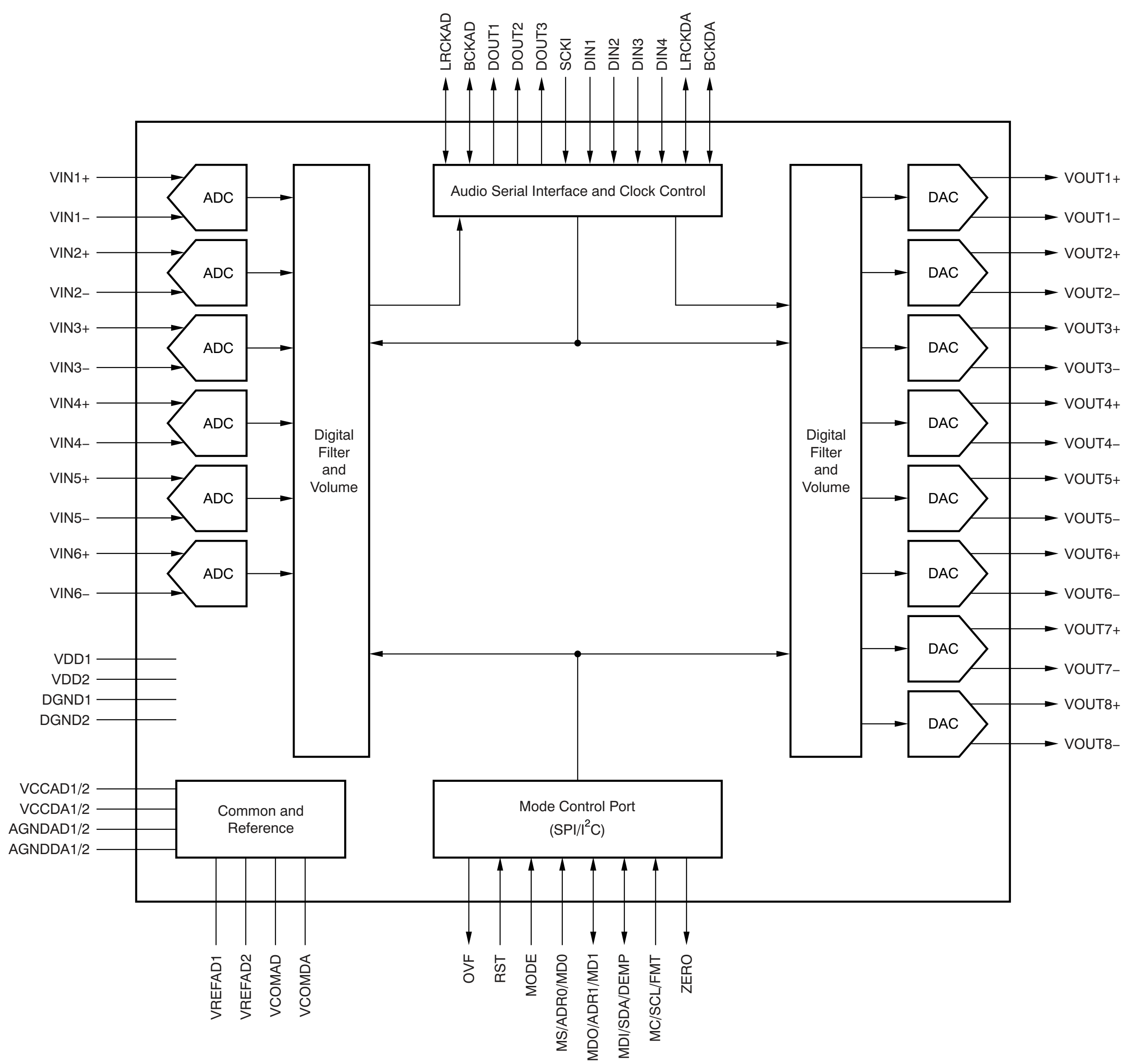
Figure 36. Power-Supply Current vs Power-Save Condition

9 Detailed Description

9.1 Overview

The PCM3168A device is a high-performance, multi-channel codec targeted for automotive audio applications, such as external amplifiers, as well as home multi-channel audio applications (for example, home theaters and A/V receivers). The PCM3168A device consists of six-channel analog-to-digital converters (ADCs) and eight-channel digital-to-analog converters (DACs). The ADC input is selectable between single-ended and differential inputs. The DAC output type is fixed with a differential configuration. The PCM3168A device supports 24-bit linear PCM input and output data in standard audio formats (left-justified, right-justified, and I^2S), DSP and TDM formats, and various sample frequencies from 8 kHz to 192 kHz (the ADC configuration supports only up to 96 kHz). The TDM format is useful to save interface bus line numbers for multi-channel audio data communication between the codec and digital audio processor. The PCM3168A device offers three modes for device control: two-wire I^2C software, four-wire SPI software, and hardware modes.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Analog Inputs

The PCM3168A device includes six ADCs, each with individual pairs of differential voltage input pins, as shown in Table 1. Additionally, the PCM3168A device has the capability of single-ended inputs. The full-scale input voltage is (0.2 × VCCAD1) V_{RMS} at the single-ended input mode and (0.4 × VCCAD1) V_{RMS} at the differential input mode. The input mode is selected by the MODE pin in hardware control mode or by register settings in the software control mode. In single-ended mode, VINx+ pins are used and VINx– pins must be terminated with AGNDAD1/2 through a capacitor or terminated with VCOMAD.

Table 1. Pin Assignments in Differential and Single-Ended Input Modes

CHANNEL	DIFFERENTIAL INPUT MODE	SINGLE-ENDED INPUT MODE
1 (ADC1)	VIN1+, VIN1–	VIN1+
2 (ADC2)	VIN2+, VIN2–	VIN2+
3 (ADC3)	VIN3+, VIN3–	VIN3+
4 (ADC4)	VIN4+, VIN4–	VIN4+
5 (ADC5)	VIN5+, VIN5–	VIN5+
6 (ADC6)	VIN6+, VIN6–	VIN6+

9.3.2 Analog Outputs

The The PCM3168A device includes eight DACs, each with individual pairs of differential voltage inputs pins, as shown in Table 2. The full-scale output voltage is (1.6 × VCCDA1) V_{PP} in differential mode. DC-coupled loads are allowed in addition to ac-coupled loads if the load resistance conforms to the specification.

Table 2. Pin Assignments for Differential Output

CHANNEL	DIFFERENTIAL OUTPUT
1 (DAC1)	VOUT1+, VOUT1–
2 (DAC2)	VOUT2+, VOUT2–
3 (DAC3)	VOUT3+, VOUT3–
4 (DAC4)	VOUT4+, VOUT4–
5 (DAC5)	VOUT5+, VOUT5–
6 (DAC6)	VOUT6+, VOUT6–
7 (DAC7)	VOUT7+, VOUT7–
8 (DAC8)	VOUT8+, VOUT8–

9.3.3 Voltage References

The PCM3168A device includes two internal references for the six-channel ADCs; these references correspond to the outputs VREFAD1 and VREFAD2. Both reference pins should be connected with an analog ground via decoupling capacitors. In addition, the PCM3168A device includes two pins for common-mode voltage output (VCOMDA for DACs and VCOMAD for ADCs). These pins should be also connected with an analog ground via decoupling capacitors. Furthermore, both common pins can be used to bias external high-impedance circuits, if they are required.

9.3.4 System Clock Input

The PCM3168A device requires an external system clock input applied at the SCKI input for ADC and DAC operation. The system clock operates at an integer multiple of the sampling frequency, or f_S. The multiples supported in ADC operation include 256 f_S, 384 f_S, 512 f_S, and 768 f_S; the multiples supported in DAC operation include 128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, and 768 f_S. Details for these system clock multiples are shown in Table 3. Figure 1 shows the SCKI timing requirements.

Table 3. System Clock Frequencies for Common Audio Sampling Rates

DEFAULT SAMPLING MODE	SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (MHz)					
	f_S (kHz)	128 f_S (1)	192 f_S (1)	256 f_S	384 f_S	512 f_S	768 f_S
Single rate	8	N/A	N/A	2.0480	3.0720 (2)	4.0960	6.1440
	16	2.0480 (1)	3.0720 (1)	4.0960	6.1440 (2)	8.1920	12.2880
	32	4.0960 (1)	6.1440 (1)	8.1920	12.2880 (2)	16.3840	24.5760
	44.1	5.6488 (1)	8.4672 (1)	11.2896	16.9344 (2)	22.5792	33.8688
	48	6.1440 (1)	9.2160 (1)	12.2880	18.4320 (2)	24.5760	36.8640
Dual rate	88.2	11.2896 (1)	16.9344 (1)	22.5792	33.8688	N/A	N/A
	96	12.2880 (1)	18.4320 (1)	24.5760	36.8640	N/A	N/A
Quad rate (1)	176.4 (1)	22.5792 (1)	33.8688 (1)	N/A	N/A	N/A	N/A
	192 (1)	24.5760 (1)	36.8640 (1)	N/A	N/A	N/A	N/A

(1) Supported only by DAC operation
(2) Requires 50% duty cycle for stable ADC performance.

9.3.5 Sampling Mode

The PCM3168A device supports two sampling modes (single rate and dual rate) in ADC operation, and three sampling modes (single rate, dual rate, and quad rate) in DAC operation. In single rate mode, the ADC and DAC operate at an oversampling frequency of x128 (except when SCKI = 128 f_S and 192 f_S). This mode is supported for sampling frequencies less than 50 kHz. In dual rate mode, the ADC and DAC operate at an oversampling frequency of x64; this mode is supported for sampling frequencies less than 100 kHz. In quad rate mode, the DAC operates at an oversampling frequency of x32. The sampling mode is automatically selected according to the ratio of system clock frequency and sampling frequency by default (for example, single rate for 512 f_S and 768 f_S, dual rate for 256 f_S and 384 f_S, and quad rate for 128 f_S and 192 f_S), but manual selection is also possible for specified combinations through the serial mode control resistor.

Table 4 and Figure 37 show the relation between the oversampling rate (OSR) of the ΔΣ modulator, noise-free shaped bandwidth, and each sampling mode setting for ADC operation. Table 5 and Figure 38 describe the relation between the oversampling rate of the digital filter and ΔΣ modulator, noise-free shaped bandwidth, and each sampling mode setting for DAC operation.

Table 4. ADC Modulator OSR and Noise-Free Shaped Bandwidth for Each Sampling Mode

SAMPLING MODE REGISTER SETTING	SYSTEM CLOCK RATE (f_S)	NOISE-FREE SHAPED BANDWIDTH (kHz)		MODULATOR OSR
		f_S = 48 kHz	f_S = 96 kHz	
Auto	512, 768	40	N/A	x128
	256, 384	20	40	x64
Single	512, 768	40	N/A	x128
	256, 384	40	N/A	x128
Dual	256, 384	20	40	x64

Table 5. DAC Digital Filter OSR, Modulator OSR, and Noise-Free Shaped Bandwidth for Each Sampling Mode

SAMPLING MODE REGISTER SETTING	SYSTEM CLOCK RATE (f_S)	NOISE-FREE SHAPED BANDWIDTH			DIGITAL FILTER OSR	MODULATOR OSR
		f_S = 48 kHz	f_S = 96 kHz	f_S = 192 kHz		
Auto	512, 768	40	N/A	N/A	x8	x128
	256, 384	20	40	N/A	x8	x64
	128, 192 (1)(2)	10	20	40	x4	x32

(1) Supported only by DAC operation.
(2) Quad mode filter characteristic is applied.

Table 5. DAC Digital Filter OSR, Modulator OSR, and Noise-Free Shaped Bandwidth for Each Sampling Mode (continued)

SAMPLING MODE REGISTER SETTING	SYSTEM CLOCK RATE (f_S)	NOISE-FREE SHAPED BANDWIDTH			DIGITAL FILTER OSR	MODULATOR OSR
		f_S = 48 kHz	f_S = 96 kHz	f_S = 192 kHz		
Single	512, 768	40	N/A	N/A	x8	x128
	256, 384	40	N/A	N/A	x8	x128
	128, 192(1)(2)	20	N/A	N/A	x4	x64
Dual	256, 384	20	40	N/A	x8	x64
	128, 192(1)(2)	20	40	N/A	x4	x64
Quad	128, 192(1)(2)	10	20	40	x4	x32

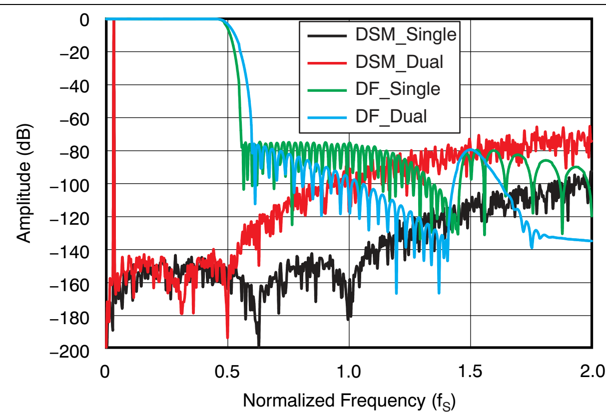


Figure 37. ADC ΔΣ Modulator and Digital Filter Characteristic

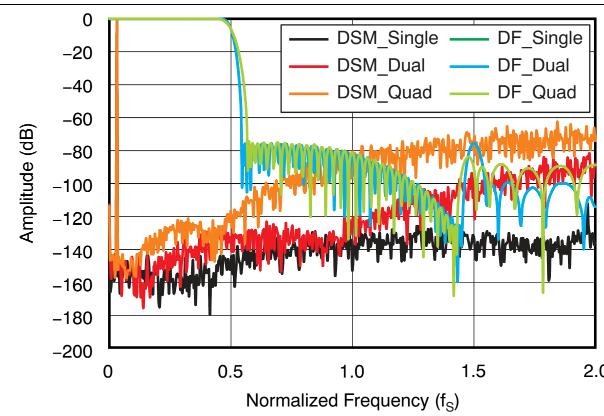


Figure 38. DAC ΔΣ Modulator and Digital Filter Characteristic

9.3.6 Reset Operation

The PCM3168A device has both an internal power-on reset circuit and an external reset circuit. The sequences for both reset circuits are illustrated in Figure 2, *Timing Requirements: Power-On Reset*, and Figure 39. Figure 2 and *Timing Requirements: Power-On Reset* describe the timing chart at the internal power-on reset. Initialization is triggered automatically at the point where V_{DD} exceeds 2.2 V typical, and the internal reset is released after 3846 SCKI clock cycles from power-on if RST is kept high and SCKI is provided. VOUT from the DACs are forced to the VCOMDA level initially (0.5 × VCCDA1) and settles at a specified level according to the rising V_{CC}. If synchronization among SCKI, BCKAD/DA, and LRCKAD/DA is maintained, VOUT starts to output with a fade-in sequence after $t_{DACDLY1}$ from the internal reset release; VOUT then provides an output that corresponds to DIN after (3846 SCKI + $t_{DACDLY1}$ + $t_{DACDLY2}$) from power-on. Meanwhile, DOUT from the ADCs begins to output with a fade-in sequence after $t_{ADCDLY1}$ from the internal reset release; DOUT then provides output corresponding to VIN after (3846 SCKI + $t_{ADCDLY1}$ + $t_{ADCDLY2}$) from power-on. If the synchronization is not held, the internal reset is not released and both operating modes are maintained at reset and power-down states; after the synchronization forms again, both the DAC and ADC return to normal operation with the above sequences.

Figure 39 illustrates a timing chart at the external reset. RST accepts an external forced reset by RST = low, and provides a device reset and power-down state that makes the lowest power dissipation state available in the PCM3168A device. If RST goes from high to low under synchronization among SCKI, BCKAD/DA, and LRCKAD/DA, the internal reset is asserted, all registers and memory are reset, and finally the PCM3168A device enters into an all power-down state. At the same time, VOUT is immediately forced into the AGNDDA1 level and DOUT becomes *0*. To begin normal operation again, toggle RST high; the same power-up sequence as power-on reset shown in Figure 2 is performed.

The PCM3168A device does not require particular power-on sequences for V_{CC} and V_{DD}; it allows V_{DD} on and then V_{CC} on, or V_{CC} on and then V_{DD} on. From the viewpoint of the *Absolute Maximum Ratings*, however, simultaneous power-on is recommended for avoiding unexpected responses on VOUTx and DOUTx. Figure 2 illustrates the response for V_{CC} on with V_{DD} on.

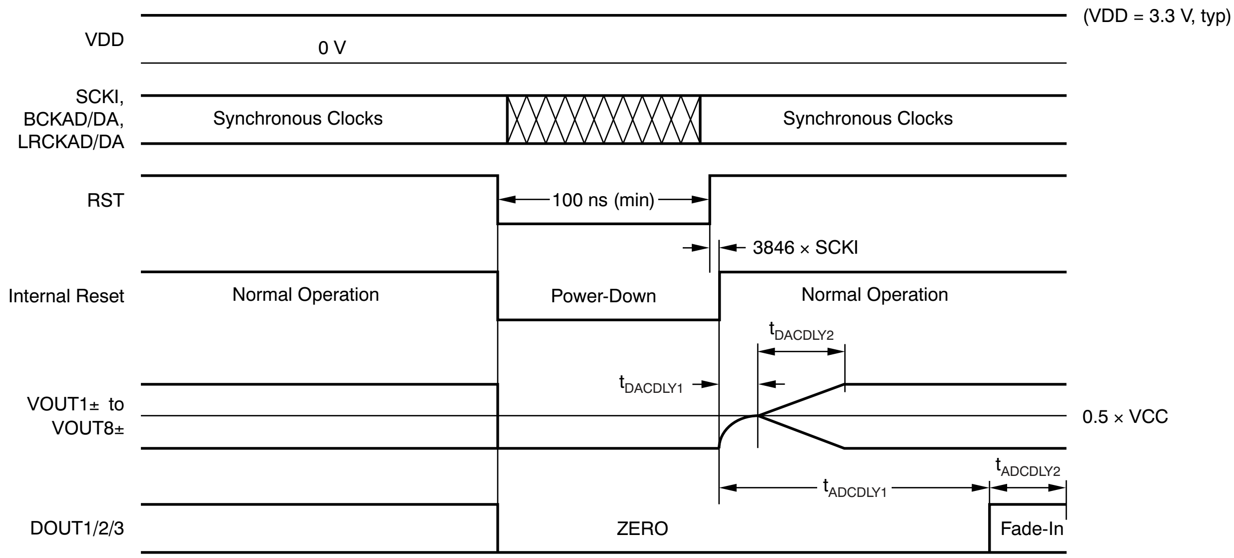


Figure 39. External Reset Timing Requirements

9.3.7 Highpass Filter (HPF)

The PCM3168A device includes a highpass filter (HPF) for all ADC channels in order to remove the DC component of the digitized input signal. The filter is located at the output of the digital decimation filter. The –3-dB corner frequency for the HPF scales with the output sampling rate, where $f_{-3\ dB} = 0.020 \times f_S/1000$. When f_S = 48 kHz, $f_{-3\ dB}$ is 0.96 Hz. The HPF function can be disabled (bypassed) by the BYP bits in two channels.

9.3.8 Overflow Flag

The PCM3168A device includes an overflow flag output for all ADC channels. As soon as any of the six-channel ADC digital outputs exceed the full-scale range, an overflow flag is forced high on the OVF pin. The overflow flag is held high for 1024 LRCKAD clock cycles. In parallel, overflow flag information is stored in the OVF bits of the mode control register, and the OVF bit is held until the mode control register is read. The overflow flag polarity can be changed by the OVFP bit. The OVF pin also indicates internal reset completion by transmitting a 4096 SCKI width pulse.

9.3.9 Zero Flag

The PCM3168A device includes a zero flag output for all DAC channels. When all of the eight-channel DACs digital inputs have continued as zero data for 1024 LRCKDA clock cycles, the zero flag is forced high on ZERO. In parallel, zero flag information is stored in the ZERO bits according to channel. The zero flag polarity can be changed by the ZREV bit. Also, the zero flag function can be selected by the AZRO bits. AND or OR logic for stereo, six channels, and eight channels can be selected.

9.3.10 Four-Wire (SPI) Serial Control

The PCM3168A device includes an SPI-compatible serial port that operates asynchronously with the audio serial interface. The control interface consists of MDI/SDA/DEMP, MDO/ADR1/MD1, MC/SCL/FMT, and MS/ADR0/MD0. MDI is the serial data input to program the mode control registers. MDO is the serial data output to read back register settings and some flags. MDO is inactive (Hi-Z, high impedance) during MS = high. MC is the serial bit clock that shifts the data into the control port. MS is the select input to enable the mode control port.

9.3.11 Control Data Word Format

All single write/read operations through the serial control port use 16-bit data words. Figure 40 shows the control data word format. The first bit is for read/write controls; *0* indicates a write operation and *1* indicates a read operation. Following the first bit are seven other bits, labeled ADR[6:0] that set the register address for the write/read operation. The eight least significant bits (LSBs), D[7:0] on MDI or MDO, contain the data to be written to the register specified by ADR[6:0], or the data read from the register specified by ADR[6:0].

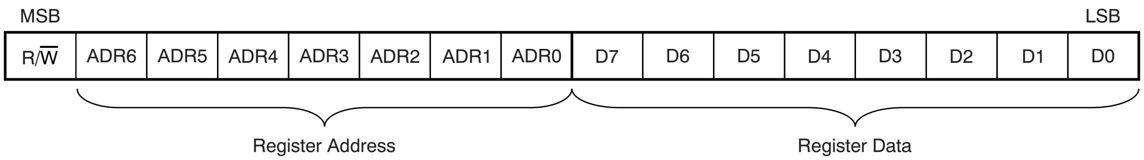
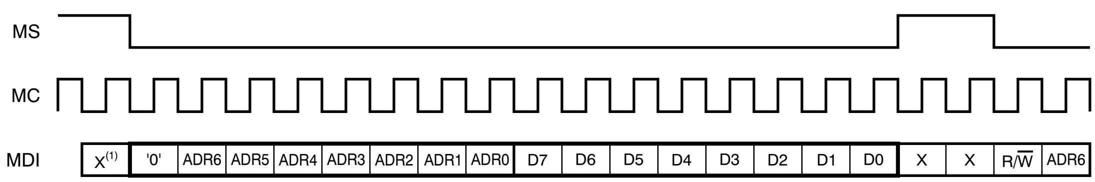


Figure 40. Control Data Word Format for MDI

9.3.12 Register Write Operation

Figure 41 shows the functional timing diagram for single write operations on the serial control port. MS is held at a high state until a register must be written. To start the register write cycle, MS is set to a low state. 16 clocks are then provided on MC, corresponding to the 16 bits of the control data word on MDI. After the 16th clock cycle has been completed, MS is set high to latch the data into the indexed mode control register.

Also, the PCM3168A device supports multiple write operations in addition to single write operations, which can be performed by sending the following N-times of the 8-bit register data after the first 16-bit register address and register data while keeping the MC clocks and MS at a low state. Closing a multiple write operation can be accomplished by setting MS to a high state.

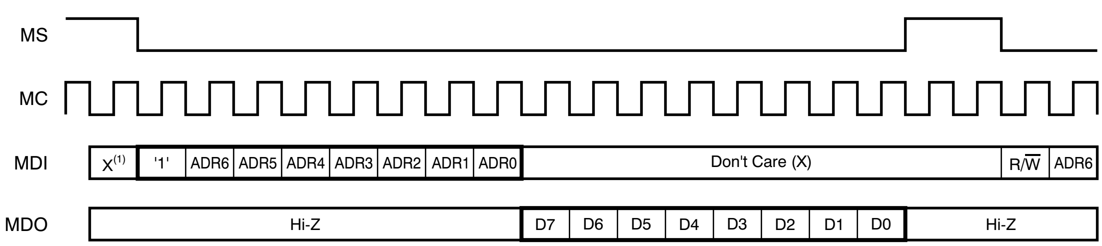


(1) X = Don't care

Figure 41. Register Write Operation

9.3.13 Register Read Operation

Figure 42 shows the functional timing diagram for single read operations on the serial control port. MS is held at a high state until a register must be read. To start the register read cycle, MS is set to a low state. 16 clocks are then provided on MC, corresponding to the first eight bits of the control data word on MDI and the second eight bits of the read-back data word from MDO. After the 16th clock cycle has been completed, MS is held high for the next write or read operation. MDO remains in a high impedance state except during the eight MC clock periods of the actual data transfer.



(1) X = Don't care

Figure 42. Register Read Operation

9.3.14 Two-Wire (I²C) Serial Control

The PCM3168A device supports an I²C-compatible serial bus and data transmission protocol for fast mode configured as a slave device. This protocol is explained in the I²C specification, version 2.0.

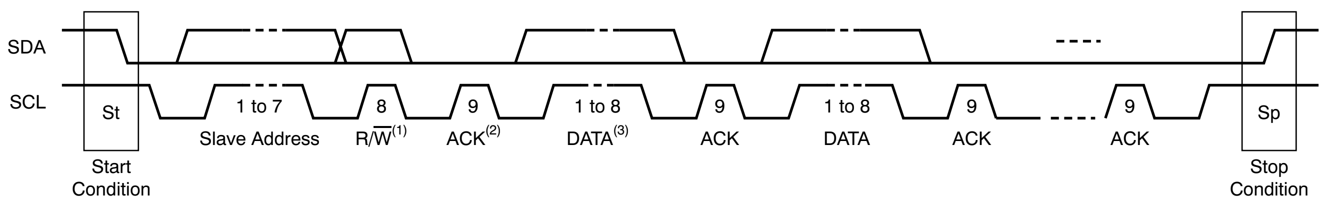
The PCM3168A device has a 7-bit slave address, as shown in Figure 43. The first five bits are the most significant bits (MSB) of the slave address and are factory-preset to *10001*. The next two bits of the address byte are selectable bits that can be set by MS/ADR0/MD0 and MDO/ADR1/MD1. A maximum of four PCM3168A device can be connected on the same bus at any one time. Each device responds when it receives its own slave address.

MSB							LSB
1	0	0	0	1	ADR1	ADR0	R/$\overline{W}$

Figure 43. Slave Address

9.3.15 Packet Protocol

A master device must control the packet protocol, which consists of the start condition, slave address with the read/write bit, data if a write operation is required, acknowledgement if a read operation is required, and stop condition. The PCM3168A device supports both slave receiver and transmitter functions. Details about DATA for both write and read operations are described in Figure 44.



(1) R/$\overline{W}$: Read operation if 1; write operation otherwise.

(2) ACK: Acknowledgement of a byte if 0, not Acknowledgement of a byte if 1.

(3) DATA: Eight bits (byte); details are described in the *Write Operation* and *Read Operation* sections.

Figure 44. DATA Operation

9.3.16 Write Operation

The PCM3168A device supports a receiver function. A master device can write to any PCM3168A device register using single or multiple accesses. The master sends a PCM3168A device slave address with a write bit, a register address, and the data. If multiple access is required, the address is that of the starting register, followed by the data to be transferred. When the data are received properly, the index register is incremented by one automatically. When the index register reaches 0x5E, the next value is 0x40. When undefined registers are accessed, the PCM3168A device does not send an acknowledgment. Figure 45 illustrates a diagram of the write operation. The register address and write data are in 8-bit, MSB-first format.

Transmitter	M	M	M	S	M	S	M	S	M	S	------	S	M
Data Type	St	Slave Address	$\overline{W}$	ACK	Reg Address	ACK	Write Data 1	ACK	Write Data 2	ACK	------	ACK	Sp

(1) M = Master device, S = Slave device, St = Start condition, $\overline{W}$ = Write, ACK = Acknowledge, and Sp = Stop condition.

Figure 45. Framework for Write Operation

9.3.17 Read Operation

A master device can read the registers from 0x40 to 0x5E of the PCM3168A device. The value of the register address is stored in an indirect index register in advance. The master sends the PCM3168A slave address with a read bit after storing the register address. Then the PCM3168A device transfers the data of the register with address that is in the indirect index register. Figure 46 shows a diagram of the read operation.

Transmitter	M	M	M	S	M	S	M	M	M	S	S	M	M
Data Type	St	Slave Address	$\overline{W}$	ACK	Reg Address	ACK	Sr	Slave Address	R	ACK	Read Data	NACK	Sp

(1) M = Master device, S = Slave device, St = Start condition, Sr = Repeated start condition, $\overline{W}$ = Write, R = Read, ACK = Acknowledge, NACK = Not acknowledge, and Sp = Stop condition.

NOTE: The slave address after the repeated start condition must be the same as the previous address.

Figure 46. Framework for Read Operation

9.4 Device Functional Modes

9.4.1 Mode Control

The PCM3168A device includes four-way mode control selectable by MODE pin, as shown in Table 6. The pull-up and pull-down resistors must be 220 kΩ ±5%. This mode control selection is sampled only when the internal reset is released by a power-on reset or by a low-to-high transition of the external reset (RST pin); a system clock is also required.

Table 6. Mode Control Selection

MODE	MODE CONTROL INTERFACE
Tied to DGND	Two-wire (I^2C) serial control, selectable analog input configuration
Tied to DGND through pull-down resistor	H/W (hardware control), differential analog input
Tied to V_{DD} through pull-up resistor	H/W (hardware control), single-ended analog input
Tied to V_{DD}	Four-wire (SPI) serial control, selectable analog input configuration

From the mode control selection described in Table 6, the functions of four pins are changed, as shown in Table 7.

Table 7. Pin Functions

PIN	PIN ASSIGNMENTS		
	SPI	I^2C	H/W
MS/ADR0/MD0	MS	ADR0	MD0
MDO/ADR1/MD1	MDO	ADR1	MD1
MDI/SDA/DEMP	MDI	SDA	DEMP
MC/SCL/FMT	MC	SCL	FMT

Both serial controls are available while RST = high and after internal reset completion, which is indicated as a negative transition (high ≥ low) of a 4096 × SCKI width pulse on the OVF pin.

9.4.2 Hardware Control Mode Configuration

The data format is selected by the MC/SCL/FMT pin between I^2S format and I^2S mode in TDM format, as shown in Table 8.

Table 8. Data Format Selection

FMT	MODE CONTROL INTERFACE
Low	I^2S audio data format
High	I^2S mode, TDM audio data format (supported only for SCKI = 128 f_S, 256 f_S, or 512 f_S)

The de-emphasis filter is enabled by the MDI/SDA/DEMP pin. The de-emphasis frequency is fixed at 44.1 kHz in hardware control mode, as shown in Table 9. The software mode provides full selections of 32 kHz, 44.1 kHz, and 48 kHz.

Table 9. Hardware Control Mode

DEMP (DE-EMPHASIS FILTER ENABLE)	DESCRIPTION
Low	44.1 kHz, de-emphasis disabled
High	44.1 kHz, de-emphasis enabled

The audio interface and the sampling mode are selected by the MS/ADR0/MD0 and MDO/ADR1/MD1 pins. The selectable multiple of the master mode audio interface is limited between 256 f_S, 384 f_S, and 512 f_S; the selectable sampling mode is limited as shown in Table 10. The software mode provides full selections.

Table 10. Selectable Sampling Mode

MD1	MD0	DESCRIPTION			
		INTERFACE MODE		SAMPLING MODE	
		ADC	DAC	ADC	DAC
Low	Low	Slave(1)	Slave(1)	Auto(2)	Auto(2)
Low	High	Master, 512 f_S	Slave(1)	Single rate	Auto(2)
High	Low	Master, 384 f_S	Slave(1)	Dual rate	Auto(2)
High	High	Master, 256 f_S	Slave(1)	Dual rate	Auto(2)

(1) The multiples between system clock and sampling frequency are automatically detected; 256 f_S, 384 f_S, 512 f_S, and 768 f_S are acceptable for ADC operation, and 128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, and 768 f_S are acceptable for DAC operation.
(2) The sampling mode is automatically set as single rate for 512 f_S and 768 f_S, dual rate for 256 f_S and 384 f_S, and quad rate for 128 f_S and 198 f_S, according to the detected multiples between the system clock and sampling clock.

9.4.3 Audio Serial Port Operation

The PCM3168A device audio serial port consists of 11 signals: BCKDA, BCKAD, LRCKDA, LRCKAD, DIN1, DIN2, DIN3, DIN4, DOUT1, DOUT2, and DOUT3. The PCM3168A device also supports audio-interface mode, slave mode, and master mode. The BCKAD/DA is a bit clock input at the slave mode and an output at the master mode. The LRCKAD/DA is a left/right word clock or frame synchronization clock input at slave mode and output at master mode. The DIN1/2/3/4 are the audio data inputs for the DAC. The DOUT1/2/3 are the audio data outputs from the ADC. BCKAD, LRCKAD and DOUT1/2/3 are used for the ADC, and BCKDA, LRCKDA and DIN1/2/3/4 are used for the DAC.

9.4.4 Audio Data Interface Formats and Timing

The PCM3168A device supports eight audio data interface formats for the ADC and DAC separately in both master and slave modes: 24-bit I^2S, 24-bit left-justified, 24-bit right-justified, 16-bit right-justified, 24-bit left-justified mode DSP, 24-bit I^2S mode DSP, 24-bit left-justified mode TDM, and 24-bit I^2S mode TDM format. The PCM3168A device also supports two audio data interface formats for the DAC and slave mode: 24-bit left-justified mode high-speed TDM and 24-bit I^2S mode high-speed TDM format. In the case of I^2S, left-justified, and right-justified data formats, 64 BCKs, 48 BCKs, and 32 BCKs per LRCK period are supported, but 48 BCKs are limited in slave mode and 32 BCKs are limited in slave mode 16-bit right-justified only. In the case of TDM data format in single rate, BCKAD/DA, LRCKAD/DA, DOUT1, and DIN1 are used. In the case of TDM data format in dual rate, BCKAD/DA, LRCKAD/DA, DOUT1/2, and DIN1/2 are used. In the case of high-speed TDM format in dual rate, BCKDA, LRCKDA, and DIN1 are used. In the case of high-speed TDM format in quad rate, BCKDA, LRCKDA, and DIN1/2 are used. TDM format and high-speed TDM format are supported only at SCKI = 512 f_S, 256 f_S, 128 f_S, and $f_{BCK} \leq f_{SCKI}$. The audio data formats are selected by MC/SCL/FMT in hardware control mode and registers 65 and 81 in software control mode. All data must be in binary twos complement, MSB first.

Figure 47 through Figure 53 show 10 audio interface data formats. Table 11 summarizes the applicable formats and describes the relationships among them and the respective restrictions with mode control.

Table 11. Audio Data Interface Formats and Sampling Rate, Bit Clock, and System Clock Restrictions

CONTROL MODE	FORMAT	I/F MODE	DATA BITS	MAX LRCK FREQUENCY (f_S)	SCKI RATE (xf_S)	BCK RATE (xf_S)	APPLICABLE PINS
Software control	I^{2}S/Left-Justified	Master/Slave	24	96 kHz (ADC) 192 kHz (DAC)	256 to 768 (ADC) 128 to 768 (DAC)	64, 48 (slave) (1)	DOUT1/2/3 DIN1/2/3/4
	Right-Justified		24, 16			64, 48 (slave) (1), 32 (slave, 16 bit) (1)	
	I^{2}S/Left-Justified DSP		24			64	
	I^{2}S/ Left-Justified TDM		24	48 kHz	256, 512	256	DOUT1, DIN1
			24	96 kHz	128 (DAC) (2), 256	128	DOUT1/2, DIN1/2
	High-Speed I^{2}S/Left-Justified TDM	Slave and DAC Only (3)	24	96 kHz	256	256	DIN1
			24	192 kHz	128	128	DIN1/2
Hardware control	I^{2}S	Master (ADC), Slave	24	96 kHz (ADC) 192 kHz (DAC)	256 to 768 (ADC) 128 to 768 (DAC)	64, 48 (slave) (1)	DOUT1/2/3 DIN1/2/3/4
	I^{2}S TDM		24	48 kHz	512	256	DOUT1, DIN1
			24	96 kHz	256	128	DOUT1/2, DIN1/2

(1) BCK = 48 f_S, 32 f_S is supported only in slave mode; BCK = 32 f_S is supported only for 16-bit data length.
(2) SCKI = 128 f_S is supported only for DAC.
(3) High-Speed I^{2}S/Left-Justified TDM format is supported only for DAC operation in slave mode.

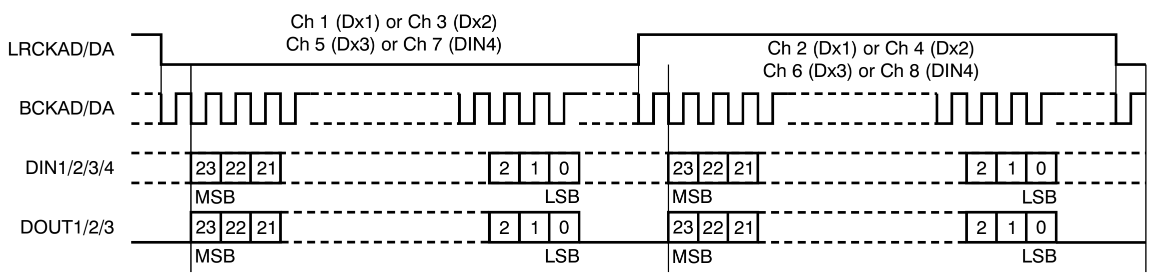


Figure 47. Audio Data Format: 24-Bit I^{2}S

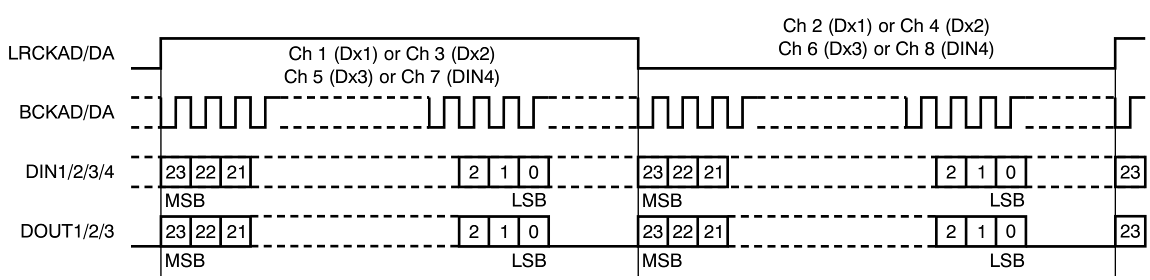


Figure 48. Audio Data Format: 24-Bit Left-Justified

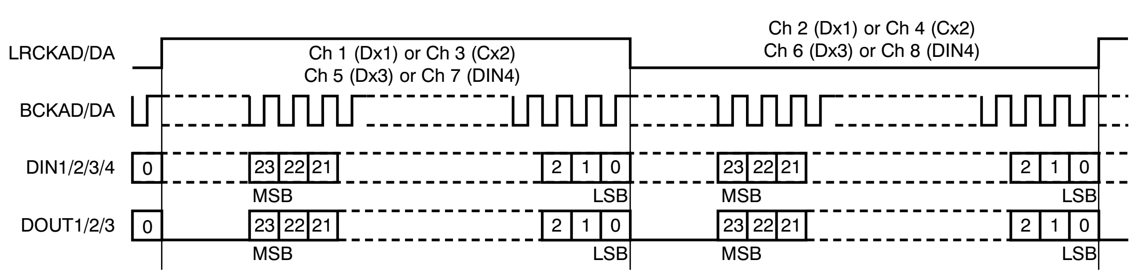


Figure 49. Audio Data Format: 24-Bit Right-Justified

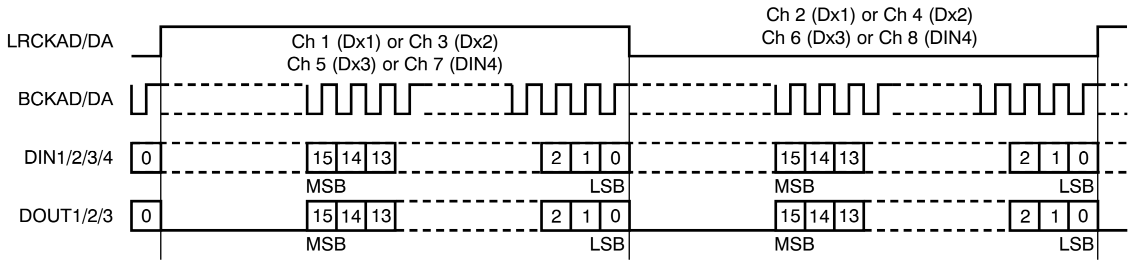


Figure 50. Audio Data Format: 16-Bit Right-Justified

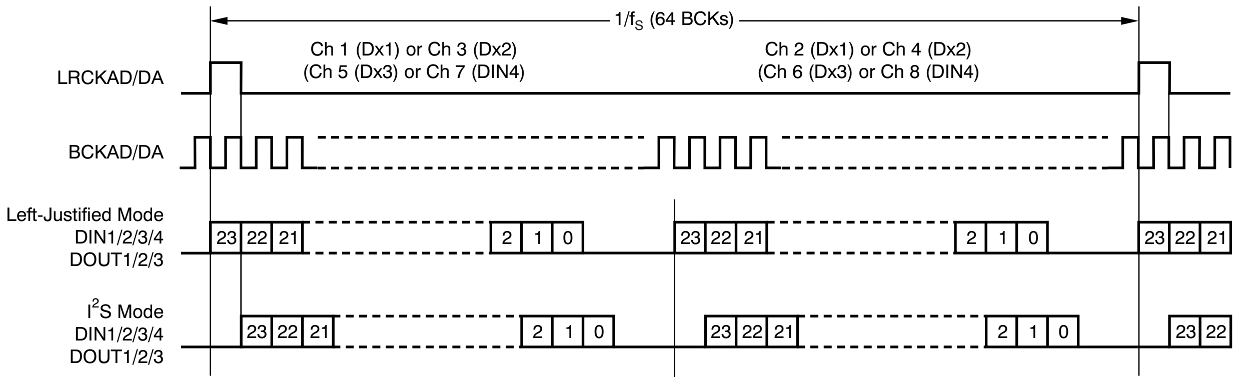


Figure 51. Audio Data Format: 24-Bit DSP Format

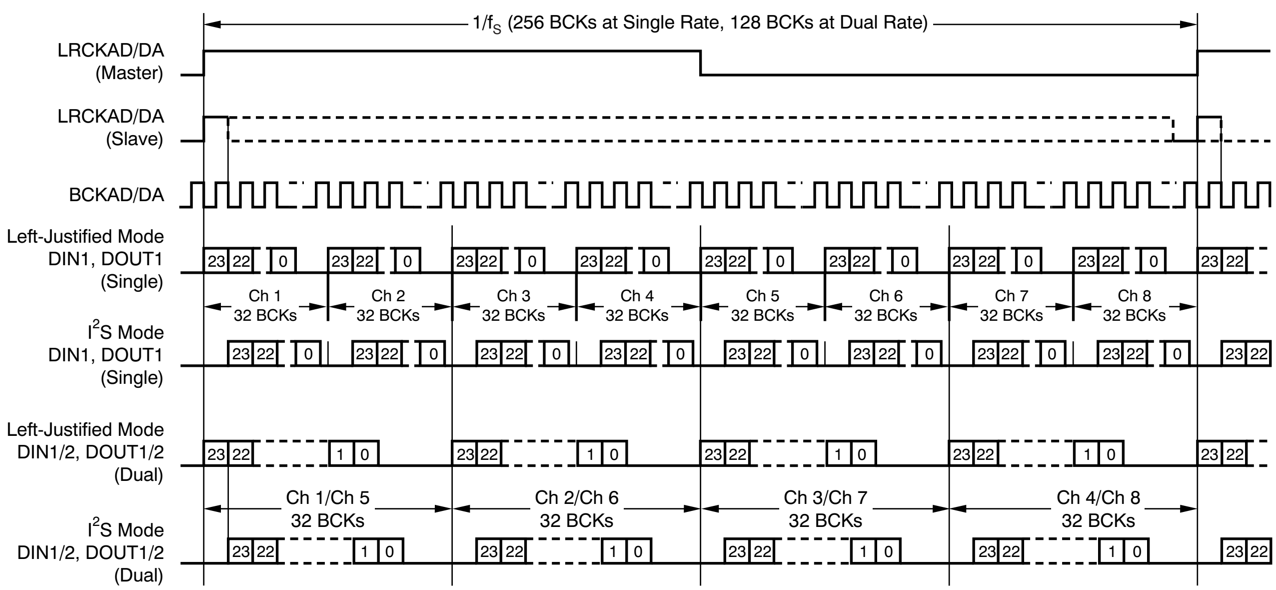


Figure 52. Audio Data Format: 24-Bit TDM Format (SCKI = 128 f_S, 256 f_S, and 512 f_S Only)

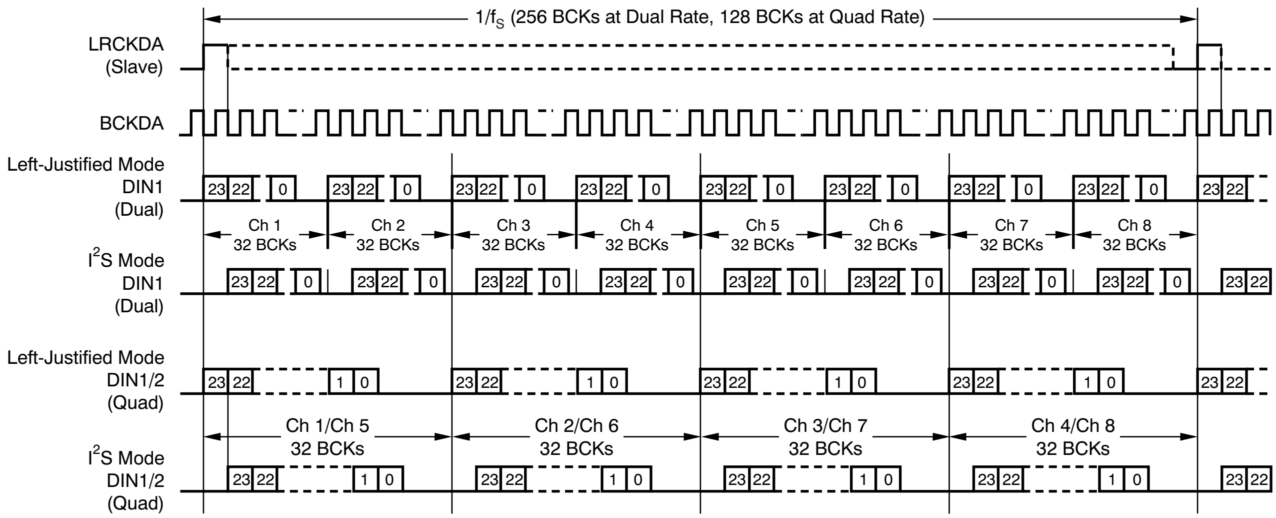


Figure 53. Audio Data Format: 24-Bit High-Speed TDM Format (SCKI = 128 f_S, 256 f_S, DAC, and Slave Mode Only)

9.4.5 Synchronization With the Digital Audio System

The PCM3168A device operates under the system clock (SCKI) and the audio sampling rate (LRCKAD/DA). Therefore, SCKI and LRCKAD/DA must have a specific relationship in slave mode. The PCM3168A device does not need a specific phase relationship between the audio interface clocks (LRCKAD/DA, BCKAD/DA) and the system clock (SCKI), but does require a specific frequency relationship (ratiometric) between LRCKAD/DA, BCKAD/DA, and SCKI.

If the relationship between SCKI and LRCKDA changes more than ±2 BCKDA clocks because of jitter, sampling frequency change, and so forth, the DAC internal operation halts within 1 / f_S, and the analog output is forced into VCOMDA (0.5 VCCDA1) until re-synchronization between SCKI, LRCKDA, and BCKDA is completed and then $t_{DACDLY3}$ passes. If the relationship between SCKI and LRCKAD changes more than ±2 BCKADs because of jitter, sampling frequency change, and so forth, the ADC internal operation halts within 1 / f_S, and the digital output is forced into a 0 code until re-synchronization between SCKI, LRCKAD, and BCKAD is completed and then $t_{ADCDLY3}$ passes. In the event the change is less than ±2 BCKAD/DAs, re-synchronization does not occur, and this analog/digital output control and discontinuity do not occur.

Figure 7 shows the DAC analog output and ADC digital output for loss of synchronization. During undefined data periods, some noise may be generated in the audio signal. Also, the transition of normal to undefined data and undefined (or zero) data to normal data creates a discontinuity of data on the analog and digital outputs, which then may generate some noise in the audio signal.

Both ADC outputs (DOUTx) and DAC outputs (VOUTx) hold the previous state if the system clock halts, but the asynchronous and re-synchronization processes would occur after the system clock resumes. Figure 7 shows DAC outputs and ADC outputs for loss of synchronization.

9.5 Register Maps

Table 12. Register Map

ADDRESS		DATA							
DAC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
64	40	MRST	SRST	—	—	—	—	SRDA1	SRDA0
65	41	PSMDA	MSDA2	MSDA1	MSDA0	FMTDA3	FMTDA2	FMTDA1	FMTDA0
66	42	OPEDA3	OPEDA2	OPEDA1	OPEDA0	FLT3	FLT2	FLT1	FLT0
67	43	REVDA8	REVDA7	REVDA6	REVDA5	REVDA4	REVDA3	REVDA2	REVDA1
68	44	MUTDA8	MUTDA7	MUTDA6	MUTDA5	MUTDA4	MUTDA3	MUTDA2	MUTDA1
69	45	ZERO8	ZERO7	ZERO6	ZERO5	ZERO4	ZERO3	ZERO2	ZERO1
70	46	ATMDDA	ATSPDA	DEMP1	DEMP0	AZRO2	AZRO1	AZRO0	ZREV
71	47	ATDA07	ATDA06	ATDA05	ATDA04	ATDA03	ATDA02	ATDA01	ATDA00
72	48	ATDA17	ATDA16	ATDA15	ATDA14	ATDA13	ATDA12	ATDA11	ATDA10
73	49	ATDA27	ATDA26	ATDA25	ATDA24	ATDA23	ATDA22	ATDA21	ATDA20
74	4A	ATDA37	ATDA36	ATDA35	ATDA34	ATDA33	ATDA32	ATDA31	ATDA30
75	4B	ATDA47	ATDA46	ATDA45	ATDA44	ATDA43	ATDA42	ATDA41	ATDA40
76	4C	ATDA57	ATDA56	ATDA55	ATDA54	ATDA53	ATDA52	ATDA51	ATDA50
77	4D	ATDA67	ATDA66	ATDA65	ATDA64	ATDA63	ATDA62	ATDA61	ATDA60
78	4E	ATDA77	ATDA76	ATDA75	ATDA74	ATDA73	ATDA72	ATDA71	ATDA70
79	4F	ATDA87	ATDA86	ATDA85	ATDA84	ATDA83	ATDA82	ATDA81	ATDA80
80	50	—	—	—	—	—	—	SRAD1	SRAD0
81	51	—	MSAD2	MSAD1	MSAD0	—	FMTAD2	FMTAD1	FMTAD0
82	52	—	PSVAD2	PSVAD1	PSVAD0	—	BYP2	BYP1	BYP0
83	53	—	—	SEAD6	SEAD5	SEAD4	SEAD3	SEAD2	SEAD1
84	54	—	—	REVAD6	REVAD5	REVAD4	REVAD3	REVAD2	REVAD1
85	55	—	—	MUTAD6	MUTAD5	MUTAD4	MUTAD3	MUTAD2	MUTAD1
86	56	—	—	OVF6	OVF5	OVF4	OVF3	OVF2	OVF1
87	57	ATMDAD	ATSPAD	—	—	—	—	—	OVFP
88	58	ATAD07	ATAD06	ATAD05	ATAD04	ATAD03	ATAD02	ATAD01	ATAD00
89	59	ATAD17	ATAD16	ATAD15	ATAD14	ATAD13	ATAD12	ATAD11	ATAD10
90	5A	ATAD27	ATAD26	ATAD25	ATAD24	ATAD23	ATAD22	ATAD21	ATAD20
91	5B	ATAD37	ATAD36	ATAD35	ATAD34	ATAD33	ATAD32	ATAD31	ATAD30
92	5C	ATAD47	ATAD46	ATAD45	ATAD44	ATAD43	ATAD42	ATAD41	ATAD40
93	5D	ATAD57	ATAD56	ATAD55	ATAD54	ATAD53	ATAD52	ATAD51	ATAD50
94	5E	ATAD67	ATAD66	ATAD65	ATAD64	ATAD63	ATAD62	ATAD61	ATAD60

9.5.1 Control Register Definitions (Software Mode Only)

The PCM3168A device has many user-programmable functions that are accessed through control registers, and is programmed through the SPI or I^2C serial control port. Table 13 shows the available mode control functions along with reset default conditions and associated register address. Table 12 lists the register map.

Table 13. User-Programmable Mode Control Functions

FUNCTION	RESET DEFAULT	REGISTER	LABEL
Mode control register reset for ADC and DAC operation	Normal operation	64	MRST
System reset for ADC and DAC operation	Normal operation	64	SRST
DAC sampling mode selection	Auto	64	SRDA[1:0]
DAC power-save mode selection	Power save	65	PSMDA
DAC master/slave mode selection	Slave	65	MSDA[2:0]
DAC audio interface format selection	I^2S	65	FMTDA[3:0]
DAC operation control	Normal operation	66	OPEDA[3:0]
DAC digital filter roll-off control	Sharp roll-off	66	FLT[3:0]
DAC output phase selection	Normal	67	REVDA[8:1]
DAC soft mute control	Mute disabled	68	MUTDA[8:1]
DAC zero flag	Not detected	69	ZERO[8:1]
DAC digital attenuation mode	Channel independent	70	ATMDDA
DAC digital attenuation speed	$N \times 2048/f_S$	70	ATSPDA
DAC digital de-emphasis function control	Disabled	70	DEMP[1:0]
DAC zero flag function selection	Independent	70	AZRO[2:0]
DAC zero flag polarity selection	High for detection	70	ZREV
DAC digital attenuation level shifting	0 dB, no attenuation	71–79	ATDAx[7:0]
ADC sampling mode selection	Auto	80	SRAD[1:0]
ADC master/slave mode selection	Slave	81	MSAD[2:0]
ADC audio interface format selection	I^2S	81	FMTAD[2:0]
ADC power-save control	Normal operation	82	PSVAD[2:0]
ADC HPF bypass control	Normal output, HPF enabled	82	BYP[2:0]
ADC input configuration control	Differential	83	SEAD[6:1]
ADC input phase selection	Normal	84	REVAD[6:1]
ADC soft mute control	Mute disabled	85	MUTAD[6:1]
ADC overflow flag	Not detected	86	OVF[6:1]
ADC digital attenuation mode	Channel independent	87	ATMDAD
ADC digital attenuation speed	$N \times 2048/f_S$	87	ATSPAD
ADC overflow flag polarity selection	High for detection	87	OVFP
ADC digital attenuation level setting	0 dB, no gain or attenuation	88–94	ATADx[7:0]

9.5.2 Register Definitions

Table 14. Register: Reset Control

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
64	40	MRST	SRST	—	—	—	—	SRDA1	SRDA0

MRST	**Mode control register reset for the ADC and DAC**	
	This bit sets the mode control register reset to the default value. Pop-noise may be generated. Returning the MRST bit to 1 is unneccesary, because it is automatically set to 1 after the mode control register is reset.	
	Default value = 1.	
	MRST	**Mode control register reset**
	0	Set default value
	1	Normal operation (default)
SRST	**System reset for the ADC and DAC**	
	This bit controls system reset, the relation between system clock and sampling clock re-synchronization, and ADC operation and DAC operation restart. The mode control register is not reset and the PCM3168A device does not go into a power-down state. The fade-in sequence is supported in the resume process, but pop-noise may be generated. Returning the SRST bit to 1 is unneccesary; it is automatically set to 1 after triggering a system reset.	
	Default value = 1.	
	SRST	**System reset**
	0	Resynchronization
	1	Normal operation (default)
SRDA[1:0]	**DAC Sampling mode select**	
	These bits control the sampling mode of DAC operation. In Auto mode, the sampling mode is automatically set according to multiples between the system clock and sampling clock, single rate for 512 f_S and 768 f_S, dual rate for 256 f_S or 384 f_S, and quad rate for 128 f_S and 192 f_S.	
	Default value = 00.	
	SRDA	**DAC Sampling mode select**
	00	Auto (default)
	01	Single rate
	10	Dual rate
	11	Quad rate

Table 15. Register: DAC Control 1

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
65	41	PSMDA	MSDA2	MSDA1	MSDA0	FMTDA3	FMTDA2	FMTDA1	FMTDA0

PSMDA	**DAC Power-save mode select**	
	This bit selects the power-save mode for the OPEDA[3:0] function. OPEDA[3:0] is the control of power-save mode and normal operation for PSMDA = 0, or OPEDA[3:0] works as the control of DAC disable (not power-save mode) and normal operation for PSMDA = 1.	
	Default value: 0.	
	PSMDA	**DAC Power-save mode select**
	0	Power-save enable mode (default)
	1	Power-save disable mode
MSDA[2:0]	**DAC Master/slave mode select**	
	These bits control the audio interface mode for DAC operation.	
	Default value: 000 (slave mode).	
	MSDA	**DAC Master/slave mode select**
	000	Slave mode (default)
	001	Master mode, 768 f_S
	010	Master mode, 512 f_S
	011	Master mode, 384 f_S
	100	Master mode, 256 f_S
	101	Master mode, 192 f_S
	110	Master mode, 128 f_S
	111	Reserved
FMTDA[3:0]	**DAC Audio interface format select**	
	These bits control the audio interface format for DAC operation. Details of the format, and any related restrictions with the system clock and master/slave mode, are described in *Audio Data Interface Formats and Timing*.	
	Default value: 0000 (24-bit I^2S format).	
	FMTDA	**DAC Audio interface format select**
	0000	24-bit I^2S format (default)
	0001	24-bit left-justified format
	0010	24-bit right-justified format
	0011	16-bit right-justified format
	0100	24-bit I^2S mode DSP format
	0101	24-bit left-justified mode DSP format
	0110	24-bit I^2S mode TDM format
	0111	24-bit left-justified mode TDM format
	1000	24-bit high-speed I^2S mode TDM format
	1001	24-bit high-speed left-justified mode TDM format
	101x	Reserved
	11xx	Reserved

Table 16. Register: DAC Control 2

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
66	42	OPEDA3	OPEDA2	OPEDA1	OPEDA0	FLT3	FLT2	FLT1	FLT0

OPEDA[3:0]	**DAC Operation control**	
	These bits control the DAC operation mode. In operation disable mode, the DAC output is cut off from DIN with a fade-out sequence, and the internal DAC data is reset. DAC output is forced into VCOMDA if PSMDA = 1, or DAC output is forced into AGNDDA and goes into a power-down state if PSMDA = 0. For normal operating mode, a fade-in sequence is applied on the DAC output in resume process. The serial mode control is effective during operation disable mode. A wait time greater than $t_{DACDLY2}$ is required for the status change because of power-save control turning on/off.	
	Default value: 0000.	
	OPEDA	**DAC Operation control**
	xxx0	DAC1/2 normal operation
	xxx1	DAC1/2 operation disable with or without power save
	xx0x	DAC3/4 normal operation
	xx1x	DAC3/4 operation disable with or without power save
	x0xx	DAC5/6 normal operation
	x1xx	DAC5/6 operation disable with or without power save
	0xxx	DAC7/8 normal operation
	1xxx	DAC7/8 operation disable with or without power save
FLT[3:0]	**DAC Digital filter roll-off control**	
	The FLT[3:0] bits allow users to select the digital filter roll-off that is best suited to their applications. Sharp and Slow filter roll-off selections are available. The filter responses for these selections are shown in *Typical Characteristics*.	
	Default value: 0000.	
	FLT	**DAC Digital filter roll-off control**
	xxx0	DAC1/2 sharp roll-off
	xxx1	DAC1/2 slow roll-off
	xx0x	DAC3/4 sharp roll-off
	xx1x	DAC3/4 slow roll-off
	x0xx	DAC5/6 sharp roll-off
	x1xx	DAC5/6 slow roll-off
	0xxx	DAC7/8 sharp roll-off
	1xxx	DAC7/8 slow roll-off

Table 17. Register: DAC Output Phase

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
67	43	REVDA8	REVDA7	REVDA6	REVDA5	REVDA4	REVDA3	REVDA2	REVDA1

REVDA[8:1]	**DAC Output phase select**	
	The REVDA[8:1] bits are used to control the phase of DAC analog signal outputs.	
	Default value: 0000 0000.	
	REVDA	**DAC Output phase select3**
	xxxx xxx0	DAC1 normal output
	xxxx xxx1	DAC1 inverted output
	xxxx xx0x	DAC2 normal output
	xxxx xx1x	DAC2 inverted output
	xxxx x0xx	DAC3 normal output
	xxxx x1xx	DAC3 inverted output
	xxxx 0xxx	DAC4 normal output
	xxxx 1xxx	DAC4 inverted output
	xxx0 xxxx	DAC5 normal output
	xxx1 xxxx	DAC5 inverted output
	xx0x xxxx	DAC6 normal output
	xx1x xxxx	DAC6 inverted output
	x0xx xxxx	DAC7 normal output
	x1xx xxxx	DAC7 inverted output
	0xxx xxxx	DAC8 normal output
	1xxx xxxx	DAC8 inverted output

Table 18. Register: DAC Soft Mute Control

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
68	44	MUTDA8	MUTDA7	MUTDA6	MUTDA5	MUTDA4	MUTDA3	MUTDA2	MUTDA1

MUTDA[8:1]	**DAC Soft Mute control**	
	These bits are used to enable or disable the Soft Mute function for the corresponding DAC outputs, VOUT. The Soft Mute function is incorporated into the digital attenuators. When Mute is disabled (MUTDA[8:1] = 0), the attenuator and DAC operate normally. When Mute is enabled by setting MUTDA[8:1] = 1, the digital attenuator for the corresponding output decreases from the current setting to infinite attenuation with an s-curve response and time set by ATSPDA. By setting MUTDA[8:1] = 0, the attenuator increases to the last attenuation level with s-curve response in the same manner as it is for decreasing levels. This configuration provides *pop and zipper noise-free* muting of the DAC output. The Soft Mute control uses the same digital attenuation level resource setting as the DAC. Mute control has priority over the digital attenuation level setting.	
	Default value: 0000 0000.	
	MUTDA	**DAC Soft Mute control**
	xxxx xxx0	DAC1 Mute disabled
	xxxx xxx1	DAC1 Mute enabled
	xxxx xx0x	DAC2 Mute disabled
	xxxx xx1x	DAC2 Mute enabled
	xxxx x0xx	DAC3 Mute disabled
	xxxx x1xx	DAC3 Mute enabled
	xxxx 0xxx	DAC4 Mute disabled
	xxxx 1xxx	DAC4 Mute enabled
	xxx0 xxxx	DAC5 Mute disabled
	xxx1 xxxx	DAC5 Mute enabled
	xx0x xxxx	DAC6 Mute disabled
	xx1x xxxx	DAC6 Mute enabled
	x0xx xxxx	DAC7 Mute disabled
	x1xx xxxx	DAC7 Mute enabled
	0xxx xxxx	DAC8 Mute disabled
	1xxx xxxx	DAC8 Mute enabled

Table 19. Register: DAC Zero Flag

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
69	45	ZERO8	ZERO7	ZERO6	ZERO5	ZERO4	ZERO3	ZERO2	ZERO1

ZERO[8:1]	**DAC Zero flag (read-only)**	
	These bits indicate the present status of the zero detect circuit for each DAC channel; these bits are read-only.	
	ZERO	**DAC Zero flag**
	xxxx xxx0	DAC1 zero input not detected
	xxxx xxx1	DAC1 zero input detected
	xxxx xx0x	DAC2 zero input not detected
	xxxx xx1x	DAC2 zero input detected
	xxxx x0xx	DAC3 zero input not detected
	xxxx x1xx	DAC3 zero input detected
	xxxx 0xxx	DAC4 zero input not detected
	xxxx 1xxx	DAC4 zero input detected
	xxx0 xxxx	DAC5 zero input not detected
	xxx1 xxxx	DAC5 zero input detected
	xx0x xxxx	DAC6 zero input not detected
	xx1x xxxx	DAC6 zero input detected
	x0xx xxxx	DAC7 zero input not detected
	x1xx xxxx	DAC7 zero input detected
	0xxx xxxx	DAC8 zero input not detected
	1xxx xxxx	DAC8 zero input detected

Table 20. Register: DAC Control 3

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
70	46	ATMDDA	ATSPDA	DEMP1	DEMP0	AZRO2	AZRO1	AZRO0	ZREV

ATMDDA	**DAC Attenuation mode**	
	This bit controls the DAC attenuation mode. ATDA1[7:0] to ATDA8[7:0] are simply used for ATMDDA = 0, and ATDA0[7:0] + ATDA1[7:0] to ATDA0[7:0] + ATDA8[7:0] in decibel number are used for ATMDDA = 1.	
	Default value: 0.	
	ATMDDA	**DAC Attenuation mode**
	0	Each channel with independent data (default)
	1	All channels with preset (independent) data + master (common) data in decibel number
ATSPDA	**DAC Attenuation speed**	
	This bit controls the DAC attenuation speed. N × 2048/f_S for ATSPDA = 0 and N × 4096/f_S for ATSPDA = 1. N is automatically selected according to the DAC sampling mode, SRDA, N = 1 for single rate, N = 2 for dual rate, and N = 4 for quad rate.	
	Default value: 0.	
	ATSPDA	**DAC Attenuation speed**
	0	N × 2048/f_S (default)
	1	N × 4096/f_S
DEMP[1:0]	**DAC Digital de-emphasis function/sampling rate control**	
	These bits are used to control the enable/disable and sampling frequency of the digital de-emphasis function.	
	Default value: 00.	
	DEMP	**DAC Digital de-emphasis function/sampling rate control**
	00	Disable (default)
	01	48 kHz enable
	10	44.1 kHz enable
	11	32 kHz enable
AZRO[2:0]	**DAC Zero flag function select**	
	The AZRO[2:0] bits are used to select the function of the zero flag pin.	
	Default value: 000.	
	AZRO	**DAC Zero flag function select**
	000	DAC1/2/3/4/5/6/7/8 (8 channel) zero input detect with AND logic (default)
	001	DAC1/2/3/4/5/6/7/8 (8 channel) zero input detect with OR logic
	010	DAC1/2/3/4/5/6 (6 channel) zero input detect with AND logic
	011	DAC1/2/3/4/5/6 (6 channel) zero input detect with OR logic
	100	DAC7/8 (2 channel) zero input detect with AND logic
	101	DAC7/8 (2 channel) zero input detect with OR logic
	11x	Reserved
ZREV	**DAC Zero flag polarity select**	
	This bit controls the polarity of the zero flag pin.	
	Default value: 0.	
	ZREV	**DAC Zero flag polarity select**
	0	High for zero detect (default)
	1	Low for zero detect

Table 21. Register: DAC Attenuation

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
71	47	ATDA07	ATDA06	ATDA05	ATDA04	ATDA03	ATDA02	ATDA01	ATDA00
72	48	ATDA17	ATDA16	ATDA15	ATDA14	ATDA13	ATDA12	ATDA11	ATDA10
73	49	ATDA27	ATDA26	ATDA25	ATDA24	ATDA23	ATDA22	ATDA21	ATDA20
74	4A	ATDA37	ATDA36	ATDA35	ATDA34	ATDA33	ATDA32	ATDA31	ATDA30
75	4B	ATDA47	ATDA46	ATDA45	ATDA44	ATDA43	ATDA42	ATDA41	ATDA40
76	4C	ATDA57	ATDA56	ATDA55	ATDA54	ATDA53	ATDA52	ATDA51	ATDA50
77	4D	ATDA67	ATDA66	ATDA65	ATDA64	ATDA63	ATDA62	ATDA61	ATDA60
78	4E	ATDA77	ATDA76	ATDA75	ATDA74	ATDA73	ATDA72	ATDA71	ATDA70
79	4F	ATDA87	ATDA86	ATDA85	ATDA84	ATDA83	ATDA82	ATDA81	ATDA80

ATDAx[7:0]	**DAC Digital attenuation level setting**		
	Where x = 0 and 1 to 8, corresponding to the DAC channel, DACx (x = 1 to 8).		
	Each DAC channel (VOUTx) has a digital attenuator function. The attenuation level can be set from 0 dB to –100 dB in 0.5-dB steps, and also can be set to infinite attenuation (mute). The attenuation level change from current value to target value is performed by incrementing or decrementing with s-curve responses and a time set by ATSPDA. While an attenuation level change sequence is in progress, new processing of the attenuation level change for new commands are ignored; any new commands are overwritten into the command buffer. The last command for the attenuation level change is performed after the present attenuation level change sequence is finished.		
	The attenuation level for each channel can be set individually using the following formula; the table below shows attenuation levels for various settings.		
	Attenuation level (dB) = 0.5 × (ATDAx[7:0]DEC – 255), where ATDAx[7:0]DEC = 0 through 255 for ATDAx[7:0]DEC = 0 through 54, attenuation is set to infinite attenuation (Mute).		
	ATDA0[7:0] are used to control all channels at the same time with attenuation data of ATDA0[7:0] + ATDAx[7:0] in decibel number, when ATMDDA is set to 1. This scheme provides preset and master volume operation.		
	Default value: 1111 1111.		
	ATDAx	**Decimal value**	**Attenuation level setting**
	1111 1111	255	0 dB, no attenuation (default)
	1111 1110	254	–0.5 dB
	1111 1101	253	–1.0 dB
	...	...	...
	1000 0001	129	–63.0 dB
	1000 0000	128	–63.5 dB
	0111 1111	127	–64 dB
	...	...	...
	0011 1000	56	–99.5 dB
	0011 0111	55	–100 dB
	0011 0110	54	Mute
	...	...	...
	0000 0000	0	Mute

Table 22. Register: ADC Sampling Mode

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
80	50	—	—	—	—	—	—	SRAD1	SRAD0

SRAD[1:0]	**ADC Sampling mode select**	
	These bits control the sampling mode of ADC operation. In Auto mode, the sampling mode is automatically set according to multiples between system clock and sampling clock, single rate for 512 f_S and 768 f_S, and dual rate for 256 f_S and 384 fS.	
	Default value: 00.	
	SRAD	**ADC Sampling mode select**
	00	Auto (default)
	01	Single rate
	10	Dual rate
	11	Reserved

Table 23. Register: ADC Control 1

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
81	51	—	MSAD2	MSAD1	MSAD0	—	FMTAD2	FMTAD1	FMTAD0

MSAD[2:0]	**ADC Master/slave mode select**	
	These bits control the audio interface mode for ADC operation.	
	Default value: 000 (slave mode).	
	MSAD	**ADC Master/slave mode select**
	000	Slave mode (default)
	001	Master mode, 768 f_S
	010	Master mode, 512 f_S
	011	Master mode, 384 f_S
	100	Master mode, 256 f_S
	101	Reserved
	110	Reserved
	111	Reserved
FMTAD[2:0]	**ADC Audio interface format select**	
	These bits control the audio interface format for ADC operation. The format details and restrictions related to the system clock and master/slave mode are described in *Audio Data Interface Formats and Timing*.	
	Default value: 000 (24-bit I^2S format).	
	FMTAD	**ADC Audio interface format select**
	000	24-bit I^2S format (default)
	001	24-bit left-justified format
	010	24-bit right-justified format
	011	16-bit right-justified format
	100	24-bit I^2S mode DSP format
	101	24-bit left-justified mode DSP format
	110	24-bit I^2S mode TDM format
	111	24-bit left-justified mode TDM format

Table 24. Register: ADC Control 2

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
82	52	—	PSVAD2	PSVAD1	PSVAD0	—	BYP2	BYP1	BYP0

PSVAD[2:0]	**ADC Power-save control**	
	These bits control the ADC power-save mode. In power-save mode, DOUT is forced into ZERO with a fade-out sequence, the internal ADC data are reset, and the ADC goes into a power-down state. For power-save mode release, a fade-in sequence is applied on DOUT in resume process. The serial mode control is enabled during this mode. Wait times greater than $t_{ADCDLY2}$ are required for the status change because of the power-save control turning on/off.	
	Default value: 000.	
	PSVAD	**ADC Power-save control**
	xx0	ADC1/2 normal operation
	xx1	ADC1/2 power-save mode
	x0x	ADC3/4 normal operation
	x1x	ADC3/4 power-save mode
	0xx	ADC5/6 normal operation
	1xx	ADC5/6 power-save mode
BYP[2:0]	**ADC HPF bypass control**	
	These bits control the HPF function and dc components of the input signal; internal dc offset is converted in bypass mode.	
	Default value: 000.	
	BYP	**ADC HPF bypass control**
	xx0	ADC1/2 normal output, HPF enabled
	xx1	ADC1/2 bypassed output, HPF disabled
	x0x	ADC3/4 normal output, HPF enabled
	x1x	ADC3/4 bypassed output, HPF disabled
	0xx	ADC5/6 normal output, HPF enabled
	1xx	ADC5/6 bypassed output, HPF disabled

Table 25. Register: ADC Input Configuration

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
83	53	—	—	SEAD6	SEAD5	SEAD4	SEAD3	SEAD2	SEAD1

SEAD[6:1]	**ADC Input configuration control**	
	These bits control the input configuration of each ADC channel, differential or single-ended.	
	Default value: 00 0000 (all ADC channels have differential inputs).	
	SEAD	**ADC Input configuration**
	xx xxx0	ADC1 differential input
	xx xxx1	ADC1 single-ended input
	xx xx0x	ADC2 differential input
	xx xx1x	ADC2 single-ended input
	xx x0xx	ADC3 differential input
	xx x1xx	ADC3 single-ended input
	xx 0xxx	ADC4 differential input
	xx 1xxx	ADC4 single-ended input
	x0 xxxx	ADC5 differential input
	x1 xxxx	ADC5 single-ended input
	0x xxxx	ADC6 differential input
	1x xxxx	ADC6 single-ended input

Table 26. Register: ADC Input Phase

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
84	54	—	—	REVAD6	REVAD5	REVAD4	REVAD3	REVAD2	REVAD1

REVAD[6:1]	**ADC Input phase select**	
	These bits are used to control the phase of analog signal inputs.	
	Default value: 00 0000.	
	REVAD	**ADC Input phase select**
	xx xxx0	ADC1 normal input
	xx xxx1	ADC1 inverted input
	xx xx0x	ADC2 normal input
	xx xx1x	ADC2 inverted input
	xx x0xx	ADC3 normal input
	xx x1xx	ADC3 inverted input
	xx 0xxx	ADC4 normal input
	xx 1xxx	ADC4 inverted input
	x0 xxxx	ADC5 normal input
	x1 xxxx	ADC5 inverted input
	0x xxxx	ADC6 normal input
	1x xxxx	ADC6 inverted input

Table 27. Register: ADC Soft Mute

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
85	55	—	—	MUTAD6	MUTAD5	MUTAD4	MUTAD3	MUTAD2	MUTAD1

MUTAD[6:1]	**ADC Soft Mute control**	
	These bits are used to enable or disable the Soft Mute function for the corresponding ADC outputs, DOUT. The Soft Mute function is incorporated into the digital attenuators. When Mute is disabled (MUTAD[6:1] = 0), the attenuator and ADC operate normally. When Mute is enabled by setting MUTAD[6:1] = 1, the digital attenuator for the corresponding output decreases from the current setting to infinite attenuation with an s-curve responses and time set by ATSPAD. By setting MUTAD[6:1] = 0, the attenuator increases to the last attenuation level with the s-curve response in same manner as for decreasing levels. This provides *pop and zipper noise-free* muting for the ADC input. The Soft Mute control uses the same digital attenuation level resource setting as the ADC. Mute control has priority over the digital attenuation level setting.	
	Default value: 00 0000.	
	MUTAD	**ADC Soft Mute control**
	xx xxx0	ADC1 Mute disabled
	xx xxx1	ADC1 Mute enabled
	xx xx0x	ADC2 Mute disabled
	xx xx1x	ADC2 Mute enabled
	xx x0xx	ADC3 Mute disabled
	xx x1xx	ADC3 Mute enabled
	xx 0xxx	ADC4 Mute disabled
	xx 1xxx	ADC4 Mute enabled
	x0 xxxx	ADC5 Mute disabled
	x1 xxxx	ADC5 Mute enabled
	0x xxxx	ADC6 Mute disabled
	1x xxxx	ADC6 Mute enabled

Table 28. Register: ADC Overflow Flag

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
86	56	—	—	OVF6	OVF5	OVF4	OVF3	OVF2	OVF1

OVF[6:1]	**ADC Overflow flag (read-only)**	
	These bits indicate the status information of an overflow detect circuit for each ADC channel; these bits are read only. 1 means an overflow has been detected in the past, and reading this register resets all OVF bits.	
	OVF	**ADC Overflow flag**
	xx xxx0	ADC1 overflow input not detected
	xx xxx1	ADC1 overflow input detected
	xx xx0x	ADC2 overflow input not detected
	xx xx1x	ADC2 overflow input detected
	xx x0xx	ADC3 overflow input not detected
	xx x1xx	ADC3 overflow input detected
	xx 0xxx	ADC4 overflow input not detected
	xx 1xx3x	ADC4 overflow input detected
	x0 xxxx	ADC5 overflow input not detected
	x1 xxxx	ADC5 overflow input detected
	0x xxxx	ADC6 overflow input not detected
	1x xxxx	ADC6 overflow input detected

Table 29. Register: ADC Control 3

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
87	57	ATMDAD	ATSPAD	—	—	—	—	—	OVFP

ATMDAD	**ADC Attenuation mode**	
	This bit controls the ADC attenuation mode. ATAD1[7:0] to ATAD6[7:0] are simply used for ATMDAD = 0, and ATAD0[7:0] + ATAD1[7:0] to ATAD0[7:0] + ATAD6[7:0] in decibel number are used for ATMDAD = 1.	
	Default value: 0.	
	ATMDAD	**ADC Attenuation mode**
	0	Each channel with independent data (default)
	1	All channels with preset (independent) data + master (common) data in decibel number
ATSPAD	**ADC Attenuation speed**	
	This bit controls the ADC attenuation Speed, N × 2048/f_S for ATSPAD = 0 and N × 4096/f_S for ATSPAD = 1. N is automatically selected according to the ADC sampling mode, SRAD: N = 1 for single and N = 2 for dual rate.	
	Default value: 0.	
	ATSPAD	**ADC Attenuation speed**
	0	N × 2048/f_S (default)
	1	N × 4096/f_S
OVFP	**ADC Overflow flag polarity select**	
	This bit controls the polarity of the overflow flag pin.	
	Default value: 0.	
	OVFP	**ADC Overflow flag polarity select**
	0	High for overflow detect (default)
	1	Low for overflow detect

Table 30. Register: ADC Attenuation

DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0
88	58	ATAD07	ATAD06	ATAD05	ATAD04	ATAD03	ATAD02	ATAD01	ATAD00
89	59	ATAD17	ATAD16	ATAD15	ATAD14	ATAD13	ATAD12	ATAD11	ATAD10
90	5A	ATAD27	ATAD26	ATAD25	ATAD24	ATAD23	ATAD22	ATAD21	ATAD20
91	5B	ATAD37	ATAD36	ATAD35	ATAD34	ATAD33	ATAD32	ATAD31	ATAD30
92	5C	ATAD47	ATAD46	ATAD45	ATAD44	ATAD43	ATAD42	ATAD41	ATAD40
93	5D	ATAD57	ATAD56	ATAD55	ATAD54	ATAD53	ATAD52	ATAD51	ATAD50
94	5E	ATAD67	ATAD66	ATAD65	ATAD64	ATAD63	ATAD62	ATAD61	ATAD60

ATADx[7:0]	**ADC Digital attenuation level setting**		
	Where x = 0 and 1 to 6, corresponding to the ADC channel, ADCx (x = 1 to 6).		
	Each ADC channel has a digital attenuator function with 20-dB gain. The attenuation level can be set from 20 dB to –100 dB in 0.5-dB steps, and also can be set to infinite attenuation (mute). The attenuation level change from current value to target value is performed by increment or decrement with s-curve response and time set by ATSPAD. While the attenuation level change sequence is in progress, new processing of an attenuation level change for a new command is ignored; the new command is overwritten into the command buffer. The last command for an attenuation level change is performed after the present attenuation level change sequence is finished.		
	The attenuation level for each channel can be set individually using the following formula, and the above table shows attenuation levels for various settings.		
	Attenuation level (dB) = 0.5 × (ATADx[7:0]DEC – 215), where ATADx[7:0]DEC = 0 through 255 for ATADx[7:0]DEC = 0 through 14, attenuation is set to infinite attenuation (Mute).		
	ATAD0[7:0] is used to control all channels at the same time with attenuation data of ATAD0[7:0] + ATADx[7:0] in decibel number, though maximum level is limited within +20 dB, when ATMDAD is set to 1. This scheme provides preset and master volume operation.		
	Default value: 1101 0111.		
	ATADx	**Decimal value**	**Attenuation level setting**
	1111 1111	255	20.0 dB
	1111 1110	254	19.5 dB
	1111 1101	253	19.0 dB
	...	...	...
	1101 1000	216	0.5 dB
	1101 0111	215	0 dB, no attenuation (default)
	1101 0110	214	–0.5 dB
	...	...	...
	0001 0000	16	–99.5 dB
	0000 1111	15	–100.0 dB
	0000 1110	14	Mute
	...	...	...
	0000 0000	0	Mute

10 Application and Implementation

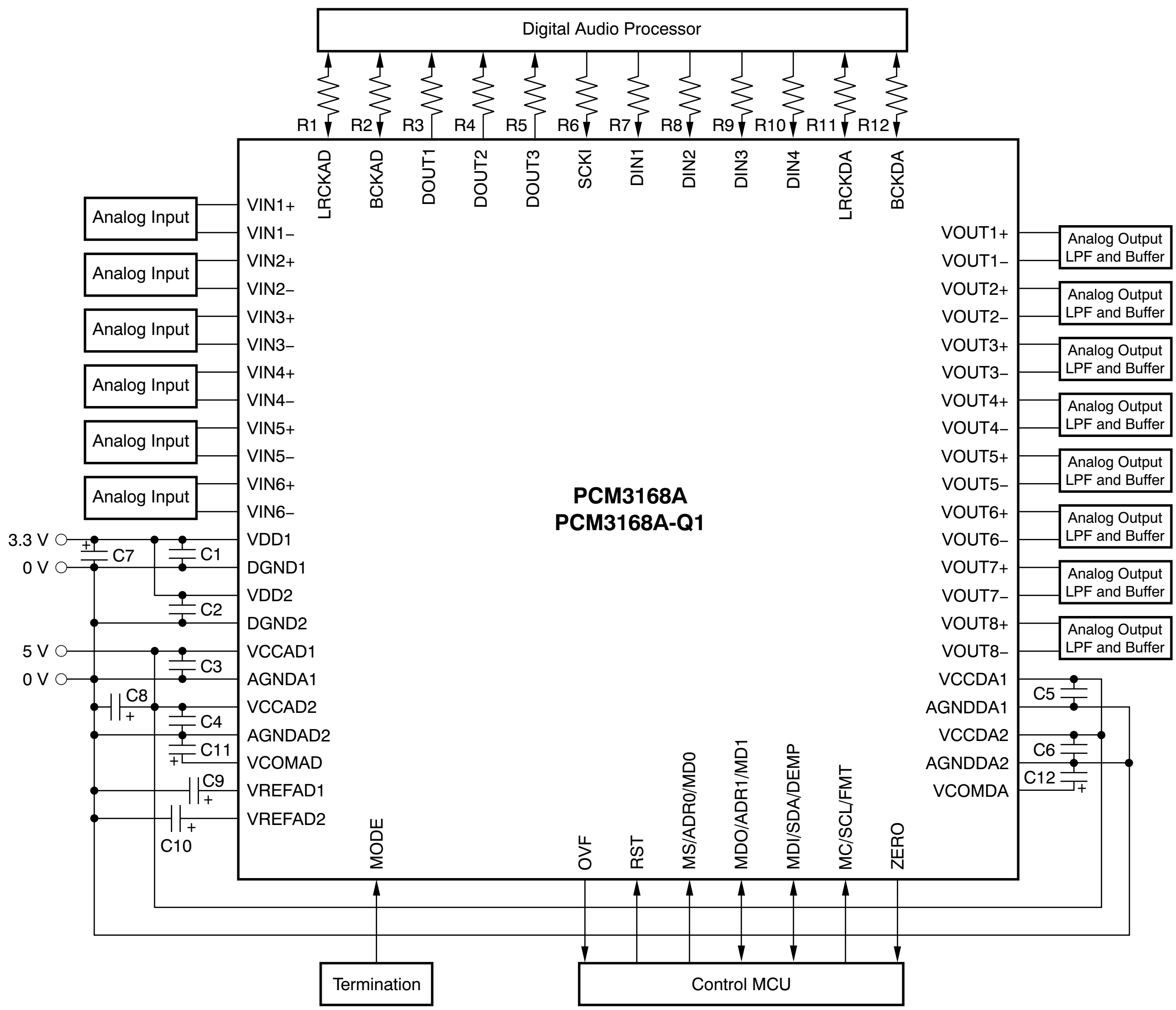
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

A typical circuit connection for six-channel analog in and eight-channel analog out is shown in Figure 54.

10.2 Typical Application



C_1 through C_6 are 1-µF ceramic capacitors dependent on power-supply quality. C_7 and C_8 are 10-µF electrolytic capacitors dependent on power-supply quality. C_9 and C_{10} are 10-µF electrolytic capacitors. C_{11} and C_{12} are 10-µF electrolytic capacitors. R_1 through R_{12} are 22-Ω to 100-Ω resistors.

Figure 54. Example Board Layout

Typical Application (continued)

10.2.1 Design Requirements

For this design example, use the parameters listed in Table 31.

Table 31. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Audio input	PCM audio, differential analog audio
Audio output	PCM audio, differential analog audio
Control	I2C, SPI

10.2.2 Detailed Design Procedure

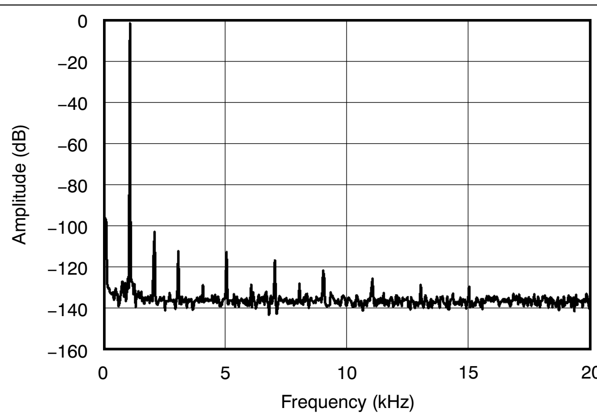
10.2.2.1 Analog Input and Output

It is recommended that input and output filters be used to condition the inputs and outputs. Input filters can be used to convert a single ended signal into a differential signal while also attenuating out of band noise. Another use of an input filter for the ADC it to reduce a 2-V_{RMS} signal to a 1-V_{RMS} input, which is the limit of the ADC input. Output filters can be used to go from differential to single ended, while reducing a differential signal that is 8 V_{PP} to a 2-V_{RMS} signal. The output filter can also attenuate out of band noise.

10.2.2.2 PCM Interface

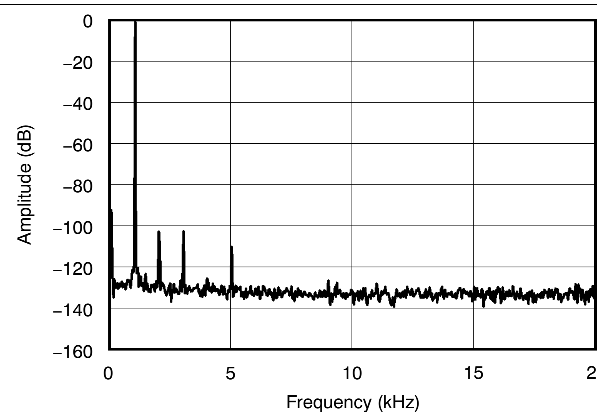
The PCM3168A has the capability of inputting 8 PCM channels over 4 data pins in normal PCM mode, or can operate in TDM mode to take in 8 channels on one data pin. The PCM3168A can also output up to 6 PCM channels over 3 data pins, or over 1 pin in TDM mode.

10.2.3 Application Curves



–1 dB, N = 32768

Figure 55. ADC Output Spectrum



0 dB, N = 32768

Figure 56. DAC Output Spectrum

10.3 System Examples

10.3.1 Typical Circuit Connections

Termination for mode control: Any one of the circuits shown in Figure 57 must be applied according to the necessary mode or configuration. Resistor value must be 220-kΩ, ±5% tolerant. The PowerPAD must be tied to the ground plane with enough electrical and thermal conductivity; see the example board layout in Figure 54.

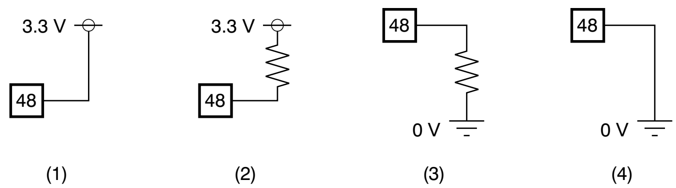
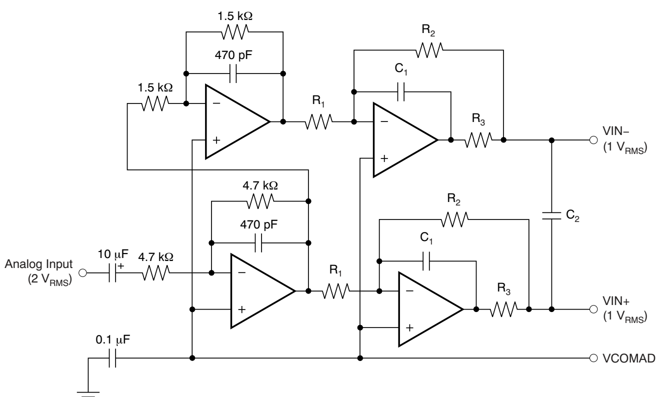


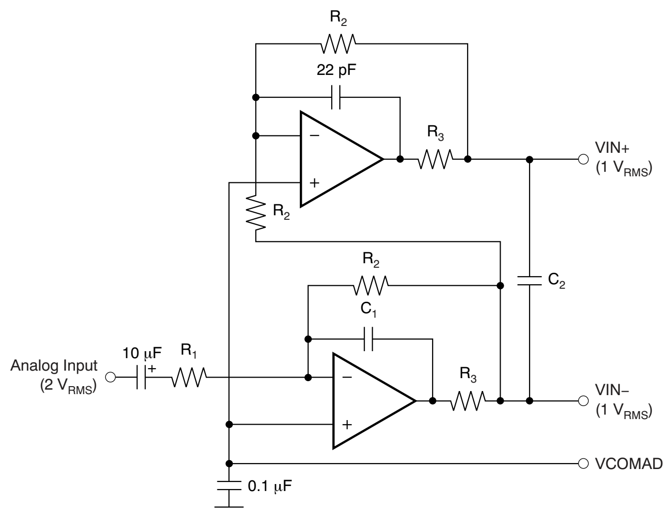
Figure 57. Typical Circuit Connections

Typical interface circuits for analog input and analog output are shown in Figure 58 through Figure 62.



Amplifier is an NE5532A x2 or OPA2134 x2; R_1 = 1.5-kΩ resistor; R_2 = 750-Ω resistor; R_3 = 47-Ω resistor; C_1 = 3300-pF capacitor; C_2 = 0.01-μF capacitor; Gain = 1; $f_{-3\ dB}$ = 45 kHz.

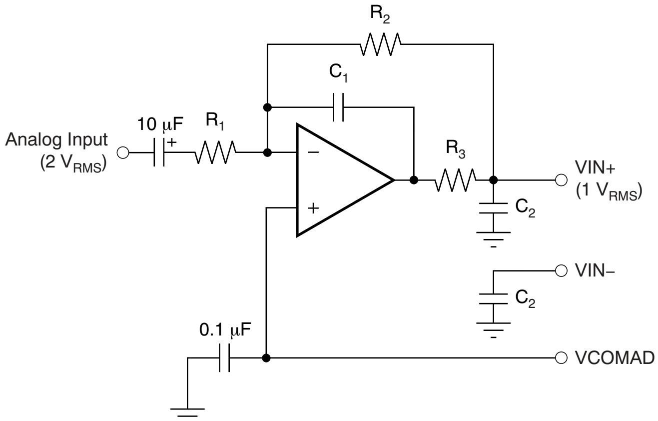
Figure 58. Single-Ended to Differential Buffer and Anti-Aliasing LPF For Differential ADC Input



Amplifier is an NE5532A x1 or OPA2134 x1; R_1 = 3-kΩ resistor; R_2 = 1.5-kΩ resistor; R_3 = 47-Ω resistor; C_1 = 2200-pF capacitor; C_2 = 0.01-μF capacitor; Gain = 1; $f_{-3\ dB}$ = 48 kHz.

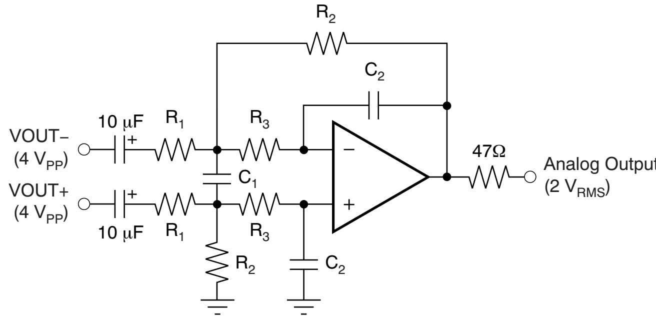
Figure 59. Single-Ended to Differential Buffer and Anti-Aliasing LPF For Differential ADC Input

System Examples (continued)



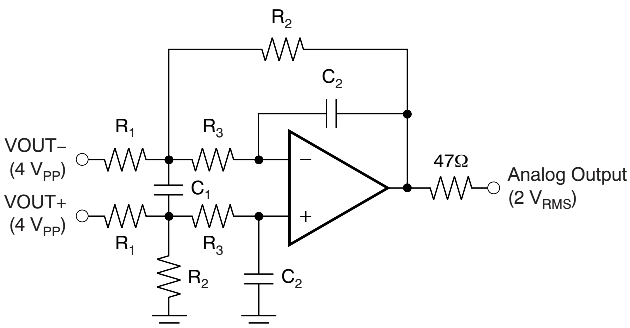
Amplifier is an NE5532A x1 or OPA2134 x1; R_1 = 3-kΩ resistor; R_2 = 1.5-kΩ resistor; R_3 = 47-Ω resistor; C_1 = 2200-pF capacitor; C_2 = 0.022-μF capacitor; Gain = 0.5; $f_{-3\ dB}$ = 48 kHz.

Figure 60. Buffer and Anti-Aliasing LPF for Single-Ended ADC Input



Amplifier is an NE5532A x1/2 or OPA2134 x1/2; R_1 = 7.5-kΩ resistor; R_2 = 5.6-kΩ resistor; R_3 = 360-Ω resistor; C_1 = 3300-pF capacitor; C_2 = 680-pF capacitor; Gain = 0.747; $f_{-3\ dB}$ = 53 kHz.

Figure 61. Post-LPF and Differential to Single-Ended Buffer for DAC Output (AC-Coupled)



Amplifier is an NE5532A x1/2 or OPA2134 x1/2; R_1 = 15-kΩ resistor; R_2 = 11-kΩ resistor; R_3 = 820-Ω resistor; C_1 = 1500-pF capacitor; C_2 = 330-pF capacitor; Gain = 0.733; $f_{-3\ dB}$ = 54 kHz.

Figure 62. Post-LPF and Differential to Single-Ended Buffer for DAC Output (DC-Coupled)

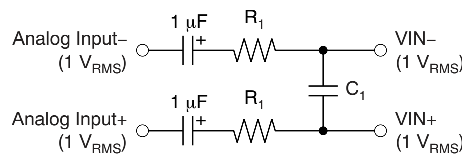


Figure 63. Basic Differential Input Circuit With Anti-Aliasing LPF for Differential ADC Input

11 Power Supply Recommendations

The PCM3168A requires a 5-V and 3.3-V nominal supply rail. The 3.3-V supply rail is needed for VDD1 and VDD2. The 5-V supply rail is needed for VCCAD1, VCCAD2, VCCDA1, and VCCDA2. The decoupling capacitors for the power supplies should be placed close to the device terminals.

12 Layout

12.1 Layout Guidelines

12.1.1 Power-Supply Pins (VCCAD1/2, VCCDA1/2, and VDD1/2)

The digital and analog power-supply pins of the PCM3168A device should be bypassed to the corresponding ground pins with 1-µF ceramic capacitors placed as close to the pins as possible. Each power-supply line (V_{CC} and V_{DD}) to the PCM3168A device should be bypassed to the corresponding ground pins with 10-µF electrolytic capacitors to maximize the dynamic performance of the ADC and DAC.

Although the PCM3168A device has two power lines to maximize the potential of dynamic performance, using one common source (for instance, a 5-V power supply for V_{CC} and a 3.3-V power supply for V_{DD} generated from one common source) is recommended to avoid unexpected power-supply trouble such as latch-up or incorrect power-supply conditions. Also, simultaneous power-on/off of V_{CC} and V_{DD} is recommended to avoid unexpected transient responses in outputs, though the power-supply sequence of V_{CC} and V_{DD} is not specified in the operation and absolute maximum ratings point of view.

12.1.2 Grounding (AGNDAD1/2, AGNDDA1/2, and DGND1/2)

To maximize the dynamic performance of the PCM3168A device, the analog and digital grounds are not connected internally. These pins should have very low impedances to avoid digital noise and signal components feeding back into the analog ground. All ground pins should be connected directly to each other under the part, and the device should be connected to the analog ground of the application, as with acceptable analog layout practices; this layout reduces the potential of noise problems.

12.1.3 VIN1±, VIN2±, VIN3±, VIN4±, VIN5±, and VIN6± Pins

In case of direct interface to VINx±, 1-µF electrolytic capacitors are recommended because the ac-coupling capacitor (which gives a 2-Hz HPF corner frequency and 47-Ω and 0.1-µF to 470-Ω and 0.001-µF differential LPF) is recommended as the anti-aliasing filter that gives a 160-kHz LPF corner frequency. If signal source impedance is not enough (too low) or input line length to the VINx± is not enough (too short), insertion of an analog front-end buffer (see Figure 58 to Figure 60) is recommended to maximize the dynamic performance. The voltage coefficient of the capacitor for an anti-aliasing filter should be considered to maximize the THD performance. A film-type capacitor is recommended; if a ceramic capacitor is used, a relatively higher voltage type is recommended.

There are three ways to terminate any unused input pins. First, terminate these pins to AGNDAD with 0.001-µF to 1-µF capacitors. This termination is applied on unused pins whose channels are configured in single-ended mode. The second form of termination is to connect the positive (+) pin and negative (–) pins together and terminating these to AGNDAD with 0.001-µF to 1-µF capacitors. This option applies to unused pins with channels that are configured in differential mode. The last termination method is to terminate the pins directly to VCOMAD; this option can be applied on unused pins with unused channels combined into two channels that are then configured in power-save mode.

12.1.4 VCOMAD and VCOMDA Pins

10-µF electrolytic capacitors are recommended between VCOMAD and AGNDAD, and VCOMDA and AGNDDA to ensure a low source impedance of ADC and DAC common voltages. These capacitors should be located as close to each pin as possible to reduce dynamic errors on the ADC and DAC common voltages.

12.1.5 VREFAD1/2 Pins

10-µF electrolytic capacitors are recommended between VREFAD1/2 and AGNDAD to ensure low source impedances of ADC references. These capacitors should be located as close to each pin as possible to reduce dynamic errors on ADC references.

Layout Guidelines (continued)

12.1.6 VOUT1±, VOU2±, VOUT3±, VOUT4±, VOUT5±, VOUT6±, VOUT7±, and VOUT8± Pins

The differential to single-ended buffer with post LPF can be directly connected (without capacitors) to these output pins (see Figure 62), thereby minimizing the use of coupling capacitors for the 2-V_{RMS} outputs. The op amp and resistors must be determined with consideration of degrading some performance through this differential to single-ended and LPF buffer; there is about 1.5-dB degradation seen in the examples of Figure 61 and Figure 62.

12.1.7 MODE Pin

This pin is a logic input with quad-state input capability. The MODE pin is high when connected to V_{DD}, low when connected to DGND, and pulled up or pulled down through an external resistor and for the two mid-states in order to distinguish the four input states. The pull-up or pull-down resistor must be 220 kΩ, ±5% in tolerance. Note that the state of the MODE pin is only sampled by a power-on or a low-to-high transition of the RST pin.

12.1.8 RST Pin

When the MODE pin setting changes to change the operating mode, the new mode setting does not take effect immediately; a RST pin toggle is required to make the new mode setting valid, and for the new mode to take effect.

12.1.9 OVF Pin

The OVF pin has two functions. It is primarily the flag for ADC overflow occurrence detection. It is also used to indicate that the internal reset sequence is complete and that the device is ready to enter serial mode control.

12.1.10 System Clock and Audio Interface Clocks

The quality of SCKI may influence dynamic performance, because the PCM3168A device (both the ADC and DAC) operates based on SCKI. Therefore, it may be required to consider the jitter, duty, and rise and fall time of the system clock.

In slave mode, the PCM3168A device does not require a specific timing relationship between BCKAD/LRCKAD and SCKI, and BCKDA/LRCKDA and SCKI; however, there is a possibility of performance degradation with a certain timing relationship between them. In that case, specific timing relationship control might resolve this performance degradation.

In master mode, there is a possibility of performance degradation because of heavy loads on BCKAD/LRCKAD, BCKDA/LRCKDA, and DOUT1/2/3. It is recommended to load these pins as lightly as possible. Note that all output clocks and signals go low; they do not go into a high-impedance state during power-save mode.

12.1.11 PowerPAD

The PowerPAD of the PCM3168A device is internally connected to the substrate of the silicon. It should be connected to the ground plane with sufficient low conductance in electrical and thermal; see Figure 54. The PowerPAD size is 7.25 mm x 7.00 mm (0.725 cm × 0.7 cm).

12.1.12 External Mute Control

For power-down ON/OFF control without the pop-noise that is generated by a DC level change on the DAC output, the external mute control is generally required. Use of the following control sequence is recommended: external mute ON, codec power-down ON, SCKI stop and resume if necessary, codec power-down OFF, and external mute OFF control.

12.2 Layout Example

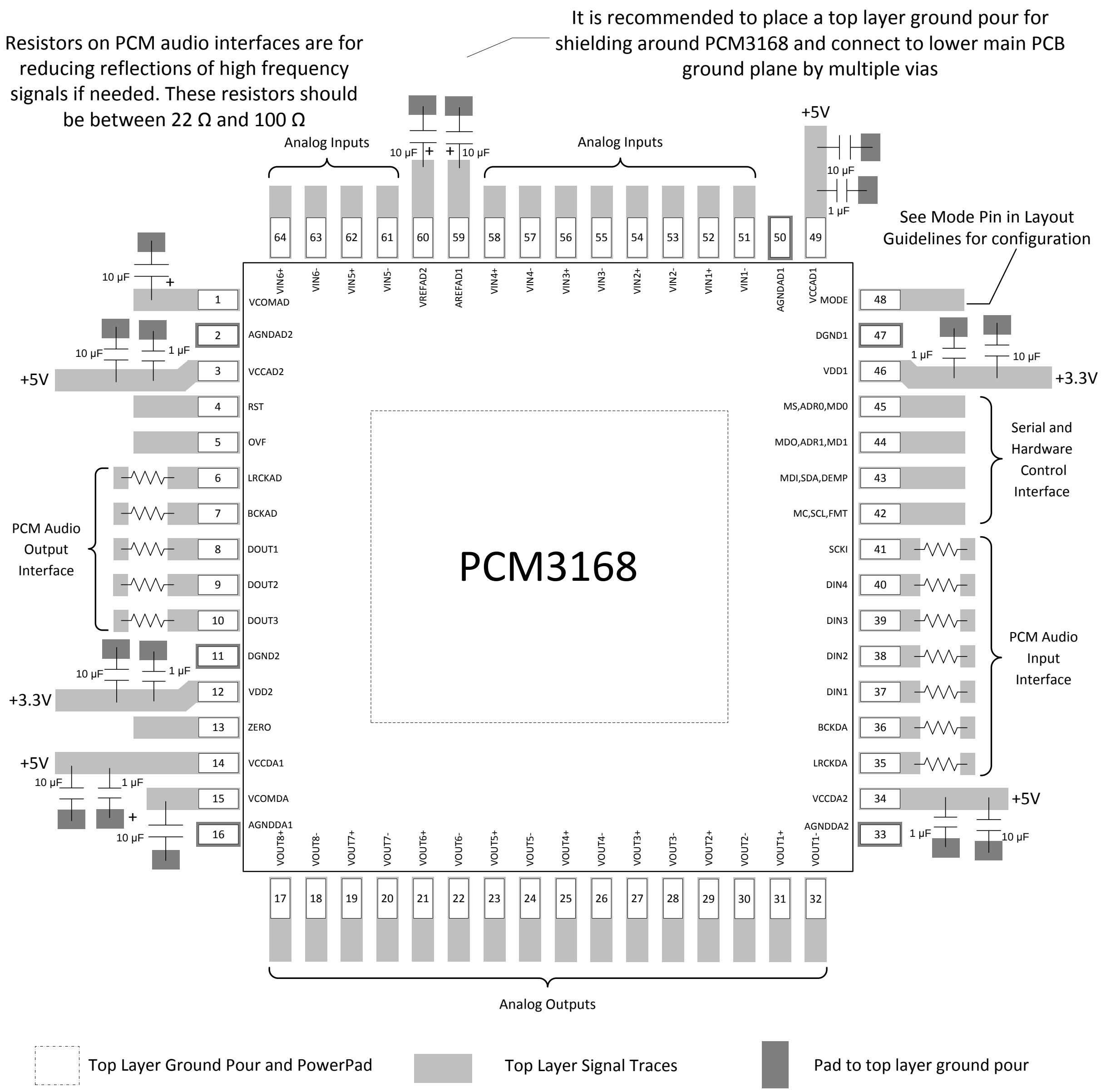


Figure 64. PCM3168A Board Layout

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation, refer to the following:

- *PCM3168PAP IBIS Model Analog & Mixed-Signal* (SLAC203)
- *PurePath™ Console Motherboard User's Guide* (SLOU366)

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
PowerPAD is a trademark of Texas Instruments Incorporated.
SPI is a trademark of Motorola.
I^2C, I^2S are trademarks of NXP Semiconductors.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM3168APAP	ACTIVE	HTQFP	PAP	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	PCM3168A	Samples
PCM3168APAPR	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	PCM3168A	Samples
PCM3168APAPRG4	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	PCM3168A	Samples
PCM3168ATPAPQ1	ACTIVE	HTQFP	PAP	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	PCM3168AQ1	Samples
PCM3168ATPAPRQ1	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	PCM3168AQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF PCM3168A, PCM3168A-Q1 :

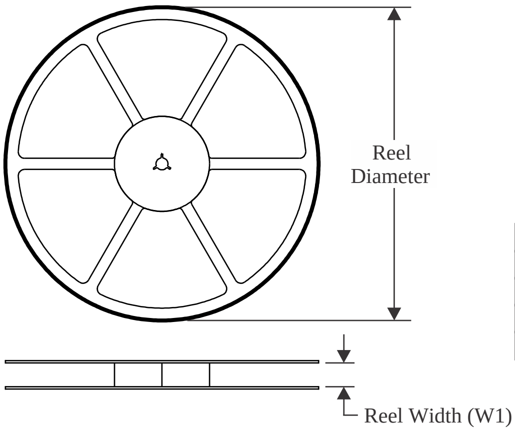
- Catalog: PCM3168A
- Automotive: PCM3168A-Q1

NOTE: Qualified Version Definitions:

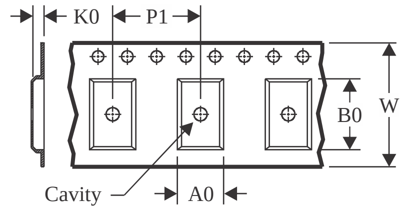
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

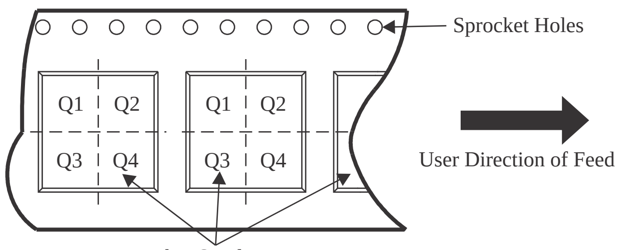


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

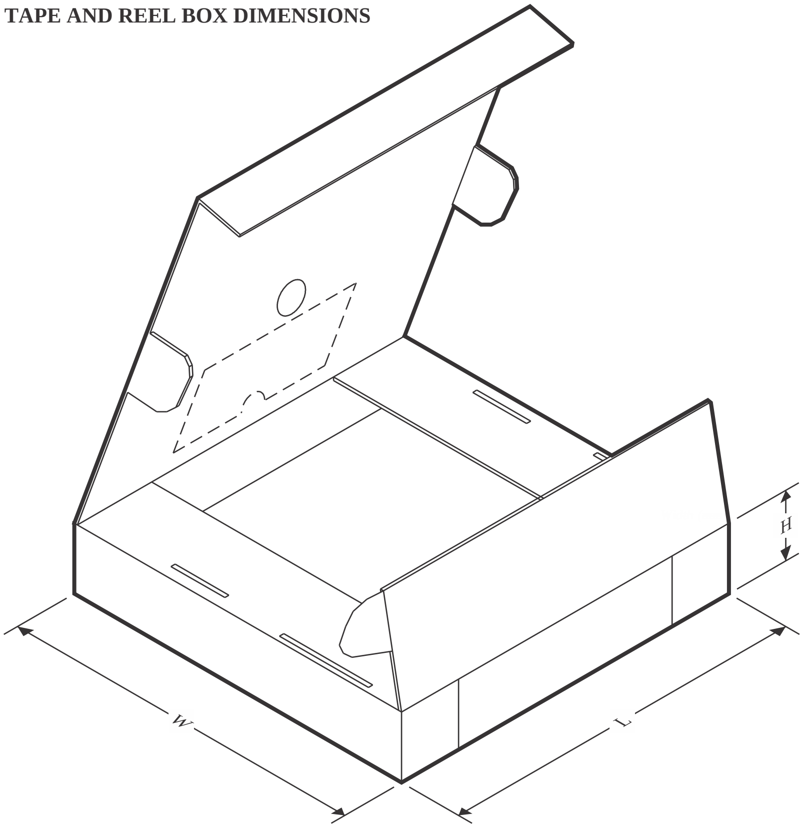
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM3168APAPR	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
PCM3168ATPAPRQ1	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

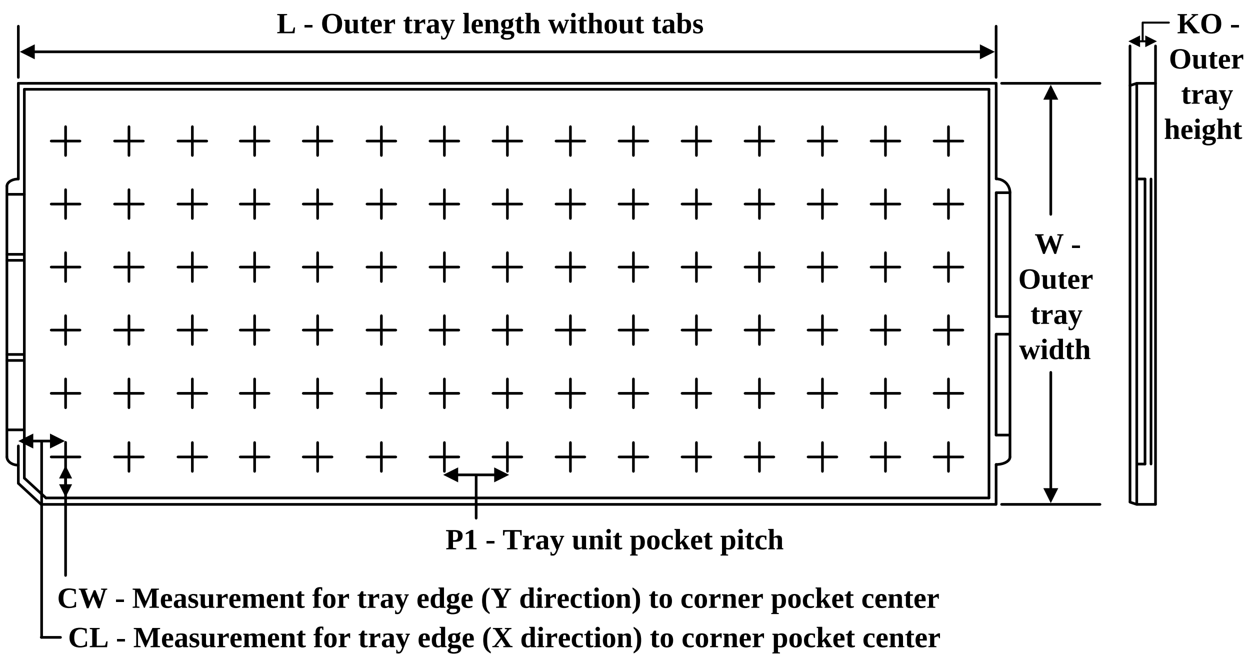
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM3168APAPR	HTQFP	PAP	64	1000	350.0	350.0	43.0
PCM3168ATPAPRQ1	HTQFP	PAP	64	1000	350.0	350.0	43.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
PCM3168APAP	PAP	HTQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
PCM3168ATPAPQ1	PAP	HTQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13

GENERIC PACKAGE VIEW

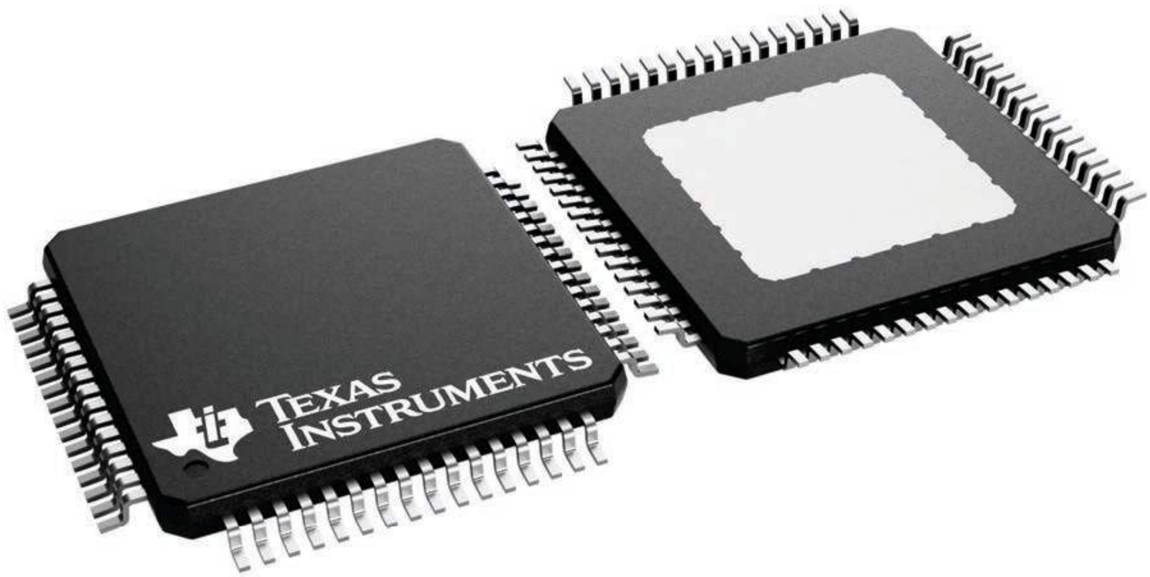
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

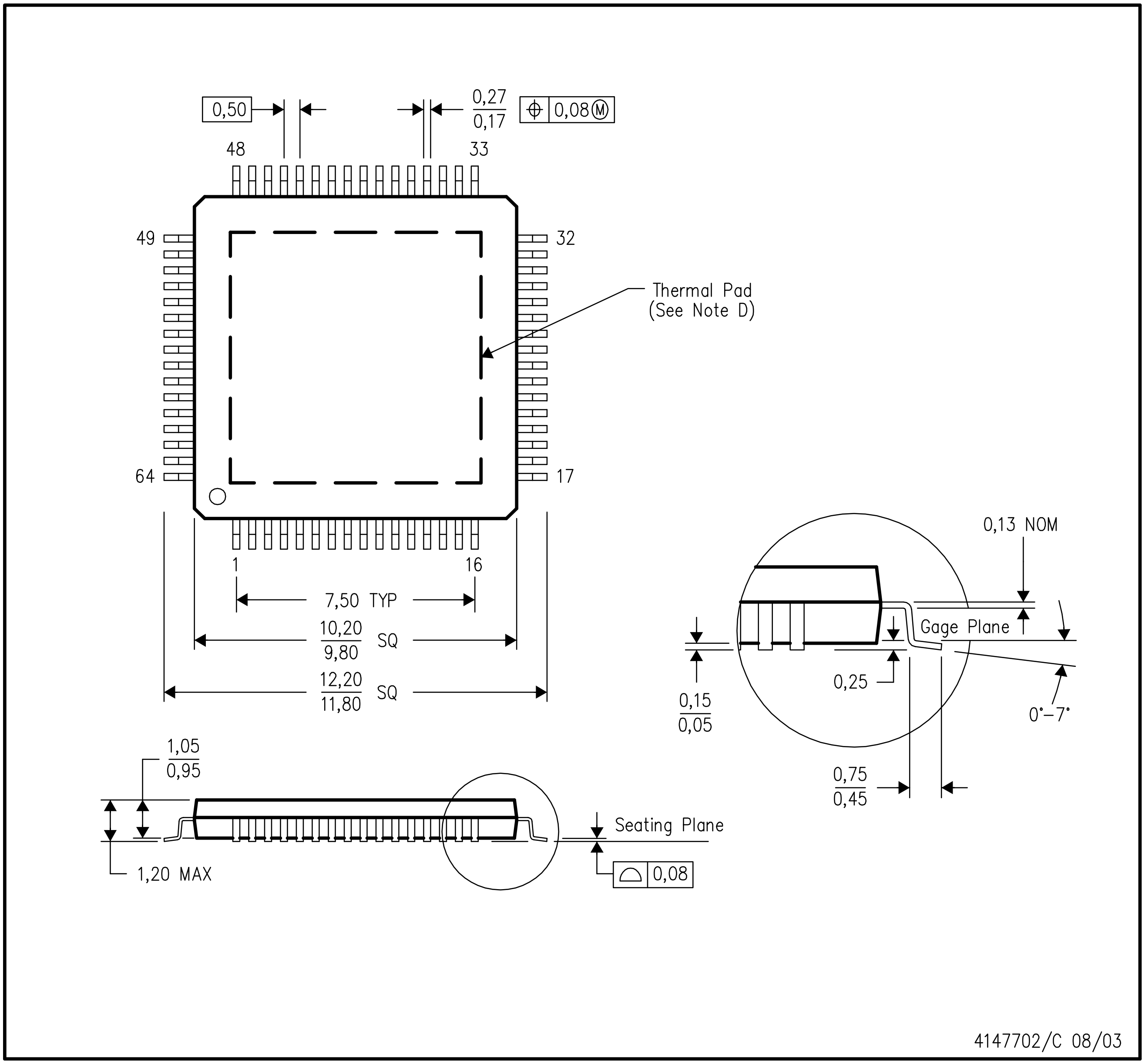
QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226442/A

PAP (S-PQFP-G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. Falls within JEDEC MS-026

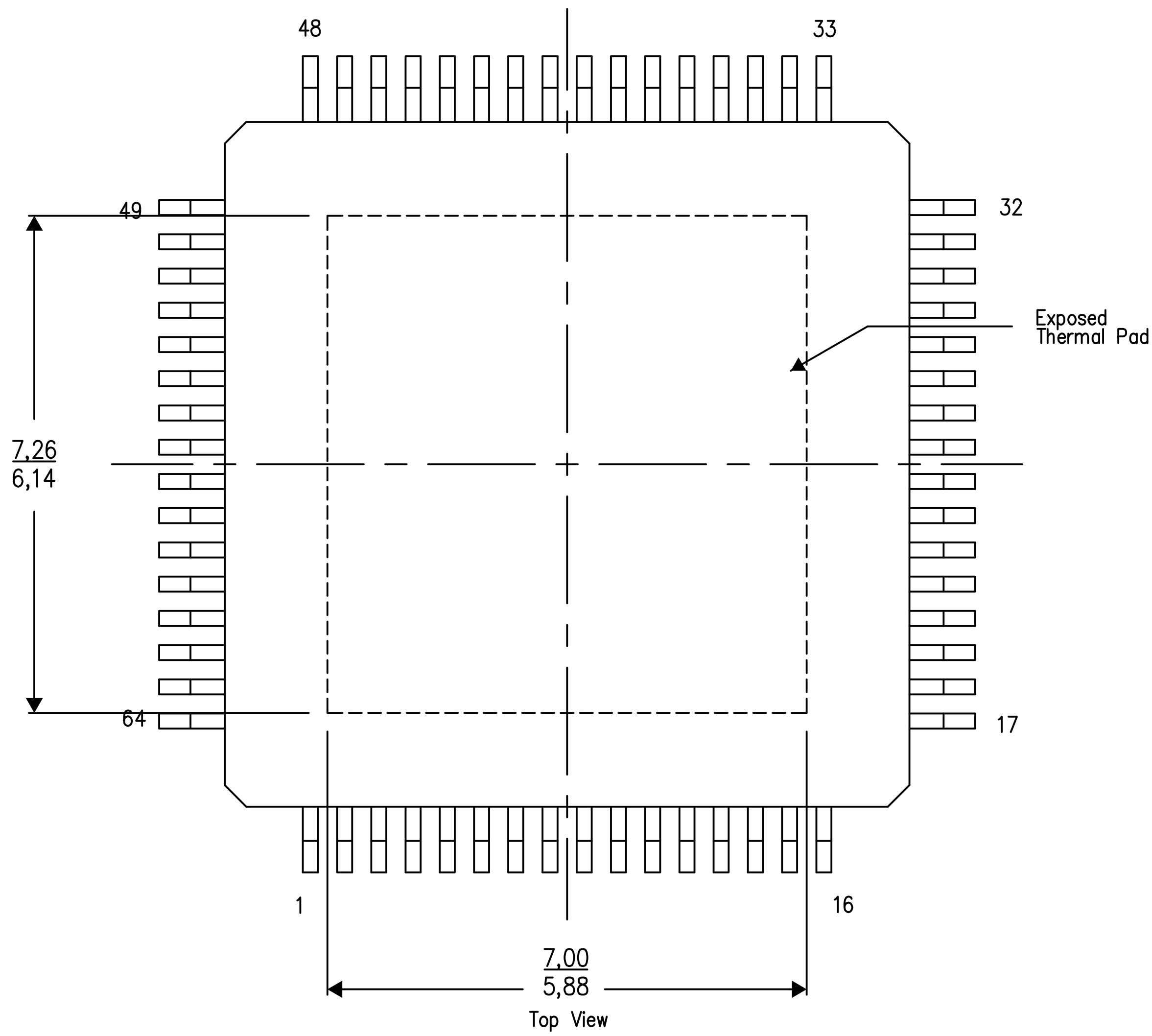
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



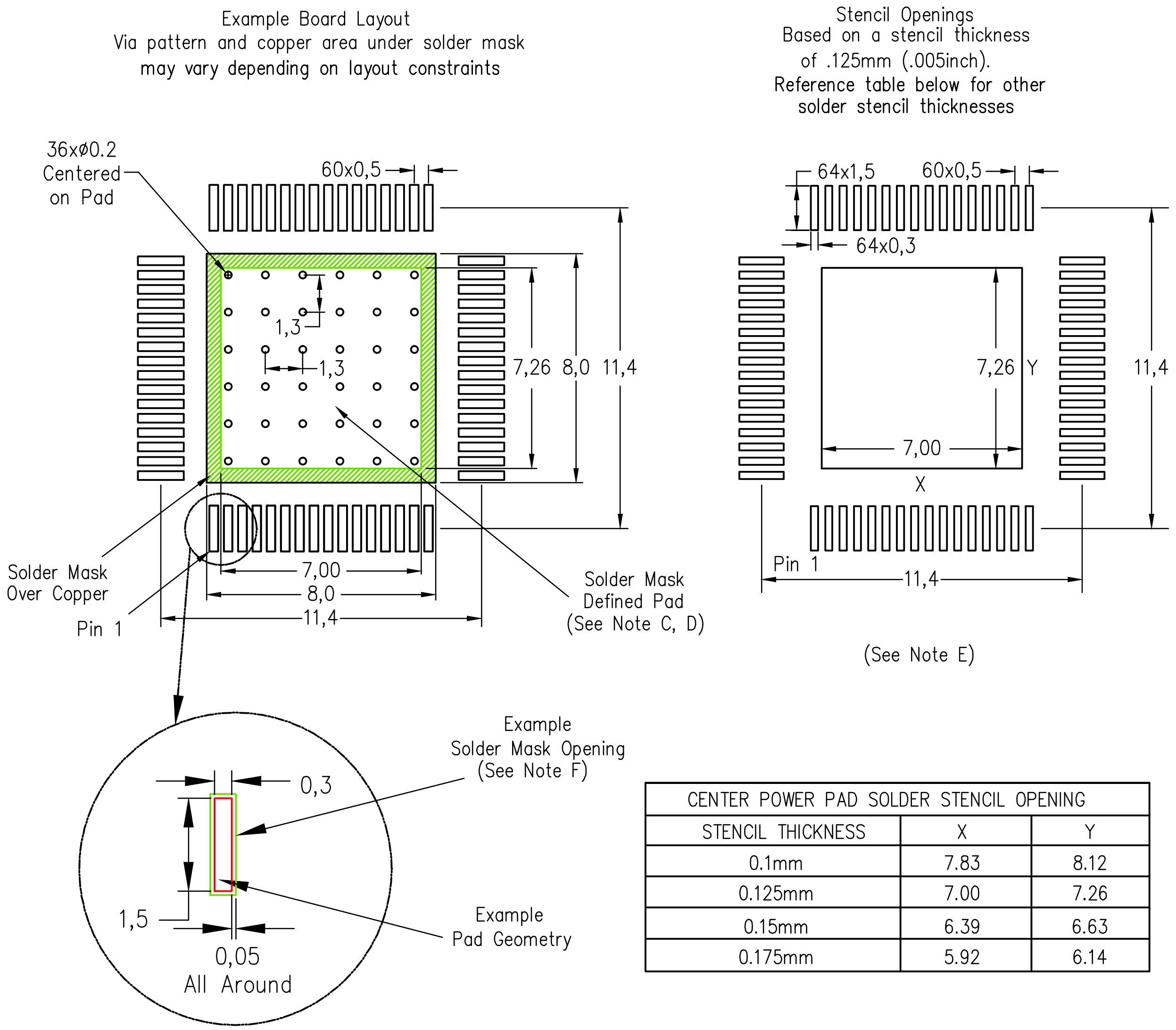
Exposed Thermal Pad Dimensions

4206326–9/P 05/14

NOTES: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



CENTER POWER PAD SOLDER STENCIL OPENING		
STENCIL THICKNESS	X	Y
0.1mm	7.83	8.12
0.125mm	7.00	7.26
0.15mm	6.39	6.63
0.175mm	5.92	6.14

4208775–9/G 03/16

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265