

# **RE46C180**

# **CMOS Programmable Ionization Smoke Detector ASIC with Interconnect, Timer Mode and Alarm Memory**

#### **Features**

- 6 12V Operation
- Low Quiescent Current Consumption
- Programmable Standby Sensitivity
- Programmable HUSH Sensitivity
- Programmable Hysteresis
- Programmable Chamber Voltage for Push-to-Test (PTT) and Chamber Test
- Programmable ±150 mV Low Battery Set Point
- Internal Ionization Chamber Test
- Internal Low Battery Test
- Internal Power-On Reset and Power-up Low Battery Test
- Alarm Memory
- Auto Alarm Locate
- Horn Synchronization
- IO Filter and Charge Dump
- Smart Interconnect
- Interconnect up to 40 Detectors
- ±5% All Internal Oscillator
- 9 Minute or 80 Second Timer for Sensitivity **Control**
- Temporal or Continuous Horn Pattern
- Guard Outputs for Ion Detector Input
- ±0.75 pA Detect Input Current
- 10-year End-of-Life Indication

#### **Description**

The RE46C180 is a next generation low power, CMOS ionization-type, smoke detector IC. With minimal external components, this circuit will provide all the required features for an ionization-type smoke detector.

An on-chip oscillator strobes power to the smoke detection circuitry for 5 ms every 10 seconds to keep the standby current to a minimum.

A check for a Low Battery condition is performed every 80s and an ionization chamber test is performed once every 320s when in Standby. The temporal horn pattern complies with the National Fire Protection Association NFPA 72® National Fire Alarm and Signaling Code® for emergency evacuation signals.

An interconnect pin allows multiple detectors to be connected, such that when one unit alarms, all units will sound. A charge dump feature quickly discharges the interconnect line when exiting a Local Alarm condition. The interconnect input is also digitally filtered.

An internal 9 minute or 80s timer can be used for a Reduced Sensitivity mode.

An alarm memory feature allows the user to determine whether the unit has previously entered a Local Alarm condition.

Utilizing low-power CMOS technology, the RE46C180 is designed for use in smoke detectors that comply with the Standard for Single and Multiple Station Smoke Alarms, UL217 and the Standard for Smoke Detectors for Fire Alarm Systems, UL268.

#### **Package Types**



#### **Functional Block Diagram**



#### **Typical Application**



#### **1.0 ELECTRICAL CHARACTERISTICS**

#### **1.1 Absolute Maximum Ratings†**



**† Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

# **DC ELECTRICAL CHARACTERISTICS**

**DC Electrical Characteristics:** Unless otherwise indicated, all parameters apply at  $T_A = -10^{\circ}$ C to +60°C,  $V_{DD}$  = 9V,  $V_{SS}$  = 0V [\(Note 1\)](#page-3-0)



<span id="page-3-2"></span><span id="page-3-1"></span><span id="page-3-0"></span>**Note 1:** Production tested at room temperature with temperature guard banded limits.

**2:** Sample test only.

**3:** Not 100% production tested.

<span id="page-3-3"></span>**4:** Same limit range at each programmable step, see [Table 4-1](#page-14-0).

## **DC ELECTRICAL CHARACTERISTICS (CONTINUED)**

**DC Electrical Characteristics:** Unless otherwise indicated, all parameters apply at  $T_A = -10^{\circ}$ C to +60°C,



**Note 1:** Production tested at room temperature with temperature guard banded limits.

**2:** Sample test only.

**3:** Not 100% production tested.

**4:** Same limit range at each programmable step, see Table 4-1.

#### **AC ELECTRICAL CHARACTERISTICS**

**AC Electrical Characteristics:** Unless otherwise indicated, all parameters apply at T<sub>A</sub> = -10°C to +60°C,



<span id="page-5-2"></span><span id="page-5-1"></span><span id="page-5-0"></span>**Note 1:** T<sub>POSC</sub> is 100% production tested. All other timing is verified by functional testing.

**2:** See timing diagram for CO alarm horn pattern.

**3:** See timing diagram for smoke alarm temporal and non-temporal horn pattern.

<span id="page-5-3"></span>**4:** See timing diagram for horn synchronization and Auto Alarm Locate (AAL).

#### **AC ELECTRICAL CHARACTERISTICS (CONTINUED)**

![](_page_6_Picture_266.jpeg)

![](_page_6_Picture_267.jpeg)

**Note 1:** T<sub>POSC</sub> is 100% production tested. All other timing is verified by functional testing.

**2:** See timing diagram for CO alarm horn pattern.

**3:** See timing diagram for smoke alarm temporal and non-temporal horn pattern.

**4:** See timing diagram for horn synchronization and Auto Alarm Locate (AAL).

#### **AC ELECTRICAL CHARACTERISTICS (CONTINUED)**

**AC Electrical Characteristics:** Unless otherwise indicated, all parameters apply at T<sub>A</sub> = -10°C to +60°C, V<sub>DD</sub> = 9V, V<sub>SS</sub> = 0V.

![](_page_7_Picture_273.jpeg)

**Note 1:** T<sub>POSC</sub> is 100% production tested. All other timing is verified by functional testing.

**2:** See timing diagram for CO alarm horn pattern.

**3:** See timing diagram for smoke alarm temporal and non-temporal horn pattern.

**4:** See timing diagram for horn synchronization and Auto Alarm Locate (AAL).

# **TEMPERATURE CHARACTERISTICS**

![](_page_8_Picture_55.jpeg)

## **2.0 PIN DESCRIPTIONS**

The descriptions of the pins are listed in [Table 2-1.](#page-9-0)

#### <span id="page-9-0"></span>**TABLE 2-1: PIN FUNCTION TABLE**

![](_page_9_Picture_127.jpeg)

#### <span id="page-10-1"></span>**3.0 DEVICE DESCRIPTIONS**

#### **3.1 Standby Internal Timing**

The internal oscillator is manufactured to ±5% tolerance. The oscillator period, TPOSC, is 625 µs. The internal clock period, TPCLK, of 10 ms is derived from the internal oscillator period.

In Standby, once every 10s, the smoke detection circuitry is powered on for 5 ms. At the conclusion of the 5 ms, the status of the smoke comparator is latched. If a Smoke condition is present, the period to the next detection decreases and additional checks are made.

In Standby, once every 80s, the Low Battery detection circuitry is powered on for 10 ms. At the conclusion of the 10 ms, the status of the Low Battery comparator is latched. RLED is enabled for 10 ms every 320s to provide a battery load in the loaded battery test.

In Standby, once every 320s, the chamber test circuitry is powered on for 5 ms. At the conclusion of the 5 ms, the status of the chamber test is latched. See **[Section 3.3 "Supervisory Tests"](#page-10-0)** for details.

#### **3.2 Smoke Detection Circuitry**

The collection electrode voltage (CEV) of the ionization chamber is compared to the stored reference voltage at the conclusion of the 5 ms smoke sample period. After the first Smoke condition is detected, the smoke detection rate increases to once every 1s. Three consecutive smoke detections will cause the device to go into Local Alarm, and the horn circuit and IO will be active. RLED will turn on for 10 ms at 1 Hz rate.

In Local Alarm, the smoke reference voltage (smoke sensitivity) is internally increased to provide alarm hysteresis.

There are three separate smoke sensitivity settings (all user programmable):

- Standby sensitivity
- Local alarm (hysteresis) sensitivity
- HUSH sensitivity

During PTT, the standby smoke sensitivity is used in smoke detection; but the CHAMBER voltage is user programmable.

The guard amplifier and outputs are always active, and will be within 50 mV of the DETECT input to reduce surface leakage. The guard outputs also allow for measurement of the DETECT input without loading the ionization chamber.

#### <span id="page-10-0"></span>**3.3 Supervisory Tests**

Once every 80s, the status of the battery voltage is checked by comparing a fraction of the  $V_{DD}$  voltage to an internal reference. In each period of 320s, the battery is checked four times. Of these four battery checks, three are unloaded and one is loaded with RLED enabled, which provides a battery load. Low battery status is latched at the end of the 10 ms RLED pulse.

If the Low Battery test fails, the horn will chirp for 10 ms every 40s, and will continue to chirp until the next loaded Low Battery check is passed. The unloaded Low Battery checks are skipped in Low Battery condition.

As a user programmable option, a Low Battery Hush mode can be selected. If a Low Battery condition exists, upon release of PTT, the unit will enter the Low Battery Hush mode, and the 10 ms horn chirp will be silenced for 8 hours. At the conclusion of the 8 hours the audible indication will resume, if the Low Battery condition still exists

In addition, every 320s, a background chamber test is performed by internally lowering the CHAMBER voltage to a pre-determined level (user programmable) for 3.7s. This will emulate a Smoke condition. At the end of this 3.7s period, the smoke detection circuitry is powered on for 5 ms, and the Smoke condition is detected.

If two consecutive chamber tests failed to detect a simulated Smoke condition, the chamber fail latch is set and the failure warning is generated. The horn will chirp three times every 40s. Each chirp is 10 ms long and three chirps are spaced at a 0.5s interval. The chamber fail warning chirp is separated from the Low Battery warning chirp by about 20s.

The horn will continue this pattern until the chamber fail latch is reset. The chamber fail latch resets when any one of the followings is active:

- Two consecutive chamber tests pass
- Local smoke alarm
- PTT smoke alarm

After the chamber test is completed, the CHAMBER voltage goes back to its normal standby level.

Chamber test is performed approximately 140s after the loaded Low Battery test.

In a Local Alarm, PTT Alarm or Remote Alarm condition, the chamber test is not performed, and the Low Battery chirping is prohibited.

#### **3.4 Push-to-Test (PTT)**

PTT is an event when TEST is activated  $(V_{H3})$ . Release of PTT is an event when TEST is deactivated  $(V<sub>H3</sub>)$ . PTT has different functions for different circumstances. In Standby, PTT tests the unit. Upon start of PTT, the CHAMBER voltage is lowered to a pre-determined level (user programmable) to emulate a Smoke condition. The smoke detection rate increases to once every 250 ms. After three consecutive smoke detections, the unit will go into a Local Alarm condition. In alarm, the smoke detection rate decreases to once every 1s. Upon release of PTT, the unit is immediately reset out of Local Alarm, and the horn is silenced. The chamber voltage goes back to the normal standby level, and the detection rate goes back to once every 10s.

When the unit exits a Local Alarm condition, the alarm memory latch is set. PTT will activate the alarm memory indication if the alarm memory latch is set and if the alarm memory indication function has been enabled. If the alarm memory indication function has not been enabled and the alarm memory latch is set, PTT will test the unit as described above. The release of PTT will always reset the alarm memory latch.

In Standby and Low Battery conditions, PTT tests the unit and RLED will be constantly enabled. This allows the user to easily identify the low battery unit without waiting for 40s to hear a horn chirp. Upon release of PTT, RLED goes back to normal standby pulse rate. The Low Battery HUSH mode is then activated, if this function is enabled.

#### **3.5 Interconnect Operation**

The bidirectional IO pin allows the interconnection of multiple detectors. In a Local Alarm condition, this pin is driven high 3.7s after a Local Alarm condition is sensed through a constant current source. Shorting this output to ground will not cause excessive current. The IO is ignored as input during a Local Alarm.

The IO also has an NMOS discharge device that is active for 0.5s after the conclusion of any type of Local Alarm. This device helps to quickly discharge any capacitance associated with the interconnect line.

If a remote active high signal is detected, the device goes into Remote Alarm and the horn will be active. RLED will be off, indicating a Remote Alarm condition. Internal protection circuitry allows the signaling unit to have higher supply voltage than the signaled unit, without excessive current draw.

The interconnect input has a 291 ms maximum digital filter. This allows for interconnection to other types of alarms (CO, for example) that may have a pulsed interconnect signal.

As a user-programmable option, the smart interconnect (smart IO) function can be selected. If the IO input is pulsed high twice with a nominal pulse on time

greater than 37 ms and within 5.4s, a CO Alarm condition is detected, and the CO temporal horn pattern will sound. The CO temporal pattern will sound at least two times, if a CO Alarm condition is detected.

#### **3.6 Reduced Sensitivity Mode (HUSH Mode)**

Upon release of PTT, the unit may or may not go into a HUSH mode, depending on the user's selection.

If the hush-in-alarm-only option is selected, then only the release of PTT in a Local Alarm condition can initiate a HUSH mode. Upon release of PTT, the unit is immediately reset out of alarm, and the horn is silenced.

If the hush-in-alarm-only option is not selected, then anytime a release of PTT occurs, the HUSH mode is initiated.

In HUSH mode, the smoke sensitivity is lowered to a pre-determined level, which is user programmable. RLED is turned on for 10 ms every 10s.

The HUSH mode period is user programmable – it can be either 9 minutes or 80s. After this period times out, the unit goes back to its standby sensitivity.

If the unit is currently in a HUSH mode, then PTT will test the unit with the standby sensitivity. Upon release of PTT, a new HUSH mode will be initiated.

As another user-programmable option, HUSH mode can be terminated earlier by a smart hush function. This function allows the HUSH mode to be canceled by either a high smoke alarm, or a remote smoke alarm. High smoke alarm is the local smoke alarm caused by a smoke level that exceeds the reduced sensitivity level.

#### **3.7 Alarm Memory**

Alarm memory is a user-programmable option. If a unit has entered a Local Alarm, when exiting that Local Alarm, the alarm memory latch is set. The GLED can be used to visually identify any unit that had previously been in a Local Alarm condition. The GLED is pulsed on three times every 40s. Each GLED pulse is 10 ms long and 1s spaced from the next pulse. This alarm memory indication period can be 0, 24, 48 hours or no limit, depending on the user's selection.

The user will be able to identify a unit with an active alarm memory anytime by PTT. Upon start of PTT, the alarm memory indication will be activated. Depending on the user's selection, it can be 4 Hz horn chirp, 4 Hz GLED pulse, or both. Upon release of PTT, the alarm memory latch will be reset.

Anytime a release of PTT occurs, the alarm memory latch will be reset. The initial visual GLED indication is not displayed if a Low Battery condition exists.

#### **3.8 End-of-Life (EOL) Indicator**

The EOL indicator is a user-programmable function. If the EOL indicator function is enabled, then approximately every 15 days of continuous operation, TEOL, the circuit will read an age count stored in EEPROM, and will increment this age. After 10 years of operation, an audible indication will be given to signal that the unit should be replaced. The EOL indicator is the same as the chamber test failure warning.

#### **3.9 Tone Pattern**

The smoke alarm tone pattern can be either a temporal pattern, or a continuous pattern, depending on the user's selection. The temporal horn pattern supports the NFPA 72® National Fire Alarm and Signaling Code<sup>®</sup> for emergency evacuation signals. The continuous pattern is a 70% duty cycle continuous pattern.

If a CO alarm is detected through the IO, the unit will sound the CO tone pattern. The CO tone pattern consists of 4 horn beeps in every 5.8s. Each horn beep is 100ms long and separated by 100ms.

#### **3.10 Horn Synchronization**

The horn synchronization function is programmable by the user.

In an interconnected system, if one unit goes into Local Alarm, other units will also go into Remote Alarm. The IO line is driven high by the origination local smoke unit, and stays high during the alarm.

If the Horn Synchronization function is enabled, at the end of every temporal horn pattern and when the horn is off, the origination unit will drive IO low, then high again. This periodic IO pulsing high and low will cause the remote smoke units to go into and out of the Remote Alarm repeatedly. Each time a unit goes into a Remote Alarm, its timing is reset. The horn sound of all remote smoke units will be synchronized with the horn sound of the origination unit.

A protection circuit ensures that the unit that goes first into a Local Alarm will be the master unit that conducts the horn synchronization. The units that go later into Local Alarm will not drive the IO line. This prevents bus contention problem.

This function works with the temporal tone pattern only.

#### **3.11 Auto Alarm Locate**

Auto Alarm Locate (AAL) is also a user-programmable function. To use AAL, the horn synchronization has to be selected first. The purpose of AAL is to let users quickly find the local alarm units just by listening. The local alarm units will sound the temporal pattern without interruption. The remote alarm units will sound the pattern with interruption. Every four temporal patterns (or 16s), the remote units are kept silenced for one pattern (or 4s).

The originating unit conducts the IO cycling. Every four temporal patterns the IO is driven low for one temporal pattern. In the remaining three temporal patterns, the IO is still pulsing to keep the horn synchronized.

The RLED of the origination unit and other local smoke units will be turned on 10 ms every 1s. The RLED of the remote smoke units will be off.

**NOTES:**

#### **4.0 USER PROGRAMMING MODES**

Tables [4-1](#page-14-0) to [4-6](#page-16-0) show the parameters for user smoke calibration.

#### <span id="page-14-0"></span>**TABLE 4-1: PARAMETRIC PROGRAMMING**

![](_page_14_Picture_481.jpeg)

- <span id="page-14-4"></span><span id="page-14-3"></span><span id="page-14-2"></span><span id="page-14-1"></span>**Note 1:**  $V_{\text{STD}}$  listed is based on  $V_{\text{DD}}$  = 9V. The actual range is  $(29/90)V_{DD} \rightarrow (60/90)V_{DD}$ , resolution is  $V_{DD}/90$ .
	- **2:**  $V_{HYS}$  is a positive offset from  $V_{STD}$ . The listed value is based on  $V_{DD} = 9V$ . The actual range is  $+(0.5/90)V_{DD} \rightarrow +(2.25/$ 90) $V_{DD}$ , resolution is  $(0.25/90)V_{DD}$ .
	- **3:** V<sub>HSH</sub> is a negative offset from V<sub>STD</sub>. The listed value is based on  $V_{DD} = 9V$ . The actual range is –(16/90) $\rm V_{DD}$   $\rightarrow$ –(1/90)V<sub>DD</sub>, resolution is V<sub>DD</sub>/90
	- **4:** V<sub>CHAMBER</sub> listed value is based on  $V_{DD}$  = 9V. Actual range is (21/90) $V_{DD} \rightarrow$  $(67.5/90)V_{DD}$ , resolution is  $(1.5/90)V_{DD}$ .

#### <span id="page-14-5"></span>TABLE 4-2: STANDBY SENSITIVITY (V<sub>STD</sub>) **PROGRAMMING CONFIGURATION**  AT  $V_{DD} = 9V$

![](_page_14_Picture_482.jpeg)

#### <span id="page-15-2"></span>**TABLE 4-3: HYSTERESIS (VHYS) PROGRAMMING CONFIGURATION**  AT  $V_{DD} = 9V$

![](_page_15_Picture_471.jpeg)

#### <span id="page-15-1"></span>TABLE 4-4: HUSH SENSITIVITY (V<sub>HSH</sub>) **PROGRAMMING CONFIGURATION**  AT  $V_{DD} = 9V$

![](_page_15_Picture_472.jpeg)

#### <span id="page-15-0"></span>**TABLE 4-5: CHAMBER VOLTAGE (VCHAMBER) PROGRAMMING CONFIGURATION**  AT  $V_{DD} = 9V$

![](_page_15_Picture_473.jpeg)

![](_page_16_Picture_382.jpeg)

#### <span id="page-16-0"></span>**TABLE 4-6: FEATURE PROGRAMMING**

#### **4.1 Calibration and Programming Procedures**

Sixteen separate programming and Test modes are available for user customization. The T2 input is used to enter these modes and step through them. To enter these modes, after power-up, T2 must be driven to  $V_{DD}$ and held at that level. To step through the modes, the TEST input must first be driven to  $V_{DD}$ . T2 is then clocked. TEST has to be high when clocking T2. Anytime T2 and TEST are both driven to low, the unit will come out of these modes and go back to the normal operation mode. FEED and IO are re-configured to become Test mode inputs. A T2 clock occurs when it switches from  $V_{SS}$  to  $V_{DD}$ . The Test mode functions are outlined in the [Table 4-7](#page-16-1).

#### <span id="page-16-1"></span>**TABLE 4-7: TEST MODE FUNCTIONS**

![](_page_16_Picture_383.jpeg)

<span id="page-16-3"></span><span id="page-16-2"></span>**Note 1:** After power-up, the unit is in M0, the normal operation mode. When in M0, if T2 is driven to  $V_{DD}$ , the unit will enter TM0.

**2:** In M0 and TM0, the digital output TESTOUT is driven by the internal IO dump signal.

<span id="page-16-4"></span>**3:** In TM3, if TEST =  $V_{SS}$ , the horn is turned on. IO is in weak pull-down; If TEST =  $V_{DD}$ , the horn is off. FEED controls IO and HB/HS.

<span id="page-16-5"></span>**4:** Valid when  $TEST = V_{DD}$ ;

<span id="page-16-6"></span>**5:** SmkCompOut – digital comparator output (high if DETECT <  $V_{\text{SEN}}$ ), low if DETECT >  $V_{\text{SEN}}$ ).

<span id="page-16-7"></span>**6:** LBCompOut – digital comparator output (high if  $V_{DD}$  < LB trip point; low if  $V_{DD}$  > LB trip point).

![](_page_17_Picture_296.jpeg)

#### **TABLE 4-7: TEST MODE FUNCTIONS (CONTINUED)**

**Note 1:** After power-up, the unit is in M0, the normal operation mode. When in M0, if T2 is driven to V<sub>DD</sub>, the unit will enter TM0.

**2:** In M0 and TM0, the digital output TESTOUT is driven by the internal IO dump signal.

**3:** In TM3, if TEST =  $V_{SS}$ , the horn is turned on. IO is in weak pull-down; If TEST =  $V_{DD}$ , the horn is off. FEED controls IO and HB/HS.

**4:** Valid when  $TEST = V_{DD}$ ;

**5:** SmkCompOut – digital comparator output (high if DETECT < V<sub>SEN</sub>; low if DETECT > V<sub>SEN</sub>).

6: LBCompOut – digital comparator output (high if V<sub>DD</sub> < LB trip point; low if V<sub>DD</sub> > LB trip point).

![](_page_18_Figure_1.jpeg)

<span id="page-18-0"></span>*FIGURE 4-1: Nominal Application Circuit for Programming.*

#### <span id="page-18-1"></span>**4.2 Smoke Calibration**

A separate calibration mode is entered for each measurement mode (Normal, Hysteresis, HUSH and PTT/ Chamber Test) so that independent limits can be set for each.

In all calibration modes the  $V_{\text{SEN}}$  voltage, which represents the smoke sensitivity level, can be accessed at T3 output. The SmkCompOut output voltage is the result of the comparison of DETECT and  $V_{\text{SFN}}$ , and can be accessed at TESTOUT output. The FEED input can be clocked to cycle through the available smoke sensitivity levels. Once the desired smoke sensitivity level is reached, the IO input is pulsed low to high to store the result.

The detailed procedure is described in the following steps:

1. Power up with the bias condition shown in [Figure 4-1.](#page-18-0) At power-up:

TEST =  $IO$  = FEED = T2 =  $V_{SS}$ ,

DETECT =  $V_{DD}$ . Now in mode M0.

- 2. Drive T2 input from  $V_{SS}$  to  $V_{DD}$  and hold at  $V_{DD}$ to enter TM0.
- 3. Drive TEST from  $V_{SS}$  to  $V_{DD}$  and hold at  $V_{DD}$ .
- 4. Apply four clock pulses to the T2 input  $(V_{DD}$  to  $V_{SS}$  and back to  $V_{DD}$ ) to enter in TM4 mode. This initiates the Calibration mode for the normal sensitivity setting. Drive TEST from  $V_{DD}$  to  $V_{SS}$ to turn on the smoke comparator and enable the T3 switch. The standby smoke sensitivity  $V_{\text{SFN}}$ will appear at T3. The smoke comparator output will appear at TESTOUT. Clock FEED to increase or decrease the  $V_{\text{SEN}}$  levels as needed. The IO input is pulsed low-to-high to save the result.
- 5. Drive TEST from  $V_{SS}$  to  $V_{DD}$  and hold at  $V_{DD}$ . Apply another clock pulse to the T2 input, to enter in TM5 mode. This initiates the Calibration mode for the hysteresis setting. Drive TEST from  $V_{DD}$  to  $V_{SS}$  to turn on the smoke comparator and enable the T3 switch. The local alarm smoke sensitivity  $V_{\text{SEN}}$  will appear at T3. The smoke comparator output will appear at TESTOUT. Clock FEED to increase or decrease the  $V_{\text{SEN}}$  levels as needed. The IO input is pulsed low-to-high to save the result.
- 6. Drive TEST from  $V_{SS}$  to  $V_{DD}$  and hold at  $V_{DD}$ . Apply another clock pulse to the T2 input, to enter in TM6 mode. This initiates the calibration mode for the HUSH sensitivity setting. Drive TEST from  $V_{DD}$  to  $V_{SS}$  to turn on the smoke comparator and enable the T3 switch. The HUSH smoke sensitivity  $V_{\text{SEN}}$  will appear at T3. The smoke comparator output will appear at TESTOUT. Clock FEED to increase or decrease the  $V_{SEN}$  levels as needed. The IO input is pulsed low-to-high to save the result
- 7. Drive TEST from  $V_{SS}$  to  $V_{DD}$  and hold at  $V_{DD}$ . Apply another clock pulse to the T2 input to enter in TM7 mode. This initiates the calibration mode for the CHAMBER voltage at PTT/Chamber Test. Drive TEST from  $V_{DD}$  to  $V_{SS}$  to turn on the smoke comparator and enable the T3 switch. The standby smoke sensitivity  $V_{SEN}$  will appear at T3. The smoke comparator output will appear at TESTOUT. Clock FEED to increase or decrease the CHAMBER voltages as needed. The IO input is pulsed low-to-high to save the result.
- 8. After sensitivity settings and CHAMBER voltage calibrations have been made, pulse IO to store all results into memory. Before this step, no settings are stored into memory.

![](_page_20_Figure_0.jpeg)

#### **4.3 Serial Read/Write Calibration**

As an alternative to the steps in **[Section 4.2, Smoke](#page-18-1) [Calibration](#page-18-1)**, the sensitivity settings can be entered directly from a Serial Read/Write Calibration mode (if the system has been well characterized).

To enter this mode, follow these steps:

1. Power up with the bias condition shown in [Figure 4-1](#page-18-0) to enter M0. At power-up:

TEST =  $IO$  = FEED = T2 =  $V_{SS}$ ,

 $DETECT = V_{DD}$ 

- 2. Drive T2 input from  $V_{SS}$  to  $V_{DD}$  and hold at  $V_{DD}$ to enter TM0.
- 3. Drive TEST from  $V_{SS}$  to  $V_{DD}$  and hold at  $V_{DD}$ .
- 4. Apply 10 clock pulses to the T2 input  $(V_{DD}$  to  $V_{SS}$  and back to  $V_{DD}$ ) to enter in TM10 mode. This enables the Serial Read/Write Calibration mode.
- 5. TEST now acts as a data input (High =  $V_{DD}$ , Low =  $V_{SS}$ ). FEED acts as the clock input (High =  $V_{DD}$ , Low =  $V_{SS}$ ). Clock in the sensitivity settings.

The data sequence should be as follows:

- 5 bit Standby Sensitivity (LSB first)
- 3 bit Hysteresis (LSB first)
- 4 bit HUSH Sensitivity (LSB first)
- 5 bit CHAMBER voltage in PTT/Chamber Test (LSB first)
- 6. After all 17 bits have been entered, pulse IO to store into the EEPROM memory.

#### **REGISTER 4-1: CALIBRATION CONFIGURATION REGISTER**

![](_page_22_Picture_168.jpeg)

bit 6 **HYTR1:** LSB

bit 4 **STTR4:** 4SB bit 3 **STTR3:** 3SB bit 2 **STTR2:** 2SB bit 1 **STTR1:** LSB

bit 5 **STTR5:** MSB (See [Table 4-2\)](#page-14-5)

![](_page_23_Figure_1.jpeg)

#### <span id="page-24-1"></span>**4.4 User Feature Selections**

User feature selections can be clocked in serially using TEST as data input, and FEED, as a clock input, then stored in the internal EEPROM.

The detailed steps are as follows:

1. Power up with the bias condition shown in [Figure 4-1.](#page-18-0) At power-up:

TEST =  $IO$  = FEED = T2 =  $V_{SS}$ , DETECT =  $V_{DD}$ . Now in mode M0.

2. Drive T2 input from  $V_{SS}$  to  $V_{DD}$  and hold at  $V_{DD}$ to enter TM0.

- 3. Drive TEST from  $V_{SS}$  to  $V_{DD}$  and hold at  $V_{DD}$ .
- 4. Apply two clock pulses to the T2 input  $(V_{DD}$  to  $V_{SS}$  and then back to  $V_{DD}$ ) to enter in TM2.
- 5. Using TEST as data and FEED as clock, shift in values of 18 bits as selected from [Register 4-2.](#page-24-0)
- 6. After shifting in data, pull IO input to  $V_{DD}$ , then  $V_{SS}$  (minimum pulse-width of 10 ms) to store shift register contents in the memory.
- 7. If any changes are required, power down the part and return to Step 1. All bit values must be reentered.

#### <span id="page-24-0"></span>**REGISTER 4-2: USER FEATURE CONFIGURATION REGISTER**

![](_page_24_Picture_292.jpeg)

![](_page_24_Picture_293.jpeg)

![](_page_24_Picture_294.jpeg)

![](_page_24_Picture_295.jpeg)

![](_page_24_Picture_296.jpeg)

![](_page_25_Picture_322.jpeg)

The minimum pulse-width for FEED is 10 µs, while the minimum pulse-width for TEST is 100 µs.

For example, for the following options, the sequence would be:

![](_page_25_Picture_323.jpeg)

![](_page_25_Picture_324.jpeg)

![](_page_26_Figure_0.jpeg)

#### **4.5 Sensitivity Verification**

After all sensitivity levels and CHAMBER voltage at PTT/Chamber Test have been entered and stored into the memory, additional Test modes are available to verify if the sensitivities are functioning as expected. [Table 4-8](#page-27-0) describes several verification tests.

#### <span id="page-27-0"></span>**TABLE 4-8: SENSITIVITY VERIFICATION DESCRIPTION**

![](_page_27_Picture_64.jpeg)

![](_page_28_Figure_0.jpeg)

#### **4.6 Serial Read/Write Calibration and User Features**

As an alternative to the steps in **[Section 4.2, Smoke](#page-18-1) [Calibration](#page-18-1)** and **[Section 4.4, User Feature Selec](#page-24-1)[tions](#page-24-1)**, the sensitivity settings and user feature selections can be entered directly from a Serial Read/Write Calibration mode.

To enter this mode, follow these steps:

1. Power up with the bias condition shown in [Figure 4-1](#page-18-0) to enter M0. At power-up:

TEST =  $IO$  = FEED = T2 =  $V_{SS}$ ,

DETECT =  $V_{DD}$ .

- 2. Drive T2 input from  $V_{SS}$  to  $V_{DD}$  and hold at  $V_{DD}$ to enter TM0.
- 3. Drive TEST from  $V_{SS}$  to  $V_{DD}$  and hold at  $V_{DD}$ .
- 4. Apply 18 clock pulses to the T2 input ( $V_{DD}$  to  $V_{SS}$  and then back to  $V_{DD}$ ) to enter in TM18 mode. This enables the Serial Read/Write Calibration and User Features modes.
- 5. TEST now acts as a data input (High =  $V_{DD}$ , Low =  $V_{SS}$ ). FEED acts as the clock input (High =  $V_{DD}$ , Low =  $V_{SS}$ ). Clock in the sensitivity settings. The data sequence should be as follows:

D1 ~ D18 User Features (18 bits, LSB first)

- D19 ~ D35 Calibration (17 bits, LSB First)
- 6. After all 35 bits have been entered, pulse IO to store into the EEPROM memory.

![](_page_29_Picture_298.jpeg)

![](_page_29_Picture_299.jpeg)

![](_page_29_Picture_300.jpeg)

![](_page_29_Picture_301.jpeg)

![](_page_29_Picture_302.jpeg)

![](_page_29_Picture_303.jpeg)

![](_page_29_Picture_304.jpeg)

![](_page_30_Picture_255.jpeg)

#### **REGISTER 4-3: SERIAL READ/WRITE REGISTER (CONTINUED)**

![](_page_31_Picture_85.jpeg)

![](_page_32_Figure_0.jpeg)

#### **4.7 Horn Test**

Test mode TM3 allows the horn to be enabled indefinitely for audibility testing.

To enter this mode, follow the next steps:

1. Power up with the bias condition shown in [Figure 4-1](#page-18-0) to enter M0. At power-up:

TEST =  $IO$  = FEED = T2 =  $V_{SS}$ ,

 $DETECT = V_{DD}$ .

- 2. Drive T2 input from  $V_{SS}$  to  $V_{DD}$  and hold at  $V_{DD}$ to enter TM0.
- 3. Drive TEST from  $V_{SS}$  to  $V_{DD}$  and hold at  $V_{DD}$ .
- 4. Apply three clock pulses to the T2 input ( $V_{DD}$  to  $V_{SS}$  and then back to  $V_{DD}$ ) to enter in TM3 mode.
- 5. Drive TEST from  $V_{DD}$  to  $V_{SS}$  to enable the horn.

![](_page_33_Figure_11.jpeg)

*FIGURE 4-7: Timing Diagram for Horn Test in Mode TM3.*

#### **4.8 Low Battery Test**

Test mode TM17 allows the low battery trip point to be tested. To enter this mode, follow these steps:

1. Power up with the bias condition shown in [Figure 4-1](#page-18-0) to enter M0. At power-up:

TEST =  $IO$  = FEED = T2 =  $V_{SS}$ ,

 $DETECT = V_{DD}$ .

- 2. Drive T2 input from  $V_{SS}$  to  $V_{DD}$  and hold at  $V_{DD}$ to enter TM0.
- 3. Drive TEST from  $V_{SS}$  to  $V_{DD}$  and hold at  $V_{DD}$ .
- 4. Apply 17 clock pulses to the T2 input  $(V_{DD}$  to  $V_{SS}$  and then back to  $V_{DD}$ ) to enter in TM17 mode.
- 5. Drive IO from  $V_{SS}$  to  $V_{DD}$  to enable the low battery testing and turn on the RLED. Sweep  $V_{DD}$  from high to low and monitor TESTOUT output. The TESTOUT output will indicate the Low Battery status (High = Low Battery detected).

![](_page_34_Figure_10.jpeg)

#### **4.9 User Lock Bit Programming**

Test mode TM19 allows users to program the user EE lock bit. Once the user EE lock bit is set, the programmed user EE data can not be changed unless the lock bit is reset.

To enter this mode, follow these steps:

1. Power up with the bias condition shown in [Figure 4-1](#page-18-0) to enter M0. At power-up:

TEST =  $IO$  = FEED = T2 =  $V_{SS}$ ,

DETECT =  $V_{DD}$ .

- 2. Drive T2 input from  $V_{SS}$  to  $V_{DD}$  and hold at  $V_{DD}$ to enter TM0.
- 3. Drive TEST from  $V_{SS}$  to  $V_{DD}$  and hold at  $V_{DD}$ .
- 4. Apply 19 clock pulses to the T2 input  $(V_{DD}$  to  $V_{SS}$  and then back to  $V_{DD}$ ) to enter in TM19 mode.
- 5. Hold TEST at  $V_{DD}$  and pulse IO once to set the lock bit and store into the EEPROM memory.
- 6. To reset the lock bit from Step 5, drive TEST to  $V_{SS}$  and pulse IO once.

![](_page_35_Figure_12.jpeg)

## **5.0 APPLICATION NOTES**

#### **5.1 Standby Current Calculation**

A calculation of the standby current is shown in [Table 5-1,](#page-36-0) based on the following conditions:

![](_page_36_Picture_227.jpeg)

#### <span id="page-36-0"></span>**TABLE 5-1: STANDBY CURRENT CALCULATION**

![](_page_36_Picture_228.jpeg)

#### $5.1.1$  FIXED  $I_{DD}$

The fixed  $I_{DD}$  is the current from the constantly active internal oscillator, bias circuit and guard amplifier.

#### 5.1.2 SMOKE CHECK

The current draw from the smoke detection circuitry during the 5 ms smoke check period.

#### 5.1.3 LOW BATTERY CHECK (UNLOADED)

The current drawn by the low battery detection circuitry during the 10 ms unloaded low battery check period.

#### 5.1.4 LOW BATTERY CHECK (LOADED)

The current drawn by the RLED during the 10 ms loaded low battery check period.

#### 5.1.5 CHAMBER TEST (SMOKE CHECK)

The current drawn by the smoke detection circuitry during the 5 ms smoke check period, while the chamber is pulled low.

#### 5.1.6 CHAMBER TEST (CHAMBER LOW)

The current drawn to pull the chamber low when the chamber test is performed.

#### 5.1.7 END-OF-LIFE (READING EE AND COUNTING)

The current drawn to read EOL bits from EE and then increase by 1.

#### 5.1.8 END-OF-LIFE (WRITING EE)

The current drawn to write EOL bits back to EE.

#### 5.1.9 TOTAL CURRENT

The average total current drawn in Standby

#### **5.2 FUNCTIONAL TIMING DIAGRAMS**

Figures [5-1](#page-37-0) to [5-8](#page-44-0) show the timing diagrams for the smoke detector functions described in **[Section 3.0,](#page-10-1) [Device Descriptions](#page-10-1)**.

<span id="page-37-0"></span>![](_page_37_Figure_3.jpeg)

FIGURE 5-2:  $T\overline{Iming D}$   $\overline{Hom}$   $\overline{Hom}$ TPLB2 Low Battery Test (Internal Signal) THON1 HORN THPER1  $\begin{array}{c}\n\hline\n\uparrow\n\end{array}$ RLED **TPLED1 Chamber Test (not to Scale)** TPCT1 Chamber Test (Internal Signal) THON1 THOF4 HORN THOF5 THPER2

# **RE46C180**

![](_page_39_Figure_1.jpeg)

![](_page_40_Figure_1.jpeg)

![](_page_41_Figure_1.jpeg)

![](_page_42_Figure_0.jpeg)

![](_page_43_Figure_1.jpeg)

<span id="page-44-0"></span>![](_page_44_Figure_1.jpeg)

**NOTES:**

## **6.0 PACKAGING INFORMATION**

#### **6.1 Package Marking Information**

![](_page_46_Figure_4.jpeg)

16-Lead Narrow SOIC (3.90 mm) Example

![](_page_46_Picture_6.jpeg)

![](_page_46_Figure_8.jpeg)

**Legend:**XX...XCustomer-specific information YYear code (last digit of calendar year) YYYear code (last 2 digits of calendar year) WWWeek code (week of January 1 is week '01') NNNAlphanumeric traceability code Pb-free JEDEC designator for Matte Tin (Sn)  $^{\star}$ This package is Pb-free. The Pb-free JEDEC designator  $(\widehat{\mathrm{e}}3)$ can be found on the outer packaging for this package. **Note**:In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

#### 16-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

![](_page_47_Figure_3.jpeg)

![](_page_47_Picture_216.jpeg)

#### Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

- 2. § Significant Characteristic.
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-017B

![](_page_48_Figure_1.jpeg)

#### 16-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

#### 16-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

![](_page_49_Figure_3.jpeg)

![](_page_49_Figure_4.jpeg)

![](_page_49_Picture_62.jpeg)

#### Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2 § Significant Characteristic
- 3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-108C Sheet 2 of 2

16-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

![](_page_50_Figure_3.jpeg)

#### RECOMMENDED LAND PATTERN

![](_page_50_Picture_45.jpeg)

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2108A

**NOTES:**

## **APPENDIX A: REVISION HISTORY**

#### **Revision B (March 2019)**

- Updated **Section 6.0 "Packaging Information"**;
- Updated **[Section "Product Identification](#page-54-0)  [System"](#page-54-0)**.

#### **Revision A (August 2011)**

Original release of this document.

**NOTES:**

#### <span id="page-54-0"></span>**PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

![](_page_54_Picture_79.jpeg)

**NOTES:**

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![](_page_57_Picture_0.jpeg)

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