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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

# TFT Display Module

## Part Number

### E26RB-FS500-N

## Overview:

- 2.6-inch TFT: 320x432 (46.76x65.85)
- 3/4 SPI+16/18- bit RGB
- 8/9/16/18-bit MCU
- 3-line/4-line Serial Interface
- White LED back-light

- Transflective/ Normally Black
- No Touch Panel
- 500 NITS
- Controller: ILI9488
- RoHS Compliant

## Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 2.を TFT-LCD contains われ×みわ pixels, and can display up to 65K▂むむY▂るるa colors♛

## Features

Low Input Voltage: 3.3V (TYP)

Display Colors of TFT LCD: 65K/262K▂るるa  colors
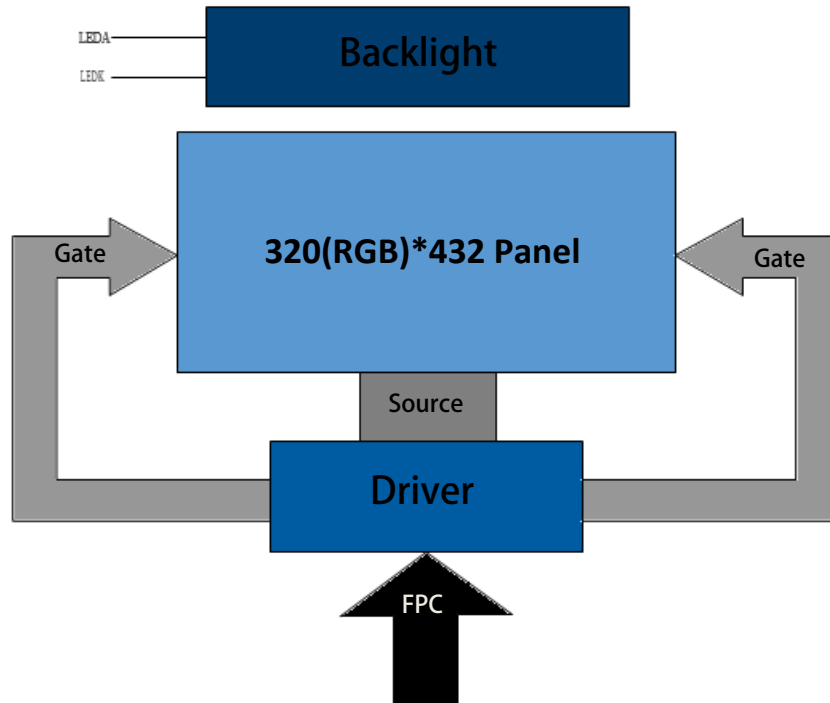
TFT Interface: 8/9/16/18□it MCU;

3/4▨it SPI+16/18▬らit RGB

3-line/4-line ‡erial ⓒnterface

| General Information Items | Specification | Unit | Note |
|---|---|---|---|
| | Main Panel | | |
| Display area (AA) | 3 .▂う▂(H)*みつひ▂(V) (2.を inch) | mm | - |
| Driver element | TFT active matrix | - | - |
| Display colors | 65K/262K▂るるa | colors | - |
| Number of pixels | われ(RGB)*みわ | dots | - |
| TFT Pixel arrangement | RGB vertical stripe | - | - |
| Pixel pitch | 0.るつる(H)*0.るわる(V) | mm | - |
| Viewing angle | ALL | o'clock | - |
| TFT Controller IC | ℟L ▂るつ | - | - |
| Display mode | Trans▂らⓒ†/Normally Black | - | - |
| Operating temperature | -われ~+▂京 | ℃ | - |
| Storage temperature | -▂か〜+8▂ゑ | ℃ | - |

### Mechanical Information

| Item | | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Module size | Horizontal(H) | | 4を7を | | mm | - |
| | Vertical(V) | | 6ゑ▂ゑ | | mm | - |
| | Depth(D) | | わを | | mm | - |
| Weight | | | るゐ | | g | - |

# 1. Block Diagram

# 2. Outline dimensions

| ReV. | Revision content description | Date |
|---|---|---|
| V0 | FIRST | 2018.01.11 |
| | | |
| | | |

| NO. | TFT Pin |
|---|---|
| 1 | GND |
| 2 | LEDA |
| 3 | LEDK |
| 4 | NC |
| 5 | CSX |
| 6 | DCX |
| 7 | WRX_SCL |
| 8 | RDX |
| 9 | SDA |
| 10 | SDO |
| 11 | DB0/B0,LSb |
| 12 | DB01/B1 |
| 13 | DB02/B2 |
| 14 | DB03/B3 |
| 15 | DB04/B4 |
| 16 | DB05/B5 |
| 17 | DB06/B6 |
| 18 | DB07/B7 |
| 19 | DB08/G0,LSb |
| 20 | DB09/G1 |
| 21 | DB10/G2 |
| 22 | DB11/G3 |
| 23 | DB12/G4 |
| 24 | DB13/G5 |
| 25 | DB14/G6 |
| 26 | DB15/G7 |
| 27 | DB16/R0 |
| 28 | DB17/R1 |
| 29 | DB18/R2 |
| 30 | DB19/R3 |
| 31 | DB20/R4 |
| 32 | DB21/R5 |
| 33 | DB22/R6 |
| 34 | DB23/R7 |
| 35 | DE |
| 36 | PCLK |
| 37 | HSYNC |
| 38 | VSYNC |
| 39 | RESX |
| 40 | IM2 |
| 41 | IM1 |
| 42 | IM0/ID |
| 43 | VCI |
| 44 | VCI |
| 45 | IOVCC |
| 46 | IOVCC |
| 47 | YU |
| 48 | XL |
| 49 | YD |
| 50 | XR |
| 51 | GND |

46.76±0.2 UP BEZEL
42.84 BEZEL OPEN
39.84 LCD AA
1.96
3.46
3.46
2.06
65.85±0.2 UP BEZEL
56.58 BEZEL OPEN
53.78 LCD AA

320 RGB*432
wide viewing

PULL TAPE

42.60
59.23
36.35±0.5

A

FRONT

2.6±0.3 LCM

FRONT    BACK

1.1Max Compent
0.13±0.03 FPC

Conduct Side    Stiffener
0.20±0.3

SIDE

2.50
3M DST T=0.05
8.00
white line

BACK

15.87±0.3
34.39±0.5
1.00 MAX
13.20

BACK

| | | | Interface type | DB Pin in use |
|---|---|---|---|---|
| 0 | 0 | 0 | RGB-888 Type B 24-bit bus CSX_DC = 0 | |
| 0 | 0 | 0 | RGB-666 Type B 18-bit bus CSX_DC = 0 | DB17-DB0 |
| 0 | 0 | 1 | MCU 8080 8-bit interface | DB8-DB0 |
| 0 | 1 | 0 | MCU 8080 16-bit interface | DB15-DB0 |
| 0 | 1 | 1 | MCU 8080 9-bit interface | DB7-DB0 |
| 1 | 0 | 1 | 3-Wire 9 BIT data serial interface | SDI SCL CS |
| 1 | 1 | 1 | 4-Wire 8 BIT data serial interface | SDI SCL CS RS |

NOTE:
1. If not use PIN, fix to the GND , IOVCC or NC.
2. If  use RGB interface must select serial interface

NOTES:

1. DISPLAY TYPE:  2.6", TFT-LCD, 65K/262K/16.7M  COLORS
2. DISPLAY MODE: NORMALLY BLACK
3. VIEWING DIRECTION:  SUPER WIDE VIEWING ANGLE
4. DRIVER IC:  ILI9488  (COG)
5. VCI: 3.3V,IOVCC:1.8-3.3V
6. OPERATING TEMP: -30°C TO 85°C
   STORAGE TEMP: -40°C TO 85°C
7. BACK LIGHT: LED WHITE, 6 LED, 15-20mA, 19.2V±0.3V
8. RoHS COMPLIANT.

15.6±0.05
2.5±0.3
2.25±0.1
2.1±0.1
1.1±0.1
1±0.1
0.3±0.1
P0.3*(51-1)=15±0.03
0.3±0.07
0.6±0.02
0.3
0.15
0.2
0.1
0.3

Detail A3:1
FH26-51S-0.3SHW

A ⟶ K

LED(B/L) CIRCUIT

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| TOLERANCE(  ) | | DRAWING NAME | E26RB-FS500-N |
|---|---|---|---|
| | | PARTS NO. | |
| UNLESS | X.X±0.3 | Drawn | Unit |
| OTHERWISE SPECIFIED | X.XX±0.2 | Checked | mm |
| Scale  1:1 | | Approve | Page 1/1 |

## 3.    Input Terminal Pin Assignment

Recommended Connector: FH26-51S-0.3SHW

| NO. | Symbol | Description | I/O |
|-----|--------|-------------|-----|
| 1 | GND | Ground. | P |
| 2 | LEDA | Cathode pin of backlight. | P |
| 3 | LEDK | Cathode pin of backlight. | P |
| 4 | NC | -- | P |
| 5 | CSX | Chip select input pin ("Low" enable). Fix this pin at VCI or GND when not in use. | I |
| 6 | DCX | Display data/command selection pin | I |
| 7 | WR(SPI_SCL) | DBI Type B: WRX pin, serves as a write signal<br>DBI Type C: SCL pin as Serial Clock when operates in the serial interface | I |
| 8 | RDX | Serves as a read signal and MCU read data at the rising edge.<br>Fix this pin at VCI or GND when not in use. | I |
| 9 | SDA | Serial input signal. The data is applied on the rising edge of the<br>SCL signal. If not used, fix this pin at VCI or GND. | I/O |
| 10 | SDO | Serial data output pin in serial bus system interface. If not used, please<br>open this pin. | O |
| 11-34 | DB0-DB23 | 24-bit parallel bi-directional data bus for MCU system and RGB<br>interface mode. Fix to GND level when not in use | I/O |
| 35 | DE | Data enable signal for RGB interface operation. Fix this pin at VCI or GND when<br>not in use. | I |
| 36 | PCLK | Dot clock signal for RGB interface operation Fix this pin at VCI or GND when<br>not in use. | I |
| 37 | HSYNC | Line synchronizing signal for RGB interface operation. Fix this pin at VCI or<br>GND when not in use | I |
| 38 | VSYNC | Frame synchronizing signal for RGB interface operation. Fix this pin at VCI<br>or GND when not in use. | I |
| 39 | RESX | This signal will reset the device and must be applied to properly initialize<br>the chip. | I |
| 40 | IM2 | MPU Parallel interface bus and serial interface select If use RGB<br>Interface must select serial interface.<br>Fix this pin at VCI and GND. | I |
| 41 | IM1 | | |
| 42 | IM0 | | |
| 43 | VCI | Supply voltage (3.3V). | P |
| 44 | VCI | | |
| 45 | IOVCC | Supply voltage For IO (1.8-3.3V) | P |
| 46 | IOVCC | | |
| 47 | YU | Touch panel Top Film Terminal | A/D |
| 48 | XL | Touch panel Left Glass Terminal | A/D |
| 49 | YD | Touch panel Bottom Film Terminal | A/D |
| 50 | XR | Touch panel Right Glass Terminal | A/D |
| 51 | GND | Ground | P |

# 4. LCD Optical Characteristics

## 4.1 Optical specification

### 4.1.1 Transmissive mode

| Item | | Symbol | Condition | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| Contrast Ratio | | CR | Θ=0 Normal viewing angle | -- | 80 | 150 | | (2) |
| Response time | Rising | TR+TF | | -- | 25 | 50 | msec | (4) |
| | Falling | | | | | | | |
| Color gamut | | S (%) | | -- | 58 | -- | % | (5) |
| Color Filter Chromaticity | White | $W_X$ | | 0.261 | 0.311 | 0.361 | | (1)(5) |
| | | $W_Y$ | | 0.287 | 0.337 | 0.387 | | |
| | Red | $R_X$ | | 0.456 | 0.506 | 0.556 | | |
| | | $R_Y$ | | 0.270 | 0.320 | 0.370 | | |
| | Green | $G_X$ | | 0.289 | 0.339 | 0.389 | | |
| | | $G_Y$ | | 0.50 | 0.550 | 0.60 | | |
| | Blue | $B_X$ | | 0.123 | 0.173 | 0.223 | | |
| | | $B_Y$ | | 0.072 | 0.122 | 0.172 | | |
| Viewing angle | Hor. | ΘL | CR>10 | 60 | 80 | -- | | (1) (6) |
| | | ΘR | | 60 | 80 | -- | | |
| | Ver. | ΘU | | 60 | 80 | -- | | |
| | | ΘD | | 60 | 80 | -- | | |
| Option View Direction | | | ALL | | | | | |

### 4.1.2 Reflective mode

| Item | Symbo | Specifications | | | Unit | Note |
|---|---|---|---|---|---|---|
| Reflection ratio (with polarizer) | R (θ=φ=0°)) | 1 | 2 | - | % | (3) |
| Reflective contrast ratio | Cr (θ=0°) | - | 5 | - | | (3) |
| Viewing angle (Cr≥ 2)* | Θ21 | - | 45 | - | deg | (1)(6) |
| | Θ22 | - | 45 | - | | |
| | Θ12 | - | 45 | - | | |
| | Θ11 | - | 45 | - | | |

## 4.2 Measuring conditions

Measuring surrounding: dark room
Ambient temperature: 25±2 ℃
15min. warm-up time.

**Optical Specification Reference Notes:**

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
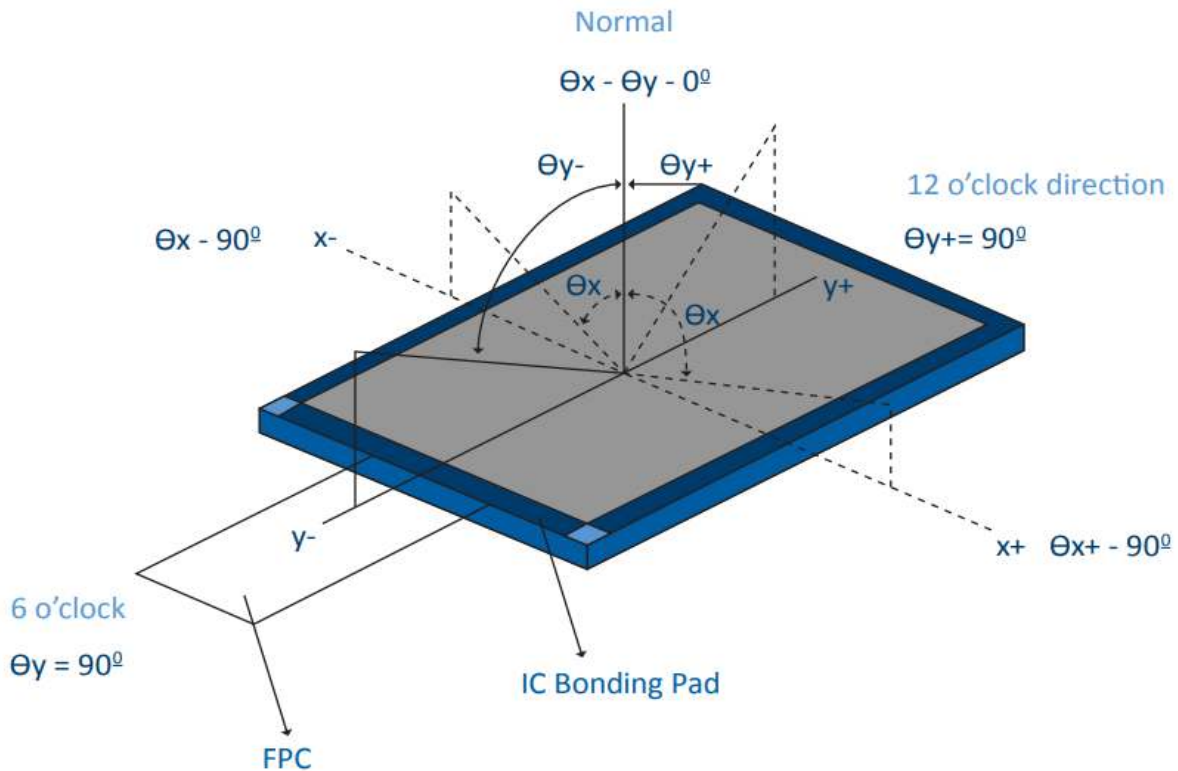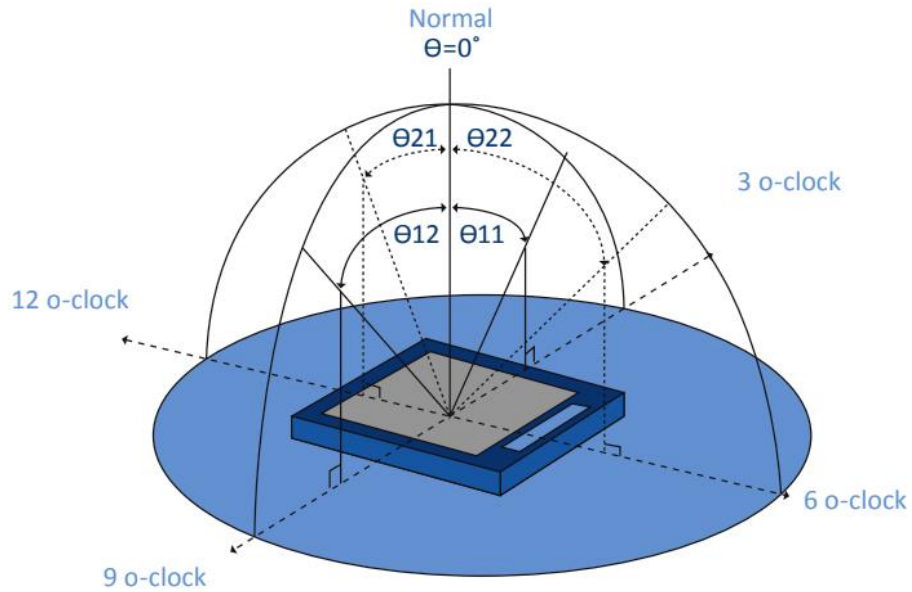
(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving.

I_o                     I_t

light source            LCD panel
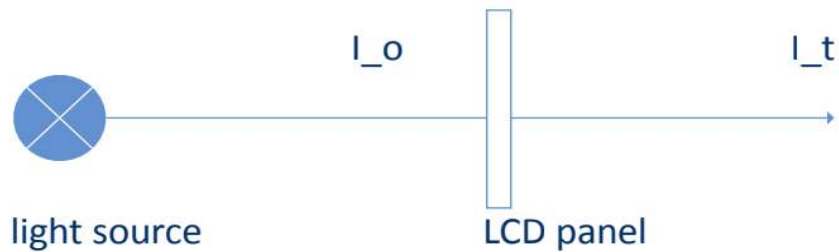
The transmittance is defined as:

$$Tr = \frac{It}{Io} \; x \; 100\%$$

Io = the brightness of the light source.
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.

white (TFT OFF) | black     (TFT ON) | white (TFT OFF)

TR              TF

100%
90%

Optical
response

10%
0%
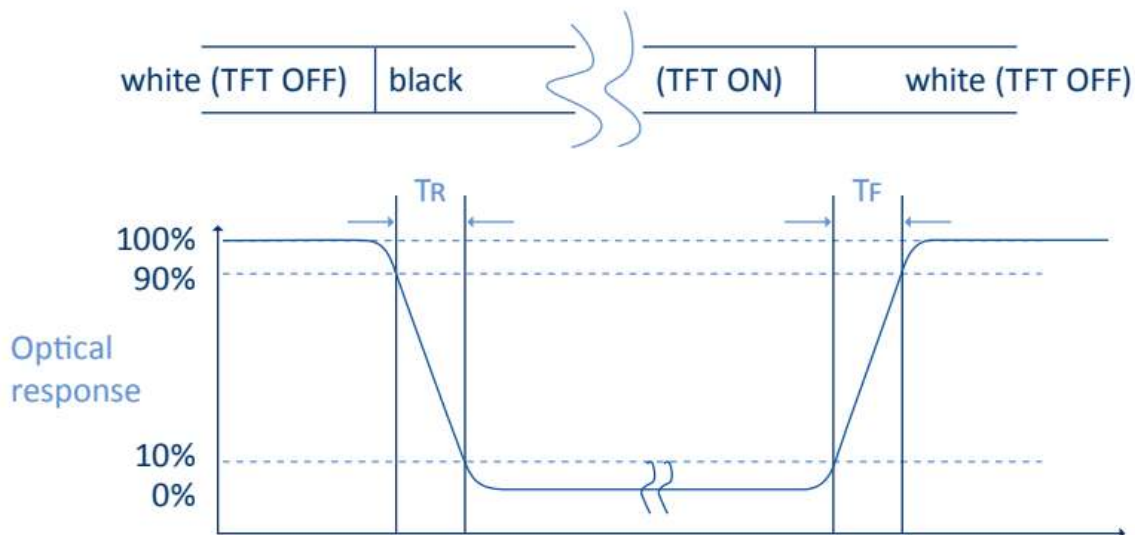
(5) Definition of Color Gamut: Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y),G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.
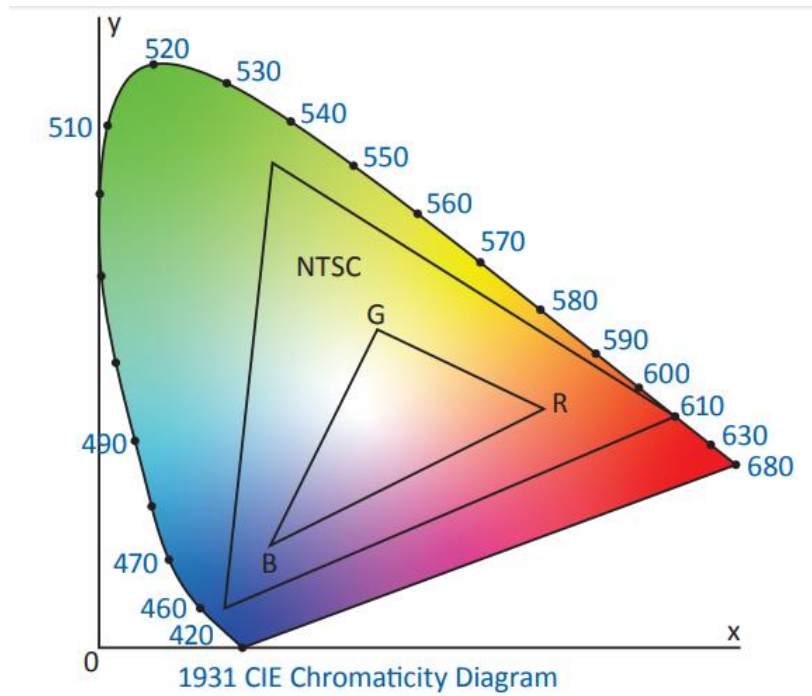


Fig. 1931 CIE chromacity diagram

Color gamut: $S = \dfrac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$

(6) Definition of Optical Measurement Setup:
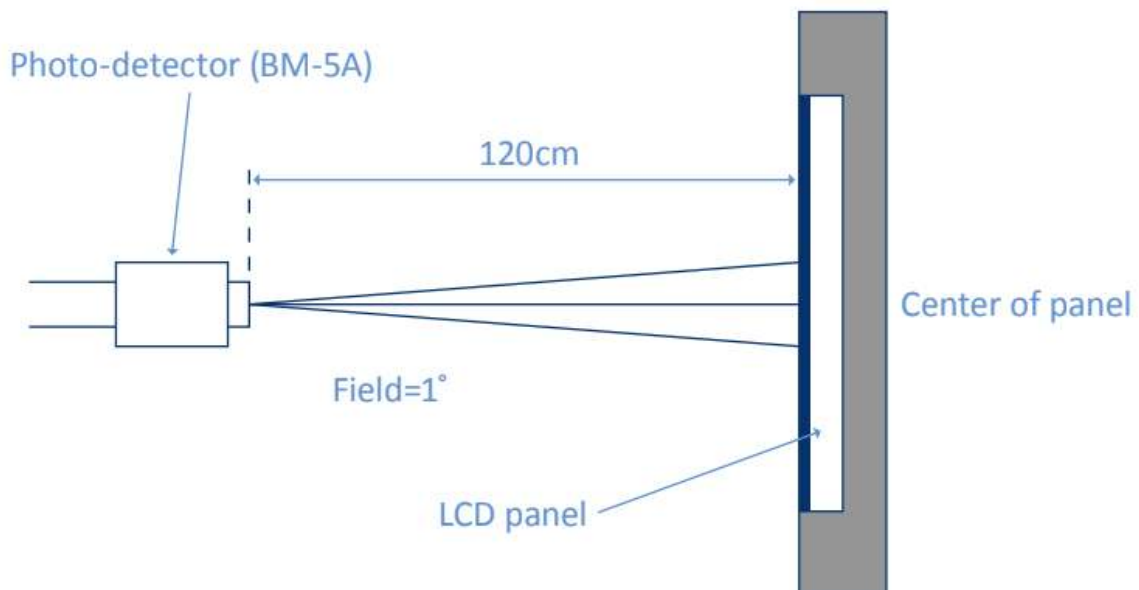
(6) Optical Measurement Setup Continued:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.
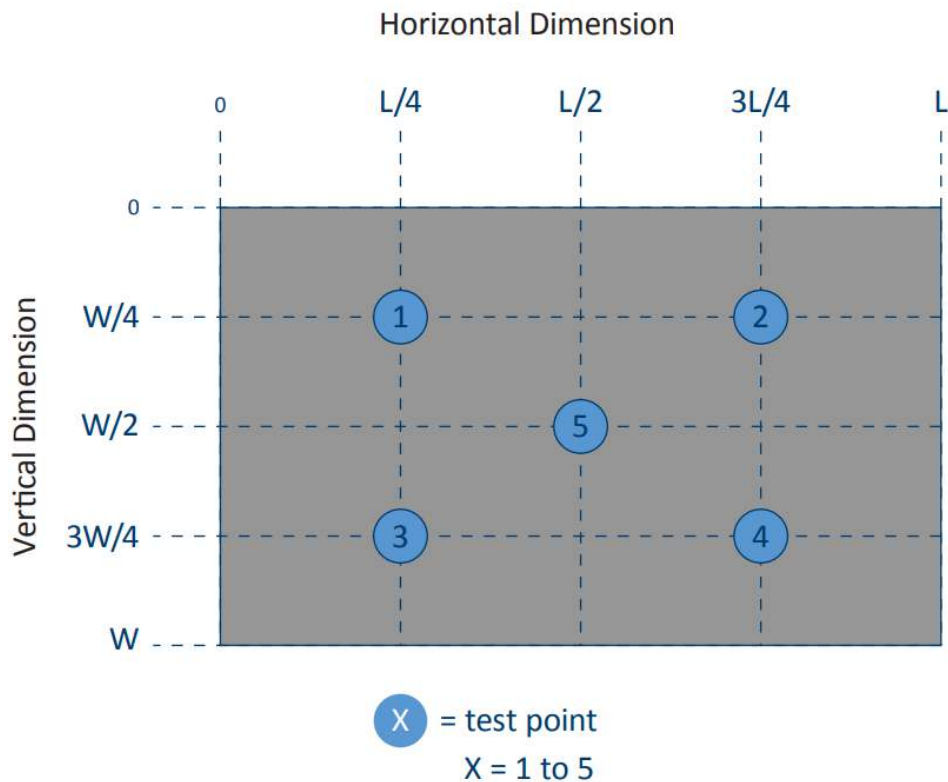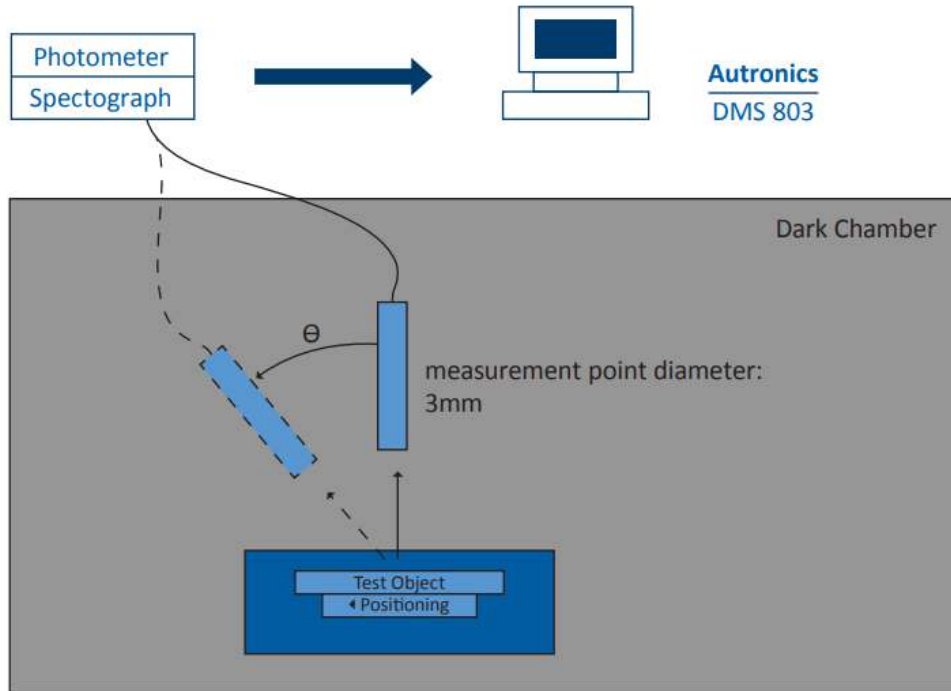
# 5. Electrical Characteristics

## 5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

| Characteristics | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Digital Supply Voltage | VCI | -0.3 | 3.3 | V |
| Interface Operation Voltage | IOVCC | -0.3 | 3.3 | V |
| Operating temperature | TOP | -30 | +85 | °C |
| Storage temperature | TST | -40 | +85 | °C |

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

## 5.2 DC Electrical Characteristics

| Characteristics | Symbol | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Digital Supply Voltage | VCI | 2.5 | 3.3 | -- | V | |
| Interface Operation Voltage | VDDIO | 1.65 | 1.8 | 3.3 | V | |
| Normal Mode Current Consumption | IDD | -- | 14 | -- | mA | |
| Level input voltage | VIH | 0.7 VDDIO | | VDDIO | V | |
| | VIL | -0.3 | | 0.3 VDDIO | V | |
| Level output voltage | VOH | 0.8 VDDIO | | VDDIO | V | |
| | VOL | GND | | 0.2 VDDIO | V | |

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## 5.3 LED Backlight Characteristics

| Item | Symbol | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Forward Current | IF | 15 | 20 | -- | mA | |
| Forward Voltage | VF | -- | 19.2 | -- | V | |
| LCM Luminance | LV | 450 | 500 | -- | cd/m2 | Note 3 |
| LED lifetime | Hr | 50000 | -- | -- | hour | Note1 & 2 |
| Uniformity | AVg | 80 | -- | -- | % | Note 3 |

The back-light system is edge-lighting type with 6 chips White LED

Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25 ±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=20mA. The LED lifetime could be decreased if operating IL is larger than 20mA. The constant current driving method is suggested.

A(+) ▷|▷|▷|▷|▷|▷| K(−)
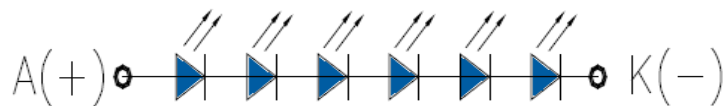
BLU CIRCUIT DIAGRAM

Note 3: Luminance Uniformity of these 9 points is defined as below:
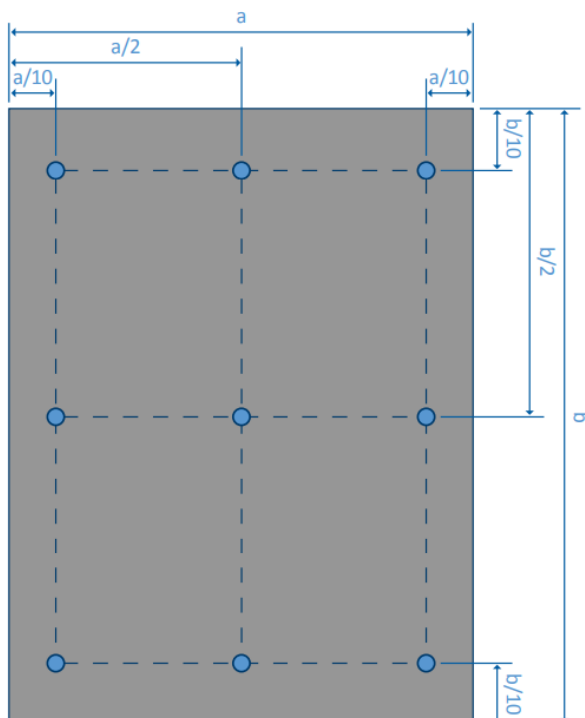
$$Luminance = \frac{(Total\ Luminance\ of\ 9\ points)}{9}$$

$$Uniformity = \frac{minimum\ luminance\ in\ 9\ points(1-9)}{maximum\ luminance\ in\ 9\ points(1-9)}$$

# 6.    AC Characteristic

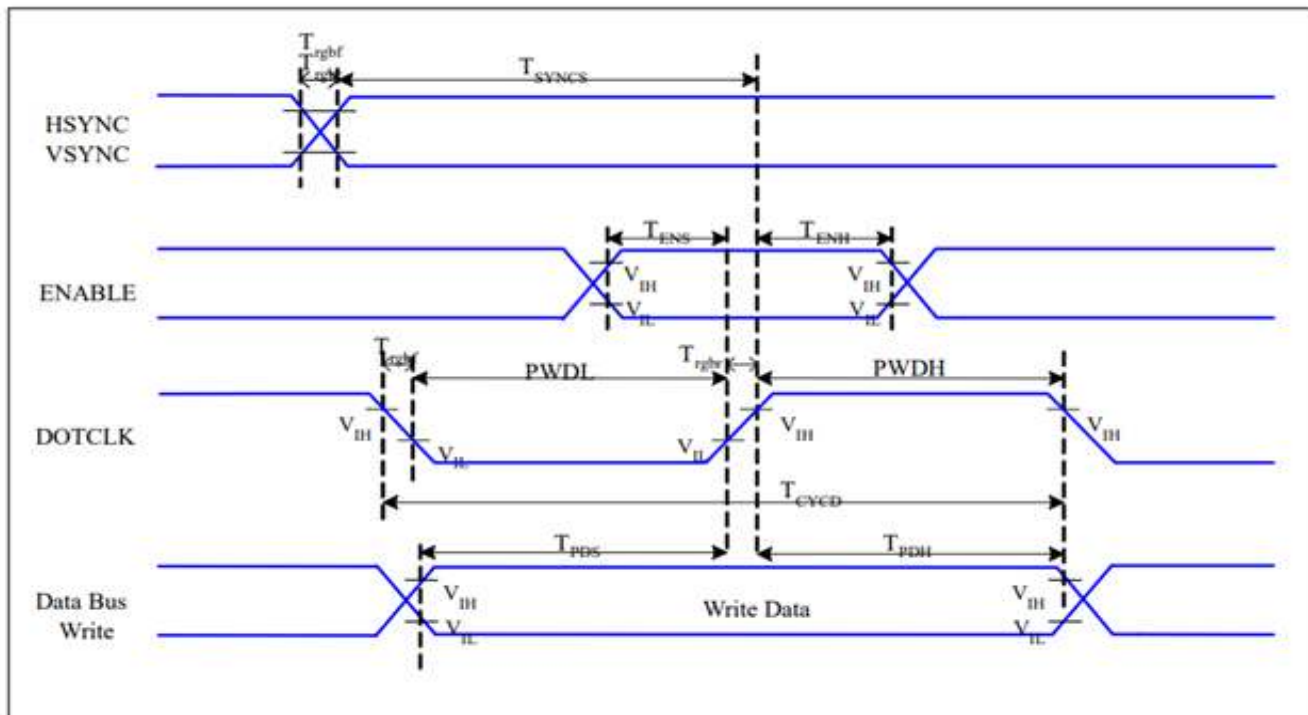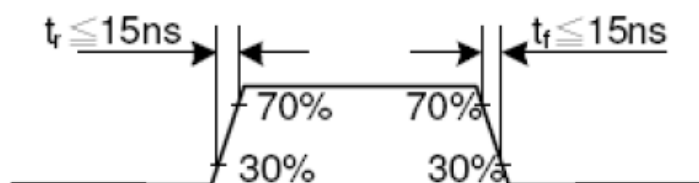## 6.1    Display Parallel 16/18/24-bit Interface Characteristics



*Figure 6.1: Parallel 16/18/24-Bit Interface Timing Diagram*

| Signal | Symbol | Parameter | Min | Max | Unit | Description |
|--------|--------|-----------|-----|-----|------|-------------|
| HSYNC/ VSYNC | $T_{SYNCS}$ | VSYNC, HSYNC setup time | 15 | - | ns | 18/16/6-bit bus RGB interface mode |
| | $T_{SYNCH}$ | VSYNC, HSYNC hold time | 15 | | | |
| DE | $T_{ENS}$ | Enable Setup Time | 15 | - | ns | |
| | $T_{ENH}$ | Enable Hold Time | 15 | - | ns | |
| DOTCLK | PWDH | DOTCLK High-level Pulse Width | 20 | - | ns | |
| | PWDL | DOTCLK Low-level Pulse Width | 20 | - | ns | |
| | $T_{CYCD}$ | DOTCLK Cycle Time | 50 | - | ns | |
| | $T_{RGHR}$, $T_{RGHF}$ | DOTCLK, HSYNC, VSYNC Rise/Fall Time | - | 15 | ns | |
| D[23:0] | $T_{PDS}$ | Data Setup Time | 15 | - | ns | |
| | $T_{PDH}$ | Data Hold Time | 15 | - | ns | |

*Table 6.1: 8/16 Bits RGB Interface Timing Characteristics*

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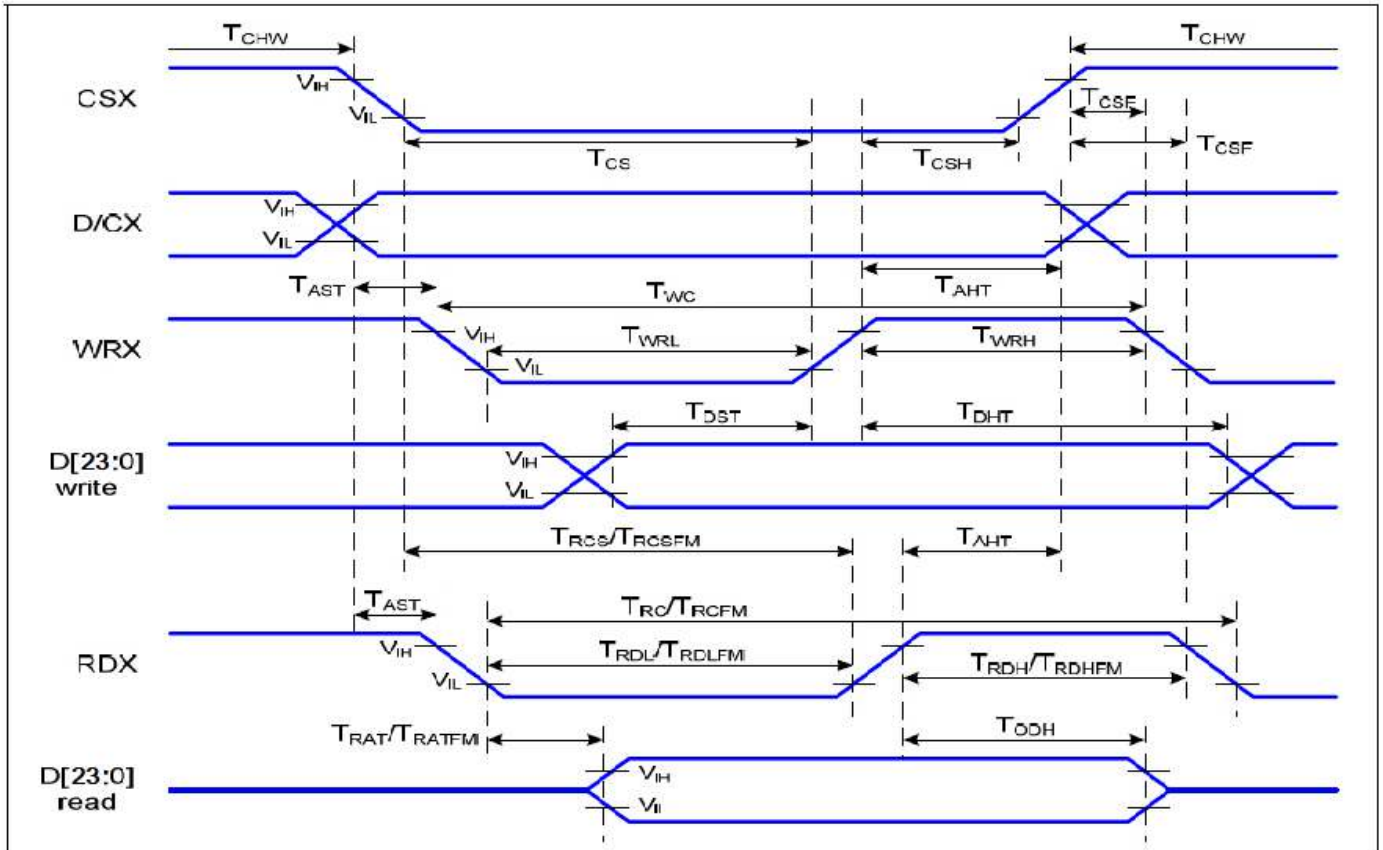## 6.2 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus



*Figure 6.2: 8080 MCU Parallel Interface Timing Diagram*

| Signal | Symbol | Parameter | Min | Max | Unit | Description |
|---|---|---|---|---|---|---|
| D/CX | $T_{AST}$ | Address setup time | 0 | - | ns | |
| | $T_{AHT}$ | Address hold time (Write/Read) | 0 | - | ns | |
| CSX | $T_{CHW}$ | Chip select "H" pulse width | 0 | - | ns | |
| | $T_{CS}$ | Chip select setup time (Write) | 15 | - | ns | |
| | $T_{RCS}$ | Chip select setup time (Read ID) | 45 | - | ns | |
| | $T_{RCSFM}$ | Chip select setup time (Read FM) | 355 | - | ns | |
| | $T_{CSF}$ | Chip select wait time (Write/Read) | 10 | - | ns | |
| | $T_{CSH}$ | Chip select hold time | 10 | - | ns | |
| WRX | $T_{WC}$ | Write cycle | 66 | - | ns | |
| | $T_{WRH}$ | Control pulse "H" duration | 15 | - | ns | |
| | $T_{WRL}$ | Control pulse "L" duration | 15 | | ns | |
| RDX (ID) | $T_{RC}$ | Read cycle (ID) | 160 | - | ns | When read ID data |
| | $T_{RDH}$ | Control pulse "H" duration (ID) | 90 | - | ns | |
| | $T_{RDL}$ | Control pulse "L" duration | 45 | - | ns | |
| RDX (FM) | $T_{RCFM}$ | Read cycle (FM) | 450 | - | ns | When read from frame memory |
| | $T_{RDHFM}$ | Control pulse "H" duration (FM) | 90 | - | ns | |
| | $T_{RDLFM}$ | Control pulse "L" duration (FM) | 355 | - | ns | |
| D[23:0], D[17:0], D[15:0], D[8:0], D[7:0] | $T_{DST}$ | Write data setup time | 10 | - | ns | For max CL=30pF For min CL=8pF |
| | $T_{DHT}$ | Write data hold time | 10 | - | ns | |
| | $T_{RAT}$ | Read access time (ID) | - | 40 | ns | |
| | $T_{RATFM}$ | Read access time (FM) | - | 340 | ns | |
| | $T_{ROD}$ | Output disable time | 20 | 80 | ns | |

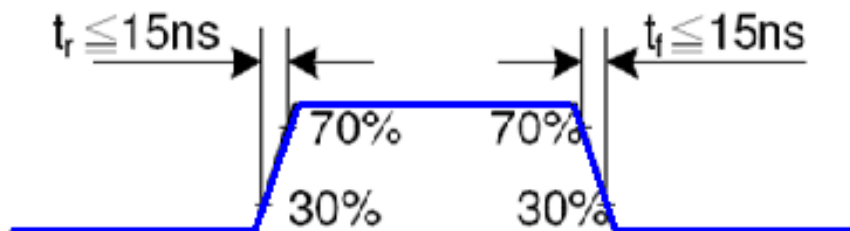*Table 6.2: 8080 MCU Parallel Interface Characteristics*

CSX timings:
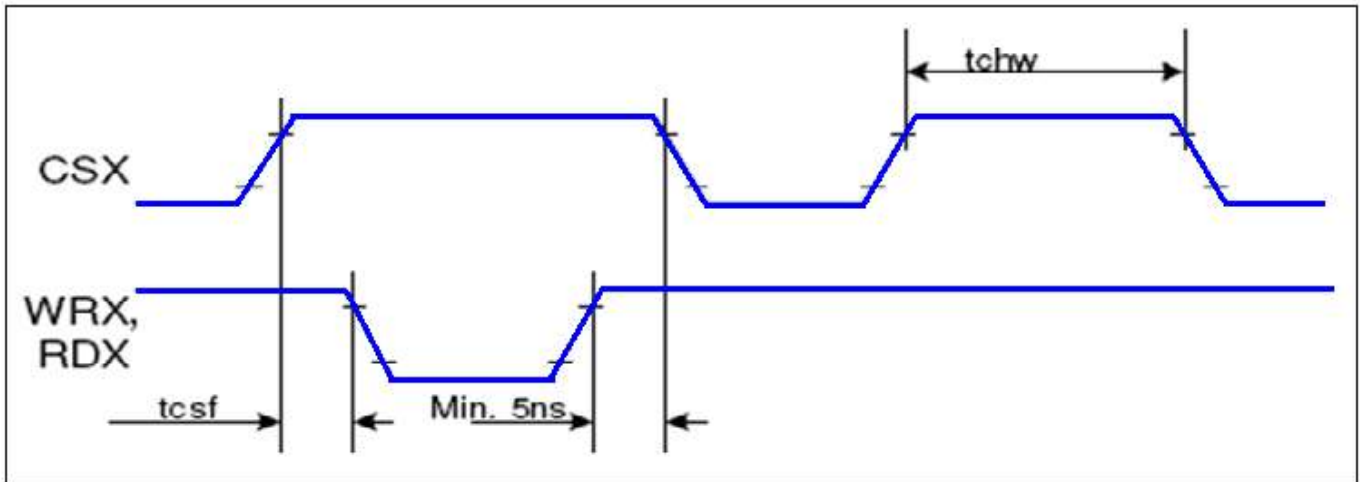


*Note: Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.*

Write to read or read to write timings:
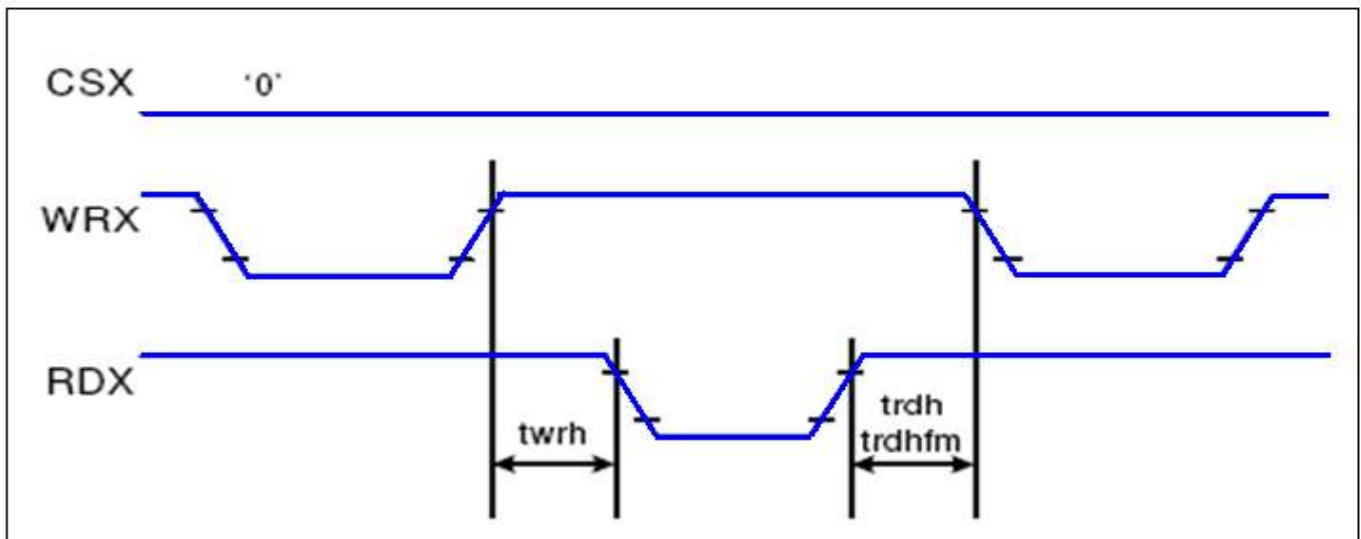


*Note: Ta = -30 to 70 C, IOVCC = 1.65V to 2.8V, VCI = 2.6V to 3.3V, GND = 0V.*

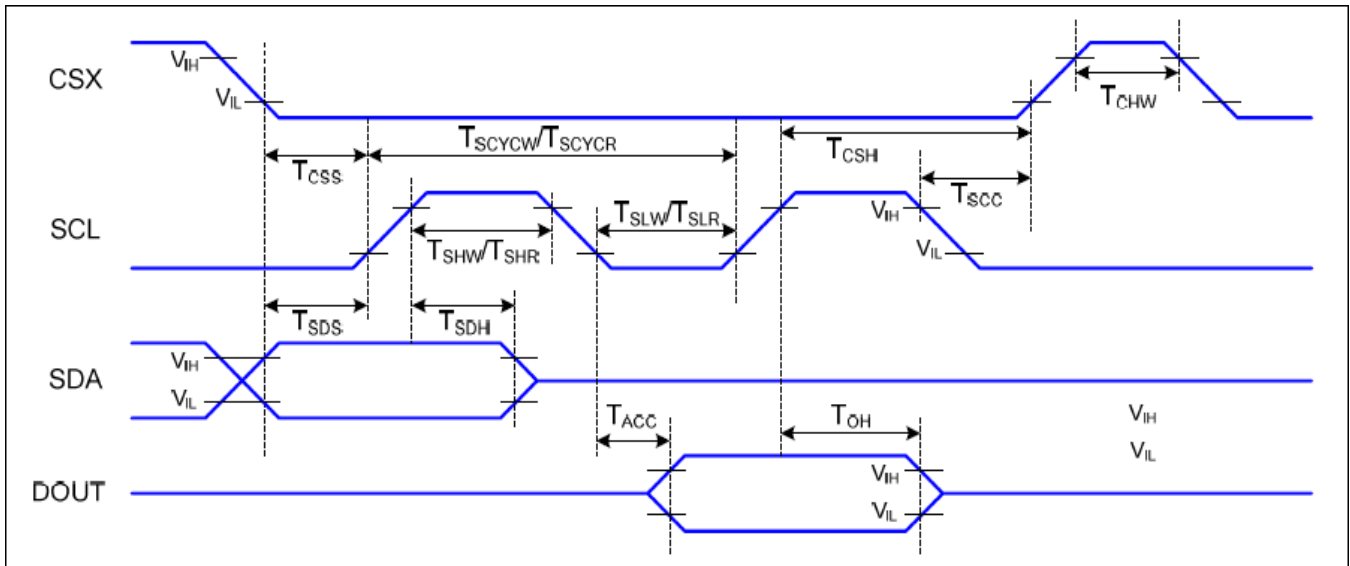## 6.3 Display Serial Interface Characteristics (3-line SPI system)



*Figure 6.3: Serial Interface 3-SPI Timing Diagram*

$VDDI = 1.64$ to $3.3V$, $VDD = 2.4$ to $3.3V$, $AGND=DGND=0V$, $Ta=-30$ to $70\ C^o$

| Signal | Symbol | Parameter | Min | Max | Unit | Description |
|--------|--------|-----------|-----|-----|------|-------------|
| CSX | $T_{CSS}$ | Chip select setup time (write) | 60 | | ns | |
| | $T_{CSH}$ | Chip select hold time (write) | 65 | | ns | |
| | $T_{CSS}$ | Chip select setup time (read) | 60 | | ns | |
| | $T_{SCC}$ | Chip select hold time (read) | 20 | | ns | |
| | $T_{CHW}$ | Chip select "H" pulse width | 40 | | ns | |
| SCL | $T_{SCYCW}$ | Serial clock cycle (write) | 100 | | ns | |
| | $T_{SHW}$ | SCL "H" pulse width (write) | 40 | | ns | |
| | $T_{SLW}$ | SCL "L" width (write) | 40 | | ns | |
| | $T_{SCYCR}$ | Serial clock cycle (read) | 150 | | ns | |
| | $T_{SHR}$ | SCL "H" pulse width (read) | 60 | | ns | |
| | $T_{SLR}$ | SCL "L" pulse width (read) | 60 | | ns | |
| SDA/SDI (Input) | $T_{SDS}$ | Data setup time (write) | 30 | | ns | |
| | $T_{SDH}$ | Data hold time (Write) | 30 | | | |
| SDA/SDO (Output) | $T_{ACC}$ | Access time (read) | 10 | 50 | ns | |
| | $T_{OH}$ | Output disable time (read) | 10 | 50 | ns | |

*Table 6.3: 3-line Serial Interface Timing Characteristics*

*Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals*

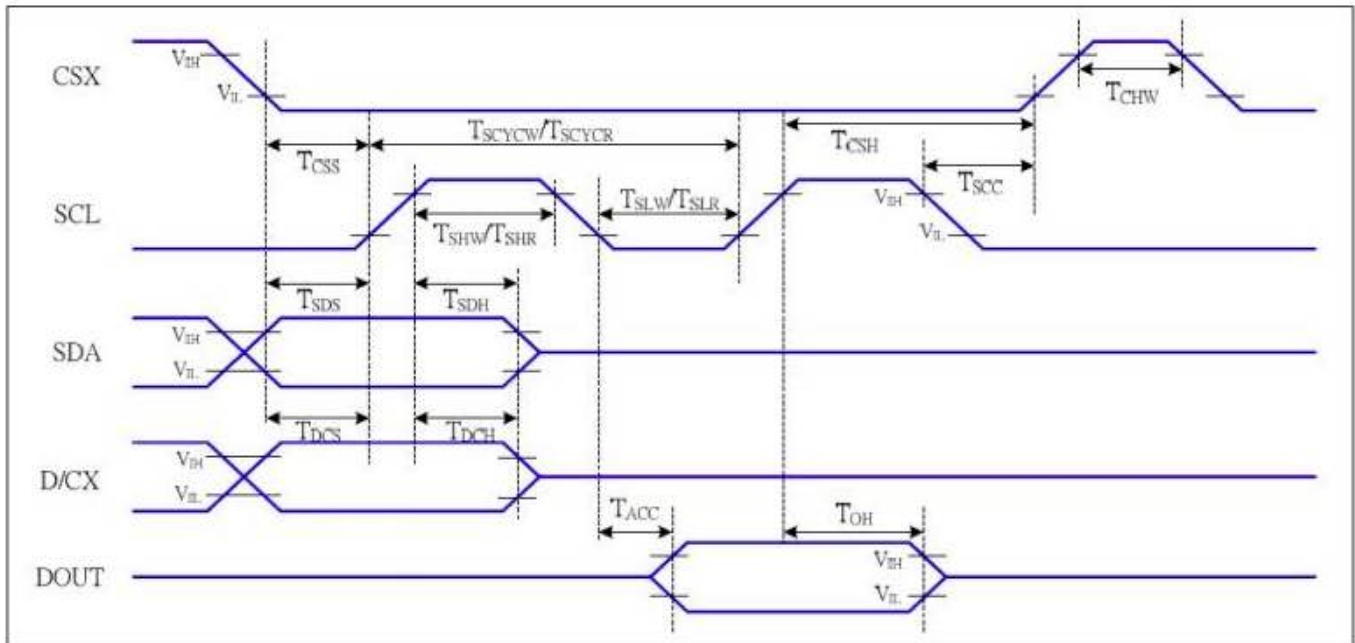## 6.4 Display Serial Interface Characteristics (4-line SPI serial)



*Figure 6.4: Serial Interface 4-SPI Timing Diagram*

| Signal | Symbol | Parameter | Min | Max | Unit | Description |
|---|---|---|---|---|---|---|
| CSX | $T_{CSS}$ | Chip select setup time (write) | 15 | | ns | |
| | $T_{CSH}$ | Chip select hold time (read) | 15 | | ns | |
| | $T_{CHW}$ | Chip select "H" pulse width | 40 | | ns | |
| SCL | $T_{SCYCW}$ | Serial clock cycle (write) | 50 | | ns | write command & data ram |
| | $T_{SHW}$ | SCL "H" pulse width (write) | 10 | | ns | |
| | $T_{SLW}$ | SCL "L" width (write) | 10 | | ns | |
| | $T_{SCYCR}$ | Serial clock cycle (read) | 150 | | ns | read command & data ram |
| | $T_{SHR}$ | SCL "H" pulse width (read) | 60 | | ns | |
| | $T_{SLR}$ | SCL "L" pulse width (read) | 60 | | ns | |
| D/CX | $T_{DCS}$ | D/CX setup time | 10 | | ns | |
| | $T_{DCH}$ | D/CX hold time | 10 | | ns | |
| SDA (DIN) | $T_{SDS}$ | Data setup time | 10 | | ns | |
| | $T_{SDH}$ | Data hold time | 10 | | ns | |
| DOUT | $T_{ACC}$ | Access time (read) | 10 | 50 | ns | For max CL=30pF For min CL=8pF |
| | $T_{OH}$ | Output disable time | 15 | 50 | ns | |

*Table 6.4: 4-line Serial Interface Timing Characteristics*

*Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.*
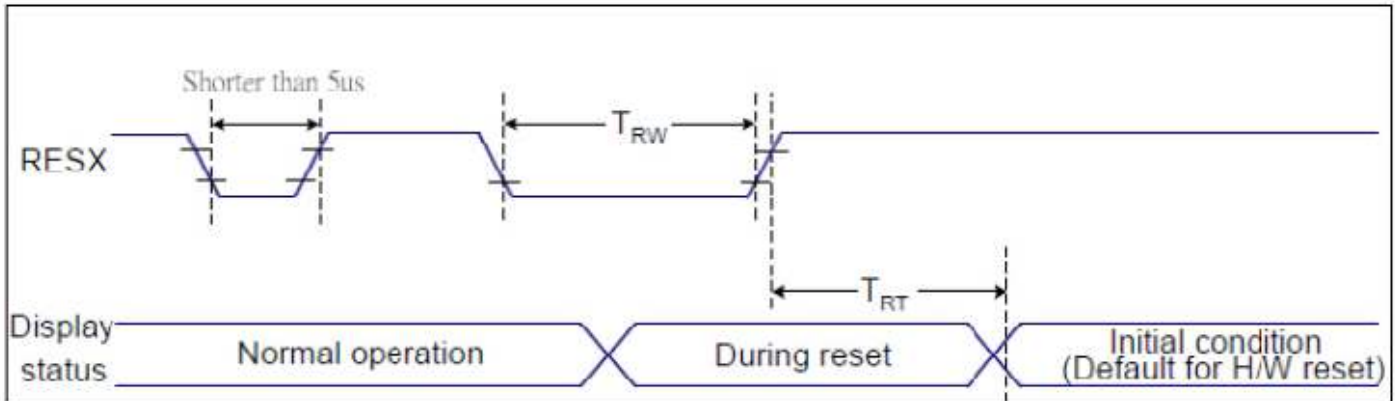
## 6.5    Reset Timing



*Figure 6.5: Reset Timing Diagram*

| Related Pins | Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| RESX | TRW | Reset pulse duration | 10 | - | us |
| | TRT | Reset cancel | - | 5 (Note 1,5) | ms |
| | | | | 120 (Note 1, 6, 7) | ms |

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

| RESX Pulse | Action |
|---|---|
| Shorter than 5us | Reset Rejected |
| Longer than 9us | Reset |
| Between 5us and 9 us | Reset starts |

3. During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:
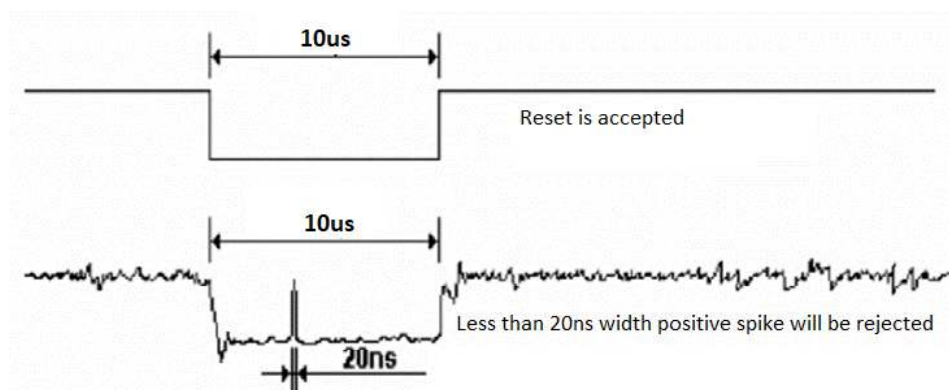


5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.

# 7. Cautions and Handling Precautions

## 7.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use finger stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the "Power ON" condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence

## 7.2 Storage and Transportation

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.