PTN3700

1.8 V simple mobile interface link bridge IC

Rev. 3 — 12 October 2011 | Product data sheet

1. General description

The PTN3700 is a 1.8 V simple mobile interface link bridge IC which can function both as a transmitter-serializer or a receiver-deserializer for RGB888 video data. When configured as transmitter (using input pin TX/RX), the PTN3700 serializes parallel CMOS video input data into 1, 2 or 3 subLVDS-based high-speed serial data channels. When configured as receiver, the PTN3700 deserializes up to 3 high-speed serial data channels into parallel CMOS video data signals.

The parallel interface of the PTN3700 is based on the conventional and widely used 24-bit wide data bus for RGB video data, plus active LOW HS (Horizontal Synchronization) and VS (Vertical Synchronization) signals, and an active HIGH DE (Data Enable) signal. An additional two auxiliary bits A[1:0] are provided to permit signaling of miscellaneous status or mode information across the link to the display. The serial interface link of the PTN3700 is based on the open Simple Mobile Interface Link (SMILi) definition. In order to keep power low while accommodating various display sizes (e.g., up to 24-bit, 60 frames per second XVGA), the number of high-speed serial channels ('lanes') is configurable from 1 to 3 depending on the bandwidth needed. The data link speed is determined by the PCLK (Pixel Clock) rate and the number of serial channels selected.

In order to maintain a low power profile, the PTN3700 has three power modes, determined by detection of an active input clock and by shutdown pin XSD. In Shutdown mode (XSD = LOW), the PTN3700 is completely inactive and consumes a minimum of current. In Standby mode (XSD = HIGH), the device is ready to switch to Active mode as soon as an active input clock signal is detected, and assume normal link operation.

In Transmitter mode, the PTN3700 performs parity calculation on the input data (R[7:0], G[7:0], B[7:0] plus HS, VS and DE data bits) and adds an odd parity bit CP to the serial transmitted data stream. The PTN3700 in Receiver mode also integrates a parity checking function, which checks for odd parity across the decoded input word (R[7:0], G[7:0], B[7:0] plus HS, VS and DE data bits), and indicates whether a parity error has occurred on its CPO out pin (active HIGH). When a parity error occurs, the most recent error-free pixel data will be output instead of the received invalid pixel data.

PTN3700 in Receiver mode offers an optional advanced frame mixing feature, which allows 18-bit displays to effectively display 24-bit color resolution by applying a patent-pending pixel data processing algorithm to the 24-bit video input data.

One of two serial transmission methods is selectable: pseudo source synchronous transmission based on the pixel clock, or true source synchronous transmission based on the bit clock. The latter uses a patent-pending methodology characterized by zero overhead and operation guaranteed free from false pixel synchronization.

The PTN3700 automatically rotates the order of the essential signals (parallel CMOS and high-speed serial data and clock) depending on whether it is operating as transmitter or as receiver (using pin TX/$\overline{\text{RX}}$). In addition, two Pinning Select bits (inputs PSEL[1:0]) allow for four additional signal order configurations. This allows for various topologies of printed circuit board or flex foil layout without crossing of traces, and enables the easy introduction of PTN3700 into an existing 'parallel' design avoiding board re-layout.

The PTN3700 is available in a 56-ball VFBGA package and operates across a temperature range of –40 °C to +85 °C.

2. Features and benefits

- Configurable as either Transmitter or Receiver
- One of two serial transmission methods selectable (pixel clock referenced pseudo source synchronous or bit clock referenced true source synchronous)
- 3 differential subLVDS high-speed serial lanes
- One differential pixel clock
- Configurable aggregate data bandwidth allowing up to 24-bit color, 60 fps XGA:
    - 1 lane at 30× serialization rate up to 650 Mbit/s
    - 2 lanes at 15× serialization rate up to 1300 Mbit/s
    - 3 lanes at 10× serialization rate up to 1.95 Gbit/s
- Parity encoding (transmitter) and detection (receiver) with last valid pixel repetition
- Advanced Frame Mixing function (in Receiver mode) for 24-bit color depth using conventional 18-bit displays or specially adapted '18-bit plus' displays
- Parallel CMOS I/O based on interface definition of RGB888 plus $\overline{\text{HS}}$, $\overline{\text{VS}}$, DE
- Very low power profile:
    - Shutdown mode for minimum idle power (< 3 μA typical)
    - Low-power Standby mode with input clock frequency auto-detect (< 3 μA typical)
    - Low active transmitter power: 18 mW (typ.) for QVGA[1] and 40 mW (typ.) for WVGA[2]
    - Low active receiver power: 15 mW (typ.) for QVGA and 36 mW (typ.) for WVGA
- Slew rate control on receiver parallel CMOS outputs
- Operates from a single 1.8 V ± 150 mV power supply
- Configurable mirroring pinout (dependent on Tx or Rx mode and PSEL[1:0] inputs) for optimum single layer flex-foil flow-through in various application scenarios
- Available in 56-ball VFBGA package

3. Applications

- High-resolution mobile phones
- Portable applications with video display capability

1. QVGA: 240 × 320 pixels at 60 Hz frame rate; 20 % non-active display data overhead; PCLK at 5.5 MHz; one-lane operation at 166 Mbit/s; 24-bit color data.
2. WVGA: 854 × 480 pixels at 60 Hz frame rate; 20 % non-active display data overhead; PCLK at 29.5 MHz; two-lane operation at 885.4 Mbit/s; 24-bit color data.

4. Ordering information

Table 1. Ordering information

Type number	Solder process	Package		
		Name	Description	Version
PTN3700EV/G	Pb-free (SnAgCu solder ball compound)	VFBGA56	plastic very thin fine-pitch ball grid array package; 56 balls; body 4 × 4.5 × 0.65 mm[1]	SOT991-1

[1] 0.5 mm ball pitch; 1.0 mm maximum package height.

4.1 Ordering options

Table 2. Ordering options

Type number	Topside mark	Temperature range
PTN3700EV/G	3700	−40 °C to +85 °C

5. Functional diagram

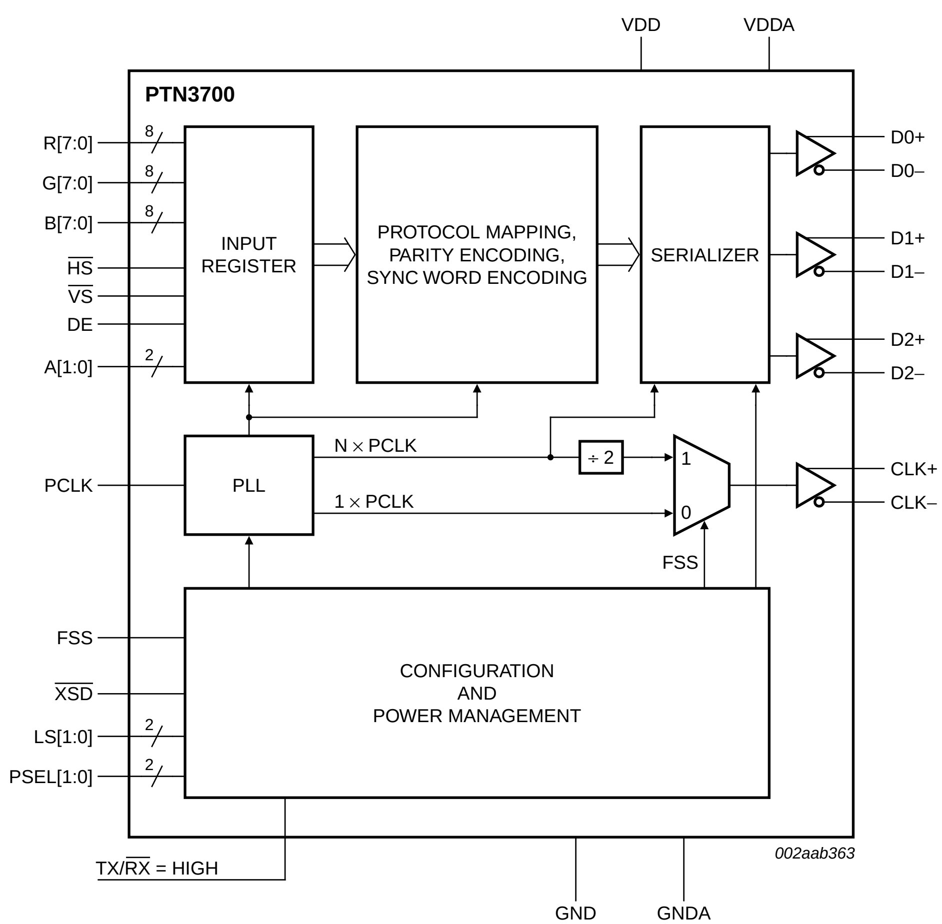


Fig 1. Functional diagram of PTN3700 in Transmitter mode

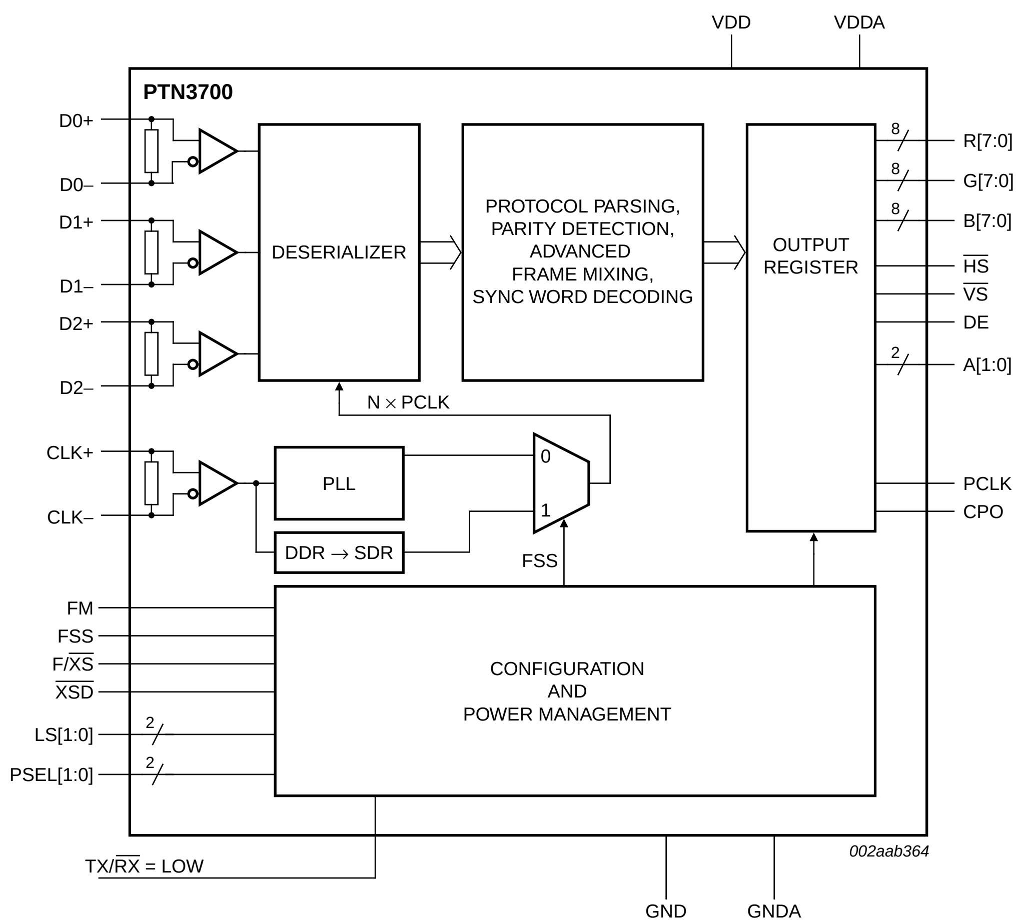
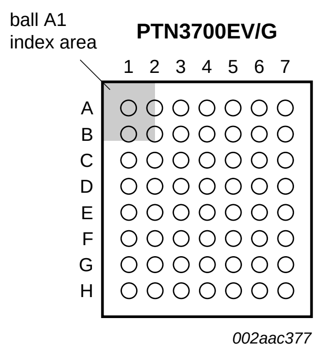


Fig 2. Functional diagram of PTN3700 in Receiver mode

6. Pinning information

6.1 Pinning



Transparent top view

Fig 3. Ball configuration for VFBGA56

	1	2	3	4	5	6	7
A	D2+	VDDA	DE	$\overline{\text{HS}}$	B0	B2	B4
B	D2–	GNDA	$\overline{\text{VS}}$	PCLK	B1	B3	B5
C	D1+	TX/$\overline{\text{RX}}$	A1	GND	VDD	B6	B7
D	D1–	VDD	PSEL0	LS0	FM	G0	G1
E	CLK+	GND	PSEL1	LS1	FSS	G2	G3
F	CLK–	F/$\overline{\text{XS}}$	A0	GND	VDD	G4	G5
G	D0+	$\overline{\text{XSD}}$	R6	R4	R2	R0	G6
H	D0–	CPO	R7	R5	R3	R1	G7

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56-ball, 7 × 8 grid; transparent top view

Fig 4. VFBGA56 ball mapping - Transmitter mode (TX/$\overline{\text{RX}}$ = HIGH); PSEL[1:0] = 00b

	1	2	3	4	5	6	7
A	D2+	VDDA	DE	$\overline{\text{HS}}$	R7	R5	R3
B	D2–	GNDA	$\overline{\text{VS}}$	PCLK	R6	R4	R2
C	D1+	TX/$\overline{\text{RX}}$	A1	GND	VDD	R1	R0
D	D1–	VDD	PSEL0	LS0	FM	G7	G6
E	CLK+	GND	PSEL1	LS1	FSS	G5	G4
F	CLK–	F/$\overline{\text{XS}}$	A0	GND	VDD	G3	G2
G	D0+	$\overline{\text{XSD}}$	B1	B3	B5	B7	G1
H	D0–	CPO	B0	B2	B4	B6	G0

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56-ball, 7 × 8 grid; transparent top view

Fig 5. VFBGA56 ball mapping - Transmitter mode (TX/$\overline{\text{RX}}$ = HIGH); PSEL[1:0] = 01b

	1	2	3	4	5	6	7
A	D0–	VDDA	DE	$\overline{\text{HS}}$	B0	B2	B4
B	D0+	GNDA	$\overline{\text{VS}}$	PCLK	B1	B3	B5
C	CLK–	TX/$\overline{\text{RX}}$	A1	GND	VDD	B6	B7
D	CLK+	VDD	PSEL0	LS0	FM	G0	G1
E	D1–	GND	PSEL1	LS1	FSS	G2	G3
F	D1+	F/$\overline{\text{XS}}$	A0	GND	VDD	G4	G5
G	D2–	$\overline{\text{XSD}}$	R6	R4	R2	R0	G6
H	D2+	CPO	R7	R5	R3	R1	G7

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56-ball, 7 × 8 grid; transparent top view

Fig 6. VFBGA56 ball mapping - Transmitter mode (TX/$\overline{\text{RX}}$ = HIGH); PSEL[1:0] = 10b

	1	2	3	4	5	6	7
A	D0–	VDDA	DE	$\overline{\text{HS}}$	R7	R5	R3
B	D0+	GNDA	$\overline{\text{VS}}$	PCLK	R6	R4	R2
C	CLK–	TX/$\overline{\text{RX}}$	A1	GND	VDD	R1	R0
D	CLK+	VDD	PSEL0	LS0	FM	G7	G6
E	D1–	GND	PSEL1	LS1	FSS	G5	G4
F	D1+	F/$\overline{\text{XS}}$	A0	GND	VDD	G3	G2
G	D2–	$\overline{\text{XSD}}$	B1	B3	B5	B7	G1
H	D2+	CPO	B0	B2	B4	B6	G0

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56-ball, 7 × 8 grid; transparent top view

Fig 7. VFBGA56 ball mapping - Transmitter mode (TX/$\overline{\text{RX}}$ = HIGH); PSEL[1:0] = 11b

	1	2	3	4	5	6	7
A	D2+	VDDA	R7	R5	R3	R1	G7
B	D2–	GNDA	R6	R4	R2	R0	G6
C	D1+	TX/$\overline{RX}$	A1	GND	VDD	G5	G4
D	D1–	VDD	PSEL0	LS0	FM	G3	G2
E	CLK+	GND	PSEL1	LS1	FSS	G1	G0
F	CLK–	F/$\overline{XS}$	A0	GND	VDD	B7	B6
G	D0+	$\overline{XSD}$	$\overline{VS}$	PCLK	B1	B3	B5
H	D0–	CPO	DE	$\overline{HS}$	B0	B2	B4

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56-ball, 7 × 8 grid; transparent top view

Fig 8. VFBGA56 ball mapping - Receiver mode (TX/$\overline{RX}$ = LOW); PSEL[1:0] = 00b

	1	2	3	4	5	6	7
A	D2+	VDDA	B0	B2	B4	B6	G0
B	D2–	GNDA	B1	B3	B5	B7	G1
C	D1+	TX/$\overline{RX}$	A1	GND	VDD	G2	G3
D	D1–	VDD	PSEL0	LS0	FM	G4	G5
E	CLK+	GND	PSEL1	LS1	FSS	G6	G7
F	CLK–	F/$\overline{XS}$	A0	GND	VDD	R0	R1
G	D0+	$\overline{XSD}$	$\overline{VS}$	PCLK	R6	R4	R2
H	D0–	CPO	DE	$\overline{HS}$	R7	R5	R3

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56-ball, 7 × 8 grid; transparent top view

Fig 9. VFBGA56 ball mapping - Receiver mode (TX/$\overline{RX}$ = LOW); PSEL[1:0] = 01b

	1	2	3	4	5	6	7
A	D0–	VDDA	R7	R5	R3	R1	G7
B	D0+	GNDA	R6	R4	R2	R0	G6
C	CLK–	TX/$\overline{RX}$	A1	GND	VDD	G5	G4
D	CLK+	VDD	PSEL0	LS0	FM	G3	G2
E	D1–	GND	PSEL1	LS1	FSS	G1	G0
F	D1+	F/$\overline{XS}$	A0	GND	VDD	B7	B6
G	D2–	$\overline{XSD}$	$\overline{VS}$	PCLK	B1	B3	B5
H	D2+	CPO	DE	$\overline{HS}$	B0	B2	B4

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56-ball, 7 × 8 grid; transparent top view

Fig 10. VFBGA56 ball mapping - Receiver mode (TX/$\overline{RX}$ = LOW); PSEL[1:0] = 10b

	1	2	3	4	5	6	7
A	D0–	VDDA	B0	B2	B4	B6	G0
B	D0+	GNDA	B1	B3	B5	B7	G1
C	CLK–	TX/$\overline{RX}$	A1	GND	VDD	G2	G3
D	CLK+	VDD	PSEL0	LS0	FM	G4	G5
E	D1–	GND	PSEL1	LS1	FSS	G6	G7
F	D1+	F/$\overline{XS}$	A0	GND	VDD	R0	R1
G	D2–	$\overline{XSD}$	$\overline{VS}$	PCLK	R6	R4	R2
H	D2+	CPO	DE	$\overline{HS}$	R7	R5	R3

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56-ball, 7 × 8 grid; transparent top view

Fig 11. VFBGA56 ball mapping - Receiver mode (TX/$\overline{RX}$ = LOW); PSEL[1:0] = 11b

6.2 Pin description

Table 3. Pin description - Transmitter mode

Symbol	Pin[1]	Type	Description
Parallel data inputs			
R[7:0], G[7:0], B[7:0]		CMOS	8-bit wide R, G, B pixel data inputs
$\overline{HS}$		CMOS	Horizontal synchronization data input, active LOW
$\overline{VS}$		CMOS	Vertical synchronization data input, active LOW
DE		CMOS	Data Enable input, active HIGH
A0, A1		CMOS	Auxiliary input bits
High-speed serial outputs			
D0+, D0−, D1+, D1−, D2+, D2−		SubLVDS driver	Serialized high-speed differential subLVDS data outputs
CLK+, CLK−		SubLVDS driver	Serialized high-speed differential subLVDS clock outputs
Clock inputs			
PCLK		CMOS	Pixel clock reference input
Configuration inputs			
TX/$\overline{RX}$		CMOS	Transmitter/Receiver configuration input pin. When HIGH, PTN3700 is configured as transmitter.
LS0, LS1		CMOS	Serialization mode program pins. Select between 1, 2 or 3 lanes. See Table 5.
PSEL0, PSEL1		CMOS	Pin mirroring select pins. See Table 6 and Table 7
$\overline{XSD}$		CMOS	Shutdown mode input pin, active LOW, puts PTN3700 in lowest-power mode by deactivating all circuitry. When HIGH, PTN3700 is either in Active mode or awaiting clock input (Standby mode)
FSS		CMOS	Fully Source Synchronous select pin. When LOW, PTN3700 uses pseudo source synchronous serial transmission mode with the pixel clock as both the reference frequency and the frame boundary delineation. When HIGH, PTN3700 uses true source synchronous transmission with a serial Double Data Rate (DDR) bit clock for the serial data. Embedded synchronization words are encoded for pixel synchronization. On both Receiver and Transmitter, the settings of the FSS pin should match. Otherwise the link will not function.
Power supply			
VDD		power	power supply voltage
VDDA		power	analog (PLL) power supply voltage
GNDA		ground	analog (PLL) ground
GND		ground	ground
Miscellaneous			
CPO, FM, F/$\overline{XS}$		CMOS	Signals are inactive in Transmitter mode and should be tied down to GND.

[1] Depends on configuration.

Table 4. Pin description - Receiver mode

Symbol	Pin[1]	Type	Description
Parallel data outputs			
R[7:0], G[7:0], B[7:0]		CMOS	8-bit wide R, G, B pixel data outputs
$\overline{\text{HS}}$		CMOS	Horizontal synchronization data output, active LOW
$\overline{\text{VS}}$		CMOS	Vertical synchronization data output, active LOW
DE		CMOS	Data Enable output, active HIGH
A0, A1		CMOS	Auxiliary output bits
High-speed serial inputs			
D0+, D0−, D1+, D1−, D2+, D2−		SubLVDS receiver	Serialized high-speed differential subLVDS data inputs
CLK+, CLK−		SubLVDS receiver	Serialized high-speed differential subLVDS clock inputs
Clock outputs			
PCLK		CMOS	Pixel clock output
Configuration inputs			
TX/$\overline{\text{RX}}$		CMOS	Transmitter/Receiver configuration input pin. When LOW, PTN3700 is configured as receiver.
LS0, LS1		CMOS	Serialization mode program pins. Select between 1, 2 or 3 lanes. See Table 5.
PSEL0, PSEL1		CMOS	Pin mirroring select pins. See Table 6 and Table 7.
$\overline{\text{XSD}}$		CMOS	Shutdown mode input pin, active LOW, puts PTN3700 in lowest-power mode by deactivating all circuitry. When HIGH, PTN3700 is either in Active mode or awaiting clock input (Standby mode).
F/$\overline{\text{XS}}$		CMOS	Program pin for fast (F/$\overline{\text{XS}}$ = HIGH) or slow (F/$\overline{\text{XS}}$ = LOW) parallel output and PCLK slew rate
FM		CMOS	Frame Mixing select pin. When LOW, Frame Mixing is disabled and PTN3700 passes 24-bit video data transparently. When HIGH, Frame Mixing is enabled and PTN3700 applies processing to the 24-bit video data resulting in 18-bit output data words encoded with 24-bit color depth. Frame Mixing is only available in Receiver mode.
FSS		CMOS	Fully Source Synchronous select pin. When LOW, PTN3700 uses pseudo source synchronous serial reception mode with the pixel clock as both the reference frequency and the frame boundary delineation. When HIGH, PTN3700 uses true source synchronous reception with embedded synchronization word decoding, with the bit clock as reference frequency. On both Receiver and Transmitter, the settings of the FSS pin should match. Otherwise the link will not function.
Parity output			
CPO		CMOS	Parity error output, active HIGH. A HIGH level indicates a parity error was detected in the current pixel data
Power supply			
VDD			power supply voltage
VDDA			analog (PLL) power supply voltage
GNDA			analog (PLL) ground
GND			ground

[1] Depends on configuration.

7. Functional description

7.1 General

A complete simple mobile interface link consists of one PTN3700 configured as transmitter (see Figure 1); two, three or four differential-pair high-speed signaling channels; and one PTN3700 configured as receiver (see Figure 2). Link power and ground are supplied to pins VDD and GND respectively (power and ground should be routed and decoupled to analog supply pin VDDA and ground pin GNDA separately for lowest jitter operation). Configuration of either transmitter or receiver mode is achieved by strapping the CMOS input pin TX/$\overline{\text{RX}}$ HIGH or LOW, respectively.

Configured as transmitter, PTN3700 accepts parallel CMOS input data including color pixel data (R[7:0], G[7:0], B[7:0]), three control bits $\overline{\text{HS}}$ (horizontal synchronization), $\overline{\text{VS}}$ (vertical synchronization), DE (data enable), auxiliary bits A[1:0] and pixel clock PCLK. The PTN3700 calculates a parity bit (excluding the auxiliary bits, see Section 7.6) and serializes the data and outputs as a high-speed serial data stream on up to three subLVDS differential outputs (D0+, D0–, D1+, D1–, D2+, D2–) depending on the serialization mode selected by pins LS[1:0] (see Section 7.2). An integrated low-jitter PLL generates internally the bit clock used for serialization of video input data, parity bit and control bits, and outputs along with the serial output data a differential pixel clock on differential subLVDS output pair CLK+ and CLK–.

Configured as receiver, PTN3700 accepts serial differential data inputs D0+, D0–, D1+, D1–, D2+, D2– and differential input clock CLK+ and CLK– from the signaling channel and deserializes the received data into parallel output data on pins R[7:0], G[7:0], B[7:0], $\overline{\text{HS}}$, $\overline{\text{VS}}$, DE and A[1:0] along with the PLL-regenerated pixel clock PCLK. Also, a parity checking function is performed on the incoming R[7:0], G[7:0], B[7:0], $\overline{\text{HS}}$, $\overline{\text{VS}}$, DE bits and an error flagged by signaling a HIGH state on CMOS output pin CPO (see Section 7.6). Serialization mode pins LS[1:0] need to be selected according to the expected serialization mode (see Section 7.2) to correctly receive and decode the up to three subLVDS differential serial inputs. To minimize EMI, the parallel outputs can be configured by tying pin F/$\overline{\text{XS}}$ either HIGH or LOW to output fast or slow output slew rates respectively.

The PTN3700 is capable of operating in either of two distinct transmission modes: Pseudo Source Synchronous mode (PSS), and Full (or 'true') Source Synchronous mode (FSS), selected by CMOS input pin FSS. In PSS mode, the pixel clock PCLK is used both as the transmission frequency reference and its rising edge as the delineation of the start of a pixel. This transmission mode relies on the Receiver PLL to reconstruct the bit clock at the receiving end. In FSS mode, the bit clock is transmitted (in DDR mode) instead of the pixel clock. Rather than achieve frame boundary detection using the pixel clock edge as in PSS mode, in FSS mode the Transmitter encodes 'synchronization words' over the link which are detected and used for data to pixel alignment by the Receiver. This methodology guarantees false-synchronization-free transmission with zero protocol overhead.

The PTN3700 can be put into very low 'Shutdown' power state by tying CMOS input pin $\overline{\text{XSD}}$ LOW. Additionally, the PTN3700 will automatically enter a low-power 'Standby' mode when no active input clock is detected on its inputs (see Section 7.5).

7.2 Link programmability

The number of high-speed serial channels used is programmed by CMOS input pins LS[1:0]. For a given link consisting of a transmitter and receiver pair of PTN3700's, the number of channels used must be programmed identically or the link will malfunction. The PTN3700, once programmed, will assume the corresponding serialization ratio as shown in Table 5. When pins LS[1:0] are both HIGH, the PTN3700 is put in a test mode which is used for production testing purposes only and should not be used in application.

The 1-lane mode is typically meant for smaller video display formats (e.g., QVGA to HVGA), while the 2-lane mode is typically used for display formats like HVGA and VGA. The 3-lane mode supports larger display formats such as VGA or XGA. Please see Section 12.1 for more information.

Table 5. Link programmability

LS1	LS0	Mode	Number of high-speed serial channels	Supported PCLK frequency range (MHz)	Guaranteed data bandwidth per channel (Mbit/s)	Guaranteed aggregate link bandwidth (Mbit/s)
L	L	00	1	4.0 to 21.6	120 to 650	650
L	H	01	2	8.0 to 43.3	120 to 650	1300
H	L	10	3	20.0 to 65.0	200 to 650	1950
H	H	11	reserved[1]	reserved	reserved	reserved

[1] Mode 11 is used for test purposes only.

7.3 Versatile signal mirroring programmability

In order to provide flexibility for different signal order and flow requirements in different applications, the PTN3700 can be programmed to mirror its signal order for the parallel and serial I/Os independently using the PSEL[1:0] inputs. The signal order also changes as a function of the TX/$\overline{RX}$ input by mirroring signals in such a way that the Transmitter and Receiver in a given link can be connected without signal crossings by simply opposing the two instances of PTN3700 and rotating one of them by 180 degrees. The truth table for the versatile signal mirroring scheme is shown in Table 6 and Table 7. The individual ball mappings are given in Figure 4 through Figure 11.

Table 6. Versatile signal mirroring programmability - Parallel I/O

Ball location[1]	TX/$\overline{RX}$			
	L		H	
	PSEL0			
	L	H	L	H
	(Receive mode)		(Transmit mode)	
H3	DE	DE	R7	B0
G3	$\overline{VS}$	$\overline{VS}$	R6	B1
H4	$\overline{HS}$	$\overline{HS}$	R5	B2
G4	PCLK	PCLK	R4	B3
H5	B0	R7	R3	B4
G5	B1	R6	R2	B5
H6	B2	R5	R1	B6
G6	B3	R4	R0	B7
H7	B4	R3	G7	G0
G7	B5	R2	G6	G1
F7	B6	R1	G5	G2
F6	B7	R0	G4	G3
E7	G0	G7	G3	G4
E6	G1	G6	G2	G5
D7	G2	G5	G1	G6
D6	G3	G4	G0	G7
C7	G4	G3	B7	R0
C6	G5	G2	B6	R1
B7	G6	G1	B5	R2
A7	G7	G0	B4	R3
B6	R0	B7	B3	R4
A6	R1	B6	B2	R5
B5	R2	B5	B1	R6
A5	R3	B4	B0	R7
B4	R4	B3	PCLK	PCLK
A4	R5	B2	$\overline{HS}$	$\overline{HS}$
B3	R6	B1	$\overline{VS}$	$\overline{VS}$
A3	R7	B0	DE	DE

[1] For PTN3700EV/G VFBGA56 package option. See also Figure 4 through Figure 11.

Table 7. Versatile signal mirroring programmability - Serial I/O

Ball location[1]	PSEL1	
	L	H
A1	D2+	D0–
B1	D2–	D0+
C1	D1+	CLK-
D1	D1–	CLK+
E1	CLK+	D1–
F1	CLK–	D1+
G1	D0+	D2–
H1	D0–	D2+

[1] For PTN3700EV/G VFBGA56 package option. See also Figure 4 through Figure 11.

7.4 High-speed data channel protocol options

The PTN3700 maps the transmission protocol in accordance with the serialization mode selected by pins LS[1:0]. In Mode 00 (1-channel), all RGB, parity and synchronization bits are serialized onto a single 30-bit sequence. In Mode 01 (2-channel), these bits are mapped onto two simultaneous 15-bit sequences divided across two lanes. In Mode 10 (3-channel), the 30 bits are serialized onto three simultaneous 10-bit sequences.

The serial bit mapping is different between pseudo-source-synchronous mode (FSS = LOW) and fully source-synchronous mode (FSS = HIGH). The mapping of the data bits in pseudo-source synchronous mode is shown in Figure 12, Figure 13 and Figure 14. (Note that the CLK in Mode 01 has an asymmetrical duty cycle of 8/15). The serial bit mapping in fully source-synchronous mode is shown in Figure 15, Figure 16 and Figure 17. Note that the fully source synchronous transmission mode is not dependent on the phase of PCLK for receiver synchronization.

7.4.1 Serial protocol bit mapping - pseudo source synchronous mode (FSS = LOW)

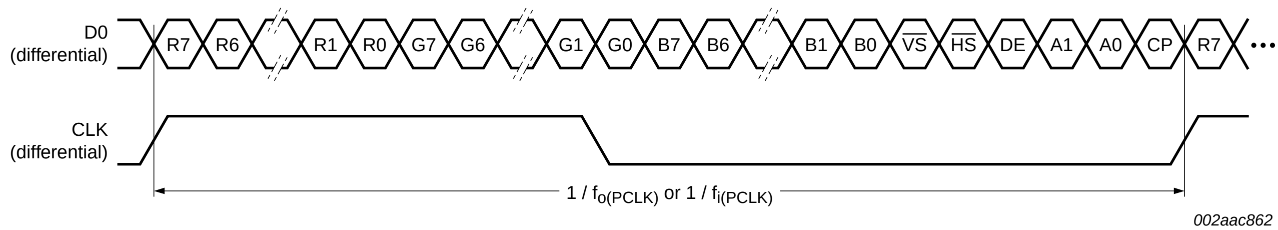


Fig 12. Mode 00 - single serial data channel mode (FSS = LOW)

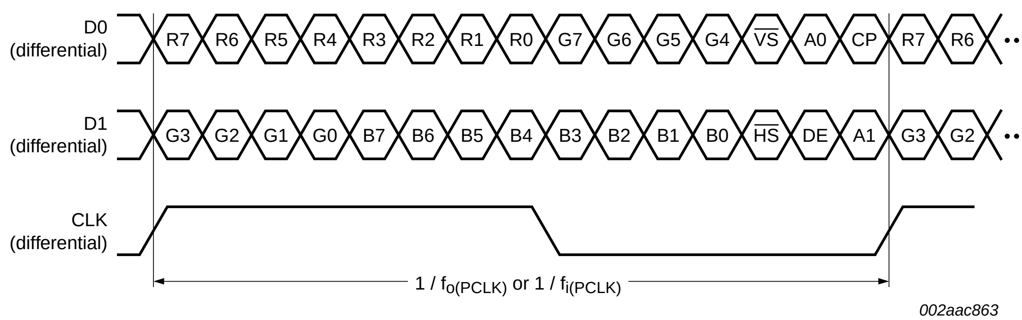


Fig 13. Mode 01 - dual serial data channel mode (FSS = LOW)

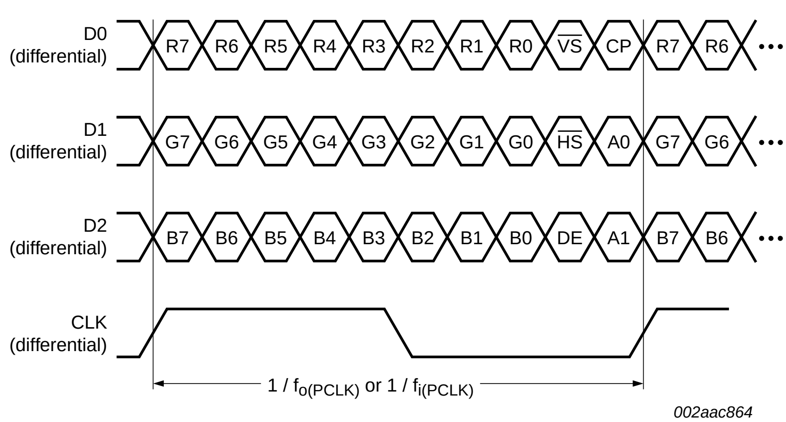


Fig 14. Mode 10 - triple serial data channel mode (FSS = LOW)

7.4.2 Serial protocol bit mapping - fully source synchronous mode (FSS = HIGH)

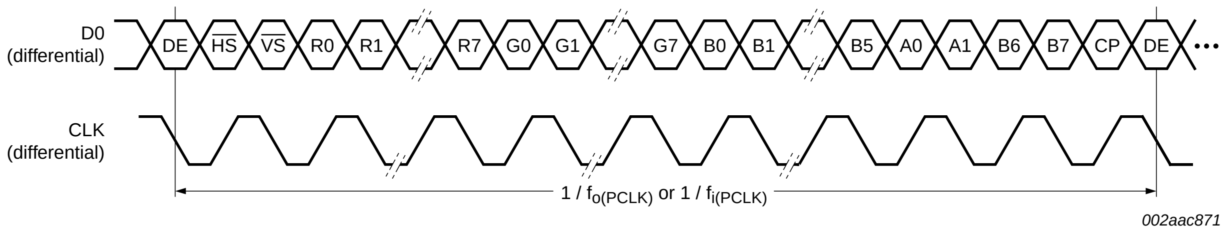


Fig 15. Mode 00 - single serial data channel mode (FSS = HIGH)

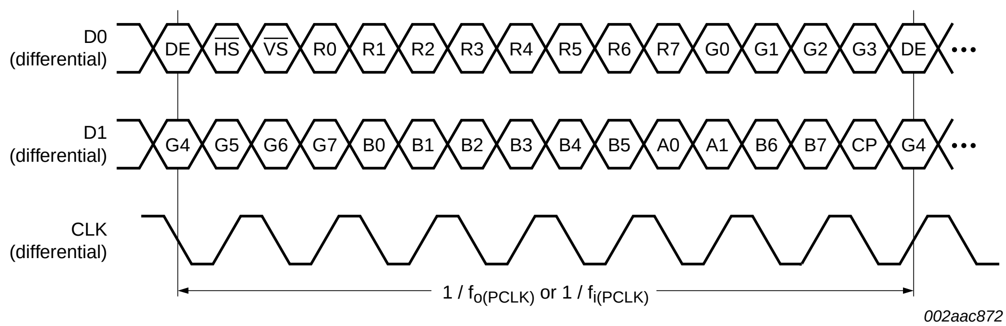


Fig 16. Mode 01 - dual serial data channel mode (FSS = HIGH)

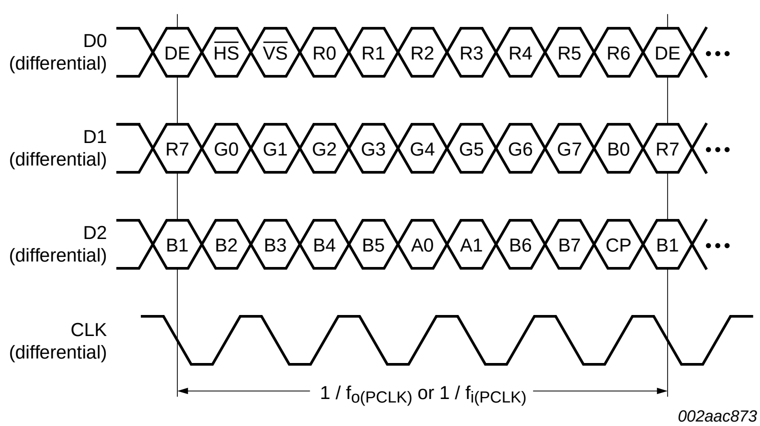


Fig 17. Mode 10 - triple serial data channel mode (FSS = HIGH)

7.4.3 PLL, PCLK, CLK and pixel synchronization

7.4.3.1 Pixel synchronization

PSS mode: The serial clock CLK provides the word boundaries explicitly for frame synchronization. At the receiver side, a PLL is needed to re-generate the bit clock, translating to a higher receiver power dissipation.

FSS mode: The serial clock CLK is truly synchronous with the serial data. Embedded synchronization words are transmitted in the non-active display area for pixel synchronization. The receiver PLL is powered down during this mode, hence the lower power consumption when compared with PSS mode. The special embedded synchronization words are guaranteed by design to never trigger false synchronization.

7.4.3.2 PLL

The PLL locks onto the PCLK input during transmit mode or the CLK input during receiver mode. It generates an internal high-speed clock, which is phase-aligned to the input clock. The PLL logic uses the lane select and transmit/receive status to determine the necessary PLL bandwidth settings and PLL divider values automatically. The PLL is able to track spread spectrum clocking to reduce EMI. The spread spectrum clock modulation frequency can be from 30 kHz to 33 kHz.

Transmitter: The internally generated clock is always aligned to the input clock PCLK.

- PSS mode: Refer to Section 7.4.1.
- FSS mode: The output clock CLK is Double Data Rate (DDR) and both clock edges are aligned to the data output.

Receiver:

- PSS mode: The PLL generates an internal clock at serial bit frequency and locks to the input clock CLK.
- FSS mode: The receiver uses Double Data Rate (DDR) input clock CLK, which is aligned to the data already.

7.4.4 $\overline{\text{HS}}$, $\overline{\text{VS}}$ and DE signal usage in various PTN3700 modes

When frame mixing is not used in PSS mode, $\overline{\text{VS}}$, $\overline{\text{HS}}$, DE, R[7:0], G[7:0], B[7:0] are treated as arbitrary user data. In this mode, PTN3700 functions as a pure serializer and deserializer, and is unaware of the meaning or polarity of $\overline{\text{VS}}$, $\overline{\text{HS}}$, DE, R[7:0], G[7:0], B[7:0]. In FSS mode, PTN3700 makes use of $\overline{\text{VS}}$, $\overline{\text{HS}}$ and DE to implement pixel synchronization with embedded sync words in the non-active display area.

When frame mixing is used, $\overline{\text{VS}}$, $\overline{\text{HS}}$, DE and R[7:0], G[7:0], B[7:0] are used to implement NXP-patented frame mixing algorithm.

Table 8 summarizes the requirements of $\overline{\text{VS}}$, $\overline{\text{HS}}$, DE and RGB in various modes.

Table 8. VS, HS, DE, and RGB requirements[1][2]

FSS	Mode	FM	VS, HS	DE	R, G, B	A[1:0]
LOW	PSS	HIGH	active LOW	active HIGH	R, G, B	X
		LOW	X	X	X	X
HIGH	FSS	HIGH	active LOW	active HIGH	R, G, B	X
		LOW	active LOW	active HIGH	X	X

[1] 'X' signifies that PTN3700 handles this signal transparently, i.e., data is transmitted and received as-is.

[2] 'R, G, B' signifies that R, G, B video data have to be input according to the exact chosen pin configuration of PTN3700, specifically:

a) Bit order reversal is not allowed, even if both the transmit data and receive data are reversed in bit order. For example, the MSB of 'R' color from video source must be input as 'R7'.

b) 'R' must be used for red color, 'G' for green color, and 'B' for blue color.

7.4.4.1 PSS mode

HS, VS and DE are treated by PTN3700 in the same way as RGB signals in PSS mode; that is, HS, VS, and DE are serialized and transmitted transparently by the PTN3700 transmitter, and transparently received and deserialized by PTN3700 receiver. Data Enable (DE) signal is typically used to signify the active display area from the non-active display area.

In the case that advanced frame mixing is not used:

- DE signal can be tied HIGH or LOW, for displays not using DE signal.
- HS and VS can be active HIGH or active LOW.

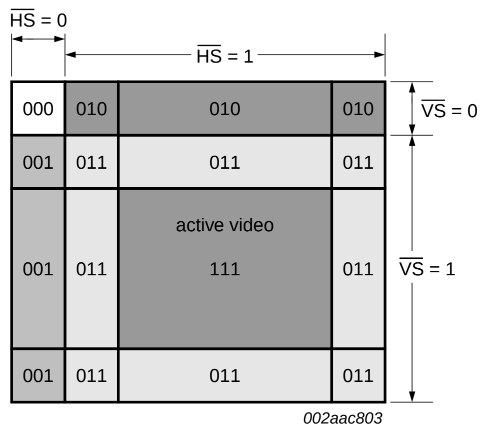
7.4.4.2 FSS mode

In FSS mode, PTN3700 uses true source synchronous transmission with a serial Double Data Rate (DDR) bit clock for the serial data.

FSS mode requires the following operating conditions:

- Active LOW HS
- Active LOW VS
- Active HIGH DE

In FSS mode, DE = 1 means active video, and PTN3700 generates embedded sync words when DE = 0. DE, VS and HS must be actively driven according to the typical video screen figure shown in Figure 18.



3 numbers correspond to [DE, $\overline{HS}$, $\overline{VS}$]

Fig 18. Typical video screen

7.5 Power modes

The PTN3700 has three different power modes to minimize power consumption of the link as a function of link activity: Shutdown mode, Standby mode, and Active mode. The truth table for the three power modes is shown in Table 9 and Table 10.

- **Shutdown mode:** By driving input pin $\overline{XSD}$ LOW, the PTN3700 assumes lowest power mode. All internal logic circuits are reset during this mode, and the link is completely inactive. The transmitter high-speed serial output channels are put in high-impedance state, and the receiver high-speed serial input channels are pulled LOW. The receiver CMOS parallel outputs will all be set HIGH with the exception of DE and PCLK which are reset LOW. However, the input buffers for the transmitter remain active, so it is recommended to stop PCLK and RGB data to achieve the lowest Shutdown mode power.
- **Standby mode:** When pin $\overline{XSD}$ is set HIGH but no input clock is active, the PTN3700 detects inactivity of the clock[3] and remains in a low-power Standby mode until an active input clock is detected. The transmitter serial outputs, receiver serial inputs and receiver parallel outputs all behave identically to their respective states in Shutdown mode.
- **Active mode:** When pin $\overline{XSD}$ is set HIGH and an active input clock is detected, PTN3700 will assume normal link operation. Current consumption depends on the PCLK frequency, number of lanes, FSS/PSS mode, data pattern, etc.

Table 9. Power modes - Transmitter mode

Inputs		Power mode	Outputs	
$\overline{XSD}$	PCLK		D0+, D0−, D1+, D1−, D2+, D2−	CLK+, CLK−
L	X	Shutdown	high-Z	high-Z
H	stopped	Standby	high-Z	high-Z
H	running	Active	active serial data	active

3. The PTN3700 clock detection circuit identifies the clock as inactive when the PCLK input signal frequency is less than 500 kHz.

Table 10. Power modes - Receiver mode

Inputs		State of serial data inputs	Power mode	Data Outputs	
$\overline{\mathrm{XSD}}$	CLK+, CLK−	D0+, D0−, D1+, D1−, D2+, D2−		R[7:0], G[7:0], B[7:0], HS, VS	DE, PCLK
L	X or floating	resistively pulled H or L	Shutdown	H	L
H	stopped	resistively pulled H or L	Standby	H	L
H	running	normal receiver state	Active	active data	active

7.6 Link error detection and correction

In Transmitter mode, PTN3700 calculates an odd parity bit and merges this into the serialized output data stream to allow the receiver to detect whether parity has been violated for its received input data. The parity bit CP is calculated across the 27-bit input data word (R[7:0], G[7:0], B[7:0], $\overline{\mathrm{HS}}$, $\overline{\mathrm{VS}}$ and DE) for every pixel transmitted, as shown in Table 11. Note that the auxiliary bits A[1:0] are excluded from the parity calculation.

Table 11. Parity encoding function table - Transmitter mode

Inputs			Encoded parity bit
$\overline{\mathrm{XSD}}$	PCLK	∑ of inputs = H (R[7:0], G[7:0], B[7:0], $\overline{\mathrm{HS}}$, $\overline{\mathrm{VS}}$, DE)	CP
H	running	odd	L
H	running	even	H
H	stopped	X or floating	undefined
L	X or floating	X or floating	undefined

In Receiver mode, the received encoded parity bit CP is compared against the received 27-bit input data word (R[7:0], G[7:0], B[7:0], $\overline{\mathrm{HS}}$, $\overline{\mathrm{VS}}$ and DE) for every pixel, and an error is flagged by setting parity error output CPO HIGH for the duration of the pixel clock period in which the error was detected. Note that the auxiliary output bits A[1:0] are excluded from the parity detection.

In addition, during the pixel clock period in which the error occurs, the last valid pixel word is output to R[7:0], G[7:0], B[7:0], $\overline{\mathrm{HS}}$, $\overline{\mathrm{VS}}$ and DE instead of the current erroneous pixel data. The last valid pixel word is defined as the data prior to the first parity error detected in any concatenation of parity errors.

If a parity error is detected but no valid previous pixel information is available, the receiver will output values R[7:0] = G[7:0] = B[7:0] = $\overline{\mathrm{HS}}$ = $\overline{\mathrm{VS}}$ = HIGH, and DE = LOW. The truth table for receiver parity function is shown in Table 12. Note that the auxiliary bits A[1:0] are not affected by the last valid pixel repetition.

Table 12. Parity decoding function table - Receiver mode

Inputs			Received parity bit	Parity output	Data outputs
$\overline{XSD}$	Clock	$\sum$ of bits received in frame = H (R[7:0], G[7:0], B[7:0], $\overline{HS}$, $\overline{VS}$, DE)	CP	CPO	R[7:0], G[7:0], B[7:0], $\overline{HS}$, $\overline{VS}$, DE[1][2]
H	running	odd	L	L	RGB_n, $\overline{HS}_n$, $\overline{VS}_n$, DE_n
H	running	even	L	H	RGB_0, $\overline{HS}_0$, $\overline{VS}_0$, DE_0
H	running	odd	H	H	RGB_0, $\overline{HS}_0$, $\overline{VS}_0$, DE_0
H	running	even	H	L	RGB_n, $\overline{HS}_n$, $\overline{VS}_n$, DE_n
H	stopped	X or floating	X	L	undefined
L	X or floating	X or floating	X	L	undefined

[1] YYY_n = current valid pixel data is output to the parallel interface.

[2] YYY_0 = most recent valid pixel data is output to the parallel interface.

7.7 Frame Mixing and Advanced Frame Mixing

When PTN3700 is configured as Receiver (TX/$\overline{RX}$ = LOW), the CMOS input FM selects whether the Frame Mixing function is turned on (FM = HIGH) or off (FM = LOW). (When PTN3700 is configured as Transmitter (TX/$\overline{RX}$ = HIGH), the Frame Mixing function is not available, and the FM input should not be used.)

Advanced Frame Mixing is a proprietary pixel mapping algorithm that features the ability to render full 24-bit color resolution (provided 24-bit source data is input) using an 18-bit or an 18-bit plus display.

When Frame Mixing is off, the full 24-bit data path is maintained unaltered for the link (transparent).

When Frame Mixing is enabled, the algorithm maps the incoming 24-bit data to the 18-bit output data, aligned to the MSB. This is illustrated in Table 13. The new 18-bit data fields ($R[7:2]_{FM}$, $G[7:2]_{FM}$ and $B[7:2]_{FM}$) contain the altered information as calculated by the Frame Mixing algorithm from the original data. One additional ‘Advanced Frame Mixing’ bit is encoded into the next lower significant bit ($R1_{AFM}$, $G1_{AFM}$ and $B1_{AFM}$) of the output data.

Table 13. Advanced Frame Mixing bit mapping (FM = HIGH)

Bit	7	6	5	4	3	2	1	0
Input data	R7	R6	R5	R4	R3	R2	R1	R0
	G7	G6	G5	G4	G3	G2	G1	G0
	B7	B6	B5	B4	B3	B2	B1	B0
Output data	$R7_{FM}$	$R6_{FM}$	$R5_{FM}$	$R4_{FM}$	$R3_{FM}$	$R2_{FM}$	$R1_{AFM}$	HIGH
	$G7_{FM}$	$G6_{FM}$	$G5_{FM}$	$G4_{FM}$	$G3_{FM}$	$G2_{FM}$	$G1_{AFM}$	HIGH
	$B7_{FM}$	$B6_{FM}$	$B5_{FM}$	$B4_{FM}$	$B3_{FM}$	$B3_{FM}$	$B1_{AFM}$	HIGH

When using Frame Mixing with normal 18-bit displays, the 6 MSBs of the parallel video data outputs (R[7:2], G[7:2] and B[7:2]) should be connected to the display driver inputs. When using special ‘18-bit plus’ display drivers (Advanced Frame Mixing capable), additionally the next lower significant bit (R1, G1 and B1) should be connected to the corresponding display driver input.

7.8 Auxiliary signals

The two auxiliary bits A[1:0] are user-supplied bits that can be additionally serialized and deserialized by the PTN3700 in transmitter and receiver modes, respectively. These auxiliary bits are transparent to the PTN3700 and can be used to transmit and receive miscellaneous status or mode information across the link to the display. Note that the auxiliary bits A[1:0] are excluded from the parity calculation and detection in the transmitter and receiver modes respectively. Even in the event of parity error being detected in the receiver mode, A[1:0] will still be deserialized as they are detected by the receiver.

8. Limiting values

Table 14. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.3	+3.0	V
V_I	input voltage	receiver		–0.3	V_{DD} + 0.5	V
V_O	output voltage	driver		–0.3	V_{DD} + 0.5	V
T_{stg}	storage temperature			–65	+150	°C
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	1500	V
		MM	[2]	-	200	V
		CDM	[3]	-	1000	V

[1] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[2] Machine Model: ANSI/EOS/ESD-S5.2.1-1999, standard for ESD sensitivity testing, Machine Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[3] Charged Device Model: ANSI/EOS/ESD-S5.3.1-1999, standard for ESD sensitivity testing, Charged Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

9. Recommended operating conditions

Table 15. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		1.65	1.8	1.95	V
V_I	input voltage		0	-	V_{DD}	V
I_{OH}	HIGH-level output current	0.8 × V_{DD}	-	-	–1	mA
I_{OL}	LOW-level output current	0.2 × V_{DD}	-	-	1	mA
T_{amb}	ambient temperature	operating in free air	–40	-	+85	°C

10. Static characteristics

Table 16. Static characteristics

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage			1.65	1.8	1.95	V
V_{IH}	HIGH-level input voltage	I_I = –10 μA		$0.7V_{DD}$	-	V_{DD}	V
V_{IL}	LOW-level input voltage	I_I = 10 μA		0	-	$0.3V_{DD}$	V
V_{OH}	HIGH-level output voltage	I_O = –1 mA		$0.8V_{DD}$	-	V_{DD}	V
V_{OL}	LOW-level output voltage	I_O = 1 mA		0	-	$0.2V_{DD}$	V
C_i	input capacitance	TX mode		-	2	4	pF
Transmitter mode, PSS mode ($TX/\overline{RX}$ = HIGH; FSS = LOW)							
I_{DD}	supply current	Shutdown mode; T_{amb} = –40 °C to +60 °C		-	4	10	μA
		Standby mode; T_{amb} = –40 °C to +60 °C		-	4	10	μA
		Active mode	[1]				
		PCLK = 6 MHz; Mode 00		-	11	12.6	mA
		PCLK = 12 MHz; Mode 00		-	15	17.3	mA
		PCLK = 20 MHz; Mode 00		-	21	23.5	mA
		PCLK = 8 MHz; Mode 01		-	13	14.8	mA
		PCLK = 22 MHz; Mode 01		-	19	21.2	mA
		PCLK = 40 MHz; Mode 01		-	26	29.3	mA
		PCLK = 20 MHz; Mode 10		-	19	21.1	mA
		PCLK = 40 MHz; Mode 10		-	26	28.8	mA
		PCLK = 65 MHz; Mode 10		-	35	36.8	mA
Transmitter mode, FSS mode ($TX/\overline{RX}$ = HIGH; FSS = HIGH)							
I_{DD}	supply current	Shutdown mode; T_{amb} = –40 °C to +60 °C		-	4	10	μA
		Standby mode; T_{amb} = –40 °C to +60 °C		-	4	10	μA
		Active mode	[1]				
		PCLK = 6 MHz; Mode 00		-	12	13.7	mA
		PCLK = 12 MHz; Mode 00		-	17	19.2	mA
		PCLK = 20 MHz; Mode 00		-	24	26.6	mA
		PCLK = 8 MHz; Mode 01		-	13	14.9	mA
		PCLK = 22 MHz; Mode 01		-	20	22.3	mA
		PCLK = 40 MHz; Mode 01		-	28	31.9	mA
		PCLK = 20 MHz; Mode 10		-	19	21.2	mA
		PCLK = 40 MHz; Mode 10		-	26	29.1	mA
		PCLK = 65 MHz; Mode 10		-	35	38.9	mA

Table 16. Static characteristics *...continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Receiver mode, PSS mode (TX/$\overline{RX}$ = LOW; FSS = LOW)[2]							
I_{DD}	supply current	Shutdown mode; T_{amb} = −40 °C to +60 °C		-	4	10	μA
		Standby mode; T_{amb} = −40 °C to +60 °C		-	4	10	μA
		Active mode	[1]				
		PCLK = 6 MHz; Mode 00		-	8	10.7	mA
		PCLK = 12 MHz; Mode 00		-	14	16.5	mA
		PCLK = 20 MHz; Mode 00		-	22	25	mA
		PCLK = 8 MHz; Mode 01		-	8.5	11	mA
		PCLK = 22 MHz; Mode 01		-	16	19.5	mA
		PCLK = 40 MHz; Mode 01		-	25	31	mA
		PCLK = 20 MHz; Mode 10		-	14	17.8	mA
		PCLK = 40 MHz; Mode 10		-	22.5	28	mA
		PCLK = 65 MHz; Mode 10		-	34	40	mA
Receiver mode, FSS mode (TX/$\overline{RX}$ = LOW; FSS = HIGH)[2]							
I_{DD}	supply current	Shutdown mode; T_{amb} = −40 °C to +60 °C		-	4	10	μA
		Standby mode; T_{amb} = −40 °C to +60 °C		-	4	10	μA
		Active mode	[1]				
		PCLK = 6 MHz; Mode 00		-	7.5	10.2	mA
		PCLK = 12 MHz; Mode 00		-	13	15.5	mA
		PCLK = 20 MHz; Mode 00		-	20.6	23.6	mA
		PCLK = 8 MHz; Mode 01		-	8.1	10.6	mA
		PCLK = 22 MHz; Mode 01		-	15.4	18.6	mA
		PCLK = 40 MHz; Mode 01		-	23.4	29.3	mA
		PCLK = 20 MHz; Mode 10		-	13.5	17.3	mA
		PCLK = 40 MHz; Mode 10		-	21.8	26.9	mA
		PCLK = 65 MHz; Mode 10		-	33	38	mA

[1] Worst-case data pattern for power dissipation is used: alternating vertical stripes. The colors of the stripes correspond to the data pattern: RGB[23:0] = 0xAA AAAA (odd stripes) / RGB[23:0] = 0x55 5555 (even stripes).

[2] Based on receiver output load (per output) of 16 pF. The loaded outputs are: PCLK, R[7:0], G[7:0], B[7:0], $\overline{HS}$, $\overline{VS}$ and DE.

11. Dynamic characteristics

11.1 Transmitter mode

Table 17. Dynamic characteristics for Transmitter mode

V_{DD} = 1.65 V to 1.95 V, T_{amb} = −40 °C to +85 °C, unless otherwise specified.
All CMOS input signals' rise time and fall time to Transmitter are stipulated to be from 1 ns to 15 ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{i(PCLK)}$	input frequency on pin PCLK	Mode 00; see Table 5	4.0	-	21.6	MHz
		Mode 01; see Table 5	8.0	-	43.3	MHz
		Mode 10; see Table 5	20.0	-	65.0	MHz
$\delta_{i(PCLK)}$	input duty cycle on pin PCLK		33	-	67	% T_{PCLK}
$t_{su(D-PCLK)}$	set-up time from data input to PCLK		2.0	-	-	ns
$t_{h(D-PCLK)}$	hold time from data input to PCLK		2.0	-	-	ns
$t_{jit(cc)}$	cycle-to-cycle jitter time	PCLK	−300	-	+300	ps
$B_{PLL(loop)}$	PLL loop bandwidth	−3 dB corner frequency of PLL loop filter response	$0.02 \times f_{i(PCLK)}$	$0.03 \times f_{i(PCLK)}$	$0.05 \times f_{i(PCLK)}$	MHz

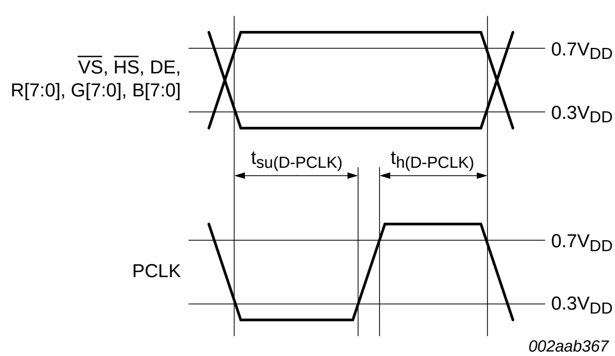


Fig 19. AC timing diagram - Transmitter mode

11.2 Receiver mode

Table 18. Dynamic characteristics for Receiver mode

V_{DD} = 1.65 V to 1.95 V, T_{amb} = –40 °C to +85 °C, unless otherwise specified.
CMOS output load C_L = 16 pF.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{o(PCLK)}$	output frequency on pin PCLK	Mode 00; see Table 5	4.0	-	21.6	MHz
		Mode 01; see Table 5	8.0	-	43.3	MHz
		Mode 10; see Table 5	20.0	-	65.0	MHz
$\delta_{o(PCLK)}$	output duty cycle on pin PCLK	Mode 00 or Mode 10; F/$\overline{XS}$ = 1	45	50	55	% T_{PCLK}
		Mode 01; F/$\overline{XS}$ = 1	48	53	59	% T_{PCLK}
$t_{sk(Q)}$	data output skew time	Mode 00; F/$\overline{XS}$ = 1	–0.5	0	1.5	ns
		Mode 01; F/$\overline{XS}$ = 1	–0.5	0	0.8	ns
		Mode 10; F/$\overline{XS}$ = 1	–0.5	0	0.8	ns
		Mode 00; F/$\overline{XS}$ = 0	–3.0	0	2.0	ns
		Mode 01; F/$\overline{XS}$ = 0	–0.5	0	2.5	ns
		Mode 10; F/$\overline{XS}$ = 0	–1.4	0	3.0	ns
$t_{jit(r)PCLK}$	PCLK rise jitter time		–0.6	0	0.6	ns
t_r	rise time	CMOS signals				
		Mode 00; F/$\overline{XS}$ = 0	8	-	18	ns
		Mode 00; F/$\overline{XS}$ = 1	4	-	10	ns
		Mode 01; F/$\overline{XS}$ = 0	4	-	10	ns
		Mode 01; F/$\overline{XS}$ = 1	1	-	3	ns
		Mode 10; F/$\overline{XS}$ = 0	4	-	10	ns
		Mode 10; F/$\overline{XS}$ = 1	1	-	3	ns
t_f	fall time	CMOS signals				
		Mode 00; F/$\overline{XS}$ = 0	8	-	18	ns
		Mode 00; F/$\overline{XS}$ = 1	4	-	10	ns
		Mode 01; F/$\overline{XS}$ = 0	4	-	10	ns
		Mode 01; F/$\overline{XS}$ = 1	1	-	3	ns
		Mode 10; F/$\overline{XS}$ = 0	4	-	10	ns
		Mode 10; F/$\overline{XS}$ = 1	1	-	3	ns
$B_{PLL(loop)}$	PLL loop bandwidth	–3 dB corner frequency of PLL loop filter response	$0.09 \times f_{o(PCLK)}$	$0.11 \times f_{o(PCLK)}$	$0.14 \times f_{o(PCLK)}$	MHz

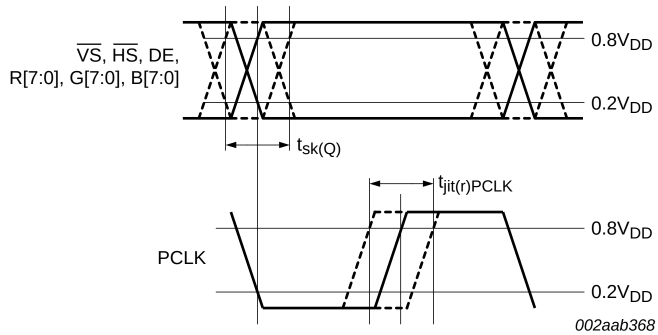


Fig 20. AC timing diagram - Receiver mode

11.3 Power-on/power-off sequence

11.3.1 Power-on sequence

Table 19. Power-on sequence timing characteristics

V_{DD} = 1.65 V to 1.95 V, T_{amb} = −40 °C to +85 °C, unless otherwise specified.
These values are for transitions of the Shutdown mode to the Standby mode and the Standby mode to the Active mode.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(VDDH-XSDH)}$	set-up time from V_{DD} HIGH to $\overline{XSD}$ HIGH	Transmitter mode	0	-	-	ms
		Receiver mode	0	-	-	ms
$t_{su(XSDH-PCLKV)}$	set-up time from $\overline{XSD}$ HIGH to PCLK valid	Transmitter mode	10	-	-	μs
$t_{d(PCLKH-DV)}$	delay time from PCLK HIGH to data valid	Transmitter mode	-	-	2	ms
$t_{d(XSDH-stb)}$	delay time from $\overline{XSD}$ HIGH to standby	Receiver mode	-	-	10	μs
$t_{d(RXDV-RXQV)}$	delay time from receiver data input valid to receiver data output valid	Receiver mode	-	-	2	ms

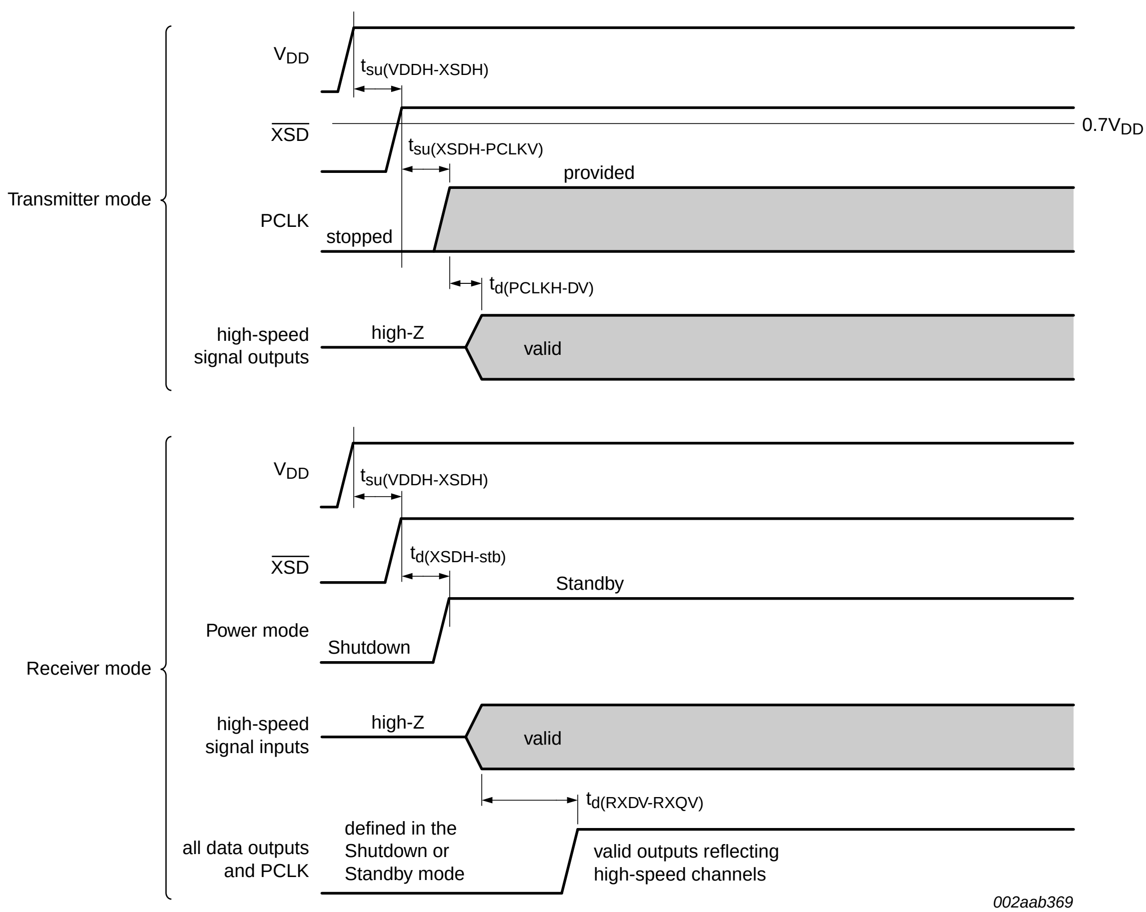


Fig 21. Power-on sequence of the link

11.3.2 Power-off sequence

Table 20. Power-off sequence timing characteristics

V_{DD} = 1.65 V to 1.95 V, T_{amb} = −40 °C to +85 °C, unless otherwise specified.
These values are for transition of the Active mode to the Standby mode.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(PCLKL-TXQZ)}$	delay time from PCLK LOW to transmitter data output float	Transmitter mode	-	-	100	µs
$t_{d(RXDZ-RXQinact)}$	receiver data input float to receiver data output inactive delay time	Receiver mode	-	-	5	µs
$t_{h(XSDL-VDDL)}$	supply voltage LOW after $\overline{XSD}$ LOW hold time	Transmitter mode	0	-	-	ms
		Receiver mode	0	-	-	ms

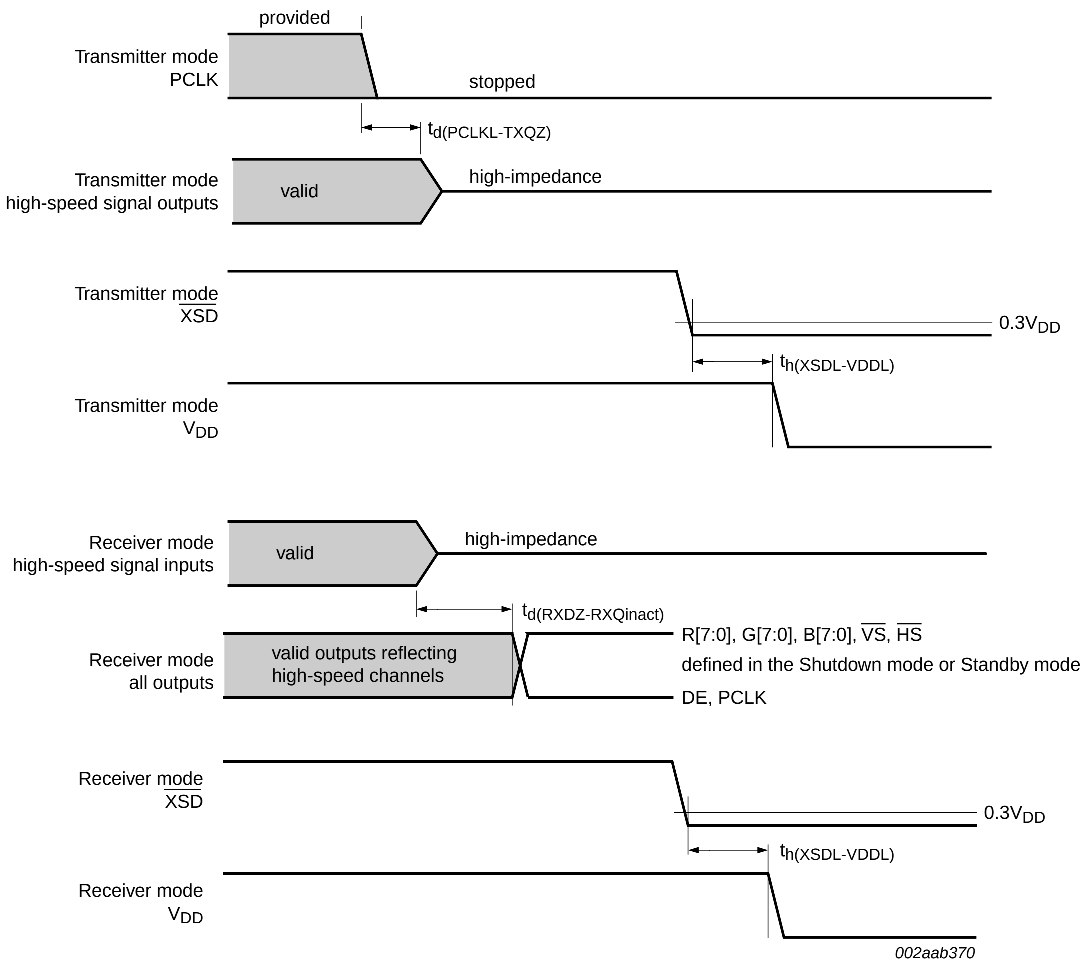


Fig 22. Power-off sequence of the link

11.4 High-speed signaling channel

Table 21. High-speed signaling channel SubLVDS output characteristics, Transmitter mode
V_{DD} = 1.65 V to 1.95 V, T_{amb} = –40 °C to +85 °C, unless otherwise specified. See Section 13.1 for testing information.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{O(dif)}$	differential output voltage	see Figure 28		100	150	200	mV
$V_{O(cm)}$	common-mode output voltage	see Figure 28		0.8	0.9	1.0	V
$V_{O(cm)ripple(p-p)}$	peak-to-peak ripple common-mode output voltage	see Figure 29		–75	-	+75	mV
$R_{o(dif)}$	differential output resistance	between complimentary outputs of any differential pair: CLK+/CLK–; D0+/D0–; D1+/D1–; D2+/D2–		80	180	280	Ω
$t_{r(dif)}$	differential rise time	from 20 % to 80 % of $V_{O(dif)}$; see Figure 30		200	-	500	ps
$t_{f(dif)}$	differential fall time	from 80 % to 20 % of $V_{O(dif)}$; see Figure 30		200	-	500	ps
f_{oper}	operating frequency			-	-	325	MHz
I_O	output current	output drive current per channel		-	-	4	mA
$\Delta V_{O(dif)}/V_{O(dif)}$	relative differential output voltage difference	between CLK+/CLK– and Dn+/Dn–, referenced to CLK+/CLK–	[1]	–10	-	+10	%
$\Delta V_{O(cm)}$	common-mode output voltage difference	between CLK+/CLK– and Dn+/Dn–		–0.1	-	+0.1	V
Δt_r	rise time difference	t_r(CLK+/CLK–) – t_r(Dn+/Dn–)		–100	-	+100	ps
Δt_f	fall time difference	t_f(CLK+/CLK–) – t_f(Dn+/Dn–)		–100	-	+100	ps
I_{LO}	output leakage current	Shutdown or Standby mode (high-impedance state)		–3.0	-	+3.0	μA
$t_{bit(CLKH-Q)}$	bit time from CLK HIGH to data output	PSS mode; Mode 00 or Mode 01; see Table 5, Figure 33	[2][3]	N × UI – 19 % × UI	N × UI	N × UI + 19 % × UI	ps
		PSS mode: Mode 10; see Table 5, Figure 33	[2][3]	N × UI – 16 % × UI	N × UI	N × UI + 16 % × UI	ps
$t_{sk(CLK-Q)}$	skew time from clock to data output	CLK edge to data output skew time; FSS mode; see Figure 35	[2]	–16 % × UI	0	+16 % × UI	ps

[1] $\Delta[\%] = \frac{V_{O(dif)CLK} - V_{O(dif)DATA}}{V_{O(dif)CLK}} \times 100\ \%$

[2] Mode 00: UI = PCLK period / 30
Mode 01: UI = PCLK period / 15
Mode 10: UI = PCLK period / 10

[3] N is defined as the bit position, where 0 ≤ N ≤ 29 (Mode 00), 0 ≤ N ≤ 14 (Mode 01) or 0 ≤ N ≤ 9 (Mode 10).

Table 22. High-speed signaling channel SubLVDS input characteristics, Receiver mode

V_{DD} = 1.65 V to 1.95 V, T_{amb} = –40 °C to +85 °C, unless otherwise specified. See Section 13.1 for testing information.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{I(dif)}$	differential input voltage	see Figure 31		70	100	450	mV
$V_{th(H)i(dif)}$	differential input HIGH-level threshold voltage	see Figure 32		+25	-	-	mV
$V_{th(L)i(dif)}$	differential input LOW-level threshold voltage	see Figure 32		-	-	–25	mV
$V_{I(cm)}$	common-mode input voltage	see Figure 31		0.4	-	1.4	V
$V_{I(cm)ripple(p-p)}$	peak-to-peak ripple common-mode input voltage	see Figure 29		–75	-	+75	mV
$R_{i(dif)}$	differential input resistance	internal termination resistor; see Figure 31		80	100	120	Ω
$t_{r(dif)}$	differential rise time	from 20 % to 80 % of $V_{I(dif)}$; see Figure 30		-	-	800	ps
$t_{f(dif)}$	differential fall time	from 80 % to 20 % of $V_{I(dif)}$; see Figure 30		-	-	800	ps
f_{oper}	operating frequency			-	-	325	MHz
$\Delta V_{I(dif)}/V_{I(dif)}$	relative differential input voltage difference	between CLK+/CLK– and Dn+/Dn–, referenced to CLK+/CLK–	[1]	–10	-	+10	%
$\Delta V_{I(cm)}$	common-mode input voltage difference	between CLK+/CLK– and Dn+/Dn–		–0.1	-	+0.1	V
Δt_r	rise time difference	t_r(CLK+/CLK–) – t_r(Dn+/Dn–)		–100	-	+100	ps
Δt_f	fall time difference	t_f(CLK+/CLK–) – t_f(Dn+/Dn–)		–100	-	+100	ps
R_{pd}	pull-down resistance	complimentary input (Dn–) to GND; input clock inactive; see Figure 31		-	1	50	kΩ
I_{LI}	input leakage current	Shutdown or Standby mode		–90	-	+90	µA
$t_{bit(CLKH-D)}$	bit time from CLK HIGH to data input	PSS mode; see Figure 34	[2][3]	N × UI – 21 % × UI	N × UI	N × UI + 21 % × UI	ps
$t_{sk(CLK-D)}$	skew time from clock to data input	CLK edge to data input skew time; FSS mode; see Figure 35	[2]	–21 % UI	0	+21 % UI	ps

[1] $$\Delta[\%] = \frac{V_{I(dif)CLK} - V_{I(dif)DATA}}{V_{I(dif)CLK}} \times 100\ \%$$

[2] Mode 00: UI = PCLK period / 30
Mode 01: UI = PCLK period / 15
Mode 10: UI = PCLK period / 10

[3] N is defined as the bit position, where 0 ≤ N ≤ 29 (Mode 00), 0 ≤ N ≤ 14 (Mode 01) or 0 ≤ N ≤ 9 (Mode 10).

12. Application information

12.1 Typical lane and PCLK configurations

The PTN3700 supports PCLK (pixel clock) frequencies from 4 MHz to 65 MHz over 1, 2 or 3 data lanes. Table 23 shows the typical number of data lanes needed, assuming blanking overhead of 20 %. Note that 20 % overhead is an example value for illustration/calculation purposes only and not a requirement.

Table 23. Typical PCLK and number of data lanes

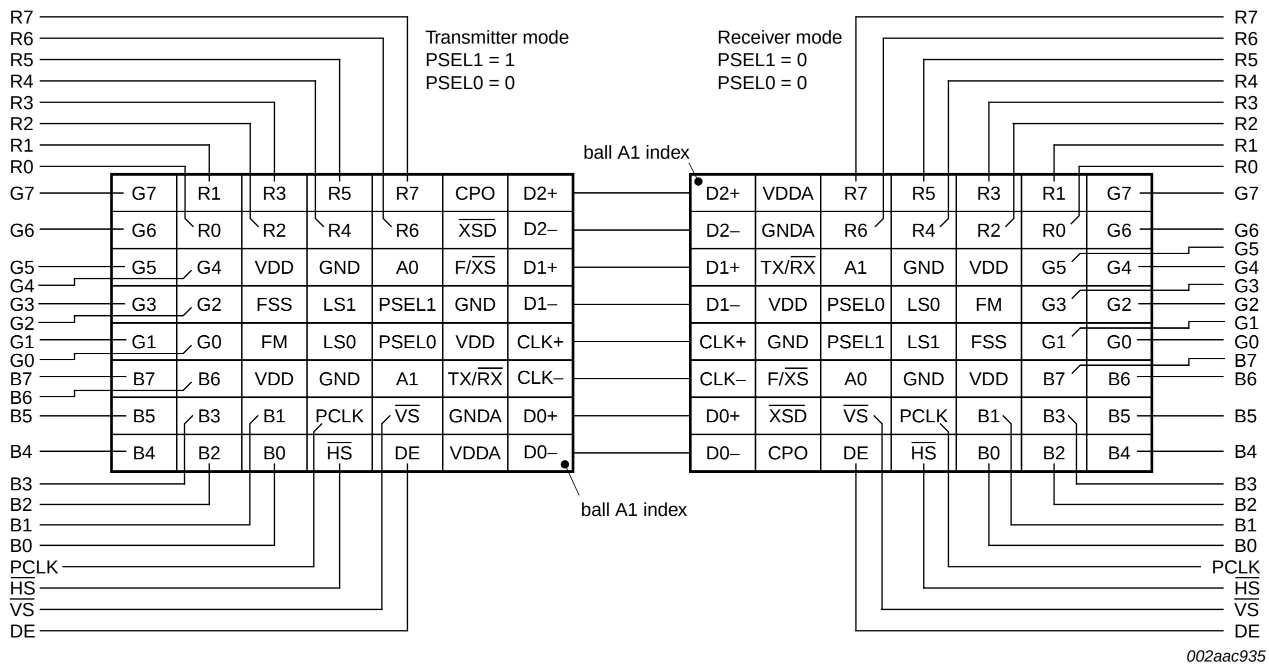
Panel	Horizontal	Vertical	Color bit	Other bits	Frame rate (Hz)	Blanking overhead	Pixel clock (MHz)	Serial aggregate data rate (Mbit/s)		
								1-lane	2-lane	3-lane
QVGA	240	320	18	12	60	20 %	5.5	165.9		
WQVGA	400	240	18	12	60	20 %	6.9	207.4		
CIF+	352	416	18	12	60	20 %	10.5	316.3	316.3	
HVGA	320	480	24	6	60	20 %	11.1	331.8	331.8	
VGA	640	480	24	6	60	20 %	22.1		663.6	663.6
WVGA	854	480	24	6	60	20 %	29.5		885.4	885.4
SVGA	800	600	24	6	60	20 %	34.6		1036.8	1036.8
XGA	1024	768	24	6	60	20 %	56.6			1698.7
720p	1280	720	24	6	60	15 %	63.6			1909.7

12.2 Pin configurations for various topologies of PCB

There are two input pins, PSEL1 and PSEL0, on the PTN3700 that allow for pinning order configurations.

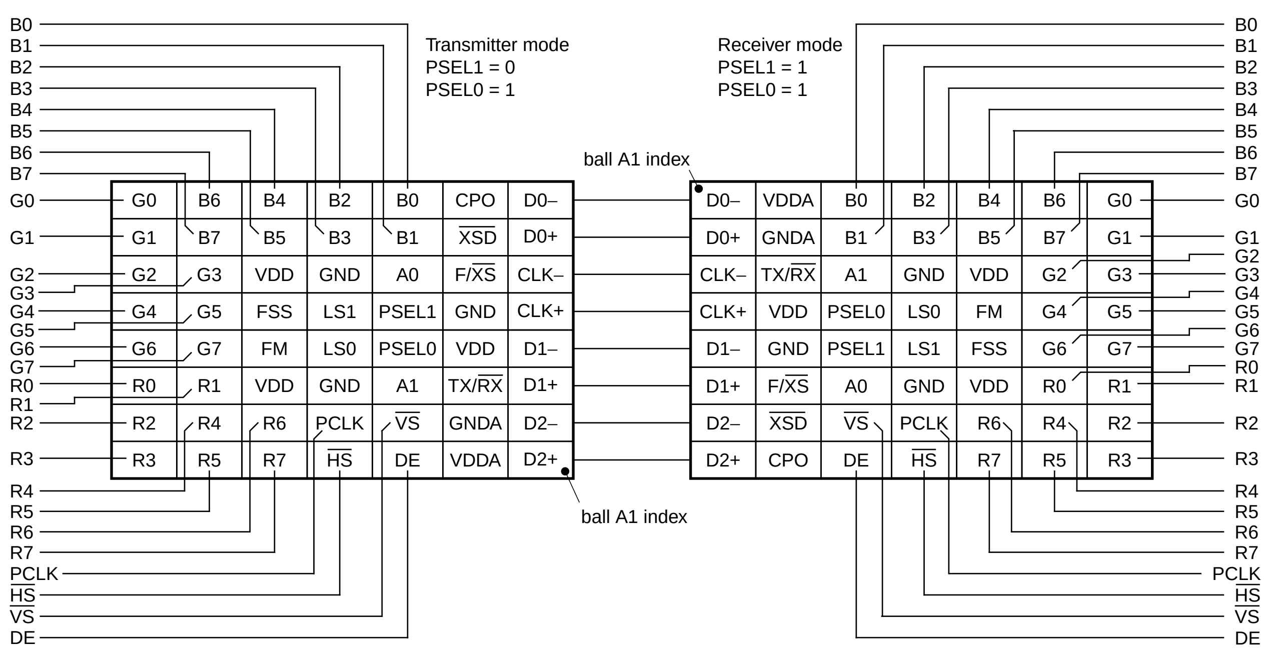
PSEL1 will change the pinning order of the serial signals, and allow for various topologies of PCB or flex layout without crossing the high-speed differential traces. The example shown in Figure 23 has set PSEL1 = 0 at receiver side, and PSEL1 = 1 at the transmitter to avoid the traces crossing. Figure 24 shows another configuration, which has PSEL1 = 1 at receiver, and PSEL1 = 0 at transmitter.

PSEL0 can configure the pinning order of the parallel signals, and enables the easy introduction of the PTN3700 into an existing parallel design avoiding board re-layout. Figure 23 and Figure 24 show two configuration examples.



Transparent top view.

Fig 23. Pinning configuration example 1



Transparent top view.

Fig 24. Pinning configuration example 2

12.3 Power decoupling configuration

The PTN3700 needs 1.8 V V_{DD} and 1.8 V V_{DDA}. Both can share the same voltage regulator, and use a 10 Ω resistor for isolation. The recommended power configuration of the decoupling is shown in Figure 25. It is recommended to install one 0.1 μF ceramic capacitor for each VDD pin and one 0.01 μF ceramic capacitor for VDDA pin, and the lead length between the IC power pins and decoupling capacitors should be as short as possible.

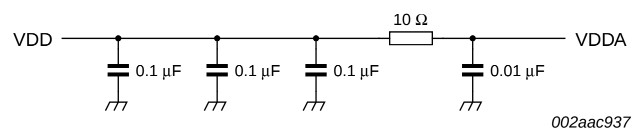


Fig 25. Power decoupling configuration

12.4 PCB/Flex layout guideline

The high data rate at the serial I/O requires some specific implementations in the PCB and flex layout design. The following practices can be used as guideline:

- The differential pair must be routed symmetrically. Keep all four pairs of differential signal traces the same length. The difference in trace length should be less than 20 mils.
- Maintain 100 Ω differential impedance.
- Do not route signals over any plane split; use only one ground plane underneath the differential signals.
- Avoid any discontinuity for signal integrity. Differential pairs should be routed on the same layer and the number of vias on the differential traces should be minimized. Test points should be placed in series and symmetrically. Stubs should not be introduced on the differential pairs.

12.5 Power-on/power-off requirement

PTN3700 does not have any external reset pin. Internally, there is Power-On Reset (POR) circuitry to reset the whole IC at power-up. In order to guarantee that POR works properly, the supply voltage V_{DD} must be powered up from ground level, as illustrated in Figure 26.

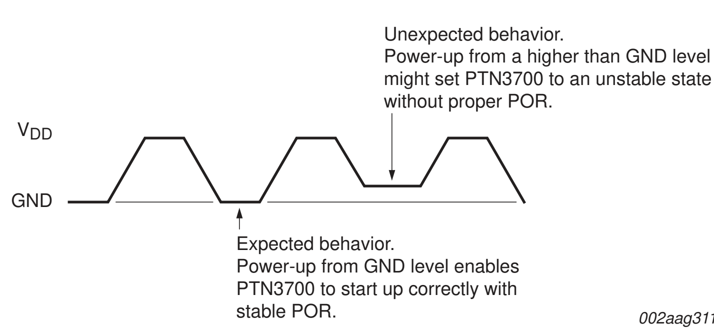


Fig 26. Expected and unexpected power-on behavior

It is recommended to have long enough of a power-off time to let V_{DD} discharge completely, reaching to ground level.

If the supply voltage V_{DD} cannot be guaranteed to start from ground level, it is recommended to hold the $\overline{XSD}$ pin at LOW during power-on.

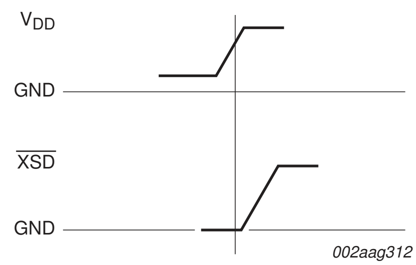


Fig 27. $\overline{XSD}$ at LOW during power-on

13. Test information

13.1 High-speed signaling channel measurements

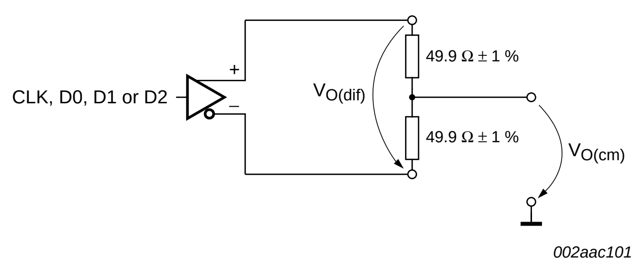


Fig 28. Transmitter termination and definition for measurement of electrical parameters

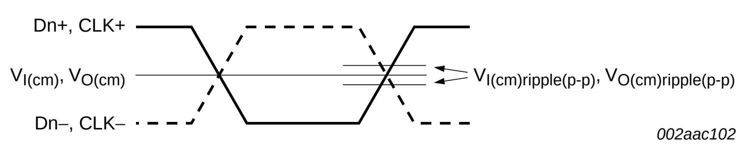


Fig 29. Voltage waveforms, common mode ripple measurement (single-ended mode)

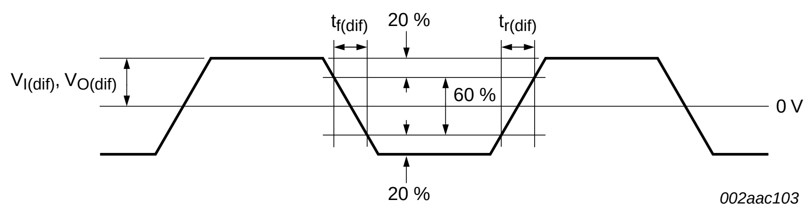


Fig 30. Voltage waveforms, differential input or output voltage and rise and fall time measurements

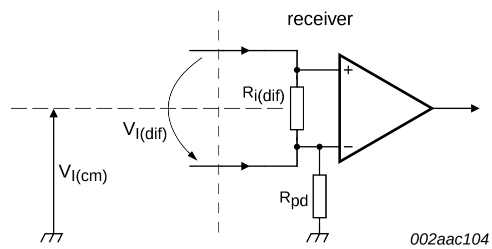


Fig 31. Receiver measurement definition for measurement of electrical parameters

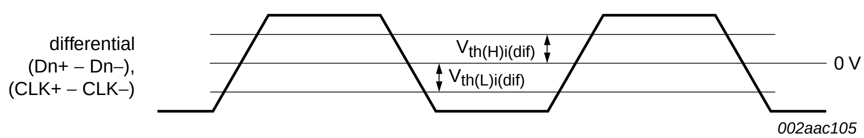


Fig 32. Voltage waveforms, input threshold voltage measurements

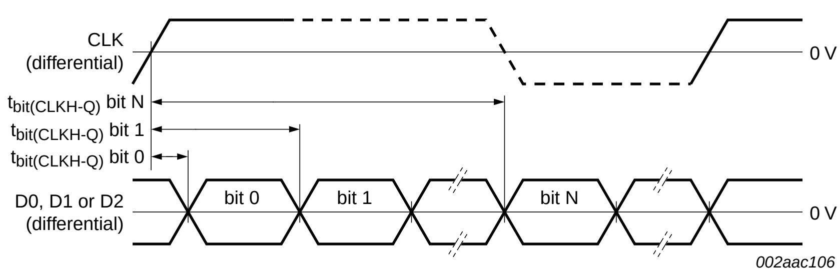


Fig 33. Transmitter high-speed serial outputs timing relationships (PSS mode)

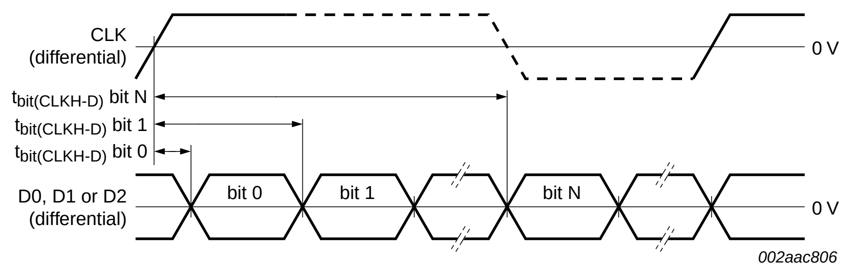


Fig 34. Receiver high-speed serial inputs timing relationships (PSS mode)

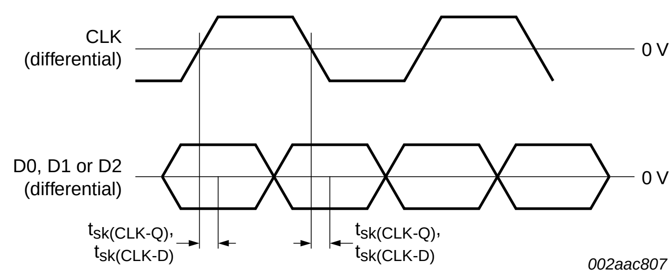
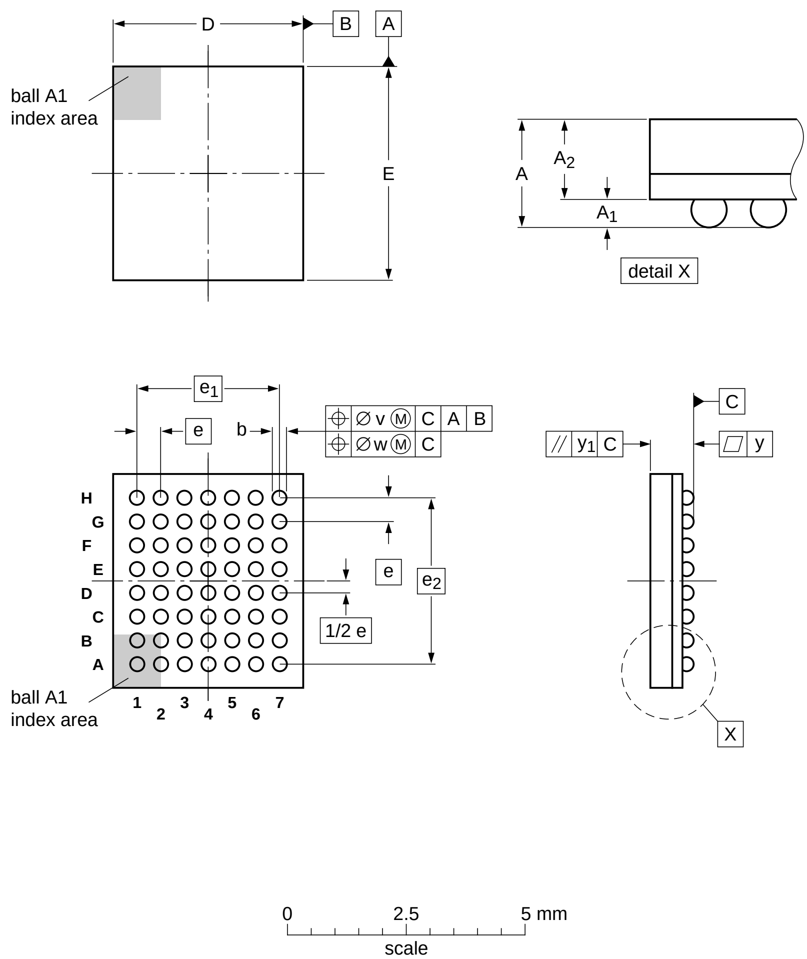


Fig 35. Transmitter and receiver high-speed serial outputs and inputs timing relationships (FSS mode)

14. Package outline

VFBGA56: plastic very thin fine-pitch ball grid array package; 56 balls; body 4 x 4.5 x 0.65 mm **SOT991-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1	0.25 0.15	0.75 0.60	0.35 0.25	4.1 3.9	4.6 4.4	0.5	3	3.5	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT991-1	- - -	- - -	- - -			~~07-02-06~~ 07-02-07

Fig 36. Package outline SOT991-1 (VFBGA56)

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 37) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 24 and 25

Table 24. SnPb eutectic process (from J-STD-020C)

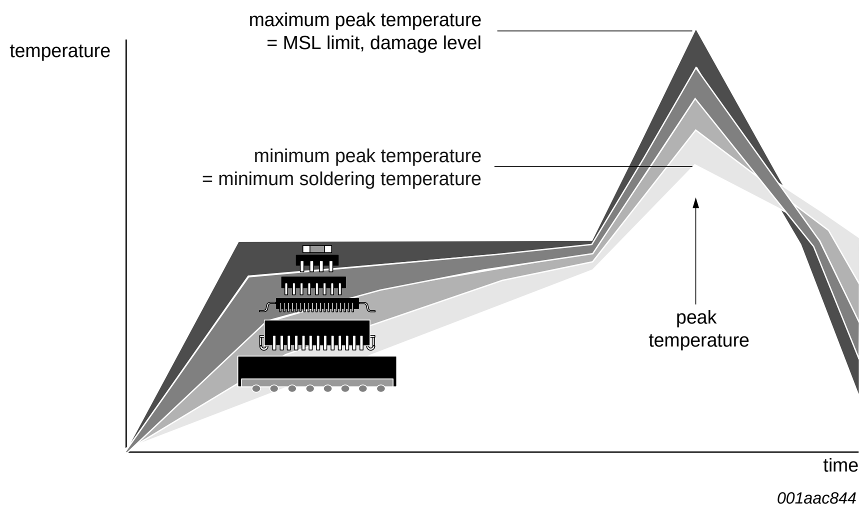
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 25. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 37.



MSL: Moisture Sensitivity Level

Fig 37. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Abbreviations

Table 26. Abbreviations

Acronym	Description
CIF	Common Intermediate Format
CMOS	Complementary Metal-Oxide Semiconductor
DDR	Double Data Rate
EMI	ElectroMagnetic Interference
fps	frames per second
HVGA	Half-size Video Graphics Array
I/O	Input/Output
LVDS	Low-Voltage Differential Signalling
MSB	Most Significant Bit
PCB	Printed-Circuit Board
PLL	Phase-Locked Loop
QVGA	Quarter Video Graphics Array
RGB	Red/Green/Blue
SMILi	Simple Mobile Interface Link
SubLVDS	Sub Low-Voltage Differential Signalling
SVGA	Super Video Graphics Array
UI	Unit Interval
VGA	Video Graphics Array
WQVGA	Wide Quarter Video Graphics Array

Table 26. Abbreviations *…continued*

Acronym	Description
WVGA	Wide Video Graphics Array
XGA	eXtended Graphics Array
XVGA	eXtended Video Graphics Array

17. Revision history

Table 27. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PTN3700 v.3	20111012	Product data sheet	-	PTN3700 v.2
Modifications:	• Table 22 "High-speed signaling channel SubLVDS input characteristics, Receiver mode": $V_{I(dif)}$ Max value changed from "200 mV" to "450 mV"			
PTN3700 v.2	20110608	Product data sheet	-	PTN3700 v.1
PTN3700 v.1	20070814	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 12 October 2011
Document identifier: PTN3700