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General Description

PSoC[®] 6 MCU is a high-performance, ultra-low-power and secured MCU platform, purpose-built for IoT applications. The PSoC 64 product line, based on the PSoC 6 MCU platform, features out-of-box security functionality, providing an isolated root-of-trust with true attestation and provisioning services. In addition, it delivers a pre-configured secured execution environment which supports system software for various IoT platforms; and enables TLS authentication, secured storage, and secured firmware management. PSoC 64 also includes a rich execution environment for application development, with RTOS support that communicates with the secured execution environment.

Features

32-bit Dual CPU Subsystem

Note: In PSoC 64 the Cortex M0+ is reserved for system functions, and is not available for applications.

- 150-MHz Arm[®] Cortex[®]-M4F (CM4) CPU with single-cycle multiply, floating point, and memory protection unit (MPU)
- 100-MHz Cortex-M0+ (CM0+) CPU with single-cycle multiply and MPU
- User-selectable core logic operation at either 1.1 V or 0.9 V
- Active CPU current slope with 1.1-V core operation
 - Cortex-M4: 40 μ A/MHz
 - Cortex-M0+: 28 μ A/MHz
- Active CPU current slope with 0.9-V core operation
 - Cortex-M4: 27 μ A/MHz
 - Cortex-M0+: 20 μ A/MHz
- Three DMA controllers

Memory Subsystem

- 1856-KB application flash, 32-KB auxiliary flash (AUXflash), and 32-KB supervisory flash (SFlash); read-while-write (RWW) support. Two 8-KB flash caches, one for each CPU
- 944-KB SRAM with three independent blocks for power and data retention control
- One-time-programmable (OTP) 1-Kb eFuse array

Hardware-Based Root-of-Trust (RoT)

- RoT based on immutable boot-up code, flash content hash, and Cypress public key that ensures firmware integrity prior to provisioning
- Supports trusted RoT handover to maintain chain of trust and establish OEM trust anchor for secured boot
- Device generates a unique device ID and a device secret key during the provisioning process, which can be used for attestation and signing

Immutable "Secure Boot" Support

- Flexible chain of trust can use different signatures for different images
- ECC-based image signature validation

Cypress Bootloader

- Open Source MCUBoot^[1] based bootloader optimized for PSoC 64
- Pre-built bootloader binary capable of validating, launching and updating signed user application images
- Tightly integrated with provisioned debug and boot policies to inherit and implement security policies

Low-Power 1.7-V to 3.6-V Operation

- Six power modes for fine-grained power management
- Deep Sleep mode current of 7 μ A with 64-KB SRAM retention
- On-chip DC-DC buck converter, <1 μ A quiescent current
- Backup domain with 64 bytes of memory and real-time clock

Flexible Clocking Options

- 8-MHz internal main oscillator (IMO) with \pm 2% accuracy
- Ultra-low-power 32-kHz internal low-speed oscillator (ILO)
- On-chip crystal oscillators (16 to 35 MHz, and 32 kHz)
- Two phase-locked loops (PLLs) for multiplying clock frequencies
- Frequency-locked loop (FLL) for multiplying IMO frequency
- Integer and fractional peripheral clock dividers

Quad-SPI (QSPI)/Serial Memory Interface (SMIF)

- Execute-In-Place (XIP) from external quad SPI flash
- On-the-fly encryption and decryption
- 4-KB cache for greater XIP performance with lower power
- Supports single, dual, quad, dual-quad, and octal interfaces with throughput up to 640 Mbps

Segment LCD Drive

- Supports up to 101 segments and up to 8 commons

Note

1. For details, refer to <https://mcuboot.com/>.

Serial Communication

- 13 run-time configurable serial communication blocks (SCBs)
 - Eight SCBs: configurable as SPI, I²C, or UART
 - Four SCBs: configurable as I²C or UART
 - One Deep Sleep SCB: configurable as SPI or I²C
- USB Full-Speed device interface
- Two independent SD Host Controller/eMMC/SD controllers

Audio Subsystem

- Two pulse density modulation (PDM) channels and two I²S channels with time division multiplexed (TDM) mode

Timing and Pulse-Width Modulation

- Thirty-two timer/counter/pulse-width modulators (TCPWMs)
- Center-aligned, edge, and pseudo-random modes
- Comparator-based triggering of kill signals

Programmable Analog

- 12-bit 2-Msps SAR ADC with differential and single-ended modes and 16-channel sequencer with result averaging
- Two low-power comparators available in system Deep Sleep and Hibernate modes
- Built-in temperature sensor connected to ADC

Up to 100 Programmable GPIOs

- Two Smart I/O™ ports (16 I/Os) enable Boolean operations on GPIO pins; available during system Deep Sleep
- Programmable drive modes, strengths, and slew rates
- Six overvoltage-tolerant (OVT) pins

Capacitive Sensing

- Cypress CapSense® sigma-delta (CSD) provides best-in-class signal-to-noise ratio (SNR), liquid tolerance, and proximity sensing
- Enables dynamic usage of both self and mutual sensing
- Automatic hardware tuning (SmartSense™)

Cryptography Accelerator

- Hardware acceleration for symmetric and asymmetric cryptographic methods and hash functions
- True random number generator (TRNG) function

Profiler

- Eight counters provide event or duration monitoring of on-chip resources

Packages

124-BGA

Device Identification and Revisions

- Product Line ID (12-bit): 0x102
- Major/Minor Die Revision ID: 1/2
- Firmware Revisions: Rom Boot: 7.1, Flash Boot: 4.0.2.1842 (see [Boot Code](#) section)

This product line has a JTAG ID which is available through the SWJ interface. It is a 32-bit ID, where:

- The most significant digit is the device revision, based on the Major Die Revision
- The next four digits correspond to the part number, for example "E4B0" as a hexadecimal number
- The three least significant digits are the manufacturer ID, in this case "069" as a hexadecimal number

The Silicon ID system call can be used by firmware to get Silicon ID and ROM Boot data. For more information, see the [technical reference manual \(TRM\)](#).

The Flash Boot version can be read directly from designated addresses 0x1600 2004 and 0x1600 2018. For more information, see the [technical reference manual \(TRM\)](#).

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Development Ecosystem

PSoC 6 MCU Resources

Cypress provides a wealth of data at www.cypress.com to help you select the right PSoC device and quickly and effectively integrate it into your design. The following is an abbreviated list of resources for PSoC 6 MCU:

- **Overview:** [PSoC Portfolio](#), [PSoC Roadmap](#)
- **Product Selectors:** [PSoC 6 MCU](#)
- **Application Notes** cover a broad range of topics, from basic to advanced level, and include the following:
 - [AN22174](#): Getting Started with PSoC 6 MCU
 - [AN218241](#): PSoC 6 MCU Hardware Design Guide
 - [AN213924](#): PSoC 6 MCU Device Firmware Update Guide
 - [AN219528](#): PSoC 6 MCU Power Reduction Techniques
 - [AN85951](#): PSoC 4, PSoC 6 MCU CapSense Design Guide
- **Code Examples** demonstrate product features and usage, and are also available on [Cypress GitHub repositories](#).
- **Technical Reference Manuals (TRMs)** provide detailed descriptions of PSoC 6 MCU architecture and registers.
- **PSoC 6 MCU Programming Specification** provides the information necessary to program PSoC 6 MCU nonvolatile memory
- **Development Tools**
 - [ModusToolbox®](#) software enables cross platform code development with a robust suite of tools and software libraries
 - [“Secure Boot” SDK](#) includes all required libraries, tools, and sample code to provision and develop applications for PSoC 64 MCUs.
 - [CY8CKIT-064B0S2-4343W^{\[2\]}](#) PSoC 64 “Secure Boot” Prototyping Kit: a low-cost hardware platform that enables design and debug of the PSoC 64 CYB0644xxZI-S2D44 product line.
 - [PSoC 6 CAD libraries](#) provide footprint and schematic support for common tools. [BSDL files](#) and [IBIS models](#) are also available.
- **Training Videos** are available on a wide range of topics including the [PSoC 6 MCU 101 series](#)
- **Cypress Developer Community** enables connection with fellow PSoC developers around the world, 24 hours a day, 7 days a week, and hosts a dedicated [PSoC 6 MCU Community](#)

Note

2. The link will be provided in a later revision.

ModusToolbox Software

ModusToolbox Software is Cypress' comprehensive collection of multi-platform tools and software libraries that enable an immersive development experience for creating converged MCU and wireless systems. It is:

- Comprehensive - it has the resources you need
- Flexible - you can use the resources in your own workflow
- Atomic - you can get just the resources you want

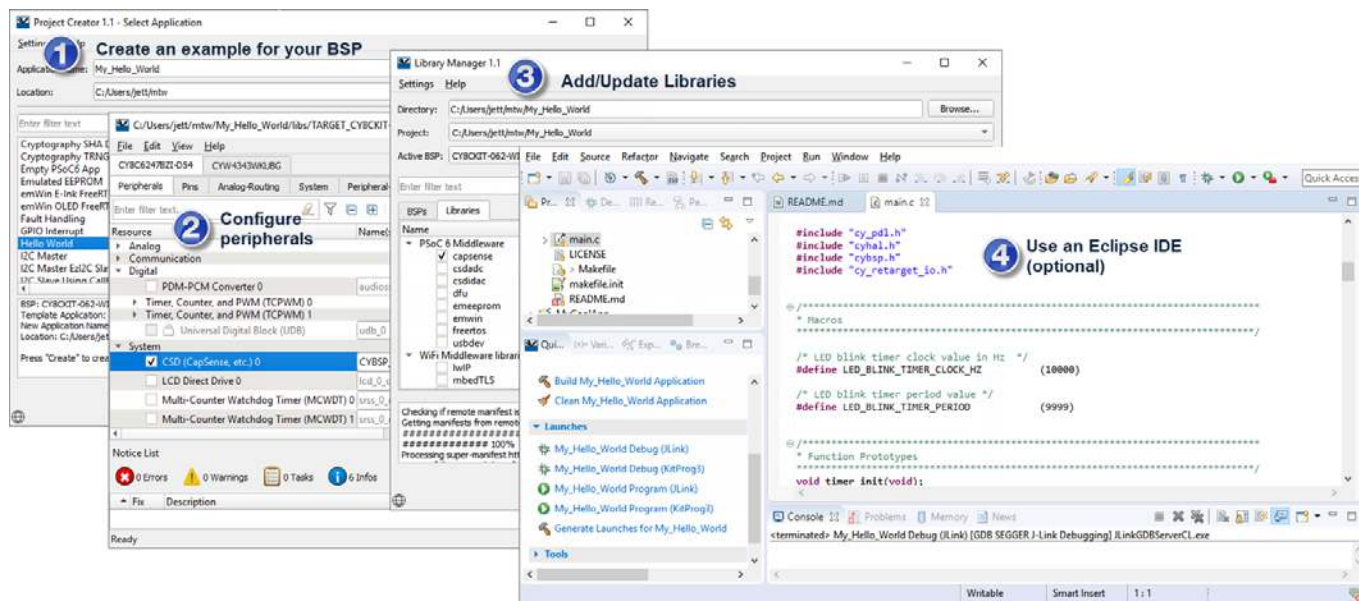
Cypress provides a large collection of code [repositories on GitHub](#). This includes:

- Board Support Packages (BSPs) aligned with Cypress kits
- Low-level resources, including a hardware abstraction layer (HAL) and peripheral driver library (PDL)
- Middleware enabling industry-leading features such as CapSense®, Bluetooth Low Energy, and mesh networks
- An extensive set of thoroughly tested [code example applications](#)

Note: The HAL provides a high-level, simplified interface to configure and use the hardware blocks on Cypress MCUs. It is a generic interface that can be used across multiple product families. For example, it wraps the PSoC 6 PDL with a simplified API, but the PDL exposes all low-level peripheral functionality. You can leverage the HAL's simpler and more generic interface for most of an application, even if one portion requires finer-grained control.

ModusToolbox Software is IDE-neutral and easily adaptable to your workflow and preferred development environment. It includes a project creator, peripheral and library configurators, a library manager, as well as the optional Eclipse IDE for ModusToolbox. For information on using Cypress tools, refer to the documentation delivered with ModusToolbox software, and [AN228571: Getting Started with PSoC 6 MCU on ModusToolbox](#).

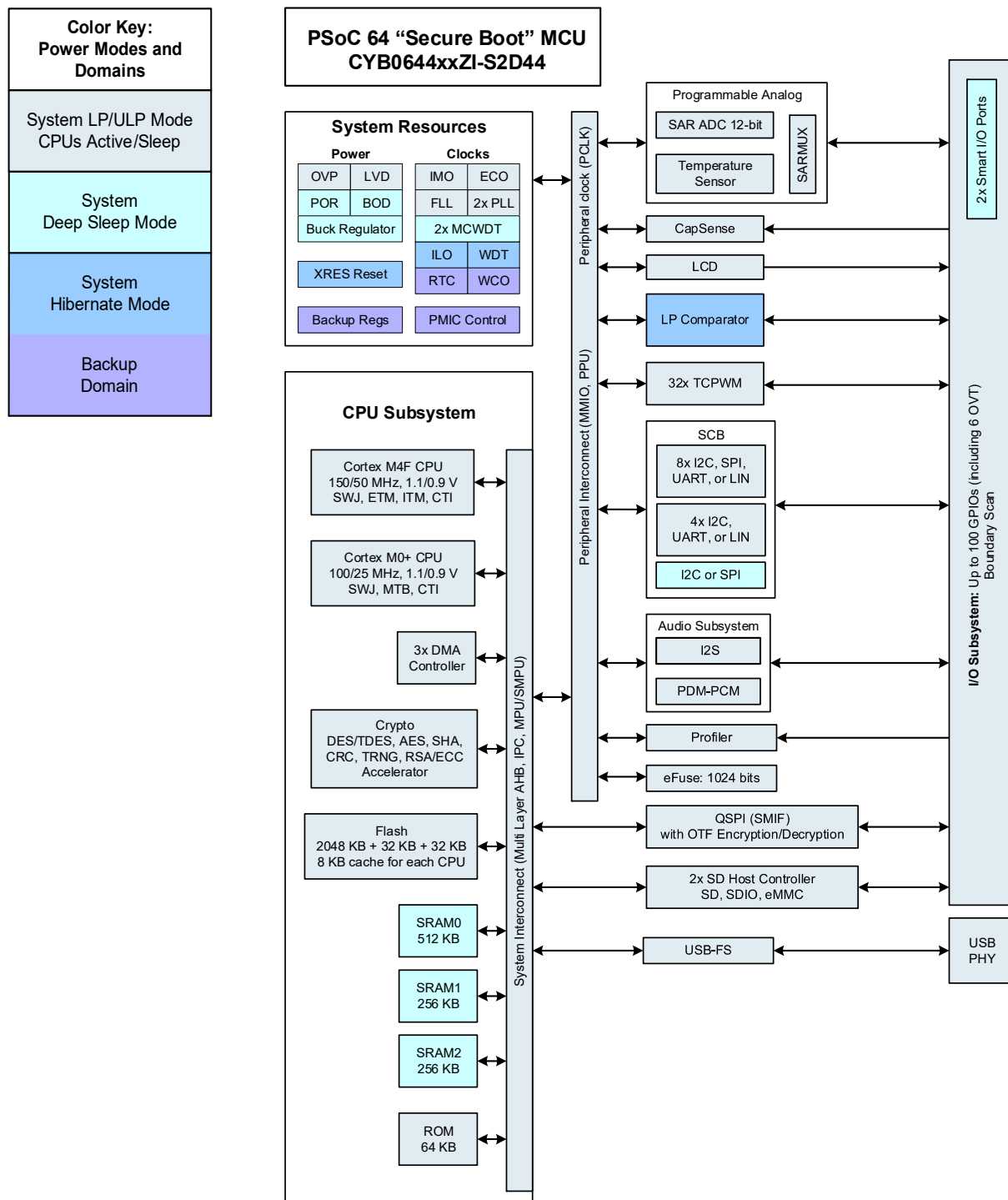
Figure 1. ModusToolbox Software Tools



Blocks and Functionality

Figure 2 shows the major subsystems and a simplified view of their interconnections. The color coding shows the lowest power mode where the particular block is still functional (for example, the SRAM is functional down to system Deep Sleep mode).

Figure 2. Block Diagram



This product line has up to 2 MB of flash; however 192 KB is reserved for system usage, leaving 1856 KB for applications. It also has up to 1 MB of SRAM; however 80 KB is reserved for system usage, leaving 944 KB for applications.

The PSoC 64 devices offer an immutable, RoT-based boot-up process, which allows only signed applications to be booted up. In addition, user assets such as keys and debug policies can be provisioned on the device in an HSM environment and made immutable. PSoC 64 also allows for root-of-trust based cryptography services which can be accessed using system calls.

There are three debug access ports, one each for CM4 and CM0+, and a system port. All debug and test interfaces can be permanently disabled during final production provisioning to avoid any malicious reprogramming or reading of flash and register contents.

PSoC 6 MCU devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware. All device interfaces can be permanently disabled for applications concerned about a reprogrammed device or starting and interrupting flash programming sequences. All programming, debug, and test interfaces can be disabled.

Complete debug-on-chip functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The Eclipse IDE for ModusToolbox provides fully integrated programming and debug support for these devices. The SWJ (SWD and JTAG) interface is fully compatible with industry-standard third party probes. With the ability to disable debug features, with very robust flash protection, and by allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, PSoC 6 provides multiple levels of device security.

Functional Description

The following sections provide an overview of the features, capabilities and operation of each functional block identified in the block diagram in [Figure 2](#). For more detailed information, refer to the following documentation:

■ Board Support Package (BSP) Documentation

BSPs are available on [GitHub](#). They are aligned with Cypress kits and provide files for basic device functionality such as hardware configuration files, startup code, and linker files. The BSP also includes other libraries that are required to support a kit. Each BSP has its own documentation, but typically includes an API reference such as the example [here](#). This [search link](#) finds all currently available BSPs on the Cypress GitHub site.

■ Hardware Abstraction Layer API Reference Manual

The Cypress Hardware Abstraction Layer (HAL) provides a high-level interface to configure and use hardware blocks on Cypress MCUs. It is a generic interface that can be used across multiple product families. You can leverage the HAL's simpler and more generic interface for most of an application, even if one portion requires finer-grained control. The [HAL API Reference](#) provides complete details. Example applications that use the HAL download it automatically from the GitHub repository.

■ Peripheral Driver Library (PDL) Application Programming Interface (API) Reference Manual

The Peripheral Driver Library (PDL) integrates device header files and peripheral drivers into a single package and supports all PSoC 6 MCU product lines. The drivers abstract the hardware functions into a set of easy-to-use APIs. These are fully documented in the [PDL API Reference](#). Example applications that use the PSoC 6 PDL download it automatically from the GitHub repository.

■ Architecture Technical Reference Manual (TRM)

The architecture TRM provides a detailed description of each resource in the device. This is the next reference to use if it is necessary to understand the operation of the hardware below the software provided by PDL. It describes the architecture and functionality of each resource and explains the operation of each resource in all modes. It provides specific guidance regarding the use of associated registers.

■ Register Technical Reference Manual

The register TRM provides a complete list of all registers in the device. It includes the breakdown of all register fields, their possible settings, read/write accessibility, and default states. All registers that have a reasonable use in typical applications have functions to access them from within PDL. Note that ModusToolbox and PDL may provide software default conditions for some registers that are different from and override the hardware defaults.

CPU and Memory Subsystem

PSoC 6 has multiple bus masters, as [Figure 2](#) shows. They are: CPUs, DMA controllers, QSPI, USB, SD Host Controllers, and a Crypto block. Generally, all memory and peripherals can be accessed and shared by all bus masters through multi-layer Arm AMBA high-performance bus (AHB) arbitration. Accesses between CPUs can be synchronized using an inter-processor communication (IPC) block.

CPUs

There are two Arm Cortex CPUs:

The Cortex-M4 (CM4) has single-cycle multiply, a floating-point unit (FPU), and a memory protection unit (MPU). It can run at up to 150 MHz. This is the main CPU, designed for a short interrupt response time, high code density, and high throughput.

CM4 implements a version of the Thumb instruction set based on Thumb-2 technology (defined in the [Armv7-M Architecture Reference Manual](#)).

The Cortex-M0+ (CM0+) has single-cycle multiply, and an MPU. It can run at up to 100 MHz; however, for CM4 speeds above 100 MHz, CM0+ and bus peripherals are limited to half the speed of CM4. Thus, for CM4 running at 150 MHz, CM0+ and peripherals are limited to 75 MHz.

In PSoC 64, the initial CM0+ frequency is set according to a provisioned security policy (see [PSoC 64 Security](#)). The frequency ranges from 8 MHz to 50 MHz. For more information, see the Architecture and Registers TRM.

CM0+ is the secondary CPU; it is used to implement system calls and device-level safety and protection features. CM0+ provides a secured, uninterruptible boot function. This helps ensure that post boot, system integrity is checked and memory and peripheral access privileges are enforced.

CM0+ implements the Armv6-M Thumb instruction set (defined in the [Armv6-M Architecture Reference Manual](#)).

The CPUs have the following power draw, at $V_{DD} = 3.3$ V and using the internal buck regulator:

Table 1. Active Current Slope at $V_{DD} = 3.3$ V Using the Internal Buck Regulator

| | | System Power Mode | |
|-----|------------|-------------------|----------------|
| | | ULP | LP |
| CPU | Cortex-M0+ | 20 μ A/MHz | 28 μ A/MHz |
| | Cortex-M4 | 27 μ A/MHz | 40 μ A/MHz |

The CPUs can be selectively placed in their Sleep and Deep Sleep power modes as defined by Arm.

Both CPUs have nested vectored interrupt controllers (NVIC) for rapid and deterministic interrupt response, and wakeup interrupt controllers (WIC) for CPU wakeup from Deep Sleep power mode.

The CPUs have extensive debug support. PSoC 6 has a debug access port (DAP) that acts as the interface for device programming and debug. An external programmer or debugger (the "host") communicates with the DAP through the device serial wire debug (SWD) or Joint Test Action Group (JTAG)

interface pins. Through the DAP (and subject to restrictions), the host can access the device memory and peripherals as well as the registers in both CPUs.

Each CPU offers debug and trace features as follows:

- CM4 supports six hardware breakpoints and four watchpoints, 4-bit embedded trace macrocell (ETM), serial wire viewer (SWV), and printf()-style debugging through the single wire output (SWO) pin.
- CM0+ supports four hardware breakpoints and two watchpoints, and a micro trace buffer (MTB) with 4-KB dedicated RAM.

PSoC 6 also has an Embedded Cross Trigger for synchronized debugging and tracing of both CPUs.

Interrupts

This product line has 168 system and peripheral interrupt sources, and supports interrupts and system exceptions on both CPUs. CM4 has 168 interrupt request lines (IRQ), with the interrupt source 'n' directly connected to IRQn. CM0+ has eight interrupts IRQ[7:0] with configurable mapping of one or more interrupt sources to any of the IRQ[7:0]. CM0+ also supports eight internal (software only) interrupts.

Each interrupt supports configurable priority levels (eight levels for CM4 and four levels for CM0+). Up to four system interrupts can be mapped to each of the CPUs' non-maskable interrupts (NMI). Up to 39 interrupt sources are capable of waking the device from Deep Sleep power mode using the WIC. Refer to the [technical reference manual](#) for details.

InterProcessor Communication (IPC)

In addition to the Arm SEV and WFE instructions, a hardware InterProcessor Communication (IPC) block is included. It includes 16 IPC channels and 16 IPC interrupt structures. The IPC channels can be used to implement data communication between the processors. Each IPC channel also implements a locking scheme which can be used to manage shared resources. The IPC interrupts let one processor interrupt the other, signaling an event. This is used to trigger events such as notify and release of the corresponding IPC channels. Some IPC channels and other resources are reserved, as [Table 2](#) shows:

Table 2. Distribution of IPC Channels and Other Resources

| Resources Available | Resources Consumed |
|---|----------------------|
| IPC channels, 16 available | 13 reserved |
| IPC interrupts, 16 available | 13 reserved |
| Other interrupts | 1 reserved |
| CM0+ NMI | Reserved |
| Other resources: clock dividers, DMA channels, etc. | 4 CM0+ interrupt mux |

Direct Memory Access (DMA) Controllers

This product line has three DMA controllers, which support CPU-independent accesses to memory and peripherals. Two of them have 29 channels each and the third has 4 channels. The

descriptors for DMA channels can be in SRAM or flash. Therefore, the number of descriptors is limited only by the size of the memory. Each descriptor can transfer data in two nested loops with configurable address increments to the source and destination. The size of data transfer per descriptor varies based on the type of DMA channel. Refer to the [technical reference manual](#) for details.

Cryptography Accelerator (Crypto)

This subsystem consists of hardware implementation and acceleration of cryptographic functions and random number generators.

The Crypto subsystem supports the following:

- Encryption/Decryption Functions
 - Data Encryption Standard (DES)
 - Triple DES (3DES)
 - Advanced Encryption Standard (AES) (128-, 192-, 256-bit)
 - Elliptic Curve Cryptography (ECC)
 - RSA cryptography functions
- Hashing functions
 - Secure Hash Algorithm (SHA)
 - SHA-1
 - SHA-224/-256/-384/-512
- Message authentication functions (MAC)
 - Hashed message authentication code (HMAC)
 - Cipher-based message authentication code (CMAC)
- 32-bit cyclic redundancy code (CRC) generator
- Random number generators
 - Pseudo random number generator (PRNG)
 - True random number generator (TRNG)

Protection Units

This product line has multiple types of protection units to control erroneous or unauthorized access to memory and peripheral registers. CM4 and CM0+ have Arm MPUs for protection at the bus master level. Other bus masters use additional MPUs. Shared memory protection units (SMPUs) help implement protection for memory resources that are shared among multiple bus masters. Peripheral protection units (PPU) are similar to SMPUs but are designed for protecting the peripheral register space.

Protection units support memory and peripheral access attributes including address range, read/write, code/data, privilege level, secured/non-secured, and protection context. Some protection unit resources are reserved for system usage; see the [technical reference manual](#) for details.

Up to eight protection contexts (boot is in protection context 0) allow access privileges for memory and system resources to be set by the boot process per protection context by bus master and code privilege level.

In PSoC 64, multiple protection contexts are used to isolate the different security levels within the device. The CM0+ makes use of several of them during the boot sequence, bootloading, system calls, etc. Protection context 6 is used for the user application code that runs on the CM4 CPU. The SMPUs are set up by default and cannot be modified by the user. See section 8 in the Architecture TRM for the protection context assignment.

Memory

PSoC 6 contains flash, SRAM, ROM, and eFuse memory blocks.

■ Flash

There is up to 2 MB of flash; however 192 KB is reserved for system usage, leaving 1856 KB for applications, organized in 256-KB sectors.

There are also two 32-KB flash sectors:

- Auxiliary flash (AUXflash), typically used for EEPROM emulation
- Supervisory flash (Sflash). Data stored in Sflash includes device trim values, [Flash Boot](#) code, and encryption keys. After the device transitions into the “Secure” lifecycle stage, Sflash can no longer be changed.

The flash has 128-bit-wide accesses to reduce power. Write operations can be performed at the row level. A row is 512 bytes. Read operations are supported in both Low Power and Ultra-Low Power modes, however write operations may not be performed in Ultra-Low Power mode.

The flash controller has two caches, one for each CPU. Each cache is 8 KB, with 4-way set associativity.

■ SRAM

There is 944 KB of SRAM available for applications. The remaining 80 KB is reserved for system usage. SRAM is provided in three banks of 432 KB, 256 KB, and 256 KB. Each SRAM bank provides control over power modes to manage power consumption. For Bank 0 (432 KB), power control and retention granularity are configurable in thirteen 32-KB regions. For banks 1 and 2 (256 KB each) power control is on a per bank basis. For normal operation, the banks can be enabled or disabled to save power. For Deep Sleep mode, the banks can also be configured to retain data.

■ ROM

The 64-KB ROM, also referred to as the supervisory ROM (SROM), provides code ([ROM Boot](#)) for several system functions. The ROM contains device initialization, flash write, security, eFuse programming, and other system-level routines. ROM code is executed only by the CM0+ CPU, in protection context 0. A system function can be initiated by either CPU, or through the DAP. This causes an NMI in CM0+, which causes CM0+ to execute the system function.

■ eFuse

A one-time-programmable (OTP) eFuse array consists of 1024 bits, all of which are reserved for system use. The bits are used for storing hash values, unique IDs, or other similar PSoC 64 parameters.

Each fuse is individually programmed; once programmed (or “blown”), its state cannot be changed. Blowing a fuse transitions it from the default state of 0 to 1. To program an eFuse, V_{DDIO0} must be at 2.5 V \pm 5%, at 14 mA.

Because blowing an eFuse is an irreversible process, programming is recommended only in mass production under controlled factory conditions. For more information, see [PSoC 6 MCU Programming Specifications](#).

Boot Code

Two blocks of code, [ROM Boot](#) and [Flash Boot](#), are pre-programmed into the device and work together to provide device startup and configuration, basic security features, lifecycle stage management and other system functions.

■ ROM Boot

On a device reset, the boot code in ROM is the first code to execute. This code performs the following:

- Integrity checks of flash boot code
 - Device trim setting (calibration)
 - Setting the device protection units
 - Setting device access restrictions for “Secure” lifecycle states
- ROM cannot be changed and acts as the root of trust in a secured system.

■ Flash Boot

Flash boot is firmware stored in SFlash that ensures that only a validated application may run on the device. It also ensures that the firmware image has not been modified, such as by a malicious third party.

Flash boot:

- Is validated by ROM Boot
- Runs after ROM Boot and before the user application
- Enables system calls
- Enables provisioning and device policy features
- Implements RoT-based services for cryptography
- Provides secured storage for keys and certificates
- Validates and launches first image based on policies provisioned in the device
- Uses mbed TLS v2.24

If the user application cannot be validated, then flash boot ensures that the device is transitioned into a safe state. Refer to the [PSoC 64 Security](#) section for more details.

Memory Map

Both CPUs have a fixed address map, with shared access to memory and peripherals. The 32-bit (4 GB) address space is divided into the Arm-defined regions shown in [Table 3](#). Note that code can be executed from the Code and External RAM regions.

Table 3. Address Map for CM4 and CM0+

| Address Range | Name | Use |
|----------------------------|------------------------|---|
| 0x0000 0000 – 0x1FFF FFFF | Code | Program code region. Data can also be placed here. It includes the exception vector table, which starts at address 0. |
| 0x2000 0000 – 0x3FFF FFFF | SRAM | Data region. This region is not supported in PSoC 6. |
| 0x4000 0000 – 0x5FFF FFFF | Peripheral | All peripheral registers. Code cannot be executed from this region. CM4 bit-band in this region is not supported in PSoC 6. |
| 0x6000 0000 – 0x9FFF FFFF | External RAM | SMIF or Quad SPI, (see the Quad-SPI/Serial Memory Interface (SMIF) section). Code can be executed from this region. |
| 0xA000 0000 – 0xDFFF FFFF | External Device | Not used. |
| 0xE000 0000 – 0xE00F FFFF | Private Peripheral Bus | Provides access to peripheral registers within the CPU core. |
| 0xE010 0A000 – 0xFFFF FFFF | Device | Device-specific system registers. |

The device memory map shown in [Table 4](#) applies to both CPUs. That is, the CPUs share access to all PSoC 6 MCU memory and peripheral registers.

Table 4. Internal Memory Address Map for CM4 and CM0+

| Address Range | Memory Type | Size |
|--|---|-------------------------|
| 0x0000 0000 – 0x0000 FFFF | ROM | 64 KB |
| 0x0800 0000 – 0x080E BFFF 0x080E C000 - 0x080F FFFF | Application SRAM System SRAM | Up to 944 KB 80 KB |
| 0x1000 0000 – 0x101C FFFF 0x101D 0000 - 0x101F FFFF | Application flash Secured code flash Used for secured boot, secured boot-loader, and system calls | Up to 1856 KB 192 KB |
| 0x1400 0000 – 0x1400 7FFF | Auxiliary flash, can be used for EE-PROM emulation | 32 KB |
| 0x1600 0000 – 0x1600 7FFF | Supervisory flash, for secured access | 32 KB |

Note that PSoC 6 SRAM is located in the Arm Code region for both CPUs (see [Table 3](#)). There is no physical memory located in the CPUs' Arm SRAM regions.

System Resources

Power System

The power system provides assurance that voltage levels are as required for each respective mode and will either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) when the power supply drops below specified levels. The design guarantees safe chip operation between power supply voltage dropping below specified levels (for example, below 1.7 V) and the reset occurring. There are no voltage sequencing requirements.

The V_{DD} supply (1.7 to 3.6 V) powers an on-chip buck regulator or a low-dropout regulator (LDO), selectable by the user. In addition, both the buck and the LDO offer a selectable (0.9 or 1.1 V) core operating voltage (V_{CCD}). The selection lets users choose between two system power modes:

- System Low Power (LP) operates V_{CCD} at 1.1 V and offers high performance, with no restrictions on device configuration.
- System Ultra Low Power (ULP) operates V_{CCD} at 0.9 V for exceptional low power, but imposes limitations on clock speeds.

In addition, a backup domain adds an “always on” functionality using a separate power domain supplied by a backup supply (V_{BACKUP}) such as a battery or supercapacitor. It includes a real-time clock (RTC) with alarm feature, supported by a 32.768-kHz watch crystal oscillator (WCO), and power-management IC (PMIC) control. Refer to [Power Supply Considerations](#) for more details.

Power Modes

PSoC 6 MCU can operate in four system and three CPU power modes. These modes are intended to minimize the average power consumption in an application. For more details on power modes and other power-saving configuration options, see the application note, [AN219528: PSoC 6 MCU Low-Power Modes and Power Reduction Techniques](#). Contact your local Cypress sales representative for the latest [technical reference manual](#).

Power modes supported by PSoC 6 MCUs, in order of decreasing power consumption, are:

- System Low Power (LP) – All peripherals and CPU power modes are available at maximum speed
- System Ultra Low Power (ULP) – All peripherals and CPU power modes are available, but with limited speed
- CPU Active – CPU is executing code in system LP or ULP mode

- CPU Sleep – CPU code execution is halted in system LP or ULP mode
- CPU Deep Sleep – CPU code execution is halted and system Deep Sleep is requested in system LP or ULP mode
- System Deep Sleep – Only low-frequency peripherals are available after both CPUs enter CPU Deep Sleep mode
- System Hibernate – Device and I/O states are frozen and the device resets on wakeup

CPU Active, Sleep, and Deep Sleep are standard Arm-defined power modes supported by the Arm CPU instruction set architecture (ISA). System LP, ULP, Deep Sleep and Hibernate modes are additional low-power modes supported by PSoC 6 MCU.

Clock System

[Figure 3](#) shows that the clock system of this product line consists of the following:

- Internal main oscillator (IMO)
- Internal low-speed oscillator (ILO)
- Watch crystal oscillator (WCO)
- External MHz crystal oscillator (ECO)
- External clock input
- Two phase-locked loops (PLLs)
- One frequency-locked loop (FLL)

Clocks may be buffered and brought out to a pin on a smart I/O port.

The default clocking when the application starts is CLK_HF[0] being driven by the IMO and the FLL. CLK_HF[0], clk_fast, clk_peri, and clk_slow are all either 50 MHz (LP mode) or 25 MHz (ULP mode). All other clocks, including all peripheral clocks, are off.

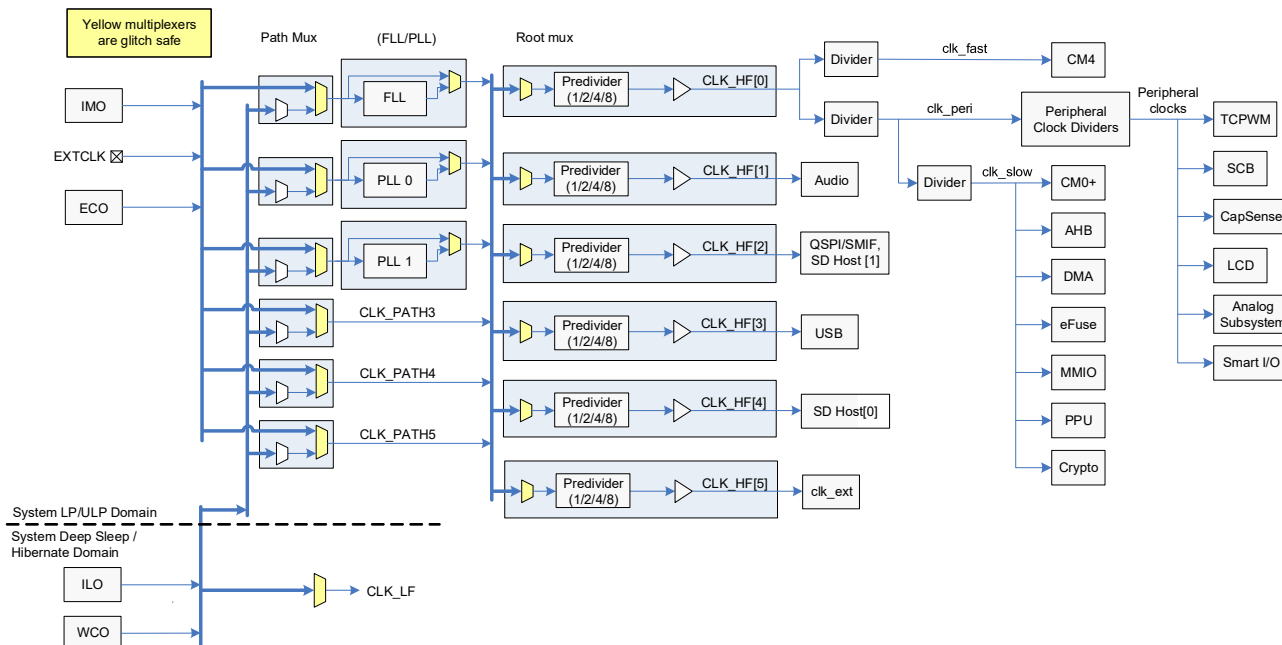
Internal Main Oscillator (IMO)

The IMO is the primary source of internal clocking. It is trimmed at the factory to achieve the specified accuracy. The IMO frequency is 8 MHz and tolerance is $\pm 2\%$.

Internal Low-speed Oscillator (ILO)

The ILO is a very low power oscillator, nominally 32 kHz, which operates in all power modes. The ILO can be calibrated against a higher accuracy clock for better accuracy.

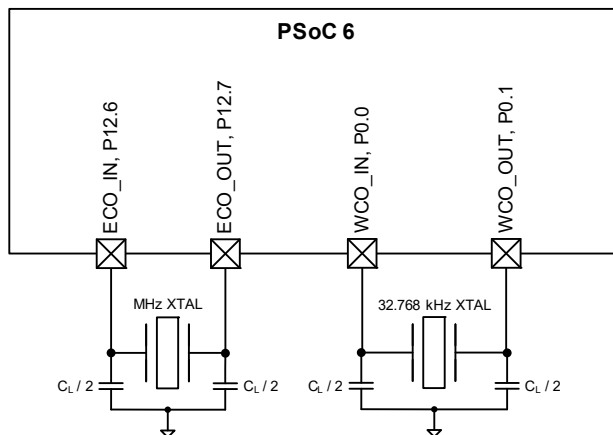
Figure 3. Clocking Diagram



External Crystal Oscillators

Figure 4 shows all of the external crystal oscillator circuits for this product line. The component values shown are typical; check [ECO Specifications](#) for the crystal values, and the crystal datasheet for the load capacitor values. The ECO and WCO require balanced external load capacitors. For more information, see the TRM and [AN218241, PSoC 6 MCU Hardware Design Considerations](#).

Figure 4. Oscillator Circuits



If the ECO is used, note that its performance is affected by GPIO switching noise. GPIO ports should be used as [Table 5](#) shows.

See also [Table 6](#) for additional restrictions for general analog subsystem use.

Table 5. ECO Usage Guidelines

| Ports | Max Frequency | Drive Strength for $V_{DD} \leq 2.7$ V | Drive Strength for $V_{DD} \leq 2.7$ V |
|-----------------|------------------------|--|--|
| Port 11 | 60 MHz for SMIF (QSPI) | DRIVE_SEL 2 | DRIVE_SEL 3 |
| Ports 12 and 13 | Slow slew rate setting | No restrictions | No restrictions |

Watchdog Timers (WDT, MCWDT)

PSoC 6 MCU has one WDT and two multi-counter WDTs (MCWDT). The WDT has a 16-bit free-running counter. Each MCWDT has two 16-bit counters and one 32-bit counter, with multiple operating modes. All of the 16-bit counters can generate a watchdog device reset. All of the counters can generate an interrupt on a match event.

The WDT is clocked by the ILO. It can generate interrupt/wakeup in system LP/ULP, Deep Sleep, and Hibernate power modes. The MCWDTs are clocked by LFCLK (ILO or WCO). It can generate periodic interrupt / wakeup in system LP/ULP and Deep Sleep power modes.

Clock Dividers

Integer and fractional clock dividers are provided for peripheral use and timing purposes. There are:

- Eight 8-bit clock dividers
- Sixteen 16-bit integer clock dividers
- Four 16.5-bit fractional clock dividers
- One 24.5-bit fractional clock divider

Trigger Routing

PSoC 6 MCU contains a trigger multiplexer block. This is a collection of digital multiplexers and switches that are used for routing trigger signals between peripheral blocks and between GPIOs and peripheral blocks.

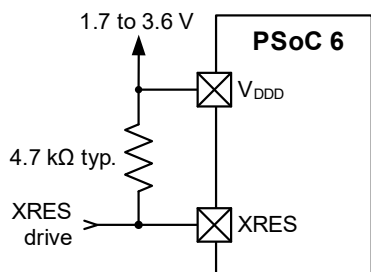
There are two types of trigger routing. Trigger multiplexers have reconfigurability in the source and destination. There are also hardwired switches called “one-to-one triggers”, which connect a specific source to a destination. The user can enable or disable the route.

Reset

PSoC 6 MCU can be reset from a variety of sources:

- Power-on reset (POR) to hold the device in reset while the power supply ramps up to the level required for the device to function properly. POR activates automatically at power-up.
- Brown-out detect (BOD) reset to monitor the digital voltage supply V_{DD} and generate a reset if V_{DD} falls below the minimum required logic operating voltage.
- External reset dedicated pin (XRES) to reset the device using an external source. The XRES pin is active low. It can be connected either to a pull-up resistor to V_{DD} , or to an active drive circuit, as Figure 5 shows. If a pull-up resistor is used, select its value to minimize current draw when the pin is pulled low; 4.7 k Ω is typical.

Figure 5. XRES Connection Diagram



- Watchdog timer (WDT or MCWDT) to reset the device if firmware fails to service it within a specified timeout period.
- Software-initiated reset to reset the device on demand using firmware.
- Logic-protection fault can trigger an interrupt or reset the device if unauthorized operating conditions occur; for example, reaching a debug breakpoint while executing privileged code.
- Hibernate wakeup reset to bring the device out of the system Hibernate power mode.

Reset events are asynchronous and guarantee reversion to a known state. Some of the reset sources are recorded in a register, which is retained through reset and allows software to determine the cause of the reset.

Programmable Analog Subsystems

12-bit SAR ADC

The 12-bit, 2-Msps SAR ADC can operate at a maximum clock rate of 36 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion. One of three internal reference voltages may be used for an ADC reference voltage. The references are, V_{DD} , $V_{DD}/2$, and V_{REF} (nominally 1.2 V and trimmed to $\pm 1\%$). An external reference may also be used, by either driving the VREF pin or routing an external reference to GPIO pin P9.7. These reference options allow ratio-metric readings or absolute readings at the accuracy of the reference used. The input range of the ADC is the full supply voltage between V_{SS} and V_{DDA}/V_{DDIOA} . The SAR ADC may be configured with a mix of single-ended and differential signals in the same configuration.

The SAR ADC’s sample-and-hold (S/H) aperture is programmable to allow sufficient time for signals with a high impedance to settle sufficiently, if required. System performance is 65 dB for true 12-bit precision provided appropriate references are used and system noise levels permit it. To improve performance in noisy conditions, an external bypass capacitor for the internal reference amplifier (through the fixed “VREF” pin), may be added.

The SAR is connected to a fixed set of pins through an input multiplexer. The multiplexer cycles through the selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 2 Msps whether it is for a single channel or distributed over several channels). The result of each channel is buffered, so that an interrupt may be triggered only when a full scan of all channels is complete. Also, a pair of range registers can be set to detect and cause an interrupt if an input exceeds a minimum and/or maximum value. This allows fast detection of out-of-range values without having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software. The SAR can also be connected, under firmware control, to most other GPIO pins via the Analog Multiplexer Bus (AMUXBUS). The SAR is not available in system Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 36 MHz). The SAR operating range is 1.71 to 3.6 V.

Temperature Sensor

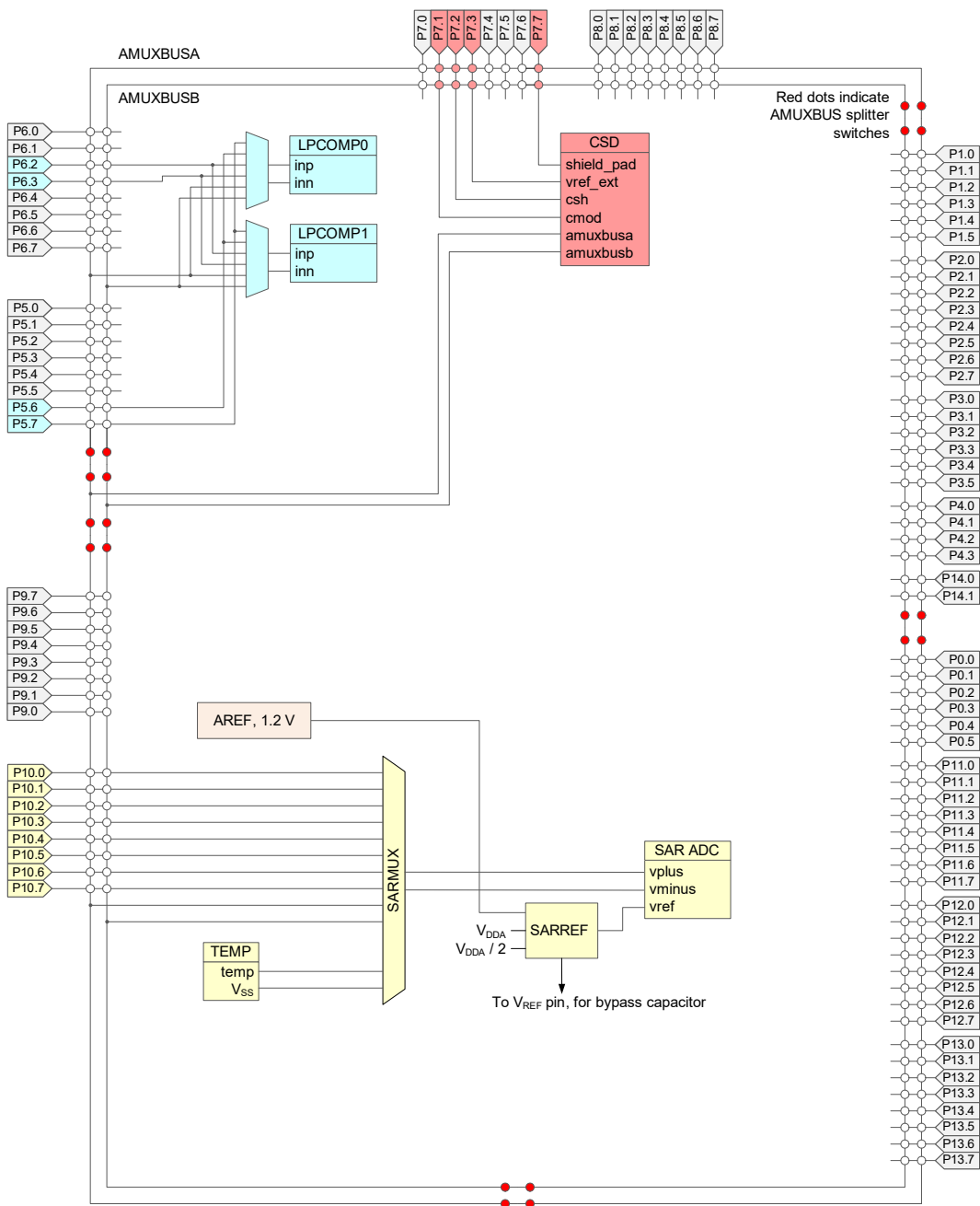
An on-chip temperature sensor is part of the SAR and may be scanned by the SAR ADC. It consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor may be connected directly to the SAR ADC as one of the measurement channels. The ADC digitizes the temperature sensor’s output and a Cypress-supplied software function may be used to convert the reading to temperature which includes calibration and linearization.

Low-Power Comparators

Two low-power comparators are provided, which can operate in all power modes. This allows other analog system resources to be disabled while retaining the ability to monitor external voltage levels during system Deep Sleep and Hibernate modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator-switch event.

Figure 6 shows an overview of the analog subsystem. This diagram is a high-level abstraction. See the TRM for detailed connectivity information.

Figure 6. Analog Subsystem



Programmable Digital

Smart I/O

Smart I/O is a programmable logic fabric that enables Boolean operations on signals traveling from device internal resources to the GPIO pins or on signals traveling into the device from external sources. A Smart I/O block sits between the GPIO pins and the high-speed I/O matrix (HSIOM) and is dedicated to a single port.

There are two Smart I/O blocks: one on Port 8 and one on Port 9. When Smart I/O is not enabled, all signals on Port 8 and Port 9 bypass the Smart I/O hardware.

Smart I/O supports:

- System Deep Sleep operation
- Boolean operations without CPU intervention
- Asynchronous or synchronous (clocked) operation

Each Smart I/O block contains a data unit (DU) and eight lookup tables (LUTs).

The DU:

- Performs unique functions based on a selectable opcode.
- Can source input signals from internal resources, the GPIO port, or a value in the DU register.

Each LUT:

- Has three selectable input sources. The input signals may be sourced from another LUT, an internal resource, an external signal from a GPIO pin, or from the DU.
- Acts as a programmable Boolean logic table.
- Can be synchronous or asynchronous.

Fixed-Function Digital

Timer/Counter/Pulse-width Modulator (TCPWM)

- The TCPWM supports the following operational modes:
 - Timer-counter with compare
 - Timer-counter with capture
 - Quadrature decoding
 - Pulse width modulation (PWM)
 - Pseudo-random PWM
 - PWM with dead time
- Up, down, and up/down counting modes
- Clock prescaling (division by 1, 2, 4, ... 64, 128)
- Double buffering of compare/capture and period values
- Underflow, overflow, and capture/compare output signals
- Supports interrupt on:
 - Terminal count – Depends on the mode; typically occurs on overflow or underflow
 - Capture/compare – The count is captured to the capture register or the counter value equals the value in the compare register
- Complementary output for PWMs
- Selectable start, reload, stop, count, and capture event signals for each TCPWM; with rising edge, falling edge, both edges, and level trigger options. The TCPWM has a Kill input to force outputs to a predetermined state.

In this device there are:

- Eight 32-bit TCPWMs
- Twenty-four 16-bit TCPWMs

Serial Communication Blocks (SCB)

This product line has 13 SCBs:

- Eight can implement either I²C, UART, or SPI.
- Four can implement either I²C or UART.
- One SCB (SCB #8) can operate in system Deep Sleep mode with an external clock; this SCB can be either SPI slave or I²C slave.

I²C Mode: The SCB can implement a full multi-master and slave interface (it is capable of multimaster arbitration). This block can operate at speeds of up to 1 Mbps (Fast Mode Plus). It also supports EZI²C, which creates a mailbox address range and effectively reduces I²C communication to reading from and writing to an array in memory. The SCB supports a 256-byte FIFO for receive and transmit.

The I²C peripheral is compatible with I²C standard-mode, Fast Mode, and Fast Mode Plus devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

UART Mode: This is a full-feature UART operating at up to 8 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common Rx and Tx lines. Common UART functions such as parity error, break detect, and frame error are supported. A 256-byte FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block supports an EZSPI mode in which the data interchange is reduced to reading and writing an array in memory. The SPI interface operates with a 25-MHz clock.

USB Full-Speed Device Interface

This product line incorporates a full-speed USB device interface. The device can have up to eight endpoints. A 512-byte SRAM buffer is provided and DMA is supported.

Note: If the USB pins are not used, connect V_{DDUSB} to ground and leave the P14.0/USB DP and P14.1/USB DM pins unconnected.

Quad-SPI/Serial Memory Interface (SMIF)

A serial memory interface is provided, running at up to 80 MHz. It supports single, dual, quad, dual-quad and octal SPI configurations, and supports up to four external memory devices. It supports two modes of operation:

- Memory-mapped I/O (MMIO), a command mode interface that provides data access via registers and FIFOs
- Execute in Place (XIP), in which AHB reads and writes are directly translated to SPI read and write transfers.

In XIP mode, the external memory is mapped into the PSoC 6 MCU internal address space, enabling code execution directly from the external memory. To improve performance, a 4-KB cache is included. XIP mode also supports AES-128 on-the-fly encryption and decryption, enabling secured storage and access of code and data in the external memory.

LCD

This block drives LCD commons and segments; routing is available to most of the GPIOs. One to eight of the GPIOs must be used for commons, the rest can be used for segments.

The LCD block has two modes of operation: high speed (8 MHz) and low speed (32 kHz). Both modes operate in system LP and ULP modes. Low-speed mode operates with reduced contrast in system Deep Sleep mode - review the number of common and segment lines, viewing angle requirements, and prototype performance before using this mode.

SD Host Controllers

This product line contains two Secure Digital (SD) host controllers. They provide communication with IoT connectivity devices such as Bluetooth, Bluetooth Low-Energy and WiFi radios, as well as combination devices. The controller also supports embedded MultiMediaCards (eMMC) and Secure Digital (SD) cards.

Several bus speed modes under the SD specification are supported:

- DS (default speed)
- HS (high speed)
- SDR12 (single data rate)
- SDR25
- SDR50
- DDR50 (double data rate)

For eMMC, the supported modes are:

- BWC (backward compatibility)
- SDR

Maximum clock restrictions and capacitive loads apply to some modes, and are also dependent on system power mode (LP/ULP). Refer to the [SD Host Controller and eMMC Specifications](#) for details.

The SD Host Controller complies with the following standards. Refer to the specifications documents for more information on the protocol and operations.

- SD Specifications Part 1 Physical Layer Specification Version 6.00, supporting card capacities for SDSC (up to 2 GB), SDHC (up to 32 GB) and SDXC (up to 2 TB).
- SD Specifications Part A2 SD Host Controller Standard Specification Version 4.20
- SD Specifications Part E1 SDIO Specifications Version 4.10
- Embedded Multi-Media Card (eMMC) Electrical Standard 5.1

The SD Host Controller is configured as a master. To be fully compatible with features provided in the driver software for speed and efficiency, it supports advanced DMA version 3 (ADMA3), defined by the SDIO standard, and has a 1-KB Rx/Tx FIFO allowing double buffering of 512-byte blocks.

GPIO

This product line has up to 100 GPIOs, which implement the following:

- Eight drive strength modes:
 - Analog input mode (input and output buffers disabled)
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL)
- Hold mode for latching previous state (used for retaining the I/O state in system Hibernate mode)
- Selectable slew rates for dV/dt -related noise control to improve EMI

The pins are organized in logical entities called ports, which are up to 8 pins in width. Data output and pin state registers store, respectively, the values to be driven on the pins and the input states of the pins.

Every pin can generate an interrupt if enabled; each port has an interrupt request (IRQ) associated with it.

Table 6. DRIVE_SEL Values

| Ports | Max Frequency | Drive Strength for $V_{DD} \leq 2.7\text{ V}$ | Drive Strength for $V_{DD} > 2.7\text{ V}$ |
|----------------|-------------------------|---|--|
| Ports 0, 1 | 8 MHz | DRIVE_SEL 2 | DRIVE_SEL 3 |
| Port 2 | 50 MHz | DRIVE_SEL 1 | DRIVE_SEL 2 |
| Ports 3 to 10 | 16 MHz; 25 MHz for SPI | DRIVE_SEL 2 | DRIVE_SEL 3 |
| Ports 11 to 13 | 80 MHz for SMIF (QSPI). | DRIVE_SEL 1 | DRIVE_SEL 2 |

Special-Function Peripherals

Audio Subsystem

This subsystem consists of the following hardware blocks:

- Two Inter-IC Sound (I²S) interfaces
 - Two PDM to PCM decoder channels
- Each of the I²S interfaces implements two independent hardware FIFO buffers – Tx and Rx, which can operate in master or slave mode. The following features are supported:
- Multiple data formats – I²S, left-justified, Time Division Multiplexed (TDM) mode A, and TDM mode B
 - Programmable channel/word lengths – 8/16/18/20/24/32 bits
 - Internal/external clock operation up to 192 ksp/s
 - Interrupt mask events – trigger, not empty, full, overflow, underflow, watchdog
 - Configurable FIFO trigger level with DMA support

The I²S interface is commonly used to connect with audio codecs, simple DACs, and digital microphones.

The port 1 pins are capable of overvoltage-tolerant (OVT) operation, where the input voltage may be higher than V_{DD} . OVT pins are commonly used with I²C, to allow powering the chip OFF while maintaining a physical connection to an operating I²C bus without affecting its functionality.

GPIO pins can be ganged to source or sink higher values of current. GPIO pins, including OVT pins, may not be pulled up higher than the absolute maximum; see [Electrical Specifications](#).

During power-on and reset, the pins are forced to the analog input drive mode, with input and output buffers disabled, so as not to crowbar any inputs and/or cause excess turn-on current.

A multiplexing network known as the high-speed I/O matrix (HSIOM) is used to multiplex between various peripheral and analog signals that may connect to an I/O pin.

Analog performance is affected by GPIO switching noise. In order to get the best analog performance, the following frequency and drive mode constraints must be applied. The DRIVE_SEL values (refer to [Table 6](#)) represent drive strengths [Architecture and Register TRMs](#). Contact your local Cypress sales representative for the latest TRM.

See also [Table 5](#) for additional restrictions for ECO use.

The PDM-to-PCM decoder implements a single hardware Rx FIFO that decodes a stereo or mono 1-bit PDM input stream to PCM data output. The following features are supported:

- Programmable data output word length – 16/18/20/24 bits
- Programmable gain amplifier (PGA) for volume control – from –12 dB to +10.5 dB in 1.5 dB steps
- Configurable PDM clock generation. Range from 384 kHz to 3.072 MHz
- Droop correction and configurable decimation rate for sampling; up to 48 ksp/s
- Programmable high-pass filter gain
- Interrupt mask events – not empty, overflow, trigger, underflow
- Configurable FIFO trigger level with DMA support

The PDM-to-PCM decoder is commonly used to connect to digital PDM microphones. Up to two microphones can be connected to the same PDM Data line.

CapSense Subsystem

CapSense is supported in PSoC 6 MCU through a CapSense sigma-delta (CSD) hardware block. It is designed for high-sensitivity self-capacitance and mutual-capacitance measurements, and is specifically built for user interface solutions.

In addition to CapSense, the CSD hardware block supports three general-purpose functions. These are available when CapSense is not being used. Alternatively, two or more functions can be time-multiplexed in an application under firmware control. The four functions supported by the CSD hardware block are:

- CapSense
- 10-bit ADC
- Programmable current sources (IDAC)
- Comparator

CapSense

Capacitive touch sensors are designed for user interfaces that rely on human body capacitance to detect the presence of a finger on or near a sensor. Cypress CapSense solutions bring elegant, reliable, and simple capacitive touch sensing functions to applications including IoT, industrial, automotive, and home appliances.

The Cypress-proprietary CapSense technology offers the following features:

- Best-in-class signal-to-noise ratio (SNR) and robust sensing under harsh and noisy conditions
- Self-capacitance (CSD) and mutual-capacitance (CSX) sensing methods
- Support for various widgets, including buttons, matrix buttons, sliders, touchpads, and proximity sensors
- High-performance sensing across a variety of materials
- Best-in-class liquid tolerance
- SmartSense™ auto-tuning technology that helps avoid complex manual tuning processes
- Superior immunity against external noise
- Spread-spectrum clocks for low radiated emissions
- Gesture and built-in self-test libraries
- Ultra-low power consumption
- An integrated graphical CapSense tuner for real-time tuning, testing, and debugging

ADC

The CapSense subsystem slope ADC offers the following features:

- Selectable 8- or 10-bit resolution
- Selectable input range: GND to V_{REF} and GND to V_{DDA} on any GPIO input
- Measurement of V_{DDA} against an internal reference without the use of GPIO or external components

IDAC

The CSD block has two programmable current sources, which offer the following features:

- 7-bit resolution
- Sink and source current modes
- A current source programmable from 37.5 nA to 609 μ A
- Two IDACs that can be used in parallel to form one 8-bit IDAC

Comparator

The CapSense subsystem comparator operates in the system Low Power and Ultra-Low Power modes. The inverting input is connected to an internal programmable reference voltage and the non-inverting input can be connected to any GPIO via the AMUXBUS.

CapSense Hardware Subsystem

Figure 7 shows the high-level hardware overview of the CapSense subsystem, which includes a delta sigma converter, internal clock dividers, a shield driver, and two programmable current sources.

The inputs are managed through analog multiplexed buses (AMUXBUS A/B). The input and output of all functions offered by the CSD block can be provided on any GPIO or on a group of GPIOs under software control, with the exception of the comparator output and external capacitors that use dedicated GPIOs.

Self-capacitance is supported by the CSD block using AMUXBUS A, an external modulator capacitor, and a GPIO for each sensor. There is a shield electrode (optional) for self-capacitance sensing. This is supported using AMUXBUS B and an optional external shield tank capacitor (to increase the drive capability of the shield driver) should this be required. Mutual-capacitance is supported by the CSD block using AMUXBUS A, two external integrated capacitors, and a GPIO for transmit and receive electrodes.

The ADC does not require an external component. Any GPIO that can be connected to AMUXBUS A can be an input to the ADC under software control. The ADC can accept V_{DDA} as an input without needing GPIOs (for applications such as battery voltage measurement).

The two programmable current sources (IDACs) in general-purpose mode can be connected to AMUXBUS A or B. They can therefore connect to any GPIO pin. The comparator resides in the delta-sigma converter. The comparator inverting input can be connected to the reference. Both comparator inputs can be connected to any GPIO using AMUXBUS B; see Figure 7. The reference has a direct connection to a dedicated GPIO; see Table 9.

The CSD block can operate in active and sleep CPU power modes, and seamlessly transition between system LP and ULP modes. It can be powered down in system Deep Sleep and Hibernate modes. Upon wakeup from Hibernate mode, the CSD block requires re-initialization. However, operation can be resumed without re-initialization upon exit from Deep Sleep mode, under firmware control.

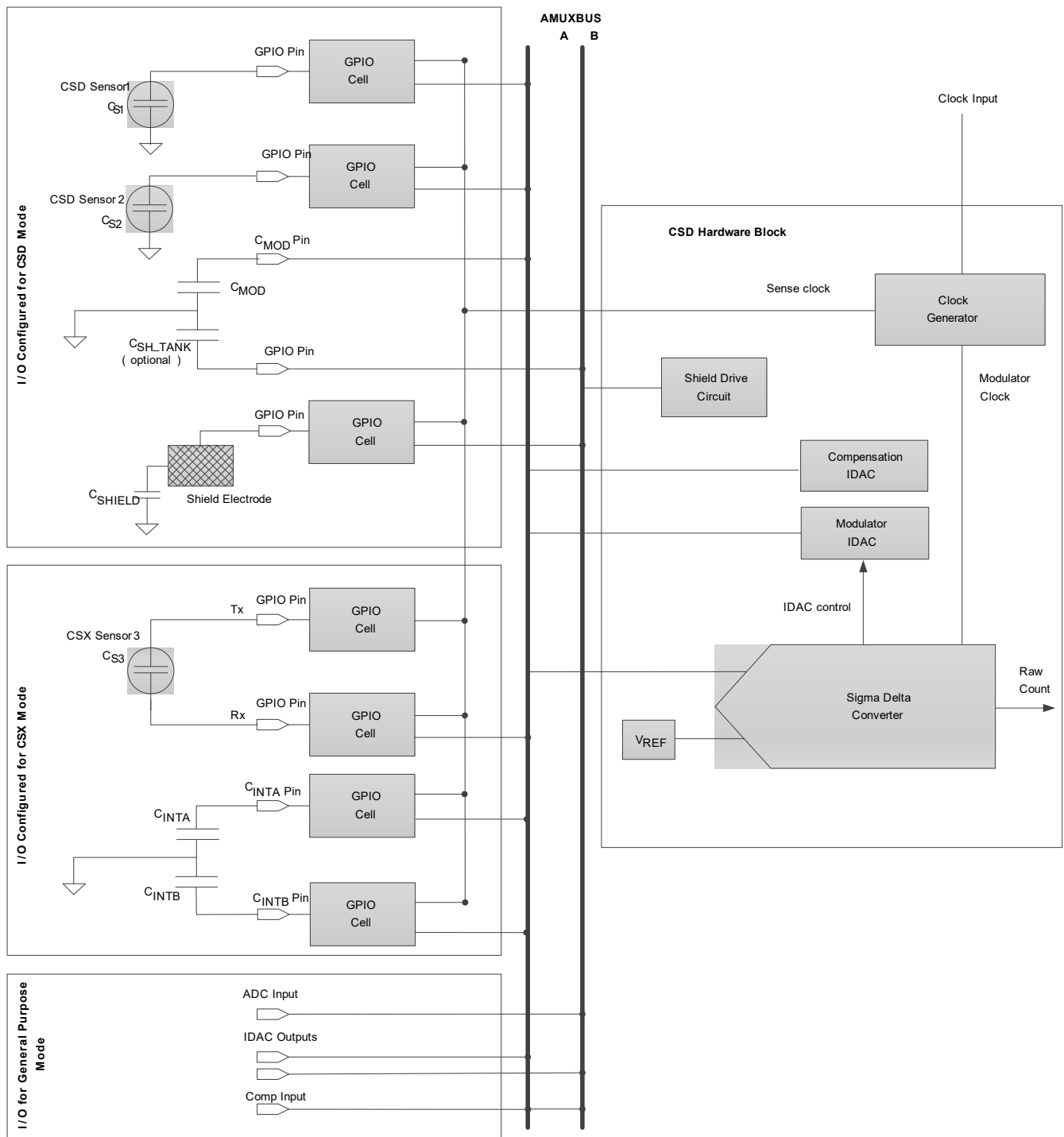
Figure 7. CapSense Hardware Subsystem


Figure 8 shows the high-level software overview. Cypress provides middleware libraries for [CapSense](#), [ADC](#), and [IDAC](#) on GitHub to enable quick integration. The Board Support Package for any kit with CapSense capabilities automatically includes the CapSense library in any application that uses the BSP.

User applications interact only with middleware to implement functions of the CSD block. The middleware interacts with underlying drivers to access hardware as necessary. The CSD driver facilitates time-multiplexing of the CSD hardware if more than one piece of CSD-related middleware is present in a project. It prevents access conflicts in this case.

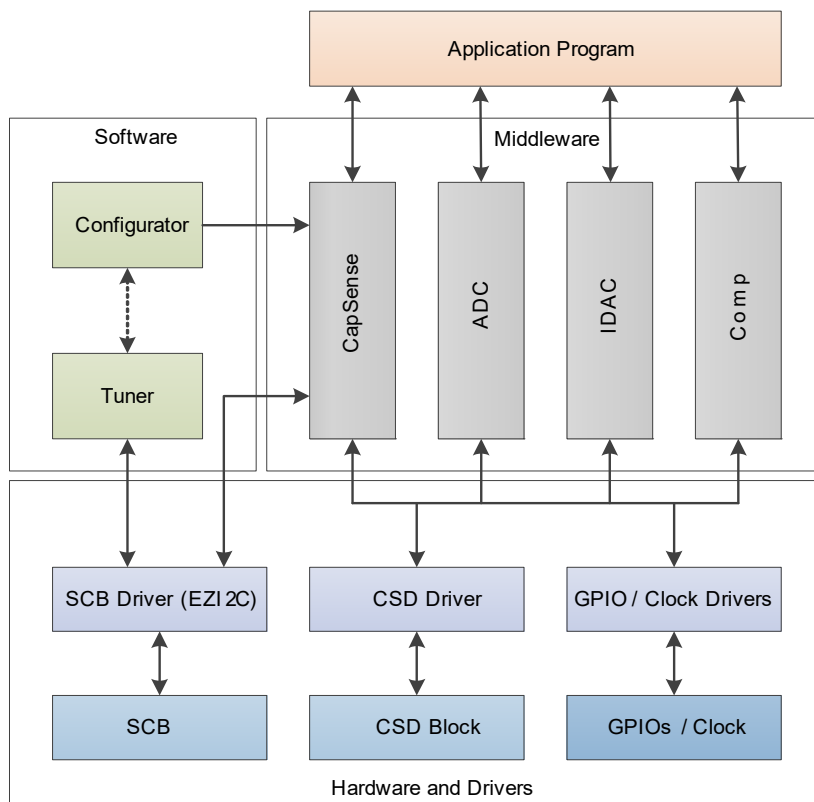
ModusToolbox Software provides a CapSense configurator to enable fast library configuration. It also provides a tuner for performance evaluation and real-time tuning of the system. The tuner requires an EZI2C communication interface in the application to enable real-time tuning capability. The tuner can update configuration parameters directly in the device as well as in the configurator.

CapSense and ADC middleware use the CSD interrupt to implement non-blocking sensing and A-to-D conversion. Therefore, interrupt service routines are a defined part of the middleware, which must be initialized by the application. Middleware and drivers can operate on either CPU. Cypress recommends using the middleware only in one CPU. If both CPUs must access the CSD driver, memory access should be managed in the application.

Refer to [AN85951: PSoC 4 and PSoC 6 MCU CapSense Design Guide](#) for more details on CSX sensing, CSD sensing, shield electrode usage and its benefits, and capacitive system design guidelines.

Refer to the API reference guides for [CapSense](#), [ADC](#), and [IDAC](#) available on GitHub.

Figure 8. CapSense Software/Firmware Subsystem



PSoC 64 Security

All PSoC 64 “Secure” MCU product lines feature enhanced security functionality. They provide an isolated root of trust (RoT) with true attestation and provisioning services. Cypress also provides a “Secure Boot” SDK User Guide, which includes all required libraries, tools, and sample code to provision PSoC 64 devices. The SDK also provides provisioning scripts with sample keys and policies, a pre-built bootloader image, and tools for signing firmware images. For more information, see the “[Secure Boot](#)” SDK User Guide.

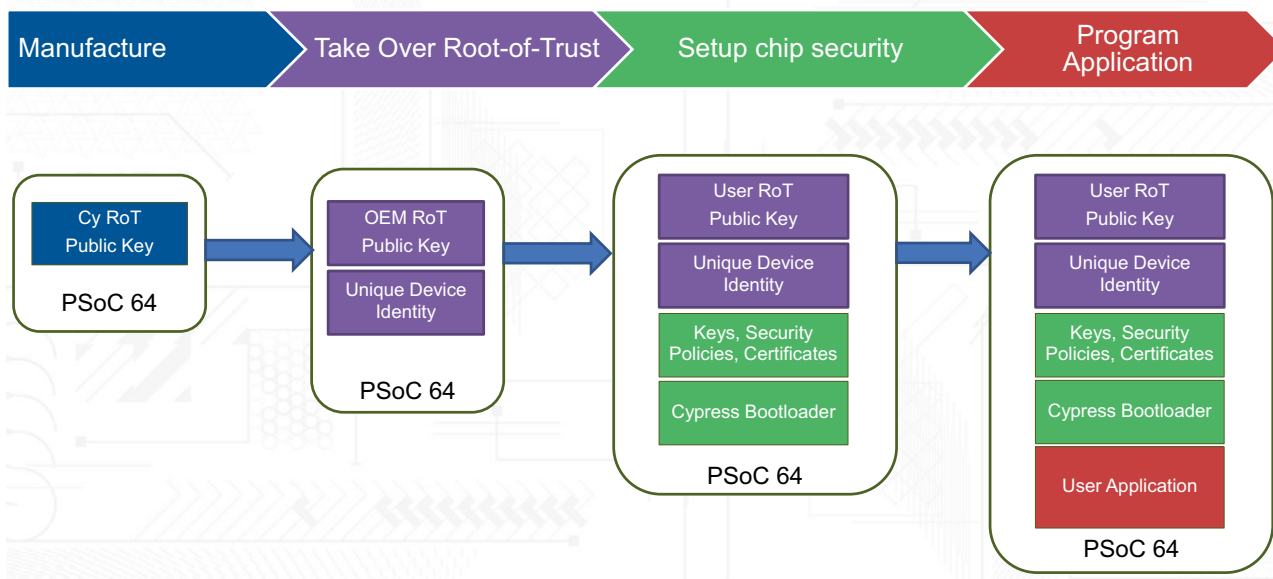
The “Secure Boot” SDK also includes entrance exam scripts. An entrance exam can optionally be run on PSoC 64 devices before provisioning to ensure that no device tampering has occurred.

The first step in using a PSoC 64 device is to inject the following information into the device - a process called provisioning:

- A set of cryptographic public keys, which are used to:
 - Transfer the RoT from Cypress to the user/OEM, as [Figure 9](#) shows
 - Validate applications
- A set of security policies that define how the device should behave
- Certificates (optional) used to bind device identity or provide a chain of trust to a higher certifying authority
- The Cypress Bootloader

Provisioning is done before an application is programmed into the device.

Figure 9. PSoC 64 Usage Processes

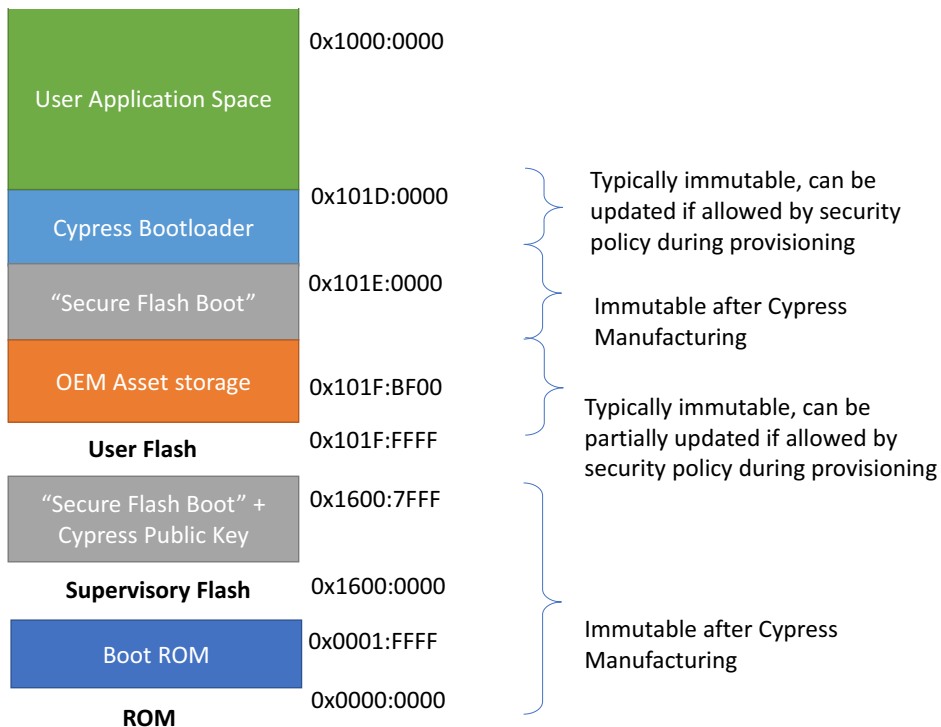


Provisioning is done using a hardware security module (HSM). An HSM is a physical computing device, placed in a secured facility, that safeguards and manages digital keys for strong authentication, and provides cryptographic processing.

After the device is provisioned, it can be programmed with signed applications. The signature and authenticity of the application is verified before control is transferred to it.

Figure 10 shows a simplified flash memory map of PSoC 64 assets and immutable sections. As noted in [Memory](#), a portion of device SRAM is also reserved for system usage.

Figure 10. PSoC 64 “Secure” MCU Asset Memory Map



Cypress Bootloader

The Cypress Bootloader is a part of the open source [MCUBoot](#) library. For more details about this library, refer to [MCUBoot Bootloader design](#). The current version of the Cypress Bootloader for this device does not support the swap-based images feature as documented in the MCUBoot design document.

The Cypress Bootloader is included in the “Secure Boot” SDK as a pre-built hex image. This image acts as the first image launched by the PSoC 64 boot code. It parses the provisioned Boot&Upgrade policy to launch an application image.

The Cypress Bootloader supports external memory over the PSoC 64 Serial Memory Interface (SMIF). The bootloader currently supports only external memory vendors who support the Serial Flash Discovery Protocol (SFDP).

The Cypress Bootloader enforces protection contexts for the bootloader code, so code running in another protection context may be prohibited from overwriting/tampering with the bootloader code. [Figure 11](#) shows the launch sequence of the Cypress Bootloader:

Figure 11. Bootloader Launch Sequence

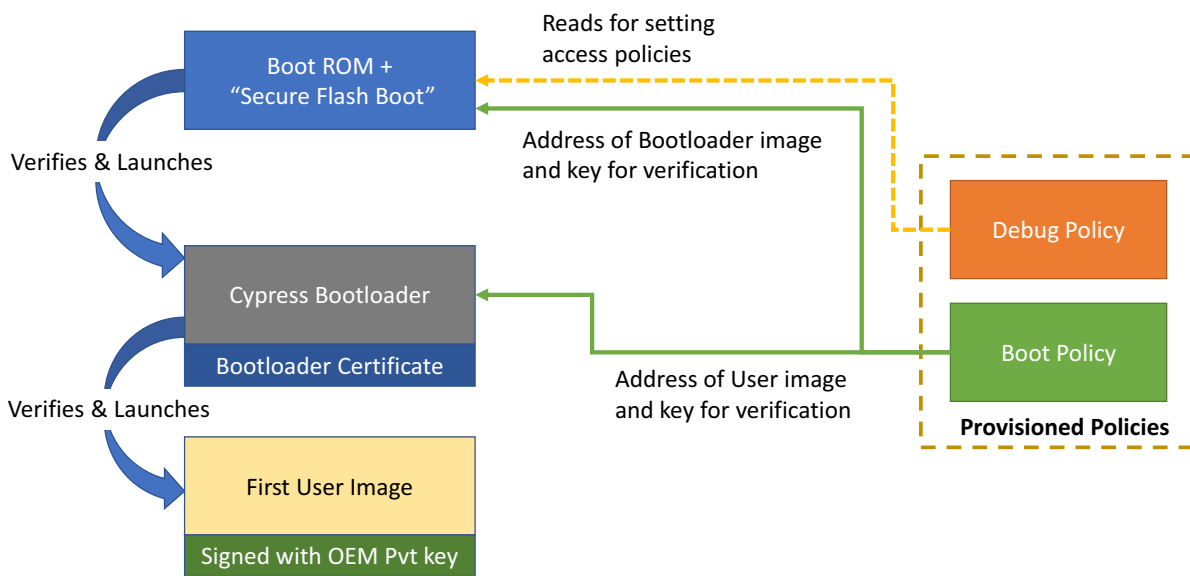
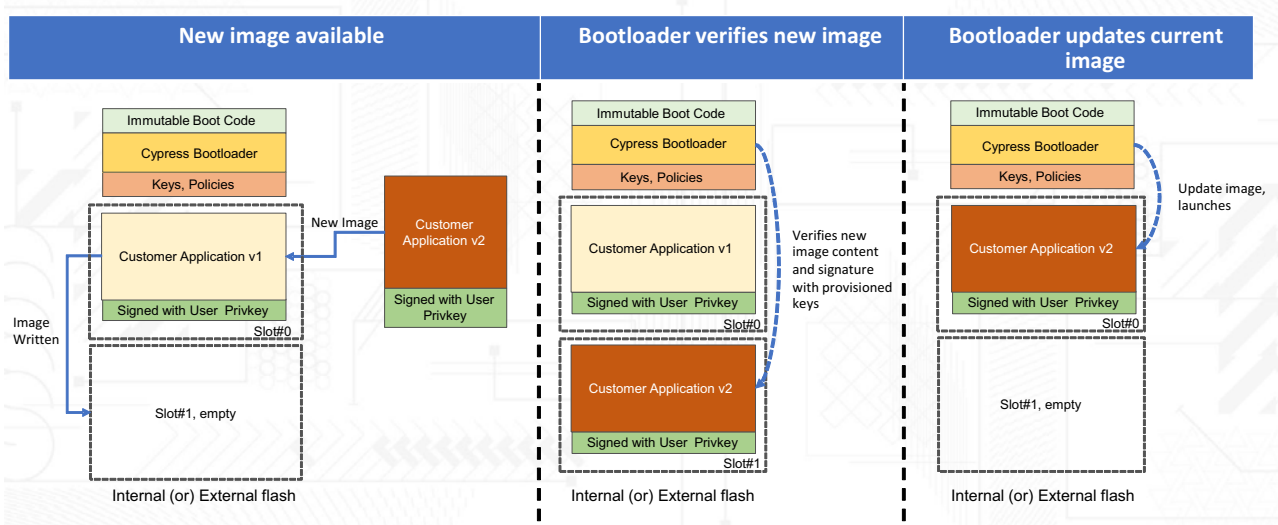


Figure 12 shows a typical application update scenario using the Cypress Bootloader:

Figure 12. Bootloader Application Update Sequence



Pinouts

Power supplies and ports correspond as follows:

- P0: V_{BACKUP}
- P1: V_{DDD} . Port 1 pins are overvoltage tolerant (OVT).
- P2, P3, P4: V_{DDIO2}
- P5, P6, P7, P8: V_{DDIO1}
- P9, P10: V_{DDIO} , V_{DDA} (V_{DDIOA} and V_{DDA} must be connected together on the PCB)
- P11, P12, P13: V_{DDIO0}
- P14: V_{DDUSB}

Table 7. Packages and Pin Information

| Pin | Packages | |
|---------------------|---------------------------|------------------|
| | 124-BGA | 100-WLCSP |
| V_{DDD} | A1 | D14 |
| V_{CCD} | A2 | C15 |
| V_{DDA} | A12 | J1 |
| V_{DDIOA} | A13 | - |
| V_{DDIO0} | C4 | A11 |
| V_{DDIO1} | K12 | K2 |
| V_{DDIO2} | L4 | M10 |
| V_{BACKUP} | D1 | C17 |
| V_{DDUSB} | M1 | J17 |
| V_{SS} | B12, C3, D4, D10, K4, K10 | D2, E13, J13, L1 |
| $V_{\text{DD_NS}}$ | J1 | J15 |
| V_{IND1} | J2 | H16 |
| XRES | F1 | E17 |
| V_{REF} | B13 | C3 |
| P0.0 | E3 | F14 |
| P0.1 | E2 | G13 |
| P0.2 | E1 | D16 |
| P0.3 | F3 | E15 |
| P0.4 | F2 | G11 |
| P0.5 | G3 | F16 |
| P1.0 | G2 | H12 |
| P1.1 | G1 | G15 |
| P1.2 | H3 | - |
| P1.3 | H2 | - |
| P1.4 | H1 | H14 |
| P1.5 | J3 | G17 |
| P2.0 | M2 | L17 |
| P2.1 | N2 | K12 |
| P2.2 | L3 | L15 |

Table 7. Packages and Pin Information *(continued)*

| Pin | Packages | |
|------|----------|-----------|
| | 124-BGA | 100-WLCSP |
| P2.3 | M3 | L13 |
| P2.4 | N3 | L11 |
| P2.5 | N1 | M16 |
| P2.6 | M4 | M14 |
| P2.7 | N4 | M12 |
| P3.0 | L5 | - |
| P3.1 | M5 | - |
| P3.2 | N5 | - |
| P3.3 | L6 | - |
| P3.4 | M6 | - |
| P3.5 | N6 | - |
| P4.0 | L7 | - |
| P4.1 | M7 | - |
| P5.0 | N7 | M8 |
| P5.1 | L8 | K10 |
| P5.2 | M8 | J11 |
| P5.3 | N8 | H10 |
| P5.4 | L9 | L9 |
| P5.5 | M9 | M6 |
| P5.6 | N9 | G9 |
| P5.7 | N10 | G7 |
| P6.0 | M10 | M4 |
| P6.1 | L10 | L7 |
| P6.2 | L11 | L5 |
| P6.3 | M11 | K8 |
| P6.4 | N11 | J9 |
| P6.5 | M12 | L3 |
| P6.6 | N12 | M2 |
| P6.7 | M13 | K4 |
| P7.0 | L13 | K6 |
| P7.1 | L12 | J7 |
| P7.2 | K13 | J3 |
| P7.3 | N13 | H8 |
| P7.4 | K11 | - |
| P7.5 | J13 | - |
| P7.6 | J12 | - |
| P7.7 | J11 | G1 |
| P8.0 | H13 | H2 |
| P8.1 | H12 | J5 |
| P8.2 | H11 | H6 |
| P8.3 | G13 | H4 |
| P8.4 | G12 | F2 |

Table 7. Packages and Pin Information *(continued)*

| Pin | Packages | |
|-------|----------|-----------|
| | 124-BGA | 100-WLCSP |
| P8.5 | G11 | - |
| P8.6 | F13 | - |
| P8.7 | F12 | - |
| P9.0 | E11 | E1 |
| P9.1 | E12 | G3 |
| P9.2 | E13 | G5 |
| P9.3 | F11 | F4 |
| P9.4 | D13 | E3 |
| P9.5 | D12 | - |
| P9.6 | D11 | - |
| P9.7 | C13 | C1 |
| P10.0 | C12 | F6 |
| P10.1 | A11 | E5 |
| P10.2 | B11 | B2 |
| P10.3 | C11 | D4 |
| P10.4 | A10 | C5 |
| P10.5 | B10 | B4 |
| P10.6 | C10 | A3 |
| P10.7 | A9 | F8 |
| P11.0 | B9 | E9 |
| P11.1 | C9 | D6 |
| P11.2 | A8 | E7 |
| P11.3 | B8 | A7 |
| P11.4 | C8 | B6 |
| P11.5 | A7 | A5 |
| P11.6 | B7 | C7 |
| P11.7 | C7 | B8 |
| P12.0 | A6 | A9 |
| P12.1 | B6 | D8 |
| P12.2 | C6 | A13 |
| P12.3 | A5 | B10 |
| P12.4 | B5 | C9 |
| P12.5 | C5 | B12 |
| P12.6 | A4 | C11 |
| P12.7 | B4 | D10 |
| P13.0 | B1 | B14 |
| P13.1 | A3 | A15 |
| P13.2 | B3 | C13 |
| P13.3 | B2 | D12 |
| P13.4 | C2 | E11 |

Table 7. Packages and Pin Information *(continued)*

| Pin | Packages | |
|--------------|----------|-----------|
| | 124-BGA | 100-WLCSP |
| P13.5 | C1 | F10 |
| P13.6 | D3 | F12 |
| P13.7 | D2 | B16 |
| P14.0/ USBDP | L2 | K14 |
| P14.1/ USBDM | L1 | K16 |

Note: If the USB pins are not used, connect V_{DDUSB} to ground and leave the P14.0/USBDP and P14.1/USBDM pins unconnected.

Note

3. DNC means Do Not Connect. Do Not Connect anything to these pins.

Each port pin has multiple alternate functions. These are defined in Table 8. The columns ACT #x and DS #y denote active (System LP/ULP) and Deep Sleep mode signals respectively.

The notation for a signal is of the form IPName[x].signal_name[u]:y.

IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there is more than one signal for a particular signal name, y = Designates copies of the signal name.

For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximize use of on-chip resources.

Table 8. Multiple Alternate Functions

| Port/ Pin | ACT #0 | ACT #1 | ACT #2 | ACT #3 | DS #2 | DS #3 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #5 | DS #6 |
|--------------|--------------------------|---------------------------|--------------|----------------|-------|-------|----------------|--------|-------------------|------------------|----------------------|--------|---------|-----------------------|------------------------|---------|---------|-------|-------|
| P0.0 | tcpwm[0].line[0]:0 | tcpwm[1].line[0]:0 | csd.csd_tx:0 | csd.csd_tx_n:0 | | | srss.ext_clk:0 | | | | scb[0].spi_select1:0 | | | peri.tr_io_input[0]:0 | | | | | |
| P0.1 | tcpwm[0].line_compl[0]:0 | tcpwm[1].line_compl[0]:0 | csd.csd_tx:1 | csd.csd_tx_n:1 | | | | | | | scb[0].spi_select2:0 | | | peri.tr_io_input[1]:0 | | | | | |
| P0.2 | tcpwm[0].line[1]:0 | tcpwm[1].line[1]:0 | csd.csd_tx:2 | csd.csd_tx_n:2 | | | | | scb[0].uart_rx:0 | scb[0].i2c_scl:0 | scb[0].spi_mosi:0 | | | | | | | | |
| P0.3 | tcpwm[0].line_compl[1]:0 | tcpwm[1].line_compl[1]:0 | csd.csd_tx:3 | csd.csd_tx_n:3 | | | | | scb[0].uart_tx:0 | scb[0].i2c_sda:0 | scb[0].spi_miso:0 | | | | | | | | |
| P0.4 | tcpwm[0].line[2]:0 | tcpwm[1].line[2]:0 | csd.csd_tx:4 | csd.csd_tx_n:4 | | | | | scb[0].uart_rts:0 | | scb[0].spi_clk:0 | | | | peri.tr_io_output[0]:2 | | | | |
| P0.5 | tcpwm[0].line_compl[2]:0 | tcpwm[1].line_compl[2]:0 | csd.csd_tx:5 | csd.csd_tx_n:5 | | | srss.ext_clk:1 | | scb[0].uart_cts:0 | | scb[0].spi_select0:0 | | | | peri.tr_io_output[1]:2 | | | | |
| P1.0 | tcpwm[0].line[3]:0 | tcpwm[1].line[3]:0 | csd.csd_tx:6 | csd.csd_tx_n:6 | | | | | scb[7].uart_rx:0 | scb[7].i2c_scl:0 | scb[7].spi_mosi:0 | | | peri.tr_io_input[2]:0 | | | | | |
| P1.1 | tcpwm[0].line_compl[3]:0 | tcpwm[1].line_compl[3]:0 | csd.csd_tx:7 | csd.csd_tx_n:7 | | | | | scb[7].uart_tx:0 | scb[7].i2c_sda:0 | scb[7].spi_miso:0 | | | peri.tr_io_input[3]:0 | | | | | |
| P1.2 | tcpwm[0].line[4]:4 | tcpwm[1].line[12]:1 | csd.csd_tx:8 | csd.csd_tx_n:8 | | | | | scb[7].uart_rts:0 | | scb[7].spi_clk:0 | | | | | | | | |
| P1.3 | tcpwm[0].line_compl[4]:4 | tcpwm[1].line_compl[12]:1 | csd.csd_tx:9 | csd.csd_tx_n:9 | | | | | scb[7].uart_cts:0 | | scb[7].spi_select0:0 | | | | | | | | |

Table 8. Multiple Alternate Functions (continued)

| Port/ Pin | ACT #0 | ACT #1 | ACT #2 | ACT #3 | DS #2 | DS #3 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #5 | DS #6 |
|--------------|--------------------------|---------------------------|---------------|-----------------|-------|-------|--------|--------|-------------------|------------------|----------------------|--------|---------|------------------------|---------|------------------------------|---------|-------|-------|
| P1.4 | tcpwm[0].line[5]:4 | tcpwm[1].line[13]:1 | csd.csd_tx:10 | csd.csd_tx_n:10 | | | | | | | scb[7].spi_select1:0 | | | | | | | | |
| P1.5 | tcpwm[0].line_compl[5]:4 | tcpwm[1].line_compl[14]:1 | csd.csd_tx:11 | csd.csd_tx_n:11 | | | | | | | scb[7].spi_select2:0 | | | | | | | | |
| P2.0 | tcpwm[0].line[6]:4 | tcpwm[1].line[15]:1 | csd.csd_tx:12 | csd.csd_tx_n:12 | | | | | scb[1].uart_rx:0 | scb[1].i2c_scl:0 | scb[1].spi_mosi:0 | | | peri.tr_io_in_put[4]:0 | | sdhc[0].card_data_3to0[0] | | | |
| P2.1 | tcpwm[0].line_compl[6]:4 | tcpwm[1].line_compl[15]:1 | csd.csd_tx:13 | csd.csd_tx_n:13 | | | | | scb[1].uart_tx:0 | scb[1].i2c_sda:0 | scb[1].spi_miso:0 | | | peri.tr_io_in_put[5]:0 | | sdhc[0].card_data_3to0[1] | | | |
| P2.2 | tcpwm[0].line[7]:4 | tcpwm[1].line[16]:1 | csd.csd_tx:14 | csd.csd_tx_n:14 | | | | | scb[1].uart_rts:0 | | scb[1].spi_clk:0 | | | | | sdhc[0].card_data_3to0[2] | | | |
| P2.3 | tcpwm[0].line_compl[7]:4 | tcpwm[1].line_compl[16]:1 | csd.csd_tx:15 | csd.csd_tx_n:15 | | | | | scb[1].uart_cts:0 | | scb[1].spi_select0:0 | | | | | sdhc[0].card_data_3to0[3] | | | |
| P2.4 | tcpwm[0].line[0]:5 | tcpwm[1].line[17]:1 | csd.csd_tx:16 | csd.csd_tx_n:16 | | | | | scb[9].uart_rx:0 | scb[9].i2c_scl:0 | scb[1].spi_select1:0 | | | | | sdhc[0].card_cmd | | | |
| P2.5 | tcpwm[0].line_compl[0]:5 | tcpwm[1].line_compl[17]:1 | csd.csd_tx:17 | csd.csd_tx_n:17 | | | | | scb[9].uart_tx:0 | scb[9].i2c_sda:0 | scb[1].spi_select2:0 | | | | | sdhc[0].clk_card | | | |
| P2.6 | tcpwm[0].line[1]:5 | tcpwm[1].line[18]:1 | csd.csd_tx:18 | csd.csd_tx_n:18 | | | | | scb[9].uart_rts:0 | | scb[1].spi_select3:0 | | | | | sdhc[0].card_detect_n | | | |
| P2.7 | tcpwm[0].line_compl[1]:5 | tcpwm[1].line_compl[18]:1 | csd.csd_tx:19 | csd.csd_tx_n:19 | | | | | scb[9].uart_cts:0 | | | | | | | sdhc[0].card_mech_write_prot | | | |
| P3.0 | tcpwm[0].line[2]:5 | tcpwm[1].line[19]:1 | csd.csd_tx:20 | csd.csd_tx_n:20 | | | | | scb[2].uart_rx:1 | scb[2].i2c_scl:1 | scb[2].spi_mosi:1 | | | peri.tr_io_in_put[6]:0 | | sdhc[0].io_volt_sel | | | |
| P3.1 | tcpwm[0].line_compl[2]:5 | tcpwm[1].line_compl[19]:1 | csd.csd_tx:21 | csd.csd_tx_n:21 | | | | | scb[2].uart_tx:1 | scb[2].i2c_sda:1 | scb[2].spi_miso:1 | | | peri.tr_io_in_put[7]:0 | | sdhc[0].card_if_pwr_en | | | |

Table 8. Multiple Alternate Functions (continued)

| Port/ Pin | ACT #0 | ACT #1 | ACT #2 | ACT #3 | DS #2 | DS #3 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #5 | DS #6 |
|--------------|--------------------------|---------------------------|---------------|-----------------|-------|-------|--------|--------|-------------------|-------------------|----------------------|--------|------------------------|---------|---------|---------|---------|-------|-------------------------|
| P3.2 | tcpwm[0].line[3]:5 | tcpwm[1].line[20]:1 | csd.csd_tx:22 | csd.csd_tx_n:22 | | | | | scb[2].uart_rts:1 | | scb[2].spi_clk:1 | | | | | | | | |
| P3.3 | tcpwm[0].line_compl[3]:5 | tcpwm[1].line_compl[20]:1 | csd.csd_tx:23 | csd.csd_tx_n:23 | | | | | scb[2].uart_cts:1 | | scb[2].spi_select0:1 | | | | | | | | |
| P3.4 | tcpwm[0].line[4]:5 | tcpwm[1].line[21]:1 | csd.csd_tx:24 | csd.csd_tx_n:24 | | | | | | | scb[2].spi_select1:1 | | | | | | | | |
| P3.5 | tcpwm[0].line_compl[4]:5 | tcpwm[1].line_compl[21]:1 | csd.csd_tx:25 | csd.csd_tx_n:25 | | | | | | | scb[2].spi_select2:1 | | | | | | | | |
| P4.0 | tcpwm[0].line[5]:5 | tcpwm[1].line[22]:1 | csd.csd_tx:26 | csd.csd_tx_n:26 | | | | | scb[7].uart_rx:1 | scb[7].i2c_scl:1 | scb[7].spi_mosi:1 | | | | | | | | peri.tr_io_in_put[8]:0 |
| P4.1 | tcpwm[0].line_compl[5]:5 | tcpwm[1].line_compl[22]:1 | csd.csd_tx:27 | csd.csd_tx_n:27 | | | | | scb[7].uart_tx:1 | scb[7].i2c_sda:1 | scb[7].spi_miso:1 | | | | | | | | peri.tr_io_in_put[9]:0 |
| P4.2 | tcpwm[0].line[6]:5 | tcpwm[1].line[23]:1 | csd.csd_tx:28 | csd.csd_tx_n:28 | | | | | scb[7].uart_rts:1 | | scb[7].spi_clk:1 | | | | | | | | |
| P4.3 | tcpwm[0].line_compl[6]:5 | tcpwm[1].line_compl[23]:1 | csd.csd_tx:29 | csd.csd_tx_n:29 | | | | | scb[7].uart_cts:1 | | scb[7].spi_select0:1 | | | | | | | | |
| P5.0 | tcpwm[0].line[4]:0 | tcpwm[1].line[4]:0 | csd.csd_tx:30 | csd.csd_tx_n:30 | | | | | scb[5].uart_rx:0 | scb[5].i2c_scl:0 | scb[5].spi_mosi:0 | | audioss[0].clk_2s_if:0 | | | | | | peri.tr_io_in_put[10]:0 |
| P5.1 | tcpwm[0].line_compl[4]:0 | tcpwm[1].line_compl[4]:0 | csd.csd_tx:31 | csd.csd_tx_n:31 | | | | | scb[5].uart_tx:0 | scb[5].i2c_sda:0 | scb[5].spi_miso:0 | | audioss[0].tx_sck:0 | | | | | | peri.tr_io_in_put[11]:0 |
| P5.2 | tcpwm[0].line[5]:0 | tcpwm[1].line[5]:0 | csd.csd_tx:32 | csd.csd_tx_n:32 | | | | | scb[5].uart_rts:0 | | scb[5].spi_clk:0 | | audioss[0].tx_ws:0 | | | | | | |
| P5.3 | tcpwm[0].line_compl[5]:0 | tcpwm[1].line_compl[5]:0 | csd.csd_tx:33 | csd.csd_tx_n:33 | | | | | scb[5].uart_cts:0 | | scb[5].spi_select0:0 | | audioss[0].tx_sdo:0 | | | | | | |
| P5.4 | tcpwm[0].line[6]:0 | tcpwm[1].line[6]:0 | csd.csd_tx:34 | csd.csd_tx_n:34 | | | | | scb[10].uart_rx:0 | scb[10].i2c_scl:0 | scb[5].spi_select1:0 | | audioss[0].rx_sck:0 | | | | | | |

Table 8. Multiple Alternate Functions (continued)

| Port/ Pin | ACT #0 | ACT #1 | ACT #2 | ACT #3 | DS #2 | DS #3 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #5 | DS #6 |
|--------------|--------------------------|---------------------------|---------------|-----------------|------------------|-------|--------|--------|--------------------|-------------------|-----------------------|--------|---------------------|------------------------|------------------------|---------|---------|---------------------|-----------------------|
| P5.5 | tcpwm[0].line_compl[6]:0 | tcpwm[1].line_compl[6]:0 | csd.csd_tx:35 | csd.csd_tx_n:35 | | | | | scb[10].uart_tx:0 | scb[10].i2c_sda:0 | scb[5].spi_select:2:0 | | audioss[0].rx_ws:0 | | | | | | |
| P5.6 | tcpwm[0].line[7]:0 | tcpwm[1].line[7]:0 | csd.csd_tx:36 | csd.csd_tx_n:36 | | | | | scb[10].uart_rts:0 | | scb[5].spi_select:3:0 | | audioss[0].rx_sdi:0 | | | | | | |
| P5.7 | tcpwm[0].line_compl[7]:0 | tcpwm[1].line_compl[7]:0 | csd.csd_tx:37 | csd.csd_tx_n:37 | | | | | scb[10].uart_cts:0 | | scb[3].spi_select:3:0 | | | | | | | | |
| P6.0 | tcpwm[0].line[0]:1 | tcpwm[1].line[8]:0 | csd.csd_tx:38 | csd.csd_tx_n:38 | scb[8].i2c_scl:0 | | | | scb[3].uart_rx:0 | scb[3].i2c_scl:0 | scb[3].spi_mosi:0 | | | | cpuss.fault_out[0] | | | | scb[8].spi_mosi:0 |
| P6.1 | tcpwm[0].line_compl[0]:1 | tcpwm[1].line_compl[8]:0 | csd.csd_tx:39 | csd.csd_tx_n:39 | scb[8].i2c_sda:0 | | | | scb[3].uart_tx:0 | scb[3].i2c_sda:0 | scb[3].spi_miso:0 | | | | cpuss.fault_out[1] | | | | scb[8].spi_miso:0 |
| P6.2 | tcpwm[0].line[1]:1 | tcpwm[1].line[9]:0 | csd.csd_tx:40 | csd.csd_tx_n:40 | | | | | scb[3].uart_rts:0 | | scb[3].spi_clk:0 | | | | | | | | scb[8].spi_clk:0 |
| P6.3 | tcpwm[0].line_compl[1]:1 | tcpwm[1].line_compl[9]:0 | csd.csd_tx:41 | csd.csd_tx_n:41 | | | | | scb[3].uart_cts:0 | | scb[3].spi_select:0:0 | | | | | | | | scb[8].spi_select:0:0 |
| P6.4 | tcpwm[0].line[2]:1 | tcpwm[1].line[10]:0 | csd.csd_tx:42 | csd.csd_tx_n:42 | scb[8].i2c_scl:1 | | | | scb[6].uart_rx:2 | scb[6].i2c_scl:2 | scb[6].spi_mosi:2 | | | peri.tr_io_input[12]:0 | peri.tr_io_output[0]:1 | | | cpuss.swj_swo | scb[8].spi_mosi:1 |
| P6.5 | tcpwm[0].line_compl[2]:1 | tcpwm[1].line_compl[10]:0 | csd.csd_tx:43 | csd.csd_tx_n:43 | scb[8].i2c_sda:1 | | | | scb[6].uart_tx:2 | scb[6].i2c_sda:2 | scb[6].spi_miso:2 | | | peri.tr_io_input[13]:0 | peri.tr_io_output[1]:1 | | | cpuss.swj_swdoe_tdi | scb[8].spi_miso:1 |
| P6.6 | tcpwm[0].line[3]:1 | tcpwm[1].line[11]:0 | csd.csd_tx:44 | csd.csd_tx_n:44 | | | | | scb[6].uart_rts:2 | | scb[6].spi_clk:2 | | | | | | | cpuss.swj_swdio_tms | scb[8].spi_clk:1 |
| P6.7 | tcpwm[0].line_compl[3]:1 | tcpwm[1].line_compl[11]:0 | csd.csd_tx:45 | csd.csd_tx_n:45 | | | | | scb[6].uart_cts:2 | | scb[6].spi_select:0:2 | | | | | | | cpuss.swj_swclk_clk | scb[8].spi_select:0:1 |

Table 8. Multiple Alternate Functions (continued)

| Port/ Pin | ACT #0 | ACT #1 | ACT #2 | ACT #3 | DS #2 | DS #3 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #5 | DS #6 |
|--------------|-------------------------|--------------------------|---------------|-----------------|-------|--------------------|--------|--------|-------------------|------------------|----------------------|-------------------|---------|-------------------------|---------|-------------------|-----------------------|-------|-------|
| P7.0 | tcpwm[0].line[4]:1 | tcpwm[1].line[12]:0 | csd.csd_tx:46 | csd.csd_tx_n:46 | | | | | scb[4].uart_rx:1 | scb[4].i2c_scl:1 | scb[4].spi_mosi:1 | | | peri.tr_io_in_put[14]:0 | | cpuss.trace_clock | | | |
| P7.1 | tcpwm[0].line_comp[4]:1 | tcpwm[1].line_comp[12]:0 | csd.csd_tx:47 | csd.csd_tx_n:47 | | | | | scb[4].uart_tx:1 | scb[4].i2c_sda:1 | scb[4].spi_miso:1 | | | peri.tr_io_in_put[15]:0 | | | | | |
| P7.2 | tcpwm[0].line[5]:1 | tcpwm[1].line[13]:0 | csd.csd_tx:48 | csd.csd_tx_n:48 | | | | | scb[4].uart_rts:1 | | scb[4].spi_clk:1 | | | | | | | | |
| P7.3 | tcpwm[0].line_comp[5]:1 | tcpwm[1].line_comp[13]:0 | csd.csd_tx:49 | csd.csd_tx_n:49 | | | | | scb[4].uart_cts:1 | | scb[4].spi_select0:1 | | | | | | | | |
| P7.4 | tcpwm[0].line[6]:1 | tcpwm[1].line[14]:0 | csd.csd_tx:50 | csd.csd_tx_n:50 | | | | | | | scb[4].spi_select1:1 | | | | | | cpuss.trace_data[3]:2 | | |
| P7.5 | tcpwm[0].line_comp[6]:1 | tcpwm[1].line_comp[14]:0 | csd.csd_tx:51 | csd.csd_tx_n:51 | | | | | | | scb[4].spi_select2:1 | | | | | | cpuss.trace_data[2]:2 | | |
| P7.6 | tcpwm[0].line[7]:1 | tcpwm[1].line[15]:0 | csd.csd_tx:52 | csd.csd_tx_n:52 | | | | | | | scb[4].spi_select3:1 | | | | | | cpuss.trace_data[1]:2 | | |
| P7.7 | tcpwm[0].line_comp[7]:1 | tcpwm[1].line_comp[15]:0 | csd.csd_tx:53 | csd.csd_tx_n:53 | | | | | | | scb[3].spi_select1:0 | cpuss.clk_fm_pump | | | | | cpuss.trace_data[0]:2 | | |
| P8.0 | tcpwm[0].line[0]:2 | tcpwm[1].line[16]:0 | csd.csd_tx:54 | csd.csd_tx_n:54 | | | | | scb[4].uart_rx:0 | scb[4].i2c_scl:0 | scb[4].spi_mosi:0 | | | peri.tr_io_in_put[16]:0 | | | | | |
| P8.1 | tcpwm[0].line_comp[0]:2 | tcpwm[1].line_comp[16]:0 | csd.csd_tx:55 | csd.csd_tx_n:55 | | | | | scb[4].uart_tx:0 | scb[4].i2c_sda:0 | scb[4].spi_miso:0 | | | peri.tr_io_in_put[17]:0 | | | | | |
| P8.2 | tcpwm[0].line[1]:2 | tcpwm[1].line[17]:0 | csd.csd_tx:56 | csd.csd_tx_n:56 | | lpcomp.dsi_comp0:0 | | | scb[4].uart_rts:0 | | scb[4].spi_clk:0 | | | | | | | | |
| P8.3 | tcpwm[0].line_comp[1]:2 | tcpwm[1].line_comp[17]:0 | csd.csd_tx:57 | csd.csd_tx_n:57 | | lpcomp.dsi_comp1:0 | | | scb[4].uart_cts:0 | | scb[4].spi_select0:0 | | | | | | | | |

Table 8. Multiple Alternate Functions (continued)

| Port/ Pin | ACT #0 | ACT #1 | ACT #2 | ACT #3 | DS #2 | DS #3 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #5 | DS #6 |
|--------------|--------------------------|---------------------------|---------------|-----------------|-------|-------|--------|--------|-------------------|-------------------|----------------------|--------|-----------------------|------------------------|---------|---------|-----------------------|-------|-------|
| P8.4 | tcpwm[0].line[2]:2 | tcpwm[1].line[18]:0 | csd.csd_tx:58 | csd.csd_tx_n:58 | | | | | scb[1].uart_rx:0 | scb[11].i2c_scl:0 | scb[4].spi_select1:0 | | | | | | | | |
| P8.5 | tcpwm[0].line_compl[2]:2 | tcpwm[1].line_compl[18]:0 | csd.csd_tx:59 | csd.csd_tx_n:59 | | | | | scb[1].uart_tx:0 | scb[11].i2c_sda:0 | scb[4].spi_select2:0 | | | | | | | | |
| P8.6 | tcpwm[0].line[3]:2 | tcpwm[1].line[19]:0 | csd.csd_tx:60 | csd.csd_tx_n:60 | | | | | scb[1].uart_rts:0 | | scb[4].spi_select3:0 | | | | | | | | |
| P8.7 | tcpwm[0].line_compl[3]:2 | tcpwm[1].line_compl[19]:0 | csd.csd_tx:61 | csd.csd_tx_n:61 | | | | | scb[1].uart_cts:0 | | scb[3].spi_select2:0 | | | | | | | | |
| P9.0 | tcpwm[0].line[4]:2 | tcpwm[1].line[20]:0 | csd.csd_tx:62 | csd.csd_tx_n:62 | | | | | scb[2].uart_rx:0 | scb[2].i2c_scl:0 | scb[2].spi_mosi:0 | | audio[0].clk_i2s_if:1 | peri.tr_io_input[18]:0 | | | cpuss.trace_data[3]:0 | | |
| P9.1 | tcpwm[0].line_compl[4]:2 | tcpwm[1].line_compl[20]:0 | csd.csd_tx:63 | csd.csd_tx_n:63 | | | | | scb[2].uart_tx:0 | scb[2].i2c_sda:0 | scb[2].spi_miso:0 | | audio[0].tx_sck:1 | peri.tr_io_input[19]:0 | | | cpuss.trace_data[2]:0 | | |
| P9.2 | tcpwm[0].line[5]:2 | tcpwm[1].line[21]:0 | csd.csd_tx:64 | csd.csd_tx_n:64 | | | | | scb[2].uart_rts:0 | | scb[2].spi_clk:0 | | audio[0].tx_ws:1 | | | | cpuss.trace_data[1]:0 | | |
| P9.3 | tcpwm[0].line_compl[5]:2 | tcpwm[1].line_compl[21]:0 | csd.csd_tx:65 | csd.csd_tx_n:65 | | | | | scb[2].uart_cts:0 | | scb[2].spi_select0:0 | | audio[0].tx_sdo:1 | | | | cpuss.trace_data[0]:0 | | |
| P9.4 | tcpwm[0].line[7]:5 | tcpwm[1].line[0]:2 | csd.csd_tx:66 | csd.csd_tx_n:66 | | | | | | | scb[2].spi_select1:0 | | audio[0].rx_sck:1 | | | | | | |
| P9.5 | tcpwm[0].line_compl[7]:5 | tcpwm[1].line_compl[0]:2 | csd.csd_tx:67 | csd.csd_tx_n:67 | | | | | | | scb[2].spi_select2:0 | | audio[0].rx_ws:1 | | | | | | |
| P9.6 | tcpwm[0].line[0]:6 | tcpwm[1].line[1]:2 | csd.csd_tx:68 | csd.csd_tx_n:68 | | | | | | | scb[2].spi_select3:0 | | audio[0].rx_sdi:1 | | | | | | |
| P9.7 | tcpwm[0].line_compl[0]:6 | tcpwm[1].line_compl[1]:2 | csd.csd_tx:69 | csd.csd_tx_n:69 | | | | | | | | | | | | | | | |
| P10.0 | tcpwm[0].line[6]:2 | tcpwm[1].line[22]:0 | csd.csd_tx:70 | csd.csd_tx_n:70 | | | | | scb[1].uart_rx:1 | scb[1].i2c_scl:1 | scb[1].spi_mosi:1 | | | peri.tr_io_input[20]:0 | | | cpuss.trace_data[3]:1 | | |

Table 8. Multiple Alternate Functions (continued)

| Port/ Pin | ACT #0 | ACT #1 | ACT #2 | ACT #3 | DS #2 | DS #3 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #5 | DS #6 |
|--------------|--------------------------|---------------------------|---------------|-----------------|-------|-------|--------|------------------|-------------------|------------------|----------------------|----------------------|-----------------------|-------------------------|------------------------|---------|-----------------------|-------|-------|
| P10.1 | tcpwm[0].line_compl[6]:2 | tcpwm[1].line_compl[22]:0 | csd.csd_tx:71 | csd.csd_tx_n:71 | | | | | scb[1].uart_tx:1 | scb[1].i2c_sda:1 | scb[1].spi_miso:1 | | | peri.tr_io_in_put[21]:0 | | | cpuss.trace_data[2]:1 | | |
| P10.2 | tcpwm[0].line[7]:2 | tcpwm[1].line[23]:0 | csd.csd_tx:72 | csd.csd_tx_n:72 | | | | | scb[1].uart_rts:1 | | scb[1].spi_clk:1 | | | | | | cpuss.trace_data[1]:1 | | |
| P10.3 | tcpwm[0].line_compl[7]:2 | tcpwm[1].line_compl[23]:0 | csd.csd_tx:73 | csd.csd_tx_n:73 | | | | | scb[1].uart_cts:1 | | scb[1].spi_select0:1 | | | | | | cpuss.trace_data[0]:1 | | |
| P10.4 | tcpwm[0].line[0]:3 | tcpwm[1].line[0]:1 | csd.csd_tx:74 | csd.csd_tx_n:74 | | | | | | | scb[1].spi_select1:1 | audios[0].pdm_clk:0 | | | | | | | |
| P10.5 | tcpwm[0].line_compl[0]:3 | tcpwm[1].line_compl[0]:1 | csd.csd_tx:75 | csd.csd_tx_n:75 | | | | | | | scb[1].spi_select2:1 | audios[0].pdm_data:0 | | | | | | | |
| P10.6 | tcpwm[0].line[1]:6 | tcpwm[1].line[2]:2 | csd.csd_tx:76 | csd.csd_tx_n:76 | | | | | | | scb[1].spi_select3:1 | | | | | | | | |
| P10.7 | tcpwm[0].line_compl[1]:6 | tcpwm[1].line_compl[2]:2 | csd.csd_tx:77 | csd.csd_tx_n:77 | | | | | | | | | | | | | | | |
| P11.0 | tcpwm[0].line[1]:3 | tcpwm[1].line[1]:1 | csd.csd_tx:78 | csd.csd_tx_n:78 | | | | smif.spi_select2 | scb[5].uart_rx:1 | scb[5].i2c_scl:1 | scb[5].spi_mosi:1 | | audio[1].clk_i2s_if:1 | peri.tr_io_in_put[22]:0 | | | | | |
| P11.1 | tcpwm[0].line_compl[1]:3 | tcpwm[1].line_compl[1]:1 | csd.csd_tx:79 | csd.csd_tx_n:79 | | | | smif.spi_select1 | scb[5].uart_tx:1 | scb[5].i2c_sda:1 | scb[5].spi_miso:1 | | audio[1].tx_sck:1 | peri.tr_io_in_put[23]:0 | | | | | |
| P11.2 | tcpwm[0].line[2]:3 | tcpwm[1].line[2]:1 | csd.csd_tx:80 | csd.csd_tx_n:80 | | | | smif.spi_select0 | scb[5].uart_rts:1 | | scb[5].spi_clk:1 | | audio[1].tx_ws:1 | | | | | | |
| P11.3 | tcpwm[0].line_compl[2]:3 | tcpwm[1].line_compl[2]:1 | csd.csd_tx:81 | csd.csd_tx_n:81 | | | | smif.spi_data3 | scb[5].uart_cts:1 | | scb[5].spi_select0:1 | | audio[1].tx_sdo:1 | | peri.tr_io_output[0]:0 | | | | |
| P11.4 | tcpwm[0].line[3]:3 | tcpwm[1].line[3]:1 | csd.csd_tx:82 | csd.csd_tx_n:82 | | | | smif.spi_data2 | | | scb[5].spi_select1:1 | | audio[1].rx_sck:1 | | peri.tr_io_output[1]:0 | | | | |

Table 8. Multiple Alternate Functions (continued)

| Port/ Pin | ACT #0 | ACT #1 | ACT #2 | ACT #3 | DS #2 | DS #3 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #5 | DS #6 |
|--------------|--------------------------|--------------------------|---------------|-----------------|-------|-------|--------|------------------|-------------------|------------------|---------------------|-----------------------|------------------------|-------------------------|---------|---------------------------|------------------------------|-------|-------|
| P11.5 | tcpwm[0].line_compl[3]:3 | tcpwm[1].line_compl[3]:1 | csd.csd_tx:83 | csd.csd_tx_n:83 | | | | smif.spi_data1 | | | scb[5].spi_select:1 | | audioss[1].rx_ws:1 | | | | | | |
| P11.6 | | | csd.csd_tx:84 | csd.csd_tx_n:84 | | | | smif.spi_data0 | | | scb[5].spi_select:1 | | audioss[1].rx_sdi:1 | | | | | | |
| P11.7 | | | | | | | | smif.spi_clk | | | | | | | | | | | |
| P12.0 | tcpwm[0].line[4]:3 | tcpwm[1].line[4]:1 | csd.csd_tx:85 | csd.csd_tx_n:85 | | | | smif.spi_data4 | scb[6].uart_rx:0 | scb[6].i2c_scl:0 | scb[6].spi_mosi:0 | | | peri.tr_io_in_put[24]:0 | | sdhc[1].card_emmc_reset_n | | | |
| P12.1 | tcpwm[0].line_compl[4]:3 | tcpwm[1].line_compl[4]:1 | csd.csd_tx:86 | csd.csd_tx_n:86 | | | | smif.spi_data5 | scb[6].uart_tx:0 | scb[6].i2c_sda:0 | scb[6].spi_miso:0 | | | peri.tr_io_in_put[25]:0 | | sdhc[1].card_detect_n | | | |
| P12.2 | tcpwm[0].line[5]:3 | tcpwm[1].line[5]:1 | csd.csd_tx:87 | csd.csd_tx_n:87 | | | | smif.spi_data6 | scb[6].uart_rts:0 | | scb[6].spi_clk:0 | | | | | | sdhc[1].card_mech_write_prot | | |
| P12.3 | tcpwm[0].line_compl[5]:3 | tcpwm[1].line_compl[5]:1 | csd.csd_tx:88 | csd.csd_tx_n:88 | | | | smif.spi_data7 | scb[6].uart_cts:0 | | scb[6].spi_select:0 | | | | | | sdhc[1].led_ctrl | | |
| P12.4 | tcpwm[0].line[6]:3 | tcpwm[1].line[6]:1 | csd.csd_tx:89 | csd.csd_tx_n:89 | | | | smif.spi_select3 | | | scb[6].spi_select:1 | audioss[0].pdm_clk:1 | | | | | sdhc[1].card_cmd | | |
| P12.5 | tcpwm[0].line_compl[6]:3 | tcpwm[1].line_compl[6]:1 | csd.csd_tx:90 | csd.csd_tx_n:90 | | | | | | | scb[6].spi_select:2 | audioss[0].pdm_data:1 | | | | | sdhc[1].clk_card | | |
| P12.6 | tcpwm[0].line[7]:3 | tcpwm[1].line[7]:1 | csd.csd_tx:91 | csd.csd_tx_n:91 | | | | | | | scb[6].spi_select:3 | | | | | | sdhc[1].card_if_pwr_en | | |
| P12.7 | tcpwm[0].line_compl[7]:3 | tcpwm[1].line_compl[7]:1 | csd.csd_tx:92 | csd.csd_tx_n:92 | | | | | | | | | | | | | sdhc[1].io_volt_sel | | |
| P13.0 | tcpwm[0].line[0]:4 | tcpwm[1].line[8]:1 | csd.csd_tx:93 | csd.csd_tx_n:93 | | | | | scb[6].uart_rx:1 | scb[6].i2c_scl:1 | scb[6].spi_mosi:1 | | audioss[1].clk_2s_if:0 | peri.tr_io_in_put[26]:0 | | sdhc[1].card_data_3to0[0] | | | |

Table 8. Multiple Alternate Functions (continued)

| Port/ Pin | ACT #0 | ACT #1 | ACT #2 | ACT #3 | DS #2 | DS #3 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #5 | DS #6 |
|--------------|--------------------------|---------------------------|----------------|------------------|-------|-------|--------|--------|--------------------|-------------------|----------------------|--------|---------------------|-----------------------|---------|---------------------------|---------|-------|-------|
| P13.1 | tcpwm[0].line_compl[0]:4 | tcpwm[1].line_compl[8]:1 | csd.csd_tx:94 | csd.csd_tx_n:94 | | | | | scb[6].uart_tx:1 | scb[6].i2c_sda:1 | scb[6].spi_miso:1 | | audioss[1].tx_sck:0 | peri.trio_input[27]:0 | | sdhc[1].card_data_3to0[1] | | | |
| P13.2 | tcpwm[0].line[1]:4 | tcpwm[1].line[9]:1 | csd.csd_tx:95 | csd.csd_tx_n:95 | | | | | scb[6].uart_rts:1 | | scb[6].spi_clk:1 | | audioss[1].tx_ws:0 | | | sdhc[1].card_data_3to0[2] | | | |
| P13.3 | tcpwm[0].line_compl[1]:4 | tcpwm[1].line_compl[9]:1 | csd.csd_tx:96 | csd.csd_tx_n:96 | | | | | scb[6].uart_cts:1 | | scb[6].spi_select0:1 | | audioss[1].tx_sdo:0 | | | sdhc[1].card_data_3to0[3] | | | |
| P13.4 | tcpwm[0].line[2]:4 | tcpwm[1].line[10]:1 | csd.csd_tx:97 | csd.csd_tx_n:97 | | | | | scb[12].uart_rx:0 | scb[12].i2c_scl:0 | scb[6].spi_select1:1 | | audioss[1].rx_sck:0 | | | sdhc[1].card_data_7to4[0] | | | |
| P13.5 | tcpwm[0].line_compl[2]:4 | tcpwm[1].line_compl[10]:1 | csd.csd_tx:98 | csd.csd_tx_n:98 | | | | | scb[12].uart_tx:0 | scb[12].i2c_sda:0 | scb[6].spi_select2:1 | | audioss[1].rx_ws:0 | | | sdhc[1].card_data_7to4[1] | | | |
| P13.6 | tcpwm[0].line[3]:4 | tcpwm[1].line[11]:1 | csd.csd_tx:99 | csd.csd_tx_n:99 | | | | | scb[12].uart_rts:0 | | scb[6].spi_select3:1 | | audioss[1].rx_sdi:0 | | | sdhc[1].card_data_7to4[2] | | | |
| P13.7 | tcpwm[0].line_compl[3]:4 | tcpwm[1].line_compl[11]:1 | csd.csd_tx:100 | csd.csd_tx_n:100 | | | | | scb[12].uart_cts:0 | | | | | | | sdhc[1].card_data_7to4[3] | | | |

Analog and Smart I/O alternate port pin functionality is provided in [Table 9](#).

Table 9. Port Pin Analog, Digital, and Smart I/O Functions

| Port/Pin | Analog |
|----------|------------------|
| P0.0 | wco_in |
| P0.1 | wco_out |
| P5.6 | lpcomp.inp_comp0 |
| P5.7 | lpcomp.inn_comp0 |
| P6.2 | lpcomp.inp_comp1 |
| P6.3 | lpcomp.inn_comp1 |
| P6.6 | swd_data |
| P6.7 | swd_clk |
| P7.2 | csd.csh_tank |
| P7.3 | csd.vref_ext |
| P7.7 | csd.shield |
| P9.7 | aref_ext_vref |
| P10.0 | sarmux_pads[0] |
| P10.1 | sarmux_pads[1] |
| P10.2 | sarmux_pads[2] |
| P10.3 | sarmux_pads[3] |
| P10.4 | sarmux_pads[4] |
| P10.5 | sarmux_pads[5] |
| P10.6 | sarmux_pads[6] |
| P10.7 | sarmux_pads[7] |
| P12.6 | eco_in |
| P12.7 | eco_out |

Table 9. Port Pin Analog, Digital, and Smart I/O Functions

| Port/Pin | Digital |
|----------|---------------------------------------|
| P0.4 | pmic_wakeup_in hibernate_wakeup[1] |
| P1.4 | hibernate_wakeup[0] |
| P0.5 | pmic_wakeup_out |
| Port/Pin | SMARTIO |
| P8.0 | smartio[8].io[0] |
| P8.1 | smartio[8].io[1] |
| P8.2 | smartio[8].io[2] |
| P8.3 | smartio[8].io[3] |
| P8.4 | smartio[8].io[4] |
| P8.5 | smartio[8].io[5] |
| P8.6 | smartio[8].io[6] |
| P8.7 | smartio[8].io[7] |
| P9.0 | smartio[9].io[0] |
| P9.1 | smartio[9].io[1] |
| P9.2 | smartio[9].io[2] |
| P9.3 | smartio[9].io[3] |
| P9.4 | smartio[9].io[4] |
| P9.5 | smartio[9].io[5] |
| P9.6 | smartio[9].io[6] |
| P9.7 | smartio[9].io[7] |

Power Supply Considerations

The following power system diagrams show typical connections for power pins for all supported packages and with and without usage of the buck regulator.

In these diagrams, the package pin is shown with the pin name, for example "V_{DDA}, A12". For V_{DDx} pins, the I/O port that is powered by that pin is also shown, for example "V_{DD}, A1; I/O port P1".

Figure 13. 124-BGA Power Connection Diagram

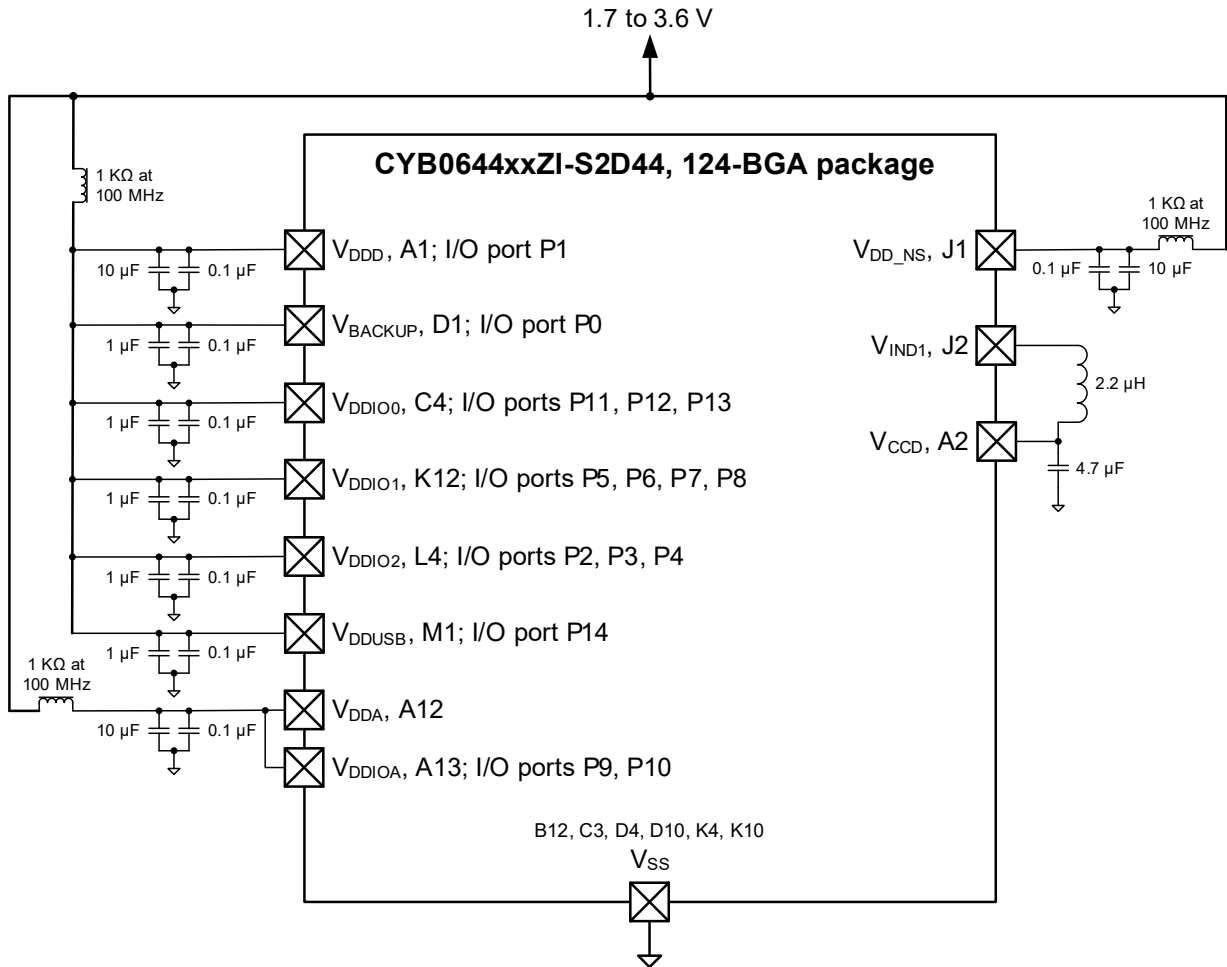
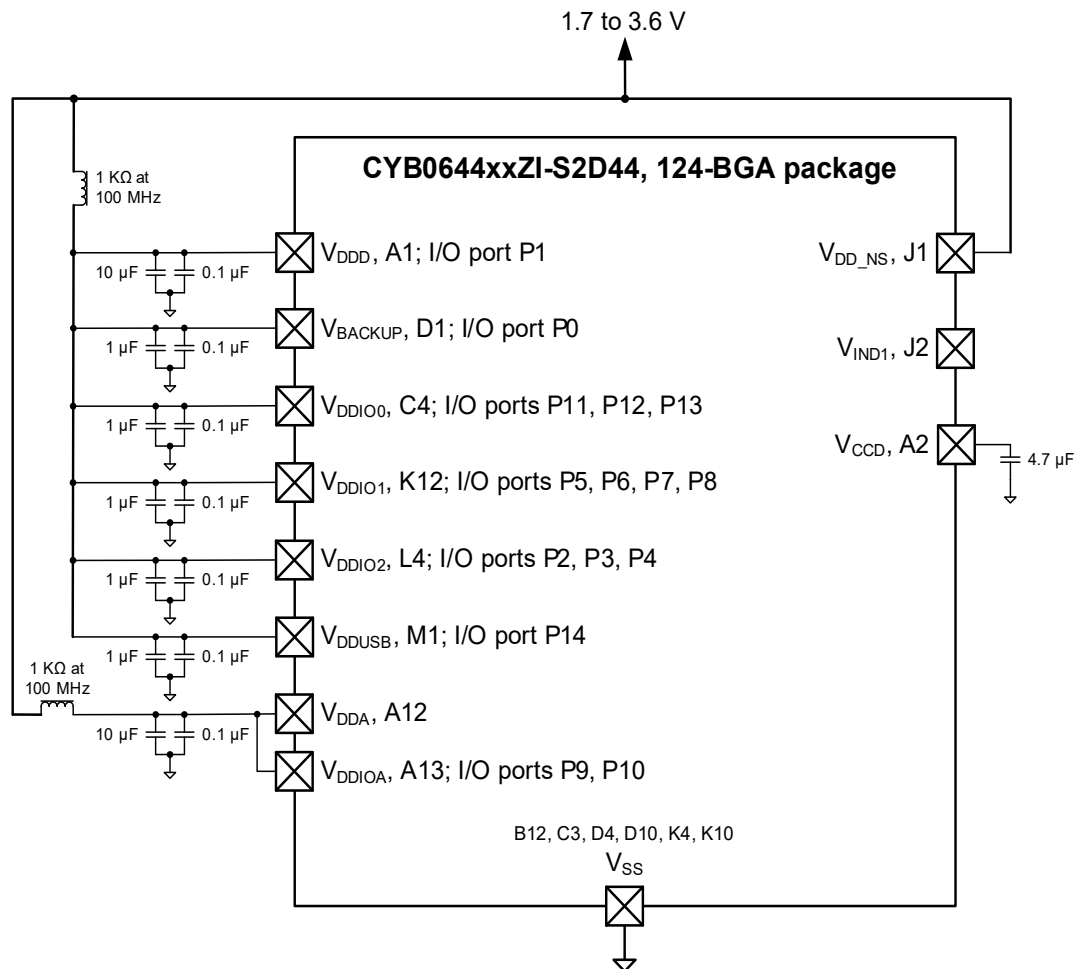
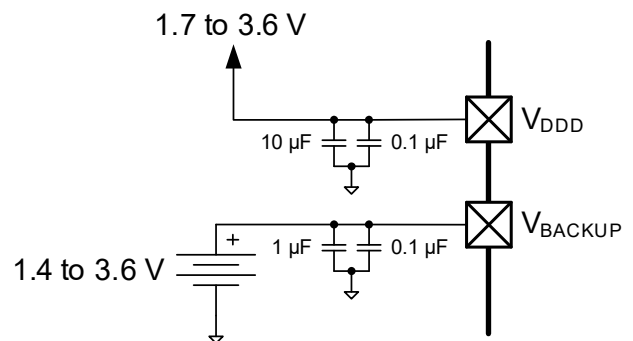


Figure 14. 124-BGA (No Buck) Power Connection Diagram


There are as many as eight V_{DDx} supply pins, depending on the package, and multiple V_{SS} ground pins. The power pins are:

- V_{DD} : the main digital supply. It powers the low dropout (LDO) regulators and I/O port 1
- V_{CCD} : the main LDO output. It requires a 4.7- μF capacitor for regulation. The LDO can be turned off when V_{CCD} is driven from the switching regulator (see below). For more information, see the power system block diagram in the device [technical reference manual \(TRM\)](#).
- V_{DDA} : the supply for the analog peripherals. Voltage must be applied to this pin for correct device initialization and boot up.
- V_{DDIOA} : the supply for I/O ports 9 and 10. It must be connected to V_{DDA} .
- V_{DDIO0} : the supply for I/O ports 11, 12, and 13.
- V_{DDIO1} : the supply for I/O ports 5, 6, 7, and 8.
- V_{DDIO2} : the supply for I/O ports 2, 3, and 4.
- V_{BACKUP} : the supply for the backup domain, which includes the 32-kHz WCO and the RTC. It can be a separate supply as low

as 1.4 V, for battery or supercapacitor backup, as [Figure 15](#) shows, otherwise it is connected to V_{DD} . It powers I/O port 0.

Figure 15. Separate Battery Connection to V_{BACKUP}


- V_{DDUSB} : the supply for the USB peripheral and the USBDP and USBDM pins. It must be 2.85 V to 3.6 V for USB operation. If USB is not used, it can be 1.7 V to 3.6 V, and the USB pins can be used as limited-capability GPIOs on I/O port 14.

Table 10 shows a summary of the I/O port supplies:

Table 10. I/O Port Supplies

| Port | Supply | Alternate Supply |
|------------|---------------------|------------------|
| 0 | V _{BACKUP} | V _{DDD} |
| 1 | V _{DDD} | - |
| 2, 3, 4 | V _{DDIO2} | - |
| 5, 6, 7, 8 | V _{DDIO1} | - |
| 9, 10 | V _{DDIOA} | V _{DDA} |
| 11, 12, 13 | V _{DDIO0} | - |
| 14 | V _{DDUSB} | - |

Note: If the USB pins are not used, connect V_{DDUSB} to ground and leave the P14.0/USBDP and P14.1/USBDM pins unconnected.

Voltage must be applied to the V_{DDD} pin, and the V_{DDA} pin as noted above, for correct device initialization and operation. If an I/O port is not being used, applying voltage to the corresponding V_{DDx} pin is optional.

- V_{SS}: ground pins for the above supplies. All ground pins should be connected together to a common ground.

In addition to the LDO regulator, a switching regulator is included. The regulator pins are:

- V_{DD_NS}: the regulator supply.
- V_{IND1}: the regulator output. It is typically used to drive V_{CCD} through an inductor.

The V_{DD} power pins are not connected on chip. They can be connected off chip, in one or more separate nets. If separate power nets are used, they can be isolated from noise from the other nets using optional ferrite beads, as indicated in the diagrams.

No external load should be placed on V_{CCD}, or V_{IND1}, whether or not these pins are used.

There are no power pin sequencing requirements; power supplies may be brought up in any order. The power management system holds the device in reset until all power pins are at the voltage levels required for proper operation.

Note: If a battery is installed on the PCB first, V_{DDD} must be cycled for at least 50 μs. This prevents premature drain of the battery during product manufacture and storage.

Bypass capacitors must be connected to a common ground from the V_{DDx} and other pins, as indicated in the diagrams. Typical practice for systems in this frequency range is to use a 10-μF or 1-μF capacitor in parallel with a smaller capacitor (0.1 μF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and bypass capacitor parasitic should be simulated for optimal bypassing.

All capacitors and inductors should be ±20% or better. The recommended inductor value is 2.2 μH ±20% (for example, TDK MLP2012H2R2MT0S1).

It is good practice to check the datasheets for your bypass capacitors, specifically the working voltage and the DC bias specifications. With some capacitors, the actual capacitance can decrease considerably when the applied voltage is a significant percentage of the rated working voltage.

For more information on pad layout, refer to [PSoC 6 CAD libraries](#).

Electrical Specifications

All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and for 1.71 V to 3.6 V except where noted.

Note: These are preliminary and subject to change.

Absolute Maximum Ratings

Table 11. Absolute Maximum Ratings^[4]

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|-----------------------------|--|------|-----|-----------------------|-------|----------------------|
| SID1 | V _{DD_ABS} | Analog or digital supply relative to V _{SS} (V _{SSD} = V _{SSA}) | -0.5 | - | 4 | V | |
| SID2 | V _{CCD_ABS} | Direct digital core voltage input relative to V _{SSD} | -0.5 | - | 1.2 | V | |
| SID3 | V _{GPIO_ABS} | GPIO voltage; V _{DDD} or V _{DDA} | -0.5 | - | V _{DD} + 0.5 | V | |
| SID4 | I _{GPIO_ABS} | Current per GPIO | -25 | - | 25 | mA | |
| SID5 | I _{GPIO_injection} | GPIO injection current per pin | -0.5 | - | 0.5 | mA | |
| SID3A | ESD_HBM | Electrostatic discharge Human Body Model | 2200 | - | - | V | |
| SID4A | ESD_CDM | Electrostatic discharge Charged Device Model | 500 | - | - | V | |
| SID5A | LU | Pin current for latchup-free operation | -100 | - | 100 | mA | |

Device-Level Specifications

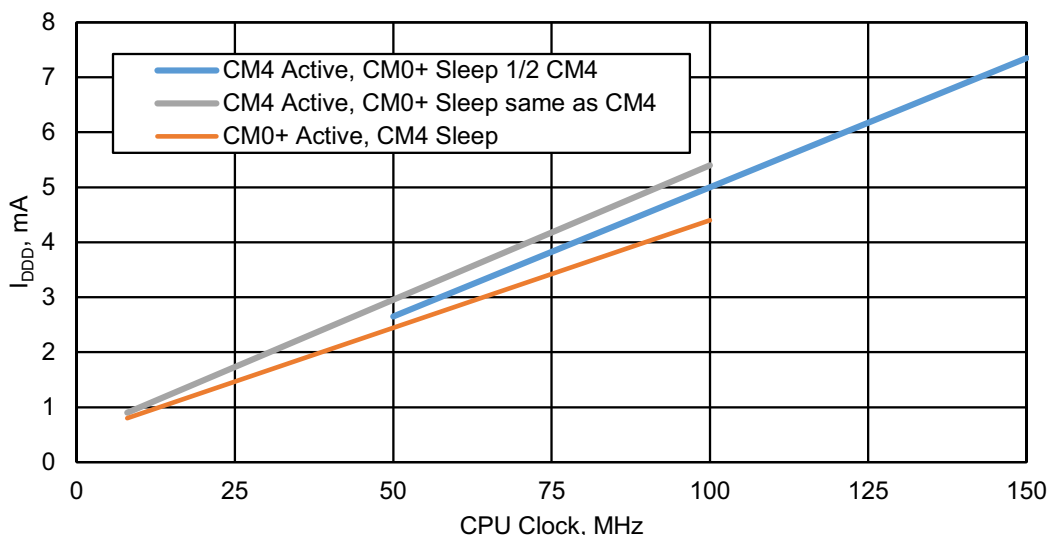
Table 14 provides detailed specifications of CPU current. Table 12 summarizes these specifications, for rapid review of CPU currents under common conditions. Note that the max frequency for CM4 is 150 MHz, and for CM0+ is 100 MHz. IMO and FLL are used to generate the CPU clocks; FLL is not used when the CPU clock frequency is 8 MHz.

Table 12. CPU Current Specifications Summary

| Condition | Range | Typ Range | Max Range |
|---|--|--------------|-------------|
| LP Mode, V _{DDD} = 3.3 V, V _{CCD} = 1.1 V, with buck regulator | | | |
| CM4 active, CM0+ sleep | Across CPUs clock ranges: 8 – 150/100 MHz; Dhrystone with flash cache enabled | 0.9–7.35 mA | 2–9.5 mA |
| CM0+ active, CM4 sleep | | 0.8–4.4 mA | 2–5.8 mA |
| CM4 sleep, CM0+ sleep | | 0.7–1.55 mA | 1.3–2.2 mA |
| CM0+ sleep, CM4 off | | 0.7–1.3 mA | 1.3–2 mA |
| Minimum regulator current mode | Across CM4/CM0+ CPU active/sleep modes | 0.64–0.85 mA | 1.2–1.5 mA |
| ULP Mode, V _{DDD} = 3.3 V, V _{CCD} = 0.9 V, with buck regulator | | | |
| CM4 active, CM0+ sleep | Across CPUs clock ranges: 8–50/25 MHz; Dhrystone with flash cache enabled | 0.65–1.85 mA | 1.2–2.5 mA |
| CM0+ active, CM4 sleep | | 0.55–1 mA | 0.95–1.5 mA |
| CM4 sleep, CM0+ sleep | | 0.45–0.85 mA | 0.9–1.2 mA |
| CM0+ sleep, CM4 off | | 0.41–0.62 mA | 0.72–1.2 mA |
| Minimum regulator current mode | Across CM4/CM0+ CPU active/sleep modes | 0.4–0.55 mA | 1–1 mA |
| Deep Sleep | Across SRAM retention | 7–9 μA | - |
| Hibernate | Across V _{DDD} | 300–2100 nA | - |

Note

- Usage above the absolute maximum conditions listed in Table 11 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Figure 16. Typical Device Currents vs. CPU Frequency; System Low Power (LP) Mode

Power Supplies
Table 13. Power Supply DC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|---------------------|--|-----|-----|-----|-------|---|
| SID6 | V _{DDD} | Internal regulator and Port 1 GPIO supply | 1.7 | – | 3.6 | V | – |
| SID7 | V _{DDA} | Analog power supply voltage. Shorted to V _{DDIOA} on PCB. | 1.7 | – | 3.6 | V | Internally unregulated supply |
| SID7A | V _{DDIO1} | GPIO supply for ports 5 to 8 when present | 1.7 | – | 3.6 | V | Must be ≥ V _{DDA} if the CapSense (CSD) block is used in the application |
| SID7B | V _{DDIO0} | GPIO supply for ports 11 to 13 when present | 1.7 | – | 3.6 | V | – |
| SID7C | V _{DDIO2} | GPIO supply for ports 2 to 4 when present | 1.7 | – | 3.6 | V | – |
| SID7D | V _{DDIOA} | GPIO supply for ports 9 and 10 when present. Must be connected to V _{DDA} on PCB. | 1.7 | – | 3.6 | V | – |
| SID7F | V _{DDUSB} | Supply for port 14 (USB or GPIO) when present | 1.7 | – | 3.6 | V | Min supply is 2.85 V for USB |
| SID6B | V _{BACKUP} | Backup power and GPIO Port 0 supply when present | 1.7 | – | 3.6 | V | Min is 1.4 V when V _{DDD} is removed |
| SID8 | V _{CCD1} | Output voltage (for core logic bypass) | – | 1.1 | – | V | System LP mode |
| SID9 | V _{CCD2} | Output voltage (for core logic bypass) | – | 0.9 | – | | ULP mode. Valid for –20 to 85 °C. |
| SID10 | C _{EFC} | External regulator voltage (V _{CCD}) bypass | 3.8 | 4.7 | 5.6 | μF | X5R ceramic or better. Value for 0.8 to 1.2 V. |
| SID11 | C _{EXC} | Power supply decoupling capacitor | – | 10 | – | μF | X5R ceramic or better |

CPU Current and Transition Times

Table 14. CPU Current and Transition Times

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|--|-----------|---|-----|------|------|-------|--|
| LP RANGE POWER SPECIFICATIONS (for V_{CCD} = 1.1 V with Buck and LDO) | | | | | | | |
| Cortex-M4. Active Mode | | | | | | | |
| Execute with Cache Disabled (Flash) | | | | | | | |
| SIDF1 | IDD1 | Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. While(1). | - | 2.85 | 4.5 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 4.1 | 5.1 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | | 6.8 | 10 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| SIDF2 | IDD2 | Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While(1). | - | 0.9 | 2.1 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 1.2 | 2.2 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | | 2.4 | 5.5 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| Execute with Cache Enabled | | | | | | | |
| SIDC1 | IDD3 | Execute from Cache; CM4 Active 150 MHz, CM0+ Sleep 75 MHz. IMO & PLL. Dhrystone. | - | 7.35 | 9.5 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 12 | 14.5 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | | 18 | 21 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| SIDC2 | IDD4 | Execute from Cache; CM4 Active 100 MHz, CM0+ Sleep 100 MHz. IMO & FLL. Dhrystone. | - | 5.4 | 6.8 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 8.95 | 10 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | | 13.8 | 17 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| SIDC3 | IDD5 | Execute from Cache; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. IMO & FLL. Dhrystone. | - | 2.65 | 3.8 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 4.25 | 5.3 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | | 6.8 | 10 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| SIDC4 | IDD6 | Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. IMO. Dhrystone. | - | 0.9 | 2 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 1.27 | 2.1 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | | 2.3 | 5.5 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |

Table 14. CPU Current and Transition Times *(continued)*

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|--|-----------|---|-----|------|------|-------|--|
| Cortex M0+. Active Mode | | | | | | | |
| Execute with Cache Disabled (Flash) | | | | | | | |
| SIDF3 | IDD7 | Execute from Flash;CM4 Off, CM0+ Active 50 MHz. With IMO & FLL. While (1). | - | 2.6 | 4 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 3.9 | 5 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | | 6.5 | 10 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| SIDF4 | IDD8 | Execute from Flash;CM4 Off, CM0+ Active 8 MHz. With IMO. While (1). | - | 0.8 | 1.5 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 1.1 | 2 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | | 2.2 | 5.5 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| Execute with Cache Enabled | | | | | | | |
| SIDC5 | IDD9 | Execute from Cache;CM4 Off, CM0+ Active 100 MHz. With IMO & FLL. Dhrystone. | - | 4.40 | 5.8 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 7.35 | 8.5 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | | 11.5 | 14.5 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| SIDC6 | IDD10 | Execute from Cache;CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone. | - | 0.8 | 2 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 1.2 | 2 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | | 2.2 | 5.5 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| Cortex M4. Sleep Mode | | | | | | | |
| SIDS1 | IDD11 | CM4 Sleep 100 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. | - | 1.55 | 2.2 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 2.4 | 3.5 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | | 4.2 | 7.2 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| SIDS2 | IDD12 | CM4 Sleep 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. | - | 1.2 | 2 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 1.75 | 2.7 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | | 3.2 | 6.3 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |
| SIDS3 | IDD13 | CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO. | - | 0.7 | 1.3 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 0.96 | 1.8 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | | 1.7 | 5 | | V _{DDD} = 1.8 to 3.3 V, LDO, max at 60 °C |

Table 14. CPU Current and Transition Times (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|-----------|--|-----|------|-----|-------|--|
| Cortex M0+. Sleep Mode | | | | | | | |
| SIDS4 | IDD14 | CM4 Off, CM0+ Sleep 50 MHz. With IMO & FLL. | - | 1.3 | 2 | mA | $V_{DDD} = 3.3\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 2.05 | 3 | | $V_{DDD} = 1.8\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 3.6 | 6.8 | | $V_{DDD} = 1.8\text{ to }3.3\text{ V}$, LDO, max at 60 °C |
| SIDS5 | IDD15 | CM4 Off, CM0+ Sleep 8 MHz. With IMO. | - | 0.7 | 1.3 | mA | $V_{DDD} = 3.3\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 0.95 | 1.5 | | $V_{DDD} = 1.8\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 1.7 | 5 | | $V_{DDD} = 1.8\text{ to }3.3\text{ V}$, LDO, max at 60 °C |
| Cortex M4. Minimum Regulator Current Mode | | | | | | | |
| SIDLPA1 | IDD16 | Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1). | - | 0.85 | 1.8 | mA | $V_{DDD} = 3.3\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 1.18 | 2 | | $V_{DDD} = 1.8\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 2.2 | 5.5 | | $V_{DDD} = 1.8\text{ to }3.3\text{ V}$, LDO, max at 60 °C |
| SIDLPA2 | IDD17 | Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone. | - | 0.9 | 1.5 | mA | $V_{DDD} = 3.3\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 1.27 | 2 | | $V_{DDD} = 1.8\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 2.2 | 5.5 | | $V_{DDD} = 1.8\text{ to }3.3\text{ V}$, LDO, max at 60 °C |
| Cortex M0+. Minimum Regulator Current Mode | | | | | | | |
| SIDLPA3 | IDD18 | Execute from Flash; CM4 Off, CM0+ Active 8 MHz. With IMO. While (1). | - | 0.8 | 1.5 | mA | $V_{DDD} = 3.3\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 1.14 | 2 | | $V_{DDD} = 1.8\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 2.1 | 5.5 | | $V_{DDD} = 1.8\text{ to }3.3\text{ V}$, LDO, max at 60 °C |
| SIDLPA4 | IDD19 | Execute from Cache; CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone. | - | 0.8 | 1.5 | mA | $V_{DDD} = 3.3\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 1.15 | 2 | | $V_{DDD} = 1.8\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 2.1 | 5.5 | | $V_{DDD} = 1.8\text{ to }3.3\text{ V}$, LDO, max at 60 °C |
| Cortex M4. Minimum Regulator Current Mode | | | | | | | |
| SIDLPS1 | IDD20 | CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO. | - | 0.65 | 1.2 | mA | $V_{DDD} = 3.3\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 0.95 | 1.7 | | $V_{DDD} = 1.8\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 1.6 | 5 | | $V_{DDD} = 1.8\text{ to }3.3\text{ V}$, LDO, max at 60 °C |

Table 14. CPU Current and Transition Times (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|-----------|---|-----|------|-----|-------|---|
| Cortex M0+. Minimum Regulator Current Mode | | | | | | | |
| SIDLPS3 | IDD22 | CM4 Off, CM0+ Sleep 8 MHz. With IMO. | - | 0.64 | 1.2 | mA | $V_{DD} = 3.3\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 0.93 | 1.7 | | $V_{DD} = 1.8\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 1.6 | 5 | | $V_{DD} = 1.8\text{ to }3.3\text{ V}$, LDO, max at 60 °C |
| ULP Range Power Specifications (for $V_{CCD} = 0.9\text{ V}$ using the Buck). ULP mode is valid from -20 to +85 °C. | | | | | | | |
| Cortex M4. Active Mode | | | | | | | |
| Execute with Cache Disabled (Flash) | | | | | | | |
| SIDF5 | IDD3 | Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. While(1). | - | 2.15 | 2.9 | mA | $V_{DD} = 3.3\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 2.85 | 3.4 | | $V_{DD} = 1.8\text{ V}$, Buck ON, Max at 60 °C |
| SIDF6 | IDD4 | Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1). | - | 0.65 | 1.2 | mA | $V_{DD} = 3.3\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 0.8 | 1.4 | | $V_{DD} = 1.8\text{ V}$, Buck ON, Max at 60 °C |
| Execute with Cache Enabled | | | | | | | |
| SIDC8 | IDD10 | Execute from Cache; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. Dhystone. | - | 1.85 | 2.5 | mA | $V_{DD} = 3.3\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 2.9 | 3.5 | | $V_{DD} = 1.8\text{ V}$, Buck ON, Max at 60 °C |
| SIDC9 | IDD11 | Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhystone. | - | 0.65 | 1.2 | mA | $V_{DD} = 3.3\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 0.8 | 1.3 | | $V_{DD} = 1.8\text{ V}$, Buck ON, Max at 60 °C |
| Cortex M0+. Active Mode | | | | | | | |
| Execute with Cache Disabled (Flash) | | | | | | | |
| SIDF7 | IDD16 | Execute from Flash; CM4 Off, CM0+ Active 25 MHz. With IMO & FLL. Write(1). | - | 1.1 | 1.5 | mA | $V_{DD} = 3.3\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 1.55 | 2.2 | | $V_{DD} = 1.8\text{ V}$, Buck ON, Max at 60 °C |
| SIDF8 | IDD17 | Execute from Flash; CM4 Off, CM0+ Active 8 MHz. With IMO. While(1). | - | 0.55 | 1.2 | mA | $V_{DD} = 3.3\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 0.73 | 1.4 | | $V_{DD} = 1.8\text{ V}$, Buck ON, Max at 60 °C |
| Execute with Cache Enabled | | | | | | | |
| SIDC10 | IDD18 | Execute from Cache; CM4 Off, CM0+ Active 25 MHz. With IMO & FLL. Dhystone. | - | 1 | 1.5 | mA | $V_{DD} = 3.3\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 1.5 | 2 | | $V_{DD} = 1.8\text{ V}$, Buck ON, Max at 60 °C |

Table 14. CPU Current and Transition Times (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|--|-----------|--|-----|------|------|-------|---|
| SIDC11 | IDD19 | Execute from Cache; CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone. | - | 0.55 | 0.95 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 0.73 | 1.3 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| Cortex M4. Sleep Mode | | | | | | | |
| SIDS7 | IDD21 | CM4 Sleep 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. | - | 0.85 | 1.2 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 1.2 | 1.8 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| SIDS8 | IDD22 | CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO. | - | 0.45 | 0.9 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 0.59 | 1 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| Cortex M0+. Sleep Mode | | | | | | | |
| SIDS9 | IDD23 | CM4 Off, CM0+ Sleep 25 MHz. With IMO & FLL. | - | 0.62 | 1.2 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 0.88 | 1.5 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| SIDS10 | IDD24 | CM4 Off, CM0+ Sleep 8 MHz. With IMO. | - | 0.41 | 0.72 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 0.58 | 1.3 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| Cortex M4. Minimum Regulator Current Mode ° | | | | | | | |
| SIDLPA5 | IDD25 | Execute from Flash. CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While(1). | - | 0.65 | 1.2 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 0.8 | 1.4 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| SIDLPA6 | IDD26 | Execute from Cache. CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone. | - | 0.6 | 1 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 0.78 | 1.4 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| Cortex M0+. Minimum Regulator Current Mode | | | | | | | |
| SIDLPA7 | IDD27 | Execute from Flash. CM4 Off, CM0+ Active 8 MHz. With IMO. While (1). | - | 0.55 | 1 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 0.75 | 1.4 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| SIDLPA8 | IDD28 | Execute from Cache. CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone. | - | 0.5 | 1 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | | 0.7 | 1.4 | | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |

Table 14. CPU Current and Transition Times (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|------------------|---|-----|------|-----|-------|--|
| Cortex M4. Minimum Regulator Current Mode | | | | | | | |
| SIDLPS5 | IDD29 | CM4 Sleep 8 MHz, CM0 Sleep 8 MHz. With IMO. | - | 0.45 | 1 | mA | $V_{DDD} = 3.3\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 0.57 | 1.1 | | $V_{DDD} = 1.8\text{ V}$, Buck ON, Max at 60 °C |
| Cortex M0+. Minimum Regulator Current Mode | | | | | | | |
| SIDLPS7 | IDD31 | CM4 Off, CM0+ Sleep 8 MHz. With IMO. | - | 0.4 | 1 | mA | $V_{DDD} = 3.3\text{ V}$, Buck ON, Max at 60 °C |
| | | | | 0.56 | 1.1 | | $V_{DDD} = 1.8\text{ V}$, Buck ON, Max at 60 °C |
| Deep Sleep Mode | | | | | | | |
| SIDDS2 | I_{DD33B} | With internal Buck enabled and 256-KB SRAM retention. | - | 20 | - | µA | |
| Hibernate Mode | | | | | | | |
| SIDHIB1 | I_{DD34} | $V_{DDD} = 1.8\text{ V}$ | - | 300 | - | nA | No clocks running |
| SIDHIB2 | I_{DD34A} | $V_{DDD} = 3.3\text{ V}$ | - | 2100 | - | nA | No clocks running |
| Power Mode Transition Times | | | | | | | |
| SID12 | T_{LPACT_ACT} | Minimum Regulator Current to LP transition time. | - | - | 35 | µs | Including PLL lock time |
| SID13 | T_{DS_LPACT} | Deep Sleep to LP transition time | - | - | 21 | µs | Guaranteed by design |
| SID14 | T_{HIB_ACT} | Hibernate to LP transition time | - | 1000 | - | µs | Including PLL lock time |

XRES

Table 15. XRES DC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|--------------------|---|----------------|------|----------------|-------|--------------------------|
| SID17 | T_{XRES_IDD} | I_{DD} when XRES asserted | - | 300 | 500 | nA | $V_{DDD} = 1.8\text{ V}$ |
| SID17A | $T_{XRES_IDD_1}$ | I_{DD} when XRES asserted | - | 2100 | 10500 | nA | $V_{DDD} = 3.3\text{ V}$ |
| SID77 | V_{IH} | Input voltage HIGH threshold | $0.7 * V_{DD}$ | - | - | V | CMOS input |
| SID78 | V_{IL} | Input voltage LOW threshold | - | - | $0.3 * V_{DD}$ | V | CMOS input |
| SID80 | C_{IN} | Input capacitance | - | 3 | - | pF | - |
| SID81 | $V_{HYSXRES}$ | Input voltage hysteresis | - | 100 | - | mV | - |
| SID82 | I_{DIODE} | Current through protection diode to V_{DD}/V_{SS} | - | - | 100 | µA | - |

Table 16. XRES AC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|-----------------------|---|-----|------|-----|-------|---------------------------|
| SID15 | T _{XRES_ACT} | POR or XRES release to Active transition time | – | 1000 | – | μs | Normal mode, 50-MHz CM0+. |
| SID16 | T _{XRES_PW} | XRES pulse width | 5 | – | – | μs | – |

GPIO
Table 17. GPIO DC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|-----------------------|--|------------------------|-----|-----------------------|-------|--------------------------------|
| SID57 | V _{IH} | Input voltage HIGH threshold | 0.7 * V _{DD} | – | – | V | CMOS Input |
| SID57A | I _{IHS} | Input current when Pad > V _{DDIO} for OVT inputs | – | – | 10 | μA | Per I ² C Spec |
| SID58 | V _{IL} | Input voltage LOW threshold | – | – | 0.3 * V _{DD} | V | CMOS Input |
| SID241 | V _{IH} | LVTTTL input, V _{DD} < 2.7 V | 0.7 * V _{DD} | – | – | V | – |
| SID242 | V _{IL} | LVTTTL input, V _{DD} < 2.7 V | – | – | 0.3 * V _{DD} | V | – |
| SID243 | V _{IH} | LVTTTL input, V _{DD} ≥ 2.7 V | 2.0 | – | – | V | – |
| SID244 | V _{IL} | LVTTTL input, V _{DD} ≥ 2.7 V | – | – | 0.8 | V | – |
| SID59 | V _{OH} | Output voltage HIGH level | V _{DD} – 0.5 | – | – | V | I _{OH} = 8 mA |
| SID62A | V _{OL} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 8 mA |
| SID63 | R _{PULLUP} | Pull-up resistor | 3.5 | 5.6 | 8.5 | kΩ | – |
| SID64 | R _{PULLDOWN} | Pull-down resistor | 3.5 | 5.6 | 8.5 | kΩ | – |
| SID65 | I _{IL} | Input leakage current (absolute value) | – | – | 2 | nA | 25 °C, V _{DD} = 3.0 V |
| SID66 | C _{IN} | Input capacitance | – | – | 5 | pF | – |
| SID67 | V _{HYSTTL} | Input hysteresis LVTTTL V _{DD} > 2.7 V | 100 | 0 | – | mV | – |
| SID68 | V _{HYS CMOS} | Input hysteresis CMOS | 0.05 * V _{DD} | – | – | mV | – |
| SID69 | I _{DIODE} | Current through protection diode to V _{DD} /V _{SS} | – | – | 100 | μA | – |
| SID69A | I _{TOT_GPIO} | Maximum total source or sink chip current | – | – | 200 | mA | – |

Table 18. GPIO AC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|-----------------------|--|-----|-----|-----|-------|--|
| SID70 | T _{RISE F} | Rise time in Fast Strong Mode. 10% to 90% of V _{DD} . | – | – | 2.5 | ns | Load = 15 pF, 8-mA drive strength |
| SID71 | T _{FALL F} | Fall time in Fast Strong Mode. 10% to 90% of V _{DD} . | – | – | 2.5 | ns | Load = 15 pF, 8-mA drive strength |
| SID72 | T _{RISE S_1} | Rise time in Slow Strong Mode. 10% to 90% of V _{DD} . | 52 | – | 142 | ns | Load = 15 pF, 8-mA drive strength, V _{DD} ≤ 2.7 V |
| SID72A | T _{RISE S_2} | Rise time in Slow Strong Mode. 10% to 90% of V _{DD} . | 48 | – | 102 | ns | Load = 15 pF, 8-mA drive strength, 2.7 V < V _{DD} ≤ 3.6 V |

Table 18. GPIO AC Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|-----------------------|--|------------------------------|-----|-----|-------|--|
| SID73 | T _{FALLS_1} | Fall time in Slow Strong Mode. 10% to 90% of V _{DD} . | 44 | – | 211 | ns | Clload = 15 pF, 8-mA drive strength, V _{DD} ≤ 2.7 V |
| SID73A | T _{FALLS_2} | Fall time in Slow Strong Mode. 10% to 90% of V _{DD} . | 42 | – | 93 | ns | Clload = 15 pF, 8-mA drive strength, 2.7 V < V _{DD} ≤ 3.6 V |
| SID73G | T _{FALL_I2C} | Fall time (30% to 70% of V _{DD}) in Slow Strong mode. | 20 * V _{DDIO} / 5.5 | – | 250 | ns | Clload = 10 pF to 400 pF, 8-mA drive strength |
| SID74 | F _{GPIOUT1} | GPIO Fout. Fast Strong mode. | – | – | 100 | MHz | 90/10%, 15-pF load, 60/40 duty cycle |
| SID75 | F _{GPIOUT2} | GPIO Fout; Slow Strong mode. | – | – | 1.5 | MHz | 90/10%, 15-pF load, 60/40 duty cycle |
| SID76 | F _{GPIOUT3} | GPIO Fout; Fast Strong mode. | – | – | 100 | MHz | 90/10%, 25-pF load, 60/40 duty cycle |
| SID245 | F _{GPIOUT4} | GPIO Fout; Slow Strong mode. | – | – | 1.3 | MHz | 90/10%, 25-pF load, 60/40 duty cycle |
| SID246 | F _{GPIOIN} | GPIO input operating frequency; 1.71 V ≤ V _{DD} ≤ 3.6 V | – | – | 100 | MHz | 90/10% V _{IO} |

Analog Peripherals

Low-Power (LP) Comparator

Table 19. LP Comparator DC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|----------|----------------------|---|-----|-----|--------------------------|-------|--------------------|
| SID84 | V _{OFFSET1} | Input offset voltage. Normal power mode. | –10 | – | 10 | mV | – |
| SID85A | V _{OFFSET2} | Input offset voltage. Low-power mode. | –25 | ±12 | 25 | mV | – |
| SID85B | V _{OFFSET3} | Input offset voltage. Ultra low-power mode. | –25 | ±12 | 25 | mV | – |
| SID86 | V _{HYST1} | Hysteresis when enabled in Normal mode | – | – | 60 | mV | – |
| SID86A | V _{HYST2} | Hysteresis when enabled in Low-power mode | – | – | 80 | mV | – |
| SID87 | V _{ICM1} | Input common mode voltage in Normal mode | 0 | – | V _{DDIO1} – 0.1 | V | – |
| SID247 | V _{ICM2} | Input common mode voltage in Low power mode | 0 | – | V _{DDIO1} – 0.1 | V | – |
| SID247A | V _{ICM3} | Input common mode voltage in Ultra low power mode | 0 | – | V _{DDIO1} – 0.1 | V | – |
| SID88 | CMRR | Common mode rejection ratio in Normal power mode | 50 | – | – | dB | – |
| SID89 | I _{CMP1} | Block current, Normal mode | – | – | 150 | μA | – |
| SID248 | I _{CMP2} | Block current, Low-power mode | – | – | 10 | μA | – |
| SID259 | I _{CMP3} | Block current in Ultra low-power mode | – | 0.3 | 0.85 | μA | – |
| SID90 | ZCMP | DC input impedance of comparator | 35 | – | – | MΩ | – |

Table 20. LP Comparator AC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|----------|----------------------|---|-----|-----|------|-------|----------------------------|
| SID91 | T _{RESP1} | Response time, Normal mode, 100 mV overdrive | – | – | 100 | ns | – |
| SID258 | T _{RESP2} | Response time, Low power mode, 100 mV overdrive | – | – | 1000 | ns | – |
| SID92 | T _{RESP3} | Response time, Ultra-low power mode, 100 mV overdrive | – | – | 20 | µs | – |
| SID92E | T _{CMP_EN1} | Time from Enabling to operation | – | – | 10 | µs | Normal and low-power modes |
| SID92F | T _{CMP_EN2} | Time from Enabling to operation | – | – | 50 | µs | Ultra-low-power mode |

Temperature Sensor
Table 21. Temperature Sensor Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|----------------------|-----------------------------|-----|-----|-----|-------|--------------------|
| SID93 | T _{SENSACC} | Temperature sensor accuracy | –5 | ±1 | 5 | °C | –40 to +85 °C |

Internal Reference
Table 22. Internal Reference Specification

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|--------------------|-------------|-------|-----|-------|-------|--------------------|
| SID93R | V _{REFBG} | – | 1.188 | 1.2 | 1.212 | V | – |

SAR ADC
Table 23. 12-bit SAR ADC DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------|------------------------------------|-----------------|-----|------------------|-------|------------------------------------|
| SID94 | A_RES | SAR ADC resolution | – | – | 12 | bits | |
| SID95 | A_CHNLS_S | Number of channels - single-ended | – | – | 16 | – | 8 full speed. |
| SID96 | A-CHNKS_D | Number of channels - differential | – | – | 8 | – | Diff inputs use neighboring I/Os |
| SID97 | A-MONO | Monotonicity | – | – | – | – | Yes. |
| SID98 | A_GAINERR | Gain error | – | – | ±0.2 | % | With external reference. |
| SID99 | A_OFFSET | Input offset voltage | – | – | 2 | mV | Measured with 1-V reference |
| SID100 | A_ISAR_1 | Current consumption at 1 Msps | – | – | 1.05 | mA | At 1 Msps. External reference mode |
| SID100A | A_ISAR_2 | Current consumption at 1 Msps | – | – | 1.3 | mA | At 1 Msps. Internal reference mode |
| SID1002 | A_ISAR_3 | Current consumption at 2 Msps | – | – | 1.65 | mA | At 2 Msps. External reference mode |
| SID1003 | A_ISAR_4 | Current consumption at 2 Msps | – | – | 2.15 | mA | At 2 Msps. Internal reference mode |
| SID101 | A_VINS | Input voltage range - single-ended | V _{SS} | – | V _{DDA} | V | |
| SID102 | A_VIND | Input voltage range - differential | V _{SS} | – | V _{DDA} | V | |
| SID103 | A_INRES | Input resistance | – | 1 | – | KΩ | |
| SID104 | A_INCAP | Input capacitance | – | 5 | – | pF | |

Table 24. 12-bit SAR ADC AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|----------|-----------|--|------|-----|-----|-------|--|
| SID106 | A_PSR | Power supply rejection ratio | 70 | – | – | dB | |
| SID107 | A_CMRR | Common mode rejection ratio | 66 | – | – | dB | Measured at 1 V |
| SID1081 | A_SAMP_1 | Sample rate with external reference With bypass cap | – | – | 2 | Msp | V _{DDA} 2.7–3.6 |
| SID1082 | A_SAMP_1 | Sample rate with external reference With bypass cap | – | – | 1 | Msp | V _{DDA} 1.7–3.6 |
| SID108A1 | A_SAMP_2 | Sample rate with V _{DD} reference; No Bypass Cap | – | – | 2 | Msp | V _{DDA} 2.7–3.6 |
| SID108A2 | A_SAMP_2 | Sample rate with V _{DD} Reference; No Bypass Cap | – | – | 1 | Msp | V _{DDA} 1.7–3.6 |
| SID108B | A_SAMP_3 | Sample rate with internal reference; With Bypass Cap. | – | – | 1 | Msp | |
| SID108C | A_SAMP_4 | Sample rate with internal reference. No Bypass Cap | – | – | 200 | ksps | |
| SID109 | A_SINAD | Signal-to-noise and distortion ratio (SINAD). | 64 | – | – | dB | F _{in} = 10 kHz |
| SID111A | A_INL | Integral non-linearity. Up to 1 Msp | –2 | – | 2 | LSB | All reference modes |
| SID111B | A_INL | Integral non-linearity. 2 Msp. | –2.5 | – | 2.5 | LSB | External reference or V _{DDA} Reference Mode, V _{REF} ≥ 2 V. V _{DDA} = 2.7 V to 3.6 V |
| SID112A | A_DNL | Differential non-linearity. Up to 1 Msp | –1 | – | 1.5 | LSB | All reference modes |
| SID112B | A_DNL | Differential non-linearity. 2 Msp. | –1 | – | 1.6 | LSB | External reference or V _{DDA} Reference Mode, V _{REF} ≥ 2 V. V _{DDA} = 2.7 to 3.6V |
| SID113 | A_THD | Total harmonic distortion. 1 Msp. | – | – | –65 | dB | F _{IN} = 10 kHz. V _{DDA} = 2.7–3.6 V |

CSD
Table 25. CapSense Sigma-Delta (CSD) Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|------------------------------|----------------------------|--|-----|-----|---------------------------|-------|--|
| CSD V2 Specifications | | | | | | | |
| SYS.PER#3 | V _{DD_RIPPLE} | Max allowed ripple on power supply, DC to 10 MHz | – | – | ±50 | mV | V _{DDA} > 2 V (with ripple), 25 °C T _A , sensitivity = 0.1 pF |
| SYS.PER#16 | V _{DD_RIPPLE_1.8} | Max allowed ripple on power supply, DC to 10 MHz | – | – | ±25 | mV | V _{DDA} > 1.75 V (with ripple), 25 °C T _A , Parasitic capacitance (C _P) < 20 pF, Sensitivity ≥ 0.4 pF |
| SID.CSD.BLK | I _{CSD} | Maximum block current | – | – | 4500 | µA | – |
| SID.CSD#15 | V _{REF} | Voltage reference for CSD and Comparator | 0.6 | 1.2 | V _{DDA} – 0.6 | V | V _{DDA} – V _{REF} ≥ 0.6 V |
| SID.CSD#15A | V _{REF_EXT} | External Voltage reference for CSD and Comparator | 0.6 | – | V _{DDA} – 0.6 | V | V _{DDA} – V _{REF} ≥ 0.6 V |
| SID.CSD#16 | I _{DAC1IDD} | IDAC1 (7-bits) block current | – | – | 1900 | µA | – |
| SID.CSD#17 | I _{DAC2IDD} | IDAC2 (7-bits) block current | – | – | 1900 | µA | – |
| SID308 | V _{CSD} | Voltage range of operation | 1.7 | – | 3.6 | V | 1.71–3.6 V |

Table 25. CapSense Sigma-Delta (CSD) Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|-----------------|--|------|-----|-----------------|---------|--|
| SID308A | $V_{COMPIDAC}$ | Voltage compliance range of IDAC | 0.6 | – | $V_{DDA} - 0.6$ | V | $V_{DDA} - V_{REF} \geq 0.6$ V |
| SID309 | $I_{DAC1DNL}$ | DNL | –1 | – | 1 | LSB | – |
| SID310 | $I_{DAC1INL}$ | INL | –3 | – | 3 | LSB | If $V_{DDA} < 2$ V then for LSB of 2.4 μ A or less |
| SID311 | $I_{DAC2DNL}$ | DNL | –1 | – | 1 | LSB | – |
| SID312 | $I_{DAC2INL}$ | INL | –3 | – | 3 | LSB | If $V_{DDA} < 2$ V then for LSB of 2.4 μ A or less |
| SNRC of the following is Ratio of counts of finger to noise. Measured typical devices at room temperature using Dual IDAC + PRS Clock Mode. Best performance is when using the PASS reference and the PLL. | | | | | | | |
| SID313_1A | SNRC_1 | SRSS Reference. IMO + FLL Clock Source. 0.1-pF sensitivity. | 5 | – | – | Ratio | 9.5-pF max. capacitance |
| SID313_1B | SNRC_2 | SRSS Reference. IMO + FLL Clock Source. 0.3-pF sensitivity. | 5 | – | – | Ratio | 31-pF max. capacitance |
| SID313_1C | SNRC_3 | SRSS Reference. IMO + FLL Clock Source. 0.6-pF sensitivity. | 5 | – | – | Ratio | 61-pF max. capacitance |
| SID313_2A | SNRC_4 | PASS Reference. IMO + FLL Clock Source. 0.1-pF sensitivity. | 5 | – | – | Ratio | 12-pF max. capacitance |
| SID313_2B | SNRC_5 | PASS Reference. IMO + FLL Clock Source. 0.3-pF sensitivity. | 5 | – | – | Ratio | 47-pF max. capacitance |
| SID313_2C | SNRC_6 | PASS Reference. IMO + FLL Clock Source. 0.6-pF sensitivity. | 5 | – | – | Ratio | 86-pF max. capacitance |
| SID313_3A | SNRC_7 | PASS Reference. IMO + PLL Clock Source. 0.1-pF sensitivity. | 5 | – | – | Ratio | 25-pF max. capacitance |
| SID313_3B | SNRC_8 | PASS Reference. IMO + PLL Clock Source. 0.3-pF sensitivity. | 5 | – | – | Ratio | 86-pF max. capacitance |
| SID313_3C | SNRC_9 | PASS Reference. IMO + PLL Clock Source. 0.6-pF sensitivity. | 5 | – | – | Ratio | 168-pF Max. capacitance |
| SID314 | $IDAC_{1CRT1}$ | Output current of IDAC1 (7 bits) in low range | 4.2 | – | 5.7 | μ A | LSB = 37.5-nA typ. |
| SID314A | $IDAC_{1CRT2}$ | Output current of IDAC1 (7 bits) in medium range | 33.7 | – | 45.6 | μ A | LSB = 300-nA typ. |
| SID314B | $IDAC_{1CRT3}$ | Output current of IDAC1 (7 bits) in high range | 270 | – | 365 | μ A | LSB = 2.4- μ A typ. |
| SID314C | $IDAC_{1CRT12}$ | Output current of IDAC1 (7 bits) in low range, 2X mode | 8 | – | 11.4 | μ A | LSB = 37.5-nA typ. 2X output stage |
| SID314D | $IDAC_{1CRT22}$ | Output current of IDAC1 (7 bits) in medium range, 2X mode | 67 | – | 91 | μ A | LSB = 300-nA typ. 2X output stage |
| SID314E | $IDAC_{1CRT32}$ | Output current of IDAC1 (7 bits) in high range, 2X mode. $V_{DDA} > 2$ V | 540 | – | 730 | μ A | LSB = 2.4- μ A typ. 2X output stage |
| SID315 | $IDAC_{2CRT1}$ | Output current of IDAC2 (7 bits) in low range | 4.2 | – | 5.7 | μ A | LSB = 37.5-nA typ. |
| SID315A | $IDAC_{2CRT2}$ | Output current of IDAC2 (7 bits) in medium range | 33.7 | – | 45.6 | μ A | LSB = 300-nA typ. |
| SID315B | $IDAC_{2CRT3}$ | Output current of IDAC2 (7 bits) in high range | 270 | – | 365 | μ A | LSB = 2.4- μ A typ. |

Table 25. CapSense Sigma-Delta (CSD) Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|----------------------------|--|-----|-----|------|-------|--|
| SID315C | IDAC ₂ CRT12 | Output current of IDAC2 (7 bits) in low range, 2X mode | 8 | – | 11.4 | μA | LSB = 37.5-nA typ. 2X output stage |
| SID315D | IDAC ₂ CRT22 | Output current of IDAC2 (7 bits) in medium range, 2X mode | 67 | – | 91 | μA | LSB = 300-nA typ. 2X output stage |
| SID315E | IDAC ₂ CRT32 | Output current of IDAC2 (7 bits) in high range, 2X mode. V _{DDA} > 2V | 540 | – | 730 | μA | LSB = 2.4-μA typ. 2X output stage |
| SID315F | IDAC ₃ CRT13 | Output current of IDAC in 8-bit mode in low range | 8 | – | 11.4 | μA | LSB = 37.5-nA typ. |
| SID315G | IDAC ₃ CRT23 | Output current of IDAC in 8-bit mode in medium range | 67 | – | 91 | μA | LSB = 300-nA typ. |
| SID315H | IDAC ₃ CRT33 | Output current of IDAC in 8-bit mode in high range. V _{DDA} > 2V | 540 | – | 730 | μA | LSB = 2.4-μA typ. |
| SID320 | IDAC _{OFFSET} | All zeroes input | – | – | 1 | LSB | Polarity set by source or sink |
| SID321 | IDAC _{GAIN} | Full-scale error less offset | – | – | ±15 | % | LSB = 2.4-μA typ. |
| SID322 | IDAC _{MIS-MATCH1} | Mismatch between IDAC1 and IDAC2 in Low mode | – | – | 9.2 | LSB | LSB = 37.5-nA typ. |
| SID322A | IDAC _{MIS-MATCH2} | Mismatch between IDAC1 and IDAC2 in Medium mode | – | – | 6 | LSB | LSB = 300-nA typ. |
| SID322B | IDAC _{MIS-MATCH3} | Mismatch between IDAC1 and IDAC2 in High mode | – | – | 5.8 | LSB | LSB = 2.4-μA typ. |
| SID323 | IDAC _{SET8} | Settling time to 0.5 LSB for 8-bit IDAC | – | – | 10 | μs | Full-scale transition. No external load. |
| SID324 | IDAC _{SET7} | Settling time to 0.5 LSB for 7-bit IDAC | – | – | 10 | μs | Full-scale transition. No external load. |
| SID325 | CMOD | External modulator capacitor. | – | 2.2 | – | nF | 5-V rating, X7R or NP0 cap. |

Table 26. CSD ADC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|--------------------------|----------------|-----------------------------------|-----|-----|-----|-------|--|
| CSDv2 ADC Specifications | | | | | | | |
| SIDA94 | A_RES | Resolution | – | – | 10 | bits | Auto-zeroing is required every milli-second |
| SID95 | A_CHNLS_S | Number of channels - single ended | – | – | – | 16 | – |
| SIDA97 | A-MONO | Monotonicity | – | – | Yes | – | V _{REF} mode |
| SIDA98 | A_GAINERR_VREF | Gain error | – | 0.6 | – | % | Reference source: SRSS (V _{REF} = 1.20 V, V _{DDA} < 2.2 V), (V _{REF} = 1.6 V, 2.2 V < V _{DDA} < 2.7 V), (V _{REF} = 2.13 V, V _{DDA} > 2.7 V) |
| SIDA98A | A_GAINERR_VDDA | Gain error | – | 0.2 | – | % | Reference source: SRSS (V _{REF} =1.20 V, V _{DDA} < 2.2V), (V _{REF} =1.6 V, 2.2 V < V _{DDA} < 2.7 V), (V _{REF} = 2.13 V, V _{DDA} > 2.7 V) |

Table 26. CSD ADC Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|---------------|--|-----------|-----|-----------|---------------|--|
| SIDA99 | A_OFFSET_VREF | Input offset voltage | – | 0.5 | – | LSB | After ADC calibration, Ref. Src = SRSS, ($V_{REF} = 1.20\text{ V}$, $V_{DDA} < 2.2\text{ V}$), ($V_{REF} = 1.6\text{ V}$, $2.2\text{ V} < V_{DDA} < 2.7\text{ V}$), ($V_{REF} = 2.13\text{ V}$, $V_{DDA} > 2.7\text{ V}$) |
| SIDA99A | A_OFFSET_VDDA | Input offset voltage | – | 0.5 | – | LSB | After ADC calibration, Ref. Src = SRSS, ($V_{REF} = 1.20\text{ V}$, $V_{DDA} < 2.2\text{ V}$), ($V_{REF} = 1.6\text{ V}$, $2.2\text{ V} < V_{DDA} < 2.7\text{ V}$), ($V_{REF} = 2.13\text{ V}$, $V_{DDA} > 2.7\text{ V}$) |
| SIDA100 | A_ISAR_VREF | Current consumption | – | 0.3 | – | mA | CSD ADC Block current |
| SIDA100A | A_ISAR_VDDA | Current consumption | – | 0.3 | – | mA | CSD ADC Block current |
| SIDA101 | A_VINS_VREF | Input voltage range - single ended | V_{SSA} | – | V_{REF} | V | ($V_{REF} = 1.20\text{ V}$, $V_{DDA} < 2.2\text{ V}$), ($V_{REF} = 1.6\text{ V}$, $2.2\text{ V} < V_{DDA} < 2.7\text{ V}$), ($V_{REF} = 2.13\text{ V}$, $V_{DDA} > 2.7\text{ V}$) |
| SIDA101A | A_VINS_VDDA | Input voltage range - single ended | V_{SSA} | – | V_{DDA} | V | ($V_{REF} = 1.20\text{ V}$, $V_{DDA} < 2.2\text{ V}$), ($V_{REF} = 1.6\text{ V}$, $2.2\text{ V} < V_{DDA} < 2.7\text{ V}$), ($V_{REF} = 2.13\text{ V}$, $V_{DDA} > 2.7\text{ V}$) |
| SIDA103 | A_INRES | Input charging resistance | – | 15 | – | k Ω | – |
| SIDA104 | A_INCAP | Input capacitance | – | 41 | – | pF | – |
| SIDA106 | A_PSR | Power supply rejection ratio (DC) | – | 60 | – | dB | – |
| SIDA107 | A_TACQ | Sample acquisition time | – | 10 | – | μs | Measured with 50- Ω source impedance. 10 μs is default software driver acquisition time setting. Settling to within 0.05%. |
| SIDA108 | A_CONV8 | Conversion time for 8-bit resolution at conversion rate = $F_{hclk} / (2^N(N + 2))$. Clock frequency = 50 MHz. | – | 25 | – | μs | Does not include acquisition time. |
| SIDA108A | A_CONV10 | Conversion time for 10-bit resolution at conversion rate = $F_{hclk} / (2^N(N + 2))$. Clock frequency = 50 MHz. | – | 60 | – | μs | Does not include acquisition time. |
| SIDA109 | A_SND_VRE | Signal-to-noise and Distortion ratio (SINAD) | – | 57 | – | dB | Measured with 50- Ω source impedance |
| SIDA109A | A_SND_VDDA | Signal-to-noise and Distortion ratio (SINAD) | – | 52 | – | dB | Measured with 50- Ω source impedance |
| SIDA111 | A_INL_VREF | Integral non-linearity. 11.6 ksps | – | – | 2 | LSB | Measured with 50- Ω source impedance |
| SIDA111A | A_INL_VDDA | Integral non-linearity. 11.6 ksps | – | – | 2 | LSB | Measured with 50- Ω source impedance |
| SIDA112 | A_DNL_VREF | Differential non-linearity. 11.6 ksps | – | – | 1 | LSB | Measured with 50- Ω source impedance |
| SIDA112A | A_DNL_VDDA | Differential non-linearity. 11.6 ksps | – | – | 1 | LSB | Measured with 50- Ω source impedance |

Digital Peripherals
Timer/Counter/PWM
Table 27. Timer/Counter/PWM (TCPWM) Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--------------|----------------|--|-----------|-----|-----|---------------|--|
| SID.TCPWM.1 | I_{TCPWM1} | Block current consumption at 8 MHz | – | – | 70 | μA | All modes (TCPWM) |
| SID.TCPWM.2 | I_{TCPWM2} | Block current consumption at 24 MHz | – | – | 180 | μA | All modes (TCPWM) |
| SID.TCPWM.2A | I_{TCPWM3} | Block current consumption at 50 MHz | – | – | 270 | μA | All modes (TCPWM) |
| SID.TCPWM.2B | I_{TCPWM4} | Block current consumption at 100 MHz | – | – | 540 | μA | All modes (TCPWM) |
| SID.TCPWM.3 | $TCPWM_{FREQ}$ | Operating frequency | – | – | 100 | MHz | Maximum = 100 MHz |
| SID.TCPWM.4 | $TPWM_{ENEXT}$ | Input trigger pulse width for all trigger events | $2/F_c$ | – | – | ns | Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected. F_c is counter operating frequency. |
| SID.TCPWM.5 | $TPWM_{EXT}$ | Output trigger pulse widths | $1.5/F_c$ | – | – | ns | Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs. F_c is counter operating frequency. |
| SID.TCPWM.5A | TC_{RES} | Resolution of counter | $1/F_c$ | – | – | ns | Minimum time between successive counts. F_c is counter operating frequency. |
| SID.TCPWM.5B | PWM_{RES} | PWM resolution | $1/F_c$ | – | – | ns | Minimum pulse width of PWM output. F_c is counter operating frequency. |
| SID.TCPWM.5C | Q_{RES} | Quadrature inputs resolution | $2/F_c$ | – | – | ns | Minimum pulse width between Quadrature phase inputs. Delays from pins should be similar. F_c is counter operating frequency. |

Serial Communication Block (SCB)
Table 28. Serial Communication Block (SCB) Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|-------------|---|-----|-----|-----|---------------|----------------------|
| Fixed I²C DC Specifications | | | | | | | |
| SID149 | I_{I2C1} | Block current consumption at 100 kHz | – | – | 30 | μA | – |
| SID150 | I_{I2C2} | Block current consumption at 400 kHz | – | – | 80 | μA | – |
| SID151 | I_{I2C3} | Block current consumption at 1 Mbps | – | – | 180 | μA | – |
| SID152 | I_{I2C4} | I ² C enabled in Deep Sleep mode | – | – | 1.7 | μA | At 60 °C. |
| Fixed I²C AC Specifications | | | | | | | |
| SID153 | F_{I2C1} | Bit rate | – | – | 1 | Mbps | – |
| Fixed UART DC Specifications | | | | | | | |
| SID160 | I_{UART1} | Block current consumption at 100 kbps | – | – | 30 | μA | – |
| SID161 | I_{UART2} | Block current consumption at 1000 kbps | – | – | 180 | μA | – |
| Fixed UART AC Specifications | | | | | | | |
| SID162A | F_{UART1} | Bit Rate | – | – | 3 | Mbps | ULP Mode |
| SID162B | F_{UART2} | | – | – | 8 | | LP Mode |

Table 28. Serial Communication Block (SCB) Specifications *(continued)*

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|--|---------------------------------|---|-----|-----|---|-------|---|
| Fixed SPI DC Specifications | | | | | | | |
| SID163 | I _{SPI1} | Block current consumption at 1 Mbps | – | – | 220 | μA | – |
| SID164 | I _{SPI2} | Block current consumption at 4 Mbps | – | – | 340 | μA | – |
| SID165 | I _{SPI3} | Block current consumption at 8 Mbps | – | – | 360 | μA | – |
| SID165A | I _{SPI4} | Block current consumption at 25 Mbps | – | – | 800 | μA | – |
| Fixed SPI AC Specifications for LP Mode (1.1 V) unless noted otherwise. | | | | | | | |
| SID166 | F _{SPI} | SPI Operating frequency externally clocked slave | – | – | 25 | MHz | 12-MHz max for ULP (0.9 V) mode |
| SID166B | F _{SPI_EXT} | SPI operating frequency master (F _{scb} is SPI clock). | – | – | F _{scb} /4 | MHz | F _{scb} max is 100 MHz in LP (1.1 V) mode, 25 MHz in ULP mode. |
| SID166A | F _{SPI_IC} | SPI slave internally clocked | – | – | 15 | MHz | 5 MHz max for ULP (0.9 V) mode |
| Fixed SPI Master mode AC Specifications for LP Mode (1.1 V) unless noted otherwise. | | | | | | | |
| SID167 | T _{DMO} | MOSI valid after SClk driving edge | – | – | 12 | ns | 20-ns max for ULP (0.9 V) mode |
| SID168 | T _{DSI} | MISO valid before SClk capturing edge | 5 | – | – | ns | Full clock, late MISO sampling |
| SID169 | T _{HMO} | MOSI data hold time | 0 | – | – | ns | Referred to Slave capturing edge |
| Fixed SPI Slave mode AC Specifications for LP Mode (1.1 V) unless noted otherwise. | | | | | | | |
| SID170 | T _{DMI} | MOSI valid before Sclck capturing edge | 5 | – | – | ns | – |
| SID171A | T _{D_{SO}_EXT} | MISO valid after Sclck driving edge in Ext. Clk. mode | – | – | 20 | ns | 35-ns max. for ULP (0.9 V) mode |
| SID171 | T _{D_{SO}} | MISO valid after Sclck driving edge in Internally Clk. mode | – | – | $\frac{T_{D_{SO_EXT}} + 3^*}{T_{SCB}}$ | ns | T _{SCB} is SCB clock period. |
| SID171B | T _{D_{SO}} | MISO Valid after Sclck driving edge in Internally Clk. Mode with median filter enabled. | – | – | $\frac{T_{D_{SO_EXT}} + 4^*}{T_{SCB}}$ | ns | T _{SCB} is SCB clock period. |
| SID172 | T _{H_{SO}} | Previous MISO data hold time | 5 | – | – | ns | – |
| SID172A | T _{SSEL_SCK1} | SSEL Valid to first SCK valid edge | 65 | – | – | ns | – |
| SID172B | T _{SSEL_SCK2} | SSEL Hold after Last SCK valid edge | 65 | – | – | ns | – |

LCD Specifications
Table 29. LCD Direct Drive DC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|-----------------------|--|-----|-----|------|-------|--------------------------|
| SID155 | C _{LCDCAP} | LCD capacitance per segment/common driver | – | 500 | 5000 | pF | – |
| SID156 | LCD _{OFFSET} | Long-term segment offset | – | 20 | – | mV | – |
| SID157 | I _{LCDDOP1} | PWM Mode current. 3.3 V bias. 8 MHz IMO. 25 °C. | – | 0.6 | – | mA | 32 × 4 segments 50 Hz |
| SID158 | I _{LCDDOP2} | PWM Mode current. 3.3 V bias. 8 MHz IMO. 25 °C. | – | 0.5 | – | mA | 32 × 4 segments 50 Hz |

Table 30. LCD Direct Drive AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------|----------------|-----|-----|-----|-------|--------------------|
| SID159 | F _{LCD} | LCD frame rate | 10 | 50 | 150 | Hz | – |

Memory
Table 31. Flash Specifications^[5]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--------------------------------|--------------------------|--|------|-----|-----|---------|------------------------------------|
| Flash DC Specifications | | | | | | | |
| SID173A | I _{PE} | Erase and program current | – | – | 6 | mA | – |
| Flash AC Specifications | | | | | | | |
| SID174 | T _{ROWWRITE} | Row write time (erase and program) | – | – | 16 | ms | Row = 512 bytes |
| SID175 | T _{ROWERASE} | Row erase time | – | – | 11 | ms | – |
| SID176 | T _{ROWPROGRAM} | Row program time after erase | – | – | 5 | ms | – |
| SID178 | T _{BULKERASE} | Bulk erase time (2048 KB) | – | – | 11 | ms | – |
| SID179 | T _{SECTORERASE} | Sector erase time (256 KB) | – | – | 11 | ms | 512 rows per sector |
| SID178S | T _{SSERIAE} | Subsector erase time | – | – | 11 | ms | 8 rows per subsector |
| SID179S | T _{SSWRITE} | Subsector write time; 1 erase plus 8 program times | – | – | 51 | ms | – |
| SID180S | T _{SWRITE} | Sector write time; 1 erase plus 512 program times | – | – | 2.6 | seconds | – |
| SID180 | T _{DEVPROG} | Total device write time | – | – | 30 | seconds | – |
| SID181 | F _{END} | Flash endurance | 100K | – | – | cycles | – |
| SID182 | F _{RET1} | Flash retention. T _A ≤ 25 °C, 100K P/E cycles | 10 | – | – | years | – |
| SID182A | F _{RET2} | Flash retention. T _A ≤ 85 °C, 10K P/E cycles | 10 | – | – | years | – |
| SID182B | F _{RET3} | Flash retention. T _A ≤ 55 °C, 20K P/E cycles | 20 | – | – | years | – |
| SID256 | T _{WS100} | Number of Wait states at 100 MHz | 3 | – | – | | LP mode. V _{CCD} = 1.1 V |
| SID257 | T _{WS50} | Number of Wait states at 50 MHz | 2 | – | – | | ULP mode. V _{CCD} = 0.9 V |

Note

5. It can take as much as 16 milliseconds to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

System Resources
Table 32. System Resources

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--|------------------------|--|------|------|------|-------|--|
| Power-On-Reset with Brown-out DC Specifications | | | | | | | |
| Precise POR (PPOR) | | | | | | | |
| SID190 | V _{FALLPPOR} | BOD trip voltage in Active and Sleep modes. V _{DDD} . | 1.54 | – | – | V | BOD reset guaranteed for levels below 1.54 V |
| SID192 | V _{FALLDPSLP} | BOD trip voltage in Deep Sleep. V _{DDD} . | 1.54 | – | – | V | – |
| SID192A | V _{DDRAMP} | Maximum power supply ramp rate (any supply) | – | – | 100 | mV/μs | Active mode |
| POR with Brown-out AC Specification | | | | | | | |
| SID194A | V _{DDRAMP_DS} | Maximum power supply ramp rate (any supply) in Deep Sleep | – | – | 10 | mV/μs | BOD operation guaranteed |
| Voltage Monitors DC Specifications | | | | | | | |
| SID195 | V _{HVDI1} | – | 1.38 | 1.43 | 1.47 | V | – |
| SID196 | V _{HVDI2} | – | 1.57 | 1.63 | 1.68 | V | – |
| SID197 | V _{HVDI3} | – | 1.76 | 1.83 | 1.89 | V | – |
| SID198 | V _{HVDI4} | – | 1.95 | 2.03 | 2.1 | V | – |
| SID199 | V _{HVDI5} | – | 2.05 | 2.13 | 2.2 | V | – |
| SID200 | V _{HVDI6} | – | 2.15 | 2.23 | 2.3 | V | – |
| SID201 | V _{HVDI7} | – | 2.24 | 2.33 | 2.41 | V | – |
| SID202 | V _{HVDI8} | – | 2.34 | 2.43 | 2.51 | V | – |
| SID203 | V _{HVDI9} | – | 2.44 | 2.53 | 2.61 | V | – |
| SID204 | V _{HVDI10} | – | 2.53 | 2.63 | 2.72 | V | – |
| SID205 | V _{HVDI11} | – | 2.63 | 2.73 | 2.82 | V | – |
| SID206 | V _{HVDI12} | – | 2.73 | 2.83 | 2.92 | V | – |
| SID207 | V _{HVDI13} | – | 2.82 | 2.93 | 3.03 | V | – |
| SID208 | V _{HVDI14} | – | 2.92 | 3.03 | 3.13 | V | – |
| SID209 | V _{HVDI15} | – | 3.02 | 3.13 | 3.23 | V | – |
| SID211 | LVI_IDD | Block current | – | 5 | 15 | μA | – |
| Voltage Monitors AC Specification | | | | | | | |
| SID212 | T _{MONTRIP} | Voltage monitor trip time | – | – | 170 | ns | – |

SWD Interface
Table 33. SWD and Trace Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|--------------------------------|--------------|---|------------|-----|-----------|-------|---|
| SWD and Trace Interface | | | | | | | |
| SID214 | F_SWDCLK2 | $1.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | – | – | 25 | MHz | LP Mode. $V_{CCD} = 1.1\text{ V}$. |
| SID214L | F_SWDCLK2L | $1.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | – | – | 12 | MHz | ULP Mode. $V_{CCD} = 0.9\text{ V}$. |
| SID215 | T_SWDI_SETUP | $T = 1/f\text{ SWDCLK}$ | $0.25 * T$ | – | – | ns | – |
| SID216 | T_SWDI_HOLD | $T = 1/f\text{ SWDCLK}$ | $0.25 * T$ | – | – | ns | – |
| SID217 | T_SWDO_VALID | $T = 1/f\text{ SWDCLK}$ | – | – | $0.5 * T$ | ns | – |
| SID217A | T_SWDO_HOLD | $T = 1/f\text{ SWDCLK}$ | 1 | – | – | ns | – |
| SID214T | F_TRCLK_LP1 | With Trace Data setup/hold times of 2/1 ns respectively | – | – | 50 | MHz | LP Mode. $V_{DD} = 1.1\text{ V}$. |
| SID215T | F_TRCLK_LP2 | With Trace Data setup/hold times of 3/2 ns respectively | – | – | 50 | MHz | LP Mode. $V_{DD} = 1.1\text{ V}$. |
| SID216T | F_TRCLK_ULP | With Trace Data setup/hold times of 3/2 ns respectively | – | – | 20 | MHz | ULP Mode. $V_{DD} = 0.9\text{ V}$. |

Internal Main Oscillator
Table 34. IMO DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|--------------------------------|-----|-----|-----|-------|--------------------|
| SID218 | I _{IMO1} | IMO operating current at 8 MHz | – | 9 | 15 | μA | – |

Table 35. IMO AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|----------------------|---------------------------------------|-----|-----|-----|-------|--------------------|
| SID223 | F _{IMOTOL1} | Frequency variation centered on 8 MHz | – | – | ±2 | % | – |
| SID227 | T _{JITR} | Cycle-to-cycle and period jitter | – | 250 | – | ps | – |

Internal Low-Speed Oscillator
Table 36. ILO DC Specification

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|---------------------------------|-----|-----|-----|-------|--------------------|
| SID231 | I _{ILO2} | ILO operating current at 32 kHz | – | 0.3 | 0.7 | μA | – |

Table 37. ILO AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------------|------------------|------|-----|------|-------|--|
| SID234 | T _{STARTILO1} | ILO startup time | – | – | 7 | μs | Startup time to 95% of final frequency |
| SID236 | TLIODUTY | ILO duty cycle | 45 | 50 | 55 | % | – |
| SID237 | F _{ILOTRIM1} | ILO frequency | 28.8 | 32 | 36.1 | kHz | Factory trimmed |

Crystal Oscillator Specifications
Table 38. ECO Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|----------------------------------|---------------------|---|-----|--------|------|-------|---|
| MHz ECO DC Specifications | | | | | | | |
| SID316 | I _{DD_MHz} | Block operating current with Clload up to 18 pF | – | 800 | 1600 | μA | Max = 35 MHz, Typ = 16 MHz |
| MHz ECO AC Specifications | | | | | | | |
| SID317 | F_MHz | Crystal frequency range | 16 | – | 35 | MHz | Some restrictions apply. Refer to the device TRM . |
| kHz ECO DC Specifications | | | | | | | |
| SID318 | I _{DD_kHz} | Block operating current with 32-kHz crystal | – | 0.38 | 1 | μA | – |
| SID321E | ESR32K | Equivalent series resistance | – | 80 | – | kΩ | – |
| SID322E | PD32K | Drive level | – | – | 1 | μW | – |
| kHz ECO AC Specifications | | | | | | | |
| SID319 | F_kHz | 32 kHz frequency | – | 32.768 | – | kHz | – |
| SID320 | T _{on_kHz} | Startup time | – | – | 500 | ms | – |
| SID320E | F _{TOL32K} | Frequency tolerance | – | 50 | 250 | ppm | – |

External Clock Specifications
Table 39. External Clock Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------------|---|-----|-----|-----|-------|--------------------|
| SID305 | EXTCLK _{FREQ} | External clock input frequency | 0 | – | 100 | MHz | – |
| SID306 | EXTCLK _{DUTY} | Duty cycle; measured at V _{DD/2} | 45 | – | 55 | % | – |

PLL Specifications
Table 40. PLL Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------|---------------------------------|--------|------|-----|-------|--------------------------|
| SID304P | PLL_IN | Input frequency to PLL block | 4 | – | 64 | MHz | |
| SID305P | PLL_LOCK | Time to achieve PLL lock | – | 16 | 35 | μs | – |
| SID306P | PLL_OUT | Output frequency from PLL block | 10.625 | – | 150 | MHz | – |
| SID307P | PLL_IDD | PLL current | – | 0.55 | 1.1 | mA | Typ. at 100 MHz out. |
| SID308P | PLL_JTR | Period jitter | – | – | 150 | ps | 100 MHz output frequency |

Table 41. Clock Source Switching Time

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------------|--|-----|-----|-----------------|---------|--------------------|
| SID262 | TCLK _{SWITCH} | Clock switching from clk1 to clk2 in clock periods; for example, from IMO (clk1) to FLL (clk2). ^[6] | – | – | 4 clk1 + 3 clk2 | periods | – |

Note

6. As an example, if the clk_path[1] source is changed from the IMO to the FLL (see [Figure 3](#)) then clk1 is the IMO and clk2 is the FLL.

FLL Specifications
Table 42. Frequency Locked Loop (FLL) Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---------|---------------|--|-------|-----|--------|--------|---|
| SID450 | FLL_RANGE | Input frequency range. | 0.001 | – | 100 | MHz | Lower limit allows lock to USB SOF signal (1 kHz). Upper limit is for External input. |
| SID451 | FLL_OUT_DIV2 | Output frequency range. V _{CCD} = 1.1 V | 24.00 | – | 100.00 | MHz | Output range of FLL divided-by-2 output |
| SID451A | FLL_OUT_DIV2 | Output frequency range. V _{CCD} = 0.9 V | 24.00 | – | 50.00 | MHz | Output range of FLL divided-by-2 output |
| SID452 | FLL_DUTY_DIV2 | Divided-by-2 output; High or Low | 47.00 | – | 53.00 | % | – |
| SID454 | FLL_WAKEUP | Time from stable input clock to 1% of final value on Deep Sleep wakeup | – | – | 7.50 | μs | With IMO input, less than 10 °C change in temperature while in Deep Sleep, and Fout ≥ 50 MHz. |
| SID455 | FLL_JITTER | Period jitter (1 sigma) at 100 MHz | – | – | 35.00 | ps | 50 ps at 48 MHz, 35 ps at 100 MHz |
| SID456 | FLL_CURRENT | CCO + Logic current | – | – | 5.50 | μA/MHz | – |

USB
Table 43. USB Specifications (USB requires LP Mode 1.1-V internal supply)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------------------------------|-----------------|---|-------|-----|------|-------|---|
| USB Block Specifications | | | | | | | |
| SID322U | Vusb_3.3 | Device supply for USB operation | 3.15 | – | 3.6 | V | USB Configured |
| SID323U | Vusb_3 | Device supply for USB operation (functional operation only) | 2.85 | – | 3.6 | V | USB Configured |
| SID325U | Iusb_config | Block supply current in Active mode | – | 8 | – | mA | V _{DDD} = 3.3 V |
| SID328 | Iusb_suspend | Block supply current in suspend mode | – | 0.5 | – | mA | V _{DDD} = 3.3 V, Device connected |
| SID329 | Iusb_suspend | Block supply current in suspend mode | – | 0.3 | – | mA | V _{DDD} = 3.3 V, Device disconnected |
| SID330U | USB_Drive_Res | USB driver impedance | 28 | – | 44 | Ω | Series resistors are on chip |
| SID331U | USB_Pulldown | USB pull-down resistors in Host mode | 14.25 | – | 24.8 | kΩ | – |
| SID332U | USB_Pullup_Idle | Idle mode range | 900 | – | 1575 | Ω | Bus idle |
| SID333U | USB_Pullup | Active mode | 1425 | – | 3090 | Ω | Upstream device transmitting |

QSPI

Table 44. QSPI Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|--|---------------|---|---------|-----|------|-------|--|
| SMIF QSPI Specifications. All specs with 15-pF load. Measured from 50% to 50% waveform transitions. | | | | | | | |
| SID390Q | Fsmifclock | SMIF QSPI output clock frequency | – | – | 80 | MHz | LP mode (1.1 V) |
| SID390QU | Fsmifclocku | SMIF QSPI output clock frequency | – | – | 50 | MHz | ULP mode (0.9 V). Guaranteed by Char. |
| SID397Q | Idd_qspi | Block current in LP mode (1.1 V) | – | – | 1900 | μA | LP mode (1.1 V) |
| SID398Q | Idd_qspi_u | Block current in ULP mode (0.9 V) | – | – | 590 | μA | ULP mode (0.9 V) |
| SID391Q | Tsetup | Input data set-up time with respect to clock capturing falling edge | 4.5 | – | – | ns | Guaranteed by characterization |
| SID392Q | Tdatahold | Input data hold time with respect to clock capturing falling edge | 1 | – | – | ns | – |
| SID393Q | Tdataoutvalid | Output data valid time with respect to clock falling edge | – | – | 3.7 | ns | 7.5-ns max for ULP mode (0.9 V) |
| SID394Q | Tholdtime | Output data hold time with respect to clock rising edge | 3 | – | – | ns | – |
| SID395Q | Tseloutvalid | Output Select valid time with respect to clock rising edge | – | – | 7.5 | ns | 15-ns max for ULP mode (0.9 V) |
| SID396Q | Tselouthold | Output Select hold time with respect to clock rising edge | Tsclk/2 | – | – | ns | Tsclk = Fsmifclk cycle time |

Audio Subsystem

Table 45. Audio Subsystem Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---------------------------|-------------|---|-------|-------|--------|-------|--------------------------------------|
| PDM Specifications | | | | | | | |
| SID400P | PDM_IDD1 | PDM Active current, stereo operation, 1-MHz clock | – | 175 | – | μA | 16-bit audio at 16 ksps |
| SID401 | PDM_IDD2 | PDM Active current, stereo operation, 3-MHz clock | – | 600 | – | μA | 24-bit audio at 48 ksps |
| SID402 ^[6] | PDM_JITTER | RMS jitter in PDM clock | –200 | – | 200 | ps | – |
| SID403 ^[6] | PDM_CLK | PDM clock speed | 0.384 | – | 3.072 | MHz | – |
| SID403A ^[6] | PDM_BLK_CLK | PDM block input clock | 1.024 | – | 49.152 | MHz | – |
| SID403B ^[6] | PDM_SETUP | Data input set-up time to PDM_CLK edge | 10 | – | – | ns | – |
| SID403C ^[6] | PDM_HOLD | Data input hold time to PDM_CLK edge | 10 | – | – | ns | – |
| SID404 ^[6] | PDM_OUT | Audio sample rate | 8 | – | 48 | ksps | – |
| SID405 ^[6] | PDM_WL | Word length | 16 | – | 24 | bits | – |
| SID406 ^[6] | PDM_SNR | Signal-to-Noise Ratio (A-weighted) | – | 100 | – | dB | PDM input, 20 Hz to 20 kHz BW |
| SID407 ^[6] | PDM_DR | Dynamic range (A-weighted) | – | 100 | – | dB | 20 Hz to 20 kHz BW, -60 dB FS |
| SID408 ^[6] | PDM_FR | Frequency response | –0.2 | – | 0.2 | dB | DC to 0.45f, DC Blocking filter off. |
| SID409 ^[6] | PDM_SB | Stop band | – | 0.566 | – | f | – |

Note

6. Guaranteed by design, not production tested.

Table 45. Audio Subsystem Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|--------------|--|-----------------------------|-----|--------------------------|-------|--|
| SID410 ^[6] | PDM_SBA | Stop band attenuation | – | 60 | – | dB | – |
| SID411 ^[6] | PDM_GAIN | Adjustable gain | –12 | – | 10.5 | dB | PDM to PCM, 1.5 dB/step |
| SID412 ^[6] | PDM_ST | Startup time | – | 48 | – | | Word Select (WS) cycles |
| I2S Specifications. The same for LP and ULP modes unless stated otherwise. | | | | | | | |
| SID415 | I2S_IDD | Block current | – | 400 | – | μA | |
| SID413 | I2S_WORD | Length of I2S Word | 8 | – | 32 | bits | |
| SID414 | I2S_WS | Word clock frequency in LP mode | – | – | 192 | kHz | 12.288-MHz bit clock with 32-bit word |
| SID414M | I2S_WS_U | Word clock frequency in ULP mode | – | – | 48 | kHz | 3.072-MHz bit clock with 32-bit word |
| SID414A | I2S_WS_TDM | Word clock frequency in TDM mode for LP | – | – | 48 | kHz | Eight 32-bit channels |
| SID414X | I2S_WS_TDM_U | Word clock frequency in TDM mode for ULP | – | – | 12 | kHz | Eight 32-bit channels |
| I2S Slave Mode | | | | | | | |
| SID430 | TS_WS | WS setup time to the following rising edge of SCK for LP mode | 5 | – | – | ns | – |
| SID430U | TS_WS_U | WS setup time to the following rising edge of SCK for ULP mode | 11 | – | – | ns | – |
| SID430A | TH_WS | WS hold time to the following edge of SCK | $T_{MCLK_SOC}^{[7]}$ +5 | – | – | ns | – |
| SID432 | TD_SDO | Delay time of TX_SDO transition from edge of TX_SCK for LP mode | $-(T_{MCLK_SOC}$ +25) | – | T_{MCLK_S} $OC+25$ | ns | Associated clock edge depends on selected polarity |
| SID432U | TD_SDO_U | Delay time of TX_SDO transition from edge of TX_SCK for ULP mode | $-(T_{MCLK_SOC}$ +70) | – | T_{MCLK_S} $OC+70$ | ns | Associated clock edge depends on selected polarity |
| SID433 | TS_SDI | RX_SDI setup time to the following edge of RX_SCK in LP mode | 5 | – | – | ns | – |
| SID433U | TS_SDI_U | RX_SDI setup time to the following edge of RX_SCK in ULP mode | 11 | – | – | ns | – |
| SID434 | TH_SDI | RX_SDI hold time to the rising edge of RX_SCK | $T_{MCLK_SOC}^{+}$ 5 | – | – | ns | – |
| SID435 | TSCKCY | TX/RX_SCK bit clock duty cycle | 45 | – | 55 | % | – |
| I2S Master Mode | | | | | | | |
| SID437 | TD_WS | WS transition delay from falling edge of SCK in LP mode | –10 | – | 20 | ns | – |
| SID437U | TD_WS_U | WS transition delay from falling edge of SCK in ULP mode | –10 | – | 40 | ns | – |
| SID438 | TD_SDO | SDO transition delay from falling edge of SCK in LP mode | –10 | – | 20 | ns | – |
| SID438U | TD_SDO | SDO transition delay from falling edge of SCK in ULP mode | –10 | – | 40 | ns | – |

Note

 7. T_{MCLK_SOC} is the internal I2S master clock period.

Table 45. Audio Subsystem Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|-------------|--|------------------------|-----|--------|-------|--|
| SID439 | TS_SDI | SDI setup time to the associated edge of SCK | 5 | – | – | ns | Associated clock edge depends on selected polarity |
| SID440 | TH_SDI | SDI hold time to the associated edge of SCK | $T_{MCLK_SOC}^+$ 5 | – | – | ns | T is TX/RX_SCK Bit Clock period. Associated clock edge depends on selected polarity. |
| SID443 | TSCKCY | SCK bit clock duty cycle | 45 | – | 55 | % | – |
| SID445 | FMCLK_SOC | MCLK_SOC frequency in LP mode | 1.024 | – | 98.304 | MHz | FMCLK_SOC = 8*Bit-clock |
| SID445U | FMCLK_SOC_U | MCLK_SOC frequency in ULP mode | 1.024 | – | 24.576 | MHz | FMCLK_SOC_U = 8 * Bit-clock |
| SID446 | TMCLKCY | MCLK_SOC duty cycle | 45 | – | 55 | % | – |
| SID447 | TJITTER | MCLK_SOC input jitter | –100 | – | 100 | ps | – |

Smart I/O

Table 46. Smart I/O Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|----------|-----------|--------------------------|-----|-----|-----|-------|--------------------|
| SID420 | SMIO_BYP | Smart I/O bypass delay | – | – | 2 | ns | – |
| SID421 | SMIO_LUT | Smart I/O LUT prop delay | – | 8 | – | ns | – |

SD Host Controller and eMMC

Table 47. SD Host Controller and eMMC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|------------|--|-----|-----|-----|-------|--------------------------------|
| SD Host Controller and eMMC Specifications (SD Host clock (see the Clocking Diagram) must be divided by 2 or more when used as source in DDR modes. Specifications are Guaranteed by Design. | | | | | | | |
| SID_SD390 | SD_DS | I/O drive select | 4 | – | 4 | mA | drive_sel = '01' for all modes |
| SID_SD391 | SD_TR | Input transition time | 0.7 | – | 3 | ns | – |
| SD:DS Timing | | | | | | | |
| SID_SD392 | SD_CLK | Interface clock period (LP mode) | – | – | 25 | MHz | (40-ns period) |
| SID_SD393 | SD_CLK | Interface clock period (ULP mode) | – | – | 8 | MHz | (125-ns period) |
| SID_SD394 | SD_DCMD_CL | I/O loading at DATA/CMD pins | – | 30 | – | pF | – |
| SID_SD395 | SD_CLK_CL | I/O loading at CLK pins | – | 30 | – | pF | – |
| SID_SD396 | SD_TS_OUT | Output: Setup time of CMD/DAT prior to CLK | 5.1 | – | – | ns | – |
| SID_SD397 | SD_HLD_OUT | Output: Hold time of CMD/DAT after CLK | 5.1 | – | – | ns | – |
| SID_SD398 | SD_TS_IN | Input: Setup time of CMD/DAT prior to CLK (LP mode) | 24 | – | – | ns | – |
| SID_SD399 | SD_TS_IN | Input: Setup time of CMD/DAT prior to CLK (ULP mode) | 109 | – | – | ns | – |
| SID_SD400 | SD_HLD_IN | Input: Hold time of CMD/DAT after CLK | 2.1 | – | – | ns | – |
| SD:HS Timing | | | | | | | |
| SID_SD401 | SD_CLK | Interface clock period (LP mode) | – | – | 45 | MHz | (20-ns period) |
| SID_SD402 | SD_CLK | Interface clock period (ULP mode) | – | – | 16 | MHz | (62.5-ns period) |

Table 47. SD Host Controller and eMMC Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|-------------------------|------------|--|------|-----|-----|-------|----------------------|
| SID_SD403 | SD_DCMD_CL | I/O loading at DATA/CMD pins | – | 30 | – | pF | – |
| SID_SD404 | SD_CLK_CL | I/O loading at CLK pins | – | 30 | – | pF | – |
| SID_SD405 | SD_TS_OUT | Output: Setup time of CMD/DAT prior to CLK | 6.1 | – | – | ns | – |
| SID_SD406 | SD_HLD_OUT | Output: Hold time of CMD/DAT after CLK | 2.1 | – | – | ns | – |
| SID_SD407 | SD_TS_IN | Input: Setup time of CMD/DAT prior to CLK (LP mode) | 8 | – | – | ns | – |
| SID_SD408 | SD_TS_IN | Input: Setup time of CMD/DAT prior to CLK (ULP mode) | 48 | – | – | ns | – |
| SID_SD409 | SD_HLD_IN | Input: Hold time of CMD/DAT after CLK | 2.5 | – | – | ns | – |
| SD:SDR-12 Timing | | | | | | | |
| SID_SD410 | SD_CLK | Interface clock period (LP mode) | – | – | 25 | MHz | (40-ns period) |
| SID_SD411 | SD_CLK | Interface clock period (ULP mode) | – | – | 8 | MHz | (125-ns period) |
| SID_SD412 | SD_CLK_DC | Duty cycle of output CLK | 30 | – | 70 | % | – |
| SID_SD413 | SD_DCMD_CL | I/O loading at DATA/CMD pins | – | 30 | – | pF | – |
| SID_SD414 | SD_CLK_CL | I/O loading at CLK pins | – | 30 | – | pF | – |
| SID_SD415 | SD_TS_OUT | Output: Setup time of CMD/DAT prior to CLK | 3.1 | – | – | ns | – |
| SID_SD416 | SD_HLD_OUT | Output: Hold time of CMD/DAT after CLK | 0.9 | – | – | ns | – |
| SID_SD417 | SD_TS_IN | Input: Setup time of CMD/DAT prior to CLK (LP mode) | 24 | – | – | ns | – |
| SID_SD418 | SD_TS_IN | Input: Setup time of CMD/DAT prior to CLK (ULP mode) | 109 | – | – | ns | – |
| SID_SD419 | SD_HLD_IN | Input: Hold time of CMD/DAT after CLK | 1.85 | – | – | ns | – |
| SD:SDR-25 Timing | | | | | | | |
| SID_SD420 | SD_CLK | Interface clock period (LP mode) | – | – | 50 | MHz | (20-ns period) |
| SID_SD421 | SD_CLK | Interface clock period (ULP mode) | – | – | 16 | MHz | (62.5-ns period) |
| SID_SD422 | SD_CLK_DC | Duty cycle of output CLK | 30 | – | 70 | % | – |
| SID_SD423 | SD_DCMD_CL | I/O loading at DATA/CMD pins | – | 30 | – | pF | – |
| SID_SD424 | SD_CLK_CL | I/O loading at CLK pins | – | 30 | – | pF | – |
| SID_SD425 | SD_TS_OUT | Output: Setup time of CMD/DAT prior to CLK | 3.1 | – | – | ns | – |
| SID_SD426 | SD_HLD_OUT | Output: Hold time of CMD/DAT after CLK | 0.9 | – | – | ns | – |
| SID_SD427 | SD_TS_IN | Input: Setup time of CMD/DAT prior to CLK (LP mode) | 5.8 | – | – | ns | – |
| SID_SD428 | SD_TS_IN | Input: Setup time of CMD/DAT prior to CLK (ULP mode) | 48 | – | – | ns | – |
| SID_SD429 | SD_HLD_IN | Input: Hold time of CMD/DAT after CLK | 1.8 | – | – | ns | – |
| SD:SDR-50 Timing | | | | | | | |
| SID_SD430 | SD_CLK | Interface clock period (LP mode) | – | – | 80 | MHz | (12.5-ns period) |

Table 47. SD Host Controller and eMMC Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|-------------------------|------------|--|------|-----|-----|-------|----------------------|
| SID_SD431 | SD_CLK | Interface clock period (ULP mode) | – | – | 32 | MHz | (31.25-ns period) |
| SID_SD432 | SD_CLK_DC | Duty cycle of output CLK | 30 | – | 70 | % | – |
| SID_SD433 | SD_DCMD_CL | I/O loading at DATA/CMD pins | – | 20 | – | pF | – |
| SID_SD434 | SD_CLK_CL | I/O loading at CLK pins | – | 20 | – | pF | – |
| SID_SD435 | SD_TS_OUT | Output: Setup time of CMD/DAT prior to CLK | 3.1 | – | – | ns | – |
| SID_SD436 | SD_HLD_OUT | Output: Hold time of CMD/DAT after CLK | 0.9 | – | – | ns | – |
| SID_SD437 | SD_TS_IN | Input: Setup time of CMD/DAT prior to CLK (LP mode) | 5 | – | – | ns | – |
| SID_SD438 | SD_TS_IN | Input: Setup time of CMD/DAT prior to CLK (ULP mode) | 23 | – | – | ns | – |
| SID_SD439 | SD_HLD_IN | Input: Hold time of CMD/DAT after CLK | 1.8 | – | – | ns | – |
| SD:DDR-50 Timing | | | | | | | |
| SID_SD440 | SD_CLK | Interface clock period (LP mode) | – | – | 40 | MHz | (25-ns period). |
| SID_SD441 | SD_CLK | Interface clock period (ULP mode) | – | – | 16 | MHz | (62.5-ns period) |
| SID_SD442 | SD_CLK_DC | Duty cycle of output CLK | 45 | – | 55 | % | – |
| SID_SD443 | SD_DCMD_CL | I/O loading at DATA/CMD pins | – | 30 | – | pF | – |
| SID_SD444 | SD_CLK_CL | I/O loading at CLK pins | – | 30 | – | pF | – |
| SID_SD445 | SD_TS_OUT | Output: Setup time of CMD/DAT prior to CLK | 3.1 | – | – | ns | – |
| SID_SD446 | SD_HLD_OUT | Output: Hold time of CMD/DAT after CLK | 0.9 | – | – | ns | – |
| SID_SD447 | SD_TS_IN | Input: Setup time of CMD/DAT prior to CLK (LP mode) | 5.75 | – | – | ns | – |
| SID_SD448 | SD_TS_IN | Input: Setup time of CMD/DAT prior to CLK (ULP mode) | 24 | – | – | ns | – |
| SID_SD449 | SD_HLD_IN | Input: Hold time of CMD/DAT after CLK | 1.8 | – | – | ns | – |
| eMMC:BWC Timing | | | | | | | |
| SID_SD450 | SD_CLK | Interface clock period (LP mode) | – | – | 26 | MHz | (38.4-ns period) |
| SID_SD451 | SD_CLK | Interface clock period (ULP mode) | – | – | 8 | MHz | (125-ns period) |
| SID_SD452 | SD_DCMD_CL | I/O loading at DATA/CMD pins | – | 30 | – | pF | – |
| SID_SD453 | SD_CLK_CL | I/O loading at CLK pins | – | 30 | – | pF | – |
| SID_SD454 | SD_TS_OUT | Output: Setup time of CMD/DAT prior to CLK | 3.1 | – | – | ns | – |
| SID_SD455 | SD_HLD_OUT | Output: Hold time of CMD/DAT after CLK | 3.1 | – | – | ns | – |
| SID_SD456 | SD_TS_IN | Input: Setup time of CMD/DAT prior to CLK (LP mode) | 9.7 | – | – | ns | – |
| SID_SD457 | SD_TS_IN | Input: Setup time of CMD/DAT prior to CLK (ULP mode) | 96 | – | – | ns | – |
| SID_SD458 | SD_HLD_IN | Input: Hold time of CMD/DAT after CLK | 8.3 | – | – | ns | – |

Table 47. SD Host Controller and eMMC Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|------------------------------------|------------|--|-----|------|-----|-------|----------------------|
| eMMC:SDR Timing | | | | | | | |
| SID_SD459 | SD_CLK | Interface clock period (LP mode) | – | – | 52 | MHz | (19.2-ns period) |
| SID_SD460 | SD_CLK | Interface clock period (ULP mode) | – | – | 16 | MHz | (62.5-ns period) |
| SID_SD461 | SD_DCMD_CL | I/O loading at DATA/CMD pins | – | 30 | – | pF | – |
| SID_SD462 | SD_CLK_CL | I/O loading at CLK pins | – | 30 | – | pF | – |
| SID_SD463 | SD_TS_OUT | Output: Setup time of CMD/DAT prior to CLK | 3.1 | – | – | ns | – |
| SID_SD464 | SD_HLD_OUT | Output: Hold time of CMD/DAT after CLK | 3.1 | – | – | ns | – |
| SID_SD465 | SD_TS_IN | Input: Setup time of CMD/DAT prior to CLK (LP mode) | 5.3 | – | – | ns | – |
| SID_SD466 | SD_TS_IN | Input: Setup time of CMD/DAT prior to CLK (ULP mode) | 48 | – | – | ns | – |
| SID_SD467 | SD_HLD_IN | Input: Hold time of CMD/DAT after CLK | 2.5 | – | – | ns | – |
| SD Host Block Current Specs | | | | | | | |
| SID_SD400SD | IDD_SD_1 | SD Host block current consumption at 100 MHz | – | 4.65 | 5 | mA | – |
| SID_SD401SD | IDD_SD_2 | SD Host block current consumption at 50 MHz | – | 3.75 | 4.3 | mA | – |

JTAG Boundary Scan
Table 48. JTAG Boundary Scan

| Spec ID# | Parameter | Description | Min | Typ | Max | Units |
|--|-----------|--|-----|-----|-----|-------|
| JTAG Boundary Scan Parameters | | | | | | |
| JTAG Boundary Scan Parameters for 1.1 V (LP) Mode Operation: | | | | | | |
| SID468 | TCKLOW | TCK LOW | 52 | – | – | ns |
| SID469 | TCKHIGH | TCK HIGH | 10 | – | – | ns |
| SID470 | TCK_TDO | TCK falling edge to output valid | – | 40 | – | ns |
| SID471 | TSU_TCK | Input valid to TCK rising edge | 12 | – | – | ns |
| SID472 | Tck_THD | Input hold time to TCK rising edge | 10 | – | – | ns |
| SID473 | TCK_TDOV | TCK falling edge to output valid (High-Z to Active). | 40 | – | – | ns |
| SID474 | TCK_TDOZ | TCK falling edge to output valid (Active to High-Z). | 40 | – | – | ns |
| JTAG Boundary Scan Parameters for 0.9 V (ULP) Mode Operation: | | | | | | |
| SID468A | TCKLOW | TCK low | 102 | – | – | ns |
| SID469A | TCKHIGH | TCK high | 20 | – | – | ns |
| SID470A | TCK_TDO | TCK falling edge to output valid | – | 80 | – | ns |
| SID471A | TSU_TCK | Input valid to TCK rising edge | 22 | – | – | ns |
| SID472A | Tck_THD | Input hold time to TCK rising edge | 20 | – | – | ns |
| SID473A | TCK_TDOV | TCK falling edge to output valid (high-Z to active). | 80 | – | – | ns |
| SID474A | TCK_TDOZ | TCK falling edge to output valid (active to high-Z). | 80 | – | – | ns |

Ordering Information

Table 49 lists the CYB0644xxZI-S2D44 part numbers and features. See also the [product selector guide](#).

Table 49. Ordering Information

| Family | Base Features | MPN | CM4 CPU Speed (LP/U LP) | CM0+ CPU Speed (LP/U LP) | Power Modes | Flash (KB) | SRAM (KB) | CapSense | Crypto | GPIO | Pin | Package |
|--------|---|-------------------|-------------------------|--------------------------|-------------|------------|-----------|----------|--------|------|-----|---------|
| 64 | Arm CM4/CM0+, DC-DC converter 12-bit SAR ADC, 2 LPCOMPs, 13 SCBs, 32 TCPWMs, 2 I2S, 2 PDM, 2 SD Host Controllers, USB-FS | CYB0644ABZI-S2D44 | 150/50 | 100/25 | FLEX | 2048 | 1024 | Y | Y | 100 | 124 | BGA |

PSoC 6 MPN Decoder
CY XX 6 A B C DD E - FF G H I JJ K L

| Field | Description | Values | Meaning | Field | Description | Values | Meaning | | |
|-------|--------------------------|------------|-------------------------|------------------|-------------------------------|--------|-------------------------------|-------|------------------------|
| CY | Cypress | CY | Cypress | E | Temperature Range | C | Consumer | | |
| XX | Firmware | 8C | Standard | | | I | Industrial | | |
| | | B0 | "Secure Boot" v1 | | | Q | Extended Industrial | | |
| | | S0 | "Standard Secure" - AWS | Cypress internal | | | | | |
| 6 | Architecture | 6 | PSoC 6 | FF | Feature Code | S2-S6 | Integrated Bluetooth LE | | |
| A | Line | 0 | Value | | | F | Single Core | | |
| | | 1 | Programmable | D | Dual Core | | | | |
| | | 2 | Performance | H | Attributes Code | 0-9 | Feature set | | |
| | | 3 | Connectivity | | | I | GPIO count | 1 | 31-50 |
| | | 4 | Secured | | | | | 2 | 51-70 |
| B | Speed | 2 | 100 MHz | 3 | 71-90 | | | | |
| | | 3 | 150 MHz | 4 | 91-110 | | | | |
| | | 4 | 150/50 MHz | JJ | Engineering sample (optional) | ES | Engineering samples or not | | |
| C | Memory Size (Flash/SRAM) | 0-3 | Reserved | | | K | Die Revision (optional) | | Base |
| | | 4 | 256K/128K | | | | | A1-A9 | Die revision |
| | | 5 | 512K/256K | | | L | Tape/Reel Shipment (optional) | T | Tape and Reel shipment |
| | | 6 | 512K/128K | | | | | | |
| | | 7 | 1024K/288K | | | | | | |
| | | 8 | 1024K/512K | | | | | | |
| | | 9 | Reserved | | | | | | |
| | | A | 2048K/1024K | | | | | | |
| DD | Package | AZ, AX | TQFP | | | | | | |
| | | LQ | QFN | | | | | | |
| | | BZ | BGA | | | | | | |
| | | FM | M-CSP | | | | | | |
| | | FN, FD, FT | WLCSP | | | | | | |

Packaging

This product line is offered in a 124-BGA package.

Table 50. Package Dimensions

| Spec ID# | Package | Description | Package Dwg # |
|----------|---------|---|---------------|
| PKG_1 | 124-BGA | 124 BGA, 9 mm × 9 mm × 1 mm height with 0.65-mm pitch | 001-97718 |

Table 51. Package Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|-----------------|---------------------------------|------------|-----|------|-----|---------|
| T _A | Operating ambient temperature | – | –40 | 25 | 85 | °C |
| T _J | Operating junction temperature | – | –40 | – | 100 | °C |
| T _{JA} | Package θ_{JA} (124-BGA) | – | – | 31.9 | – | °C/watt |
| T _{JC} | Package θ_{JC} (124-BGA) | – | – | 11 | – | °C/watt |

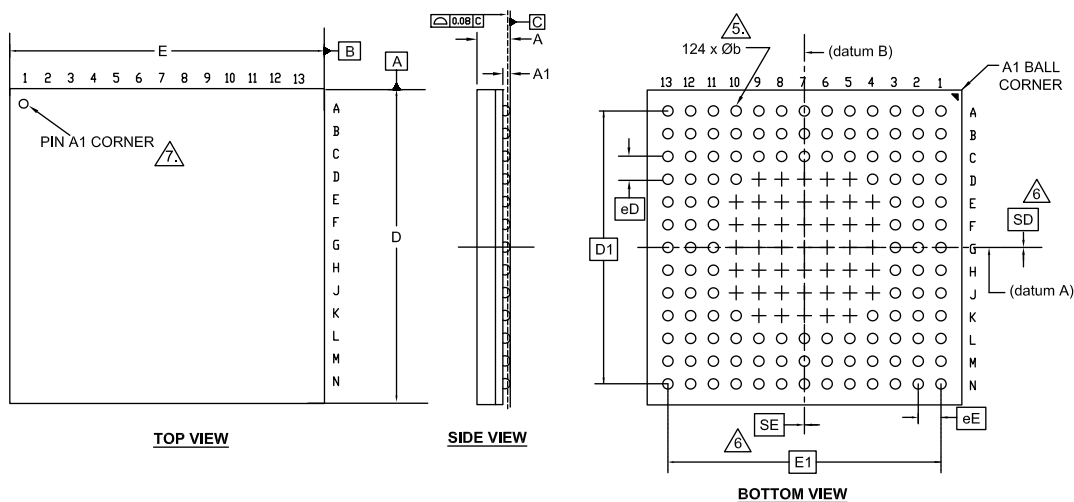
Table 52. Solder Reflow Peak Temperature

| Package | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|--------------|--------------------------|----------------------------------|
| All packages | 260 °C | 30 seconds |

Table 53. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

| Package | MSL |
|---------|-------|
| 124-BGA | MSL 3 |

Figure 17. 124-BGA 9.0 × 9.0 × 1.0 mm



| SYMBOL | DIMENSIONS | | |
|--------|------------|------|------|
| | MIN. | NOM. | MAX. |
| A | - | - | 1.00 |
| A1 | 0.16 | 0.21 | 0.26 |
| D | 8.90 | 9.00 | 9.10 |
| E | 8.90 | 9.00 | 9.10 |
| D1 | 7.80 BSC | | |
| E1 | 7.80 BSC | | |
| MD | 13 | | |
| ME | 13 | | |
| N | 124 | | |
| ∅ b | 0.25 | 0.30 | 0.35 |
| eD | 0.65 BSC | | |
| eE | 0.65 BSC | | |
| SD | 0 | | |
| SE | 0 | | |

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS.
- SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
- "e" REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
- JEDEC SPECIFICATION NO. REF. : MO-280.

001-97718 *B

Acronyms

| Acronym | Description |
|---------|---|
| 3DES | triple DES (data encryption standard) |
| ADC | analog-to-digital converter |
| ADMA3 | advanced DMA version 3, a Secure Digital data transfer mode |
| AES | advanced encryption standard |
| AHB | AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus |
| AMUX | analog multiplexer |
| AMUXBUS | analog multiplexer bus |
| API | application programming interface |
| Arm® | advanced RISC machine, a CPU architecture |
| BGA | ball grid array |
| BOD | brown-out detect |
| BREG | backup registers |
| BWC | backward compatibility (eMMC data transfer mode) |
| CAD | computer aided design |
| CCO | current controlled oscillator |
| ChaCha | a stream cipher |
| CM0+ | Cortex-M0+, an Arm CPU |
| CM4 | Cortex-M4, an Arm CPU |
| CMAC | cypher-based message authentication code |
| CMOS | complementary metal-oxide-semiconductor, a process technology for IC fabrication |
| CMRR | common-mode rejection ratio |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| CSD | CapSense Sigma-Delta |
| CSV | clock supervisor |
| CSX | Cypress mutual capacitance sensing method. See also CSD |
| CTI | cross trigger interface |
| DAC | digital-to-analog converter, see also IDAC, VDAC |
| DAP | debug access port |
| DDR | double data rate |
| DES | data encryption standard |
| DFT | design for test |
| DMA | direct memory access, see also TD |
| DNL | differential nonlinearity, see also INL |
| DSI | digital system interconnect |
| DU | data unit |
| ECC | error correcting code |
| ECC | elliptic curve cryptography |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| EMI | electromagnetic interference |
| eMMC | embedded MultiMediaCard |

| Acronym | Description |
|--------------------------|---|
| ESD | electrostatic discharge |
| ETM | embedded trace macrocell |
| FIFO | first-in, first-out |
| FLL | frequency locked loop |
| FPU | floating-point unit |
| FS | full-speed |
| GND | Ground |
| GPIO | general-purpose input/output, applies to a PSoC pin |
| HMAC | Hash-based message authentication code |
| HSIOM | high-speed I/O matrix |
| I/O | input/output, see also GPIO, DIO, SIO, USBIO |
| I ² C, or IIC | Inter-Integrated Circuit, a communications protocol |
| I ² S | inter-IC sound |
| IC | integrated circuit |
| IDAC | current DAC, see also DAC, VDAC |
| IDE | integrated development environment |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| INL | integral nonlinearity, see also DNL |
| IOSS | input output subsystem |
| IoT | internet of things |
| IPC | inter-processor communication |
| IRQ | interrupt request |
| ISR | interrupt service routine |
| ITM | instrumentation trace macrocell |
| JTAG | Joint Test Action Group |
| LCD | liquid crystal display |
| LIN | Local Interconnect Network, a communications protocol |
| LP | low power |
| LS | low-speed |
| LUT | lookup table |
| LVD | low-voltage detect, see also LVI |
| LVI | low-voltage interrupt |
| LVTTTL | low-voltage transistor-transistor logic |
| MAC | multiply-accumulate |
| MCU | microcontroller unit |
| MCWDT | multi-counter watchdog timer |
| MISO | master-in slave-out |
| MMIO | memory-mapped input output |
| MOSI | master-out slave-in |
| MPU | memory protection unit |
| MSL | moisture sensitivity level |
| MSPS | million samples per second |
| MTB | micro trace buffer |
| MUL | multiplier |

| Acronym | Description |
|---------|--|
| NC | no connect |
| NMI | nonmaskable interrupt |
| NVIC | nested vectored interrupt controller |
| NVL | nonvolatile latch, see also WOL |
| OTP | one-time programmable |
| OVP | over voltage protection |
| OVT | overvoltage tolerant |
| PASS | programmable analog subsystem |
| PCB | printed circuit board |
| PCM | pulse code modulation |
| PDM | pulse density modulation |
| PHY | physical layer |
| PICU | port interrupt control unit |
| PLL | phase-locked loop |
| PMIC | power management integrated circuit |
| POR | power-on reset |
| PPU | peripheral protection unit |
| PRNG | pseudo random number generator |
| PSoC® | Programmable System-on-Chip™ |
| PSRR | power supply rejection ratio |
| PWM | pulse-width modulator |
| QD | quadrature decoder |
| QSPI | quad serial peripheral interface |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| ROM | read-only memory |
| RSA | Rivest–Shamir–Adleman, a public-key cryptography algorithm |
| RTC | real-time clock |
| RWW | read-while-write |
| RX | receive |
| S/H | sample and hold |
| SAR | successive approximation register |
| SARMUX | SAR ADC multiplexer bus |
| SC/CT | switched capacitor/continuous time |
| SCB | serial communication block |
| SCL | I ² C serial clock |
| SD | Secure Digital |
| SDA | I ² C serial data |
| SDR | single data rate |
| Sflash | supervisory flash |
| SHA | secure hash algorithm |
| SINAD | signal to noise and distortion ratio |
| SMPU | shared memory protection unit |
| SNR | signal-to-noise ratio |
| SOF | start of frame |

| Acronym | Description |
|---------|--|
| SONOS | silicon-oxide-nitride-oxide-silicon, a flash memory technology |
| SPI | Serial Peripheral Interface, a communications protocol |
| SRAM | static random access memory |
| SROM | supervisory read-only memory |
| SRSS | system resources subsystem |
| SWD | serial wire debug, a test protocol |
| SWJ | serial wire JTAG |
| SWO | single wire output |
| SWV | single-wire viewer |
| TCPWM | timer, counter, pulse-width modulator |
| TDM | time division multiplexed |
| THD | total harmonic distortion |
| TQFP | thin quad flat package |
| TRM | technical reference manual |
| TRNG | true random number generator |
| TX | transmit |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UDB | universal digital block |
| ULP | ultra-low power |
| USB | Universal Serial Bus |
| WCO | watch crystal oscillator |
| WDT | watchdog timer |
| WIC | wakeup interrupt controller |
| WLCSP | wafer level chip scale package |
| XIP | execute-in-place |
| XRES | external reset input pin |

Document Conventions

Units of Measure

Table 54. Units of Measure

| Symbol | Unit of Measure |
|--------|------------------------|
| °C | degrees Celsius |
| dB | decibel |
| fF | femto farad |
| Hz | hertz |
| KB | 1024 bytes |
| kbps | kilobits per second |
| hr | hour |
| KHz | kilohertz |
| kΩ | kilo ohm |
| ksps | kilosamples per second |
| LSB | least significant bit |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msps | megasamples per second |
| μA | microampere |
| μF | microfarad |

Table 54. Units of Measure *(continued)*

| Symbol | Unit of Measure |
|--------|----------------------|
| μH | microhenry |
| μs | microsecond |
| μV | microvolt |
| μW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| nV | nanovolt |
| W | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| sps | samples per second |
| sqrtHz | square root of hertz |
| V | volt |

Errata

This section describes the errata for the CYB0644xxZI-S2D44 product line. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Compare this document to the device's datasheet for a complete functional description.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

| Part Number | Device Characteristics |
|-------------------|--------------------------------|
| CYB0644xxZI-S2D44 | CYB0644xxZI-S2D44 Product Line |

Qualification Status

Engineering Samples

Errata Summary

This table defines the errata applicability to available PSoC 6 CYB0644xxZI-S2D44 devices.

| Items | PSoC CYB0644xxZI-S2D44 | Silicon Revision | Fix Status |
|---------------------------------------|---------------------------|--------------------|------------------------------|
| [1.]DMA controllers are not available | All | Production silicon | Resolution planned by Q4 '22 |

| 1. DMA controllers are not available | |
|--------------------------------------|--|
| Problem Definition | The two 29-channel DMA controllers are not available. Register access to these controllers is not available. The 4-channel controller is available; there are no USB or audio connections to it. |
| Parameters Affected | The two 29-channel DMA controllers |
| Trigger Condition(s) | Attempt to use either of the 29-channel DMA controllers, by accessing their registers |
| Scope of Impact | CPU exceptions are generated |
| Workaround | Use the 4-channel controller for DMA operations |
| Fix Status | Investigation underway. Fix planned by Q3'21. |

Revision History

| Description Title: PSoC 6 MCU: CYB0644xxZI-S2D44 Datasheet Document Number: 002-28802 | | | |
|--|---------|-----------------|--|
| Revision | ECN | Submission Date | Description of Change |
| ** | 6711017 | 10/24/2019 | New datasheet |
| *A | 6776273 | 01/16/2020 | Updated Features . Updated Blocks and Functionality and Functional Description . Updated Pinouts and Power Supply Considerations . Updated Packaging . |
| *B | 6854009 | 04/17/2020 | Updated Features . Updated Functional Description . Updated SAR ADC 1 Msps references to 2 Msps. Removed reference to e.MMC DDR mode Updated Pinouts . Updated Electrical Specifications . Edited SAR Specs to split V _{DDA} dependent specs into separate specs instead of having qualifying comments. Also moved Supply Range specs from Description column to Details/Conditions column. Added SAR ADC 2 Msps supply current specs. Updated SAR ADC input impedance RC values to support 9RC 2 Msps sampling. Updated PSoC 6 MPN Decoder . |
| *C | 6891487 | 06/11/2020 | Updated Development Ecosystem , GPIO , and LCD sections. Added External Crystal Oscillators . |
| *D | 6973720 | 10/09/2020 | Updated Flexible Clocking Options and Block Diagram . Updated list of application notes and links in PSoC 6 MCU Resources . Updated ModusToolbox Software . Updated amount of available SRAM in Features , Blocks and Functionality , Memory , Table 4 and Ordering Information . Updated Clocking Diagram . Updated the PSoC 64 Security section. Deleted the 128-TQFP package. Deleted the "Ports 9 and 10" row from Table 6 . Updated Power Supply Considerations . Updated CPUs and added InterProcessor Communication (IPC) . Updated Analog Subsystem diagram. Removed 128-TQFP package information. Update the XRES bullet in Reset , SID15 Description and Conditions , and System Resources (Power-On-Reset specifications). Updated SD Host Controllers and SD Host Controller and eMMC Specifications . Updated description and conditions for SID262 and SID237. Updated SID7A conditions, SID7C description, and SID8 conditions. Integrated ECO erratum into External Crystal Oscillators . Added ECO Usage Guidelines table. Added footnote to TMCLK_SOC specs. Updated Errata . |

Description Title: PSoC 6 MCU: CYB0644xxZI-S2D44 Datasheet
Document Number: 002-28802

| | | | |
|----|---------|------------|---|
| *E | 7147463 | 06/01/2021 | <p>Changed BLE references to Bluetooth LE.</p> <p>Updated Security terminology to Infineon standards.</p> <p>Added Table 12 and Figure 16 in Electrical Specifications.</p> <p>Removed SIDDS1 and SIDDS1_B and updated Typ values for SIDDS2 and SIDDS2_B.</p> <p>Corrected typo in Ordering Information.</p> <p>Errata: Added "DMA controllers are not available" and deleted erratum "Cryptographic SysCall API version".</p> |
| *F | 7231613 | 08/18/2021 | <p>Updated SIDDS2 - Corrected Deep Sleep current values</p> <p>Removed "System Deep Sleep power higher than specification" errata item.</p> |
| *G | 7469751 | 11/24/2021 | <p>Removed Preliminary tag from the datasheet.</p> <p>Updated SIDC1 description.</p> <p>Updated details/conditions for SID7A.</p> <p>Updated SID325U, SID328, and SID329 description.</p> <p>Updated Errata.</p> |
| *H | 7787179 | 10/26/2022 | <p>Added device identification and revision information in Features.</p> <p>Added spec SID415 and SID304P.</p> <p>Added footnote "Guaranteed by design, not production tested" for specs SID402 - SID412.</p> <p>Updated Clock System and PLL Specifications.</p> <p>Updated Protection Units.</p> |

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