ISL24201

Programmable VCOM Calibrator with EEPROM

FN7586
Rev 1.00
December 9, 2010

The ISL24201 provides an 8-bit programmable current sink that is used in conjunction with an external voltage divider and buffer amplifier to generate a voltage source that is positioned between the analog supply voltage and ground. The current sink's resolution is controlled by an external resistor, R_{SET}, and the span of the V_{COM} voltage is controlled by the voltage divider resistor ratio and the source impedance of R_1 and R_2. This device has an 8-bit data register and 8-bit EEPROM for storing a volatile and a permanent value for its output. The ISL24201 has an I^2C bus interface that is used to read and write to its registers and EEPROM. At power-up the EEPROM value is transferred to the data register and output.

The ISL24201 is available in an 8 Ld 3mm x 3mm TDFN package. This package has a maximum height of 0.8mm for very low profile designs. The ambient operating temperature range is
-40°C to +85°C.

Features

- 8-bit, 256-Step, Adjustable Sink Current Output
- 4.5V to 18V Analog Supply Voltage Operating Range
- 2.25V to 3.6V Logic Supply Voltage Operating Range
- 400kHz, I^2C Interface
- On-Chip 8-Bit EEPROM
- Output Guaranteed Monotonic Over-Temperature
- Pb-free (RoHS-compliant)

Applications

- LCD Panel V_{COM} Generator
- Electrophoretic Display V_{COM} Generator
- Resistive Sensor Driver
- Low Power Current Loop

Related Literature

- See AN1621 for ISL24201 Evaluation Board Application Note "ISL24201IRTZ-EVALZ Evaluation Board User Guide"

Typical Application

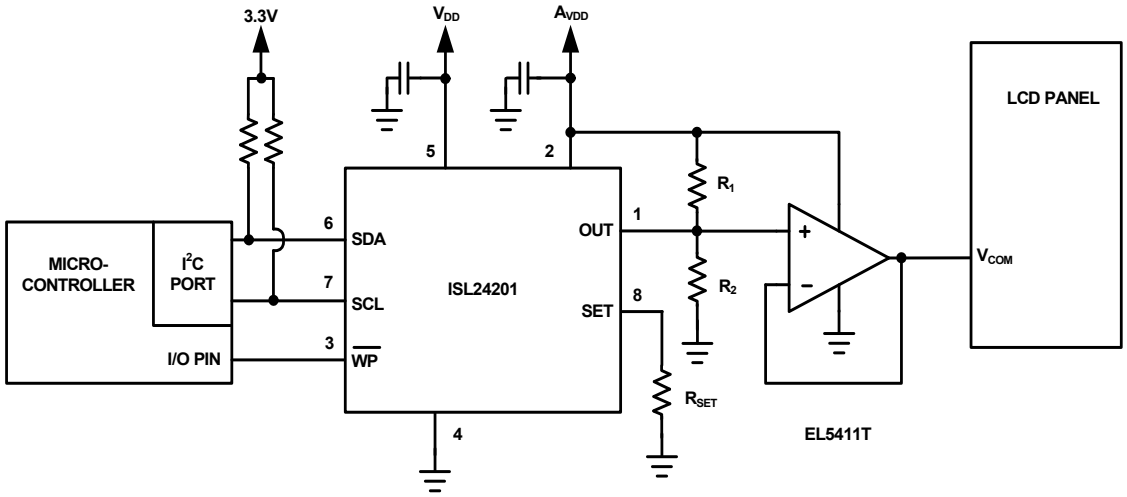


FIGURE 1. APPLICATION SHOWING ISL24201 WITH A BUFFER AMPLIFIER

Block Diagram

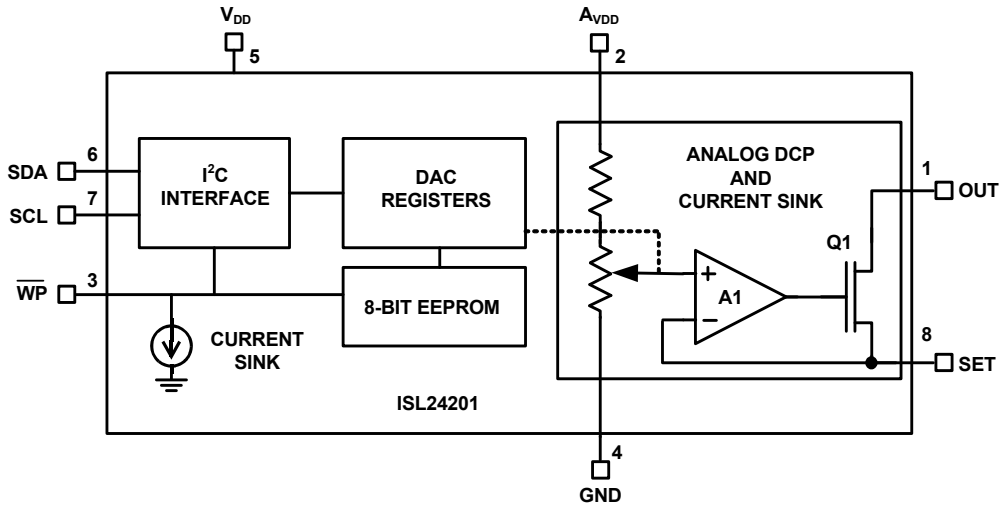
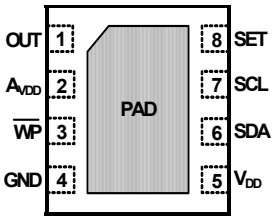


FIGURE 2. BLOCK DIAGRAM OF THE ISL24201

Pin Configuration

ISL24201
(8 LD TDFN)
TOP VIEW



(THERMAL PAD CONNECTS TO GND)

Pin Descriptions

PIN NAME	PIN NUMBER	FUNCTION
OUT	1	Adjustable Sink Current Output Pin. The current sunk into the OUT pin is equal to the DAC setting times the maximum adjustable sink current divided by 256. See the “SET” pin function description below (pin 8) for the maximum adjustable sink current setting.
A_{VDD}	2	High-Voltage Analog Supply. Bypass to GND with 0.1µF capacitor.
WP	3	EEPROM Write Protect. Active Low. 0 = Programming disabled; 1 = Programming allowed. This pin has an internal pull-down current sink
GND	4	Ground connection.
V_{DD}	5	System power supply input. Bypass to GND with 0.1µF capacitor.
SDA	6	I^2C Serial Data Input and Output
SCL	7	I^2C Clock Input
SET	8	Maximum Sink Current Adjustment Point. Connect a resistor from SET to GND to set the maximum adjustable sink current of the OUT pin. The maximum adjustable sink current is equal to (A_{VDD}/20) divided by R_{SET}.
PAD	-	Thermal pad should be connected to system ground plane to optimize thermal performance.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	INTERFACE	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL24201IRTZ	201Z	I^2C	-40 to +85	8 Ld 3x3 TDFN	L8.3x3A
ISL24201IRTZ-EVALZ	Evaluation Board				

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page ISL24201. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

Supply Voltage
- A_{VDD} to GND 20V
- V_{DD} to GND 4V

Input Voltage with respect to Ground
- SET 4V
- SCL, SDA and WP . . . . . V_{DD}+0.3V

Output Voltage with respect to Ground
- OUT . . . . . A_{VDD}

Continuous Output Current
- OUT 5mA

ESD Ratings
- Human Body Model (Tested per JESD22-A114) 7kV
- Machine Model (Tested per JESD22-A115) 250V
- Charged Device Model (Tested per JESD22-C101) 1.5kV

Latch Up (Tested per JESD 78, Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld TDFN Package (Notes 4, 5)	53	11

Moisture Sensitivity (see Technical Brief TB363)
- All Packages . . . . . Level 1

Maximum Die Temperature . . . . . +150°C

Storage Temperature . . . . . -65°C to +150°C

Pb-free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Operating Range
- A_{VDD} . . . . . 4.5V to 19V
- V_{DD} . . . . . 2.25V to 3.6V

Ambient Operating Temperature . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Test Conditions: V_{DD} = 3.3V, A_{VDD} = 18V, R_{SET} = 5kΩ, R_1 = 10kΩ, R_2 = 10kΩ, (See Figure 5); unless otherwise specified. Typicals are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
DC CHARACTERISTICS						
V_{DD}	V_{DD} Supply Range - Operating		**2.25**		**3.6**	V
A_{VDD}	A_{VDD} Supply Range Supporting EEPROM Programming		**10.8**		**19**	V
A_{VDD}	A_{VDD} Supply Range for Wide-Supply Operation (not supporting EEPROM Programming)		**4.5**		**19**	V
I_{DD}	V_{DD} Supply Current	$\overline{WP}$ = SCL = SDA = V_{DD}		37	**65**	µA
I_{AVDD}	A_{VDD} Supply Current	$\overline{WP}$ = SCL = SDA = V_{DD}		24	**38**	µA
OUT CHARACTERISTICS						
SET_{ZSE}	SET Zero-Scale Error				±**3**	LSB
SET_{FSE}	SET Full-Scale Error				±**8**	LSB
V_{OUT}	OUT Voltage Range	I_{OUT} < 0.5mA	V_{SET} + **0.4**		A_{VDD}	V
SET_{VD}	SET Voltage Drift			7		µV/°C
I_{OUT}	Maximum OUT Sink Current			4		mA
INL	Integral Non-Linearity				±**2**	LSB
DNL	Differential Non-Linearity				±**1**	LSB
I^2C INPUTS AND OUTPUT						
I^2CV_{IH}	SDA, SCL Logic 1 Input Voltage		**1.44**			V
I^2CV_{IL}	SDA, SCL Logic 0 Input Voltage				**0.55**	V
I^2C_H	SDA, SCL Hysteresis			260		mV
I_L	Input Leakage Current of SDA, SCL				±**1**	µA
VOL_S	SDA Output Logic Low	I = -3mA			**0.4**	V
V_{IH}	$\overline{WP}$ Input Logic High		**0.7V_{DD}**			V
V_{IL}	$\overline{WP}$ Input Logic Low				**0.3V_{DD}**	V
$V_{\overline{WP}H}$	$\overline{WP}$ Input Hysteresis			260		mV
$IL_{\overline{WP}N}$	$\overline{WP}$ Input Leakage Current		**-0.20**	-0.5	**-1**	µA

Electrical Specifications Test Conditions: V_{DD} = 3.3V, A_{VDD} = 18V, R_{SET} = 5kΩ, R_1 = 10kΩ, R_2 = 10kΩ, (See Figure 5); unless otherwise specified. Typicals are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
I²C TIMING						
f_{CLK}	I²C Clock Frequency				400	kHz
t_{SCH}	I²C Clock High Time		0.6			µs
t_{SCL}	I²C Clock Low Time		1.3			µs
t_{DSP}	I²C Spike Rejection Filter Pulse Width		0		50	ns
t_{SDS}	I²C Data Set Up Time		250			ns
t_{SDH}	I²C Data Hold Time		250			ns
t_{BUF}	I²C Time Between Stop and Start		200			µs
t_{STS}	I²C Repeated Start Condition Set-up		0.6			µs
t_{STH}	I²C Repeated Start Condition Hold		0.6			µs
t_{SPS}	I²C Stop Condition Set-up		0.6			µs
C_{SDA}	SDA Pin Capacitance				10	pF
C_S	SCL Pin Capacitance				10	pF
t_W	EEPROM Write Cycle Time				100	ms

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Application Information

The ISL24201 provides the ability to adjust the V_{COM} voltage during production test and alignment, under digital control, to minimize the flicker of an LCD panel. A digitally controlled potentiometer (DCP), with 256 steps of resolution, adjusts the sink current of the OUT pin. Figure 3 shows the V_{COM} adjustment using a mechanical potentiometer circuit and the equivalent circuit replacement with the ISL24201.

The output is connected to an external voltage divider, as shown in Figure 3, so that the ISL24201 will have the ability to reduce the voltage on the output by increasing the OUT pin sink current. The amount of current sunk is controlled by the I²C serial interface.

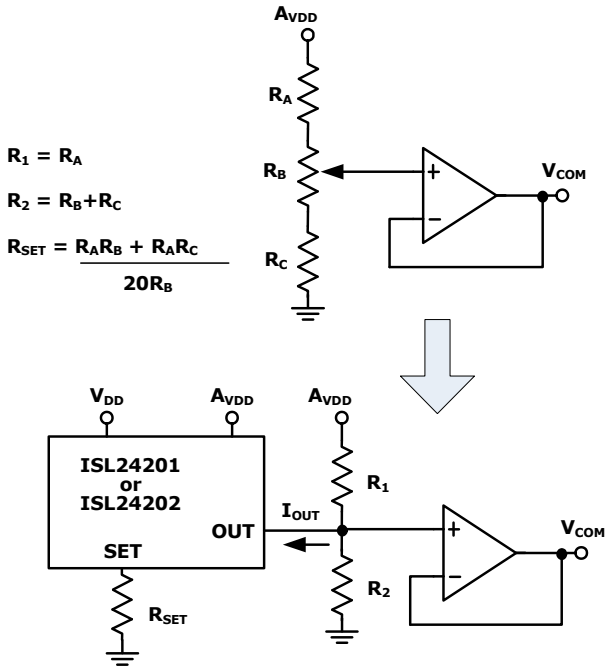


FIGURE 3. MECHANICAL ADJUSTMENT REPLACEMENT

DCP (Digitally Controlled Potentiometer)

Figure 4 shows the relationship between the register value and the resistor string of the DCP. Note that the register value of zero actually selects the first step of the resistor string. The output voltage of the DCP is given by Equation 1:

$$V_{DCP} = \left(\frac{RegisterValue + 1}{256}\right)\left(\frac{A_{VDD}}{20}\right) \quad \text{(EQ. 1)}$$

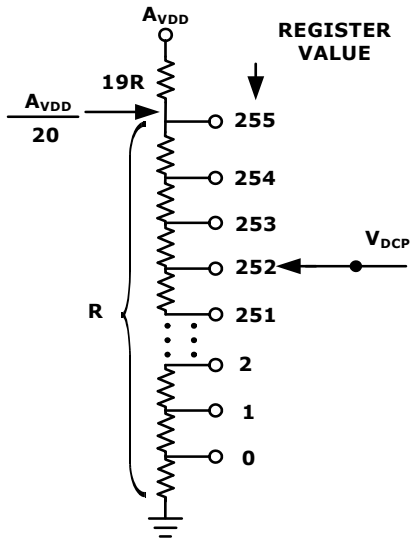


FIGURE 4. SIMPLIFIED SCHEMATIC OF DIGITAL CONTROL POTENTIOMETER (DCP)

Output Current Sink

Figure 5 shows the schematic of the OUT pin current sink. The circuit made up of amplifier A1, transistor Q1, and resistor R_{SET} forms a voltage controlled current source.

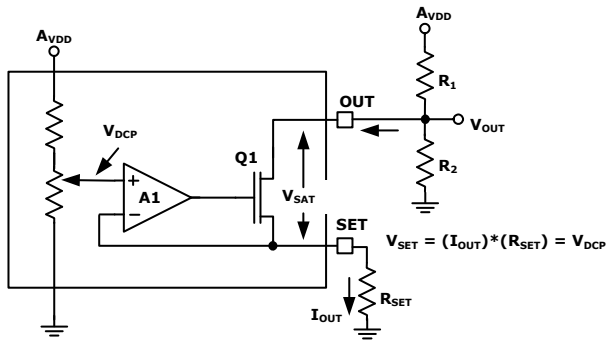


FIGURE 5. CURRENT SINK CIRCUIT

The external R_{SET} resistor sets the full-scale sink current that determines the lowest output voltage of the external voltage divider R_1 and R_2. I_{OUT} is calculated as shown by Equation 2:

$$I_{OUT} = \frac{V_{DCP}}{R_{SET}} = \left(\frac{RegisterValue + 1}{256}\right)\left(\frac{A_{VDD}}{20}\right)\left(\frac{1}{R_{SET}}\right) \quad \text{(EQ. 2)}$$

The maximum value of I_{OUT} can be calculated by substituting the maximum register value of 255 into Equation 2, resulting in Equation 3:

$$I_{OUT(MAX)} = \frac{A_{VDD}}{20R_{SET}} \quad \text{(EQ. 3)}$$

Equation 2 can also be used to calculate the unit sink current step size by removing the Register Value term from it as shown in Equation 4.

$$I_{STEP} = \frac{A_{VDD}}{(256)(20)(R_{SET})} \quad \text{(EQ. 4)}$$

The voltage difference between the OUT pin and SET pin, which are also the drain and source of the output transistor, should be greater than the minimum saturation voltage for the $I_{OUT(MAX)}$ being used. This will keep the output transistor in its saturation region to maintain linear operation over the full range of register values.

Figure 6 shows I_{DS} vs V_{DS} for transistor Q1. The line labeled "Minimum Saturation Voltage" is the minimum voltage that should be maintained across the drain and source of Q1. To find the minimum saturation voltage for a specific condition, locate the voltage at the intersection of the $I_{OUT(MAX)}$ value from Equation 3 and the line labeled "Minimum Saturation Voltage".

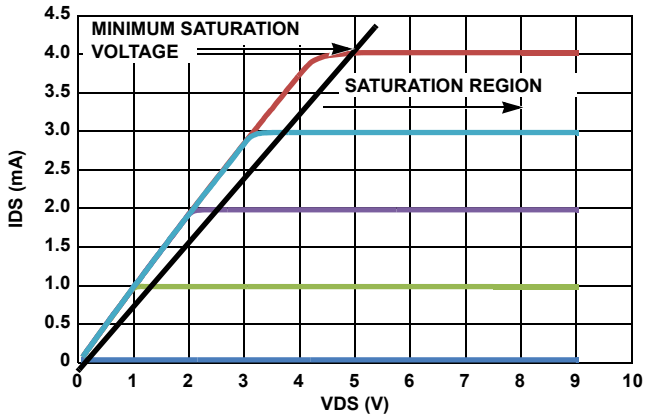


FIGURE 6. I_{DS} vs V_{DS} FOR THE ISL24201 OUTPUT TRANSISTOR

The maximum voltage on the SET pin is $A_{VDD}/20$ and is added to the minimum voltage difference between the V_{OUT} and SET pins to calculate the minimum V_{OUT} voltage, as shown in Equation 5.

$$V_{OUT}(MIN) \geq \frac{A_{VDD}}{20} + MinimumSaturationVoltage \quad \text{(EQ. 5)}$$

Output Voltage

The output voltage, V_{OUT}, of the OUT pin can be calculated from Equation 6:

$$V_{OUT} = A_{VDD}\left(\frac{R_2}{R_1+R_2}\right)\left(1-\frac{RegisterValue+1}{256}\left(\frac{R_1}{20R_{SET}}\right)\right) \quad \text{(EQ. 6)}$$

While Equation 6 can be used to calculate the output voltage, it does not help select the values of R_1, R_2 and R_{SET} to obtain a specific range of V_{COM} voltages.

Output Voltage Span Calculation

The span of the output voltage is typically centered around the nominal V_{COM} voltage value, which is typically near half of the A_{VDD} voltage. The high V_{COM} voltage occurs with the register value of zero, while the low V_{COM} voltage occurs with the register value of 255. Figure 7 shows the definition of several terms used later in the text.

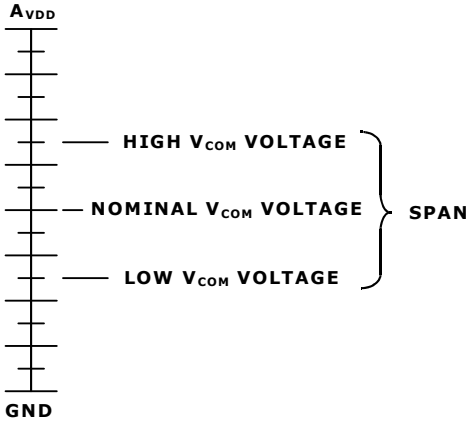


FIGURE 7. VOLTAGE LEVELS FOR V_{COM}

There are three variables that control the V_{COM} calibrator's operating point; the span of the V_{COM} voltage, the maximum current sink and the source impedance of the resistive divider.

Figure 8 shows a range of operating points for these three variables and a quick way to estimate a specific operating point. The X-axis is the span of the V_{COM} voltage (High V_{COM} Voltage - Low V_{COM} Voltage), and the Y-axis is the maximum sink current set by R_{SET}. The individual plots of each R_{TH} show the V_{COM} span plotted against the maximum OUT sink current given that value of source impedance of the voltage divider. R_{TH} is the Thevenin equivalent resistance of the voltage divider R_1 and R_2, which is the resistance of the parallel combination of R_1 and R_2, as shown in Equation 7.

$$R_{TH} = \frac{R_1R_2}{R_1+R_2} \quad \text{(EQ. 7)}$$

The span of the V_{COM} voltage is shown by Equation 8.

$$V_{COM}SPAN = I_{SET}(R_{TH}) \quad \text{(EQ. 8)}$$

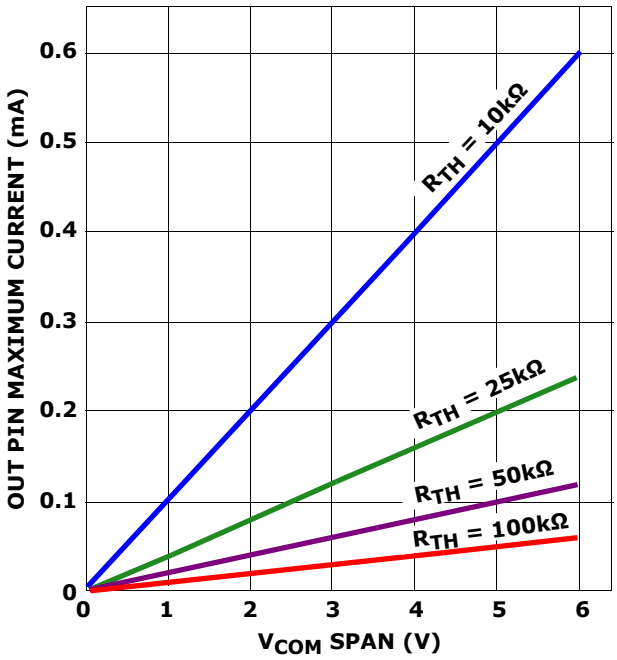


FIGURE 8. GRAPH of V_{COM} SPAN vs MAXIMUM OUTCURRENT AND R_{TH}

To make a final selection of the resistor values for R_1 and R_2, The supply voltage A_{VDD} and the value of R_{SET} are specified. The calculations for R_1 and R_2 are shown in Equations 9 and 10:

$$R_1 = \frac{40R_{SET}(SPAN)}{A_{VDD}+SPAN} \quad \text{(EQ. 9)}$$

$$R_2 = \frac{40R_{SET}(SPAN)}{A_{VDD}-SPAN} \quad \text{(EQ. 10)}$$

The R_1 and R_2 calculations are based on the span of the V_{COM} voltage being centered at half the A_{VDD} voltage.

As an example, A_{VDD} = 15V, the maximum value for I_{SET} is selected to be 100µA and the required span is 2V. Using Figure 8 as a guide, the V_{COM} maximum is equal to 8.5V and the V_{COM} minimum is equal to 6.5V. Rearranging equation and calculation the value of R_{SET}:

$$R_{SET} = \frac{A_{VDD}}{20I_{OUT}(MAX)} = \frac{15}{20(0.000100)} = 7500\Omega \quad \text{(EQ. 11)}$$

Calculating the value of R_1 is shown in Equation 12.

$$R_1 = \frac{40(7500)(2)}{15+2} = 39.29k\Omega \quad \text{(EQ. 12)}$$

Calculating the value of R_2 is shown in Equation 13.

$$R_2 = \frac{40(7500)(2)}{15-2} = 46.15k\Omega \quad \text{(EQ. 13)}$$

Table 1 shows the calculated results of the V_{COM} voltage with these values.

TABLE 1. EXAMPLE V_{OUT} vs REGISTER VALUE

REGISTER VALUE	V_{OUT} (V)
0	8.49
20	8.34
40	8.18
60	8.02
80	7.87
100	7.71
120	7.55
127	7.50
140	7.40
160	7.24
180	7.09
200	6.93
220	6.77
240	6.62
255	6.50

Figure 6 is used to find the minimum saturation voltage for an I_{OUT} maximum of 100µA, which is about 0.3V. The minimum V_{OUT} is 6.5V, which also meets the minimum V_{OUT} - V_{SET} requirements specified in Equation 14:

$$V_{OUT}MIN = 6.5V > \frac{15V}{20} + 0.3V = 1.05V \quad \text{(EQ. 14)}$$

OUT Pin Leakage Current

When the voltage on the OUT pin is greater than 10V, there is a leakage current flowing into the pin in addition to the I_{SET} current. Figure 9 shows the I_{SET} current and the OUT pin current for OUT pin voltage up to 19V. In applications where the voltage on the OUT pin will be greater than 10V, the actual output voltage will be lower than the voltage calculated by Equation 6. The graph in Figure 9 was measured with R_{SET} = 4.99kΩ.

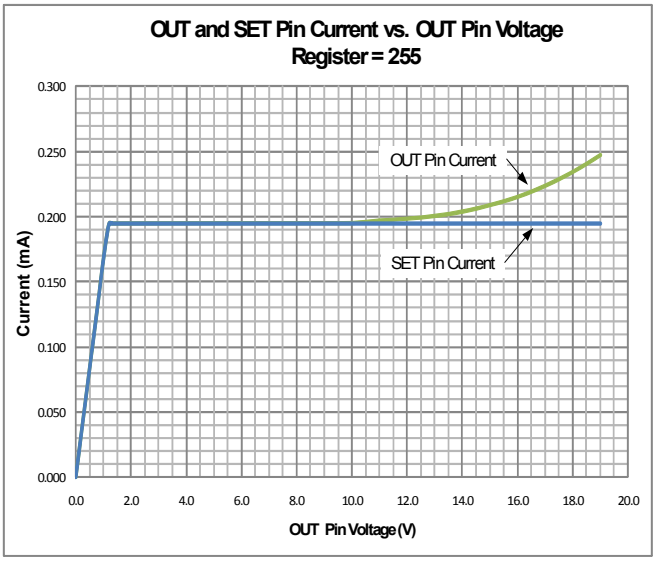


FIGURE 9. OUT PIN LEAKAGE CURRENT

Power Supply Sequence

The recommended power supply sequencing is shown in Figure 10. When applying power, V_{DD} should be applied before or at the same time as A_{VDD}. The minimum time for t_{VS} is 0µs. When removing power, the sequence of V_{DD} and A_{VDD} is not important.

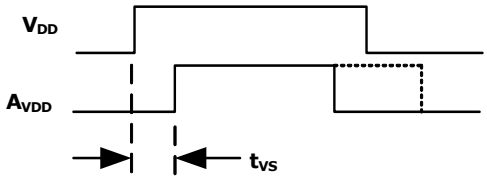


FIGURE 10. POWER SUPPLY SEQUENCE

Do not remove V_{DD} or A_{VDD} within 100ms of the start of the EEPROM programming cycle. Removing power before the EEPROM programming cycle is completed may result in corrupted data in the EEPROM.

Operating and Programming Supply Voltage and Current

To program the EEPROM, A_{VDD} must be ≥10.8V. If programming is not required, the ISL24201 will operate over an A_{VDD} range of 4.5V to 19V.

During EEPROM programming, I_{DD} and I_{AVDD} will temporarily be higher than their quiescent currents. Figure 11 shows a typical I_{DD} and I_{AVDD} current profile during EEPROM programming. The current pulses are Erase and Write cycles. The EEPROM programming algorithm is shown in Figure 12. The algorithm allows up to 4 erase cycles and 4 programming cycles, however typical parts only require 1 cycle of each, sometimes 2 when A_{VDD} is near the minimum 10.8V limit.

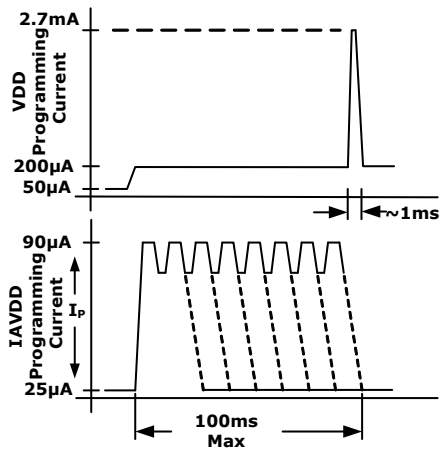


FIGURE 11. I_{DD} AND I_{AVDD} CURRENT PROFILE DURING EEPROM PROGRAMMING

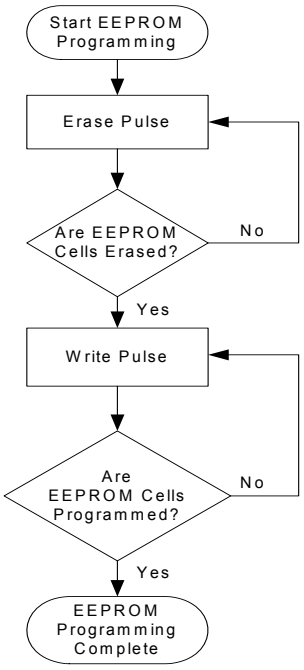


FIGURE 12. EEPROM PROGRAMMING FLOWCHART

ISL24201 Programming

The ISL24201 accepts I^2C bus address and data when the $\overline{WP}$ pin is at or above V_{IH} (>0.7V_{DD}). The ISL24201 ignores the I^2C bus when the $\overline{WP}$ pin is at or below V_{IL} (<0.3V_{DD}). Figure 13 shows the serial data format for writing the register and programming the EEPROM. Figure 14 shows the serial data format for reading the DAC register. Table 2 shows the truth table for reading and writing the device.

TABLE 2. ISL24201 READ AND WRITE CONTROL

$\overline{WP}$ PIN	I^2C BITS		FUNCTION
	R/W	PROGRAM	
0	1	X	Read Register.
0	0	1	Will acknowledge I^2C transactions. Will not write to register
0	0	0	Will acknowledge I^2C transactions. Will not write to EEPROM.
1	1	X	Read DAC Register
1	0	1	Write DAC Register
1	0	0	Program EEPROM

Programming the EEPROM memory transfers the current DAC register value to the EEPROM and occurs when the control bits select the programming mode and the A_{VDD} voltage is >10.8V. After the EEPROM programming cycle is started, the $\overline{WP}$ pin can be returned to logic low while the while it completes, which takes a maximum of 100ms.

The ISL24201 uses a 6 bit I^2C address, which is “100111xx”. The complete read and write protocol is shown in Figures 13 and 14.

I^2C Bus Signals

The ISL24201 uses fixed voltages for its I^2C thresholds, rather than the percentage of V_{DD} described in the I^2C specification (see Table 3). This should not cause a problem in most systems, but the I^2C logic levels in a specific design should be checked to ensure they are compatible with the ISL24201.

TABLE 3. ISL24201 I^2C BUS LOGIC LEVELS

SYMBOL	ISL24201	I^2C STANDARD
I^2CV_{IL}	0.55V	0.3*V_{DD}
I^2CV_{IH}	1.44V	0.7*V_{DD}

I²C Read and Write Format

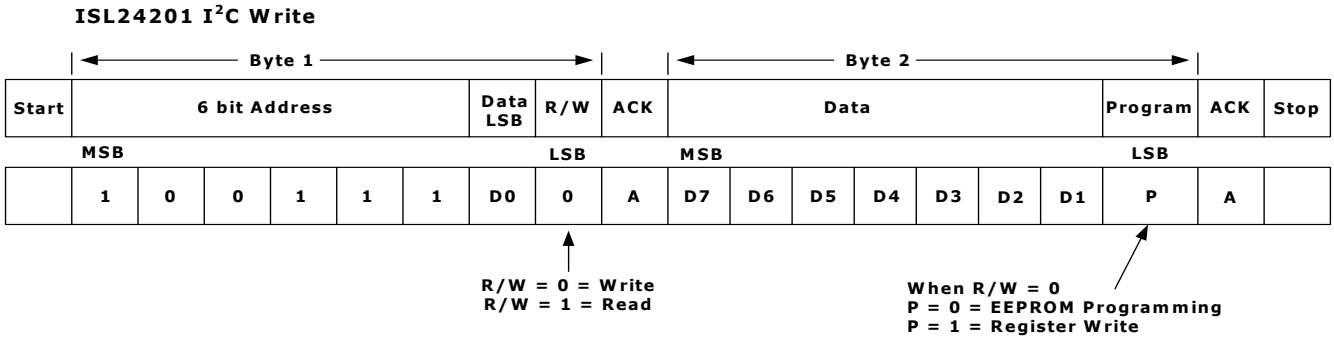


FIGURE 13. I²C WRITE FORMAT

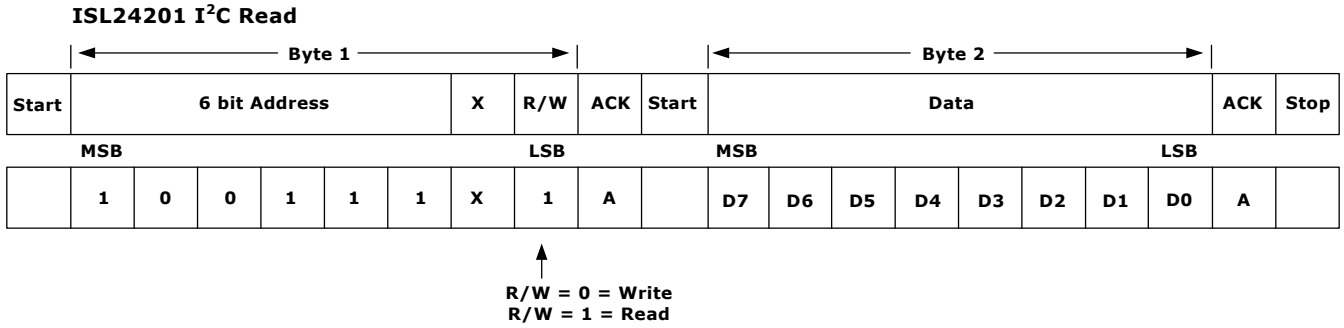


FIGURE 14. I²C READ FORMAT

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
12/9/10	FN7586.1	On page 5, corrected MIN spec for “tBUF” from 125µs to 200µs.
12/1/10	FN7586.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL24201

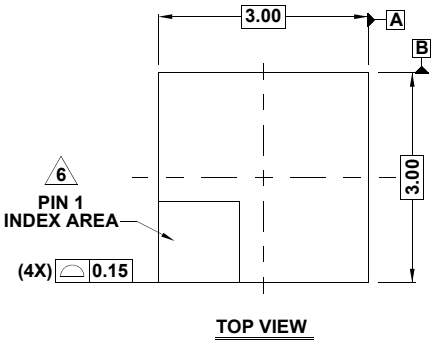
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/sear

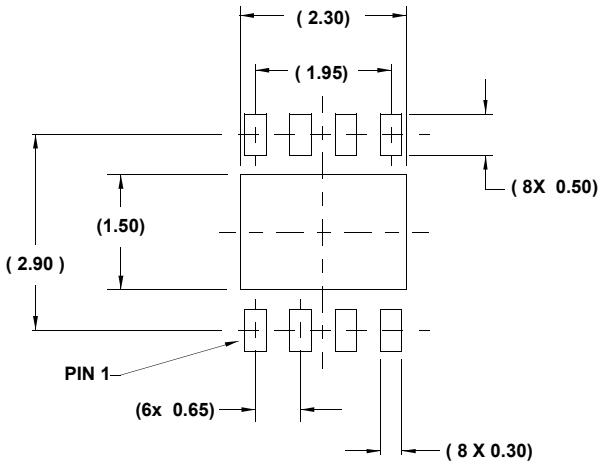
Package Outline Drawing

L8.3x3A

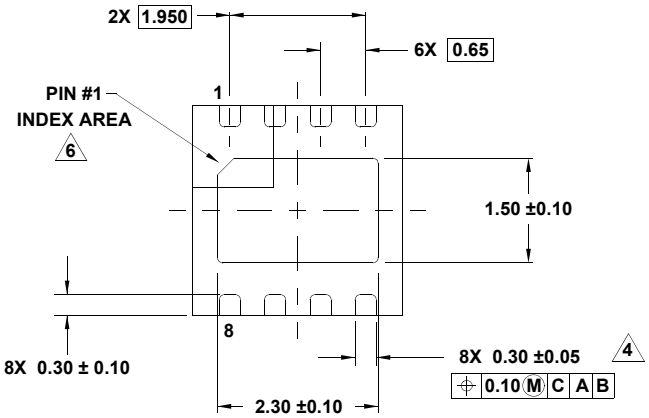
8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 4, 2/10



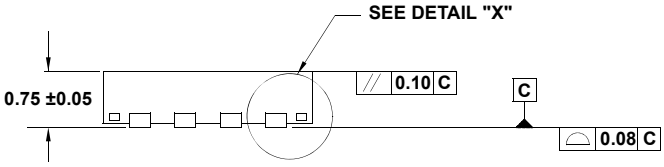
TOP VIEW



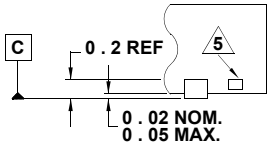
TYPICAL RECOMMENDED LAND PATTERN



BOTTOM VIEW



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.20mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229 WEEC-2 except for the foot length.