PCIX I/O System Clock Generator with EMI Control Features

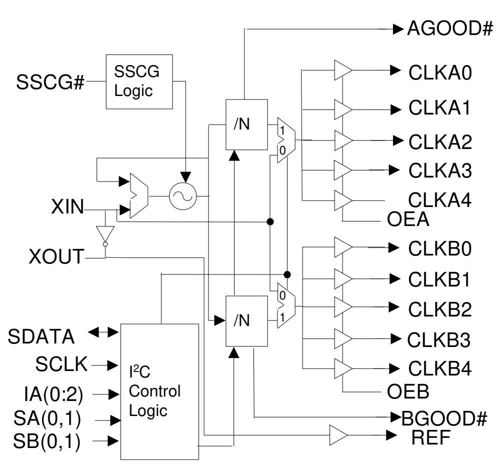
Features

- **Dedicated clock buffer power pins for reduced noise, crosstalk and jitter**
- **Input clock frequency of 25 MHz to 33.3 MHz**
- **Output frequencies of XINx1, XINx2, XINx3 and XINx4**
- **Output grouped in two banks of five clocks each**
- **One REF XIN clock output**
- **SMBus clock control interface for individual clock disabling and SSCG control and individual back frequency selection**
- **Output clock duty cycle is 50% (± 5%)**
- **< 250 ps skew between output clocks within a bank**
- **Output jitter < 250 psec (175 psec with all outputs at the same frequency)**
- **Spread Spectrum feature for reduced electromagnetic interference (EMI)**
- **OE pins for entire output bank enable control and testability**
- **48-pin SSOP and TSSOP packages**

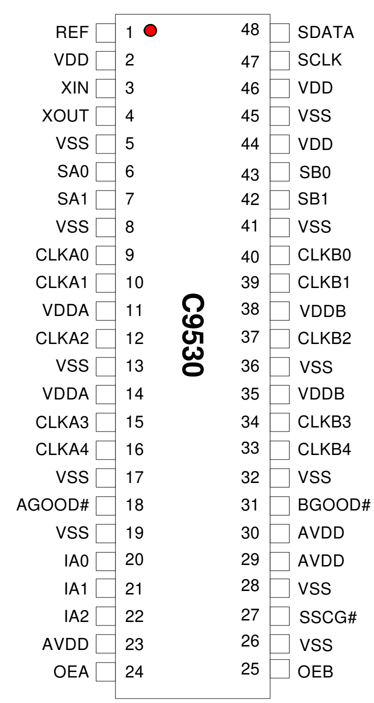
Table 1. Test Mode Logic Table[1]

Input Pins			Output Pins	
OEA	**SA1**	**SA0**	**CLKA**	
OEB	**SB1**	**SB0**	**CLKB**	**REF**
HIGH	LOW	LOW	XIN	XIN
HIGH	LOW	HIGH	2 * XIN	XIN
HIGH	HIGH	LOW	3 * XIN	XIN
HIGH	HIGH	HIGH	4 * XIN	XIN
LOW	X	X	Three-state	Three-state

Block Diagram



Pin Configuration



Note:
1. A and B banks have separate frequency select and output enable controls. XIN is the frequency of the clock on the device's XIN pin. OEA and OEB will three-state REF.

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Pin Description[3]

Pin[2]	Name	PWR[4]	I/O	Description
3	XIN	VDDA	I	**Crystal Buffer input pin**. Connects to a crystal, or an external clock source. Serves as input clock TCLK, in Test mode.
4	XOUT	VDDA	O	**Crystal Buffer output pin**. Connects to a crystal only. When a Can Oscillator is used or in Test mode, this pin is kept unconnected.
1	REF	VDD	O	**Buffered inverted outputs of the signal applied at Xin**, typically 33.33 or 25.0 MHz
24*	OEA	VDD	I	**Output Enable for clock bank A**. Causes the CLKA output clocks to be in a three-state condition when driven to a logic low level.
25*	OEB	VDD	I	**Output Enable for clock bank B**. Causes the CLKB output clocks to be in a three-state condition when driven to a logic low level.
18	AGOOD#	VDD	O	When this output signal is a logic low level, it indicates that the **output clocks of the A bank are locked to the input reference clock**. This output is latched.
31	BGOOD#	VDD	O	When this output signal is at a logic low level, it indicates that the **output clocks of the B bank are locked to the input reference clock**. This output is latched.
6*, 7*	SA(0,1)	VDD	I	**Clock Bank A selection bits**. These control the clock frequency that will be present on the outputs of the A bank of buffers. See *Table 1* for frequency codes and selection values.
43*, 42*	SB(0,1)	VDD	I	**Clock Bank B selection bits**. These control the clock frequency that will be present on the outputs of the B bank of buffers. See *Table 1* for frequency codes and selection values.
20*, 21*, 22*	IA(0:2)	VDD	I	**SMBus address selection input pins**. See *Table 3* SMBus Address table.
27*	SSCG#	VDD	I	Enables Spread Spectrum clock modulation when at a logic low level, see *Spread Spectrum Clocking* on page 6.
48	SDATA	VDD	I/O	**Data for the internal SMBus circuitry**.
47	SCLK	VDD	I	**Clock for the internal SMBus circuitry**.
11, 14	VDDA	–	PWR	**3.3V common power supply pin for Bank A PCI clocks CLKA**.
38, 35	VDDB	–	PWR	**3.3V common power supply pin for Bank B PCI clocks CLKB**.
2, 44, 46	VDD	–	PWR	**Power supply for internal Core logic**.
23, 29, 30	AVDD	–	PWR	**Power for internal analog circuitry**. This supply should have a separately decoupled current source from VDD.
9, 10, 12, 15, 16	CLKA (0:4)	VDDA	O	**A bank of five XINx1, XINx2, XINx3 and XINx4 output clocks**.
40, 39, 37, 34, 33	CLKB (0:4)	VDDB	O	**A bank of five XINx1, XINx2, XINx3 and XINx4 output clocks**.
5, 8, 13, 17, 19, 26, 28, 32, 36, 41, 45	VSS	–	PWR	**Ground pins for the device**.

Notes:

2. Pin numbers ending with * indicate that they contain device internal pull-up resistors that will insure that they are sensed as a logic 1 if no external circuitry is connected to them.
3. A bypass capacitor (0.1 µF) should be placed as close as possible to each V_{DD} pin. If these bypass capacitors are not close to the pins their high-frequency filtering characteristic will be cancelled by the lead inductance of the trace.
4. PWR = Power connection, I = Input, O = Output and I/O = both input and output functionality of the pin(s).

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required.

Data Protocol

The clock driver serial protocol accepts block write a operations from the controller. The bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. The C9530 does not support the Block Read function.

The block write protocol is outlined in *Table 2*. The addresses are listed in *Table 3*.

Table 2. Block Read and Block Write Protocol

Block Write Protocol	
Bit	**Description**
1	Start
2:8	Slave address – 7 bits
9	Write = 0
10	Acknowledge from slave
11:18	Command Code – 8 bits ‘00000000’ stands for block operation
19	Acknowledge from slave
20:27	Byte Count – 8 bits
28	Acknowledge from slave
29:36	Data byte 1 – 8 bits
37	Acknowledge from slave
38:45	Data byte 2 – 8 bits
46	Acknowledge from slave
....	....
....	Data Byte (N–1) – 8 bits
....	Acknowledge from slave
....	Data Byte N – 8 bits
....	Acknowledge from slave
....	Stop

Table 3. SMBus Address Selection Table

SMBus Address of the Device	IA0 Bit (Pin 10)	IA1 Bit (Pin 11)	IA2 Bit (Pin 12)
DE	0	0	0
DC	1	0	0
DA	0	1	0
D8	1	1	0
D6	0	0	1
D4	1	0	1
D0	0	1	1
D2	1	1	1

Serial Control Registers

Byte 0: Function Select Register

Bit	@Pup	Name	Description
7	1	TESTEN	Test Mode Enable. 1 = Normal operation, 0 = Test mode
6	0	SSEN	Spread Spectrum modulation control bit (effective only when Bit 0 of this register is set to a 0) 0 = OFF, 1= ON
5	1	SSSEL	SSCG Spread width select. 1 = 0.5%, 0 = 1.0% See *Table 4* below for clarification
4	0	S1	SB1 Bank MSB frequency control bit (effective only when Bit 0 of this register is set to a 0)
3	0	S0	SB0 Bank LSB frequency control bit (effective only when Bit 0 of this register is set to a 0)
2	0		SA1 Bank MSB frequency control bit (effective only when Bit 0 of this register is set to a 0)

Byte 0: Function Select Register (continued)

Bit	@Pup	Name	Description
1	0		SA0 Bank LSB frequency control bit (effective only when Bit 0 of this register is set to a 0)
0	1	HWSEL	Hardware/SMBus frequency control. 1 = Hardware (pins 6, 7, 42, 43 and 27), 0 = SMBus Byte 0 bits 1-4, & 6

Table 4. Clarification Table for Byte0, bit 5

Byte0, bit6	Byte0, bit5	Description
0	0	Frequency generated from second PLL
0	1	Frequency generated from XIN
1	0	Spread @ –1.0%
1	1	Spread @ –0.5%

Table 5. Test Table

Test Function Clock	Outputs		
	CLKA	CLKB	REF
Frequency	XIN/6	XIN/4	XIN

Byte 1: A Bank and REF Clock Control Register

Bit	@Pup	Name	Description
7	1		Reserved
6	1		Reserved
5	1	REFEN	REF Output Enable 0 = Disable, 1= Enable
4	1		CLKA4 Output Enable 0 = Disable, 1= Enable
3	1		CLKA3 Output Enable 0 = Disable, 1= Enable
2	1		CLKA2 Output Enable 0 = Disable, 1= Enable
1	1		CLKA1 Output Enable 0 = Disable, 1= Enable
0	1		CLKA0 Output Enable 0 = Disable, 1= Enable

Byte 2: PCI Register

Bit	@Pup	Name	Description
7	1		Reserved
6	1		Reserved
5	1		Reserved
4	1	18	CLKB4 Output Enable 0 = Disable, 1= Enable
3	1	19	CLKB3 Output Enable 0 = Disable, 1= Enable
2	1	22	CLKB2 Output Enable 0 = Disable, 1= Enable
1	1	23	CLKB1 Output Enable 0 = Disable, 1= Enable
0	1	24	CLKB0 Output Enable 0 = Disable, 1= Enable

Table 6. Suggested Oscillator Crystal Parameters

Parameter	Description	Conditions	Min	Typ.	Max.	Unit
F_o	Frequency		33.0	33.33	33.5	MHz
T_C	Tolerance	See *Note 5*	–	–	±100	PPM
T_S		Stability (T_A –10 to +60C) *Note 5*	–	–	±100	PPM
T_A		Aging (first year @ 25C) *Note 5*	–	–	5	PPM
	Operating Mode	Parallel Resonant, *Note 5*	–	–	–	
C_{XTAL}	Load Capacitance	The crystal's rated load. *Note 5*	–	20	–	pF
R_{ESR}	Effective Series Resistance (ESR)	Note 6	–	40	–	Ohms

Internal Crystal Oscillator

This device will operate in two input reference clock configurations. In its simplest mode a 33.33-MHz fundamental cut parallel resonant crystal is attached to the XIN and XOUT pins.

In the second mode a 33.33-MHz input reference clock is driven in on the IN clock from an external source. In this application the XOUT pin must be left disconnected.

Output Clock Three-state Control

All of the clocks in Bank A (CLKA) and Bank B (CLKB) may be placed in a three-state condition by bringing their relevant OE pins (OEA and OEB) to a logic LOW state. This transition to and from a state and active condition is a totally asynchronous event and clock glitching may occur during the transitioning states. This function is intended as a board level testing feature. When the output clocks are being enabled and disabled in active environments the SMBus control register bits are the preferred mechanism to control these signals in an orderly and predictable manner.

Output Clock Frequency Control

All of the output clocks have their frequency selected by the logic state of the S0 and S1 control bits. The source of these control signals is determined by the SMBus register Byte 0 bit 0. At initial power-up this bit is set of a logic 1 state and thus the frequency selections are controlled by the logic levels present on the device's S(0,1) pins. If the application does not use an SMBus interface then hardware frequency selection S(0,1) must be used. If it is desired to control the output clocks using an SMBus interface, then this bit (B0b0) must first be set to a low state. After this is done the device will use the contents of the internal SMBus register Bytes 0 Bits 3 and 4 to control the output clock's frequency.

The following formula and schematic may be used to understand and calculate either the loading specification of a crystal for a design or the additional discrete load capacitance that must be used to provide the correct load to a known load rated crystal

$$C_L = \frac{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) \times (C_{XOUTPCB}) + C_{XOUTFTG}) + C_{XOUTDISC})}{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) + (C_{XOUTPCB}) + C_{XOUTFTG}) + C_{XOUTDISC})}$$

where:

C_{XTAL} .... = The load rating of the crystal.

C_{XINFTG}= The clock generators XIN pin effective device internal capacitance to ground.

$C_{XOUTFTG}$= The clock generators XOUT pin effective device internal capacitance to ground.

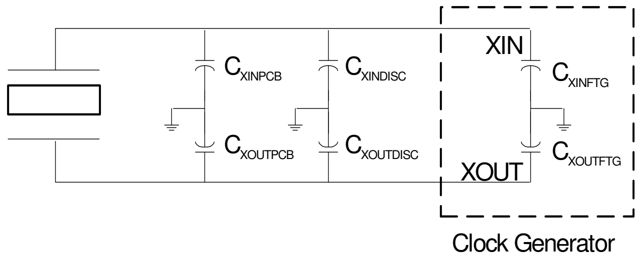
C_{XINPCB}= The effective capacitance to ground of the crystal to device PCB trace.

$C_{XOUTPCB}$= The effective capacitance to ground of the crystal to device PCB trace.

$C_{XINDISC}$= Any discrete capacitance that is placed between the XIn pin and ground.

$C_{XOUTDISC}$= Any discrete capacitance that is placed between the XIn pin and ground.

Notes:
5. For best performance and accurate frequencies from this device, it is recommended but not mandatory that the chosen crystal meets or exceeds these specifications.
6. Larger values may cause this device to exhibit oscillator startup problems.



As an example and using this formula for this data sheet's device, a design that has no discrete loading capacitors (C_{DISC}) and each of the crystal device PCB traces has a capacitance (C_{PCB}) to ground of 4 pF (typical value) would calculate as follows.

Therefore, to obtain output frequencies that are as close to this data sheets specified values as possible, in this design example, you should specify a parallel cut crystal that is designed to work into a load of 20 pF.

$$C_L = \frac{(4\text{ pF} + 36\text{ pF} + 0\text{ pF})\ \mathbf{x}\ (4\text{ pF} + 36\text{ pF} + 0\text{ pF})}{(4\text{ pF} + 36\text{ pF} + 0\text{ pF})\ \mathbf{x}\ (4\text{ pF} + 36\text{ pF} + 0\text{ pF})}$$

$$= \frac{40 \text{ x } 40}{40 \text{ x } 40}$$

$$= \frac{1600}{80}$$

$$= 20\text{ pF}$$

Spread Spectrum Clocking

Down Spread Description

Spread Spectrum is a modulation technique for distributing clock period over a certain bandwidth (called Spread Bandwidth). This technique allows the distribution of the undesirable electromagnetic energy (EMI) over a wide range of frequencies therefore reducing the average radiated energy present at any frequency over a given time period. As the spread is specified as a percentage of the resting (non-spread) frequency value, it is effective at the fundamental and, to a greater extent, at all it's harmonics.

In this device, Spread Spectrum is enabled externally through pin 27 (SSCG#) or internally via SMBus Byte 0 Bit 0 and 6. Spread spectrum is enabled externally when the SSCG# pin is low. This pin has an internal device pull up resistor, which causes its state to default to a high (Spread Spectrum disabled) unless externally forced to a low. It may also be enabled by programming SMBus Byte 0 Bit 0 LOW (to enable SMBus control of the function) and then programming SMBus Byte 0 Bit 6 LOW to set the feature active.

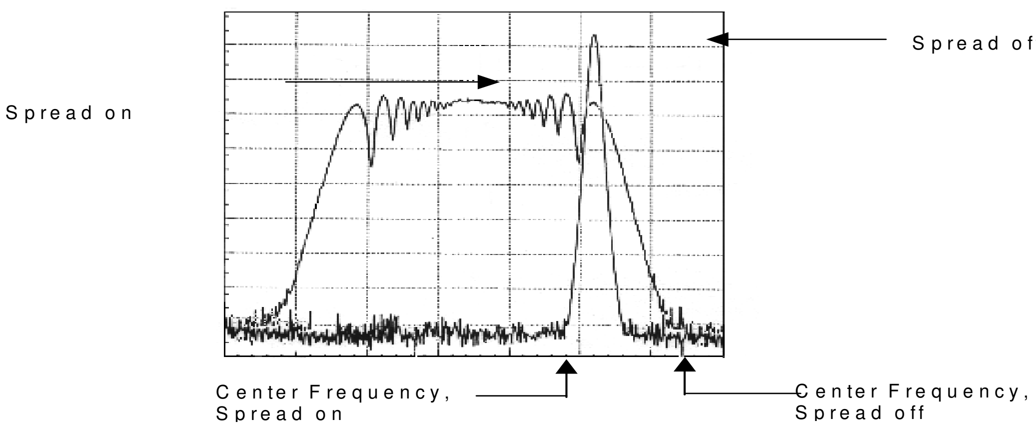


Figure 1. Spread Spectrum

Table 7. Spectrum Spreading Selection Table[7]

Output Clock Frequency	% of Frequency Spreading		Mode
	SMBus Byte 0 Bit 5 = 0	SMBus Byte 0 Bit 5 = 1	
33.3 MHz (XIN)	1.0% (–1.0% + 0%)	0.5% (–0.5% + 0%)	Down Spread
66.6 MHz (XIN*2)	1.0% (–1.0% + 0%)	0.5% (–0.5% + 0%)	Down Spread
100.0 MHz (XIN*3)	1.0% (–1.0% + 0%)	0.5% (–0.5% + 0%)	Down Spread
133.3 MHz (XIN*4)	1.0% (–1.0% + 0%)	0.5% (–0.5% + 0%)	Down Spread

Note:

7. When SSCG is enabled, the device will down spread the clock over a range that is 1% of its resting frequency. This means that for a 100-MHz output clock frequency will sweep through a spectral range from 99 to 100 MHz.

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD},V_{DDP}	Core Supply Voltage		–0.5	4.6	V
V_{DDA}	Analog Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non Functional	–65	+150	°C
T_A	Temperature, Operating Ambient	Functional	0	70	°C
T_J	Temperature, Junction	Functional	–	150	°C
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V
$Ø_{JC}$	Dissipation, Junction to Case	Mil-Spec 883E Method 1012.1	15		°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	45		°C/W
UL–94	Flammability Rating	At 1/8 in.	V – 0		
MSL	Moisture Sensitivity Level		1		

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}, V_{DDA}, V_{DDB}	3.3 Operating Voltage	3.3V ± 5%	3.135	3.465	V
V_{ILI2C}	Input Low Voltage	SDATA, SCLK	–	1.0	V
V_{IHI2C}	Input High Voltage	SDATA, SCLK	2.2	–	–
V_{IL}	Input Low Voltage	S(A,B)O, S(A,B)1, OE(A,B)	V_{SS} – 0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{DD} + 0. 5	V
I_{IL}	Input Leakage Current	except pull-ups or pull-downs $0 < V_{IN} < V_{DD}$	–5	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 1 mA	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1 mA	2.4	–	V
I_{OZ}	High-Impedance Output Current		–10	10	µA
C_{IN}	Input Pin Capacitance		2	5	pF
C_{OUT}	Output Pin Capacitance		3	6	pF
L_{IN}	Pin Inductance		–	7	nH
C_{XTAL}	Crystal Pin Capacitance	From XIN and XOUT pins to ground	32	38	pF
V_{XIH}	Xin High Voltage		$0.7V_{DD}$	V_{DD}	V
V_{XIL}	Xin Low Voltage		0	$0.3V_{DD}$	V
I_{DD}	Dynamic Supply Current	At 133 MHz and all outputs loaded per *Table 8*	–	300	mA
I_{PD}	Power-down Supply Current	PD# Asserted	–	1	mA

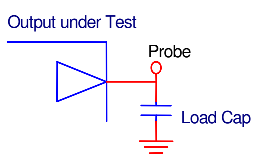
AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
T_{DC}	XIN Duty Cycle	The device will operate reliably with input duty cycles up to 30/70%.	45	55	%
XIN_{FREQ}	XIN Frequency	When Xin is driven from an external clock source	25	33.3	MHz

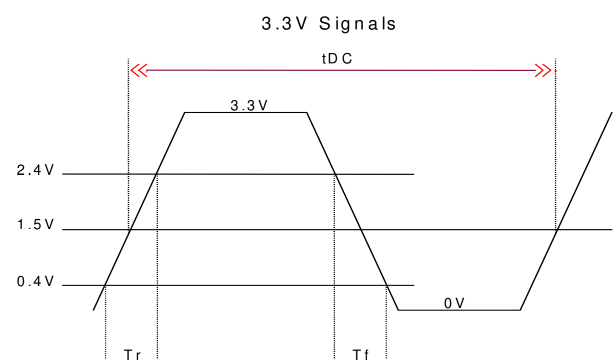
AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
T_R / T_F	XIN Rise and Fall Times	Measured between 0.3V_{DD} and 0.7V_{DD}	–	10.0	ns
T_{CCJ}	XIN Cycle to Cycle Jitter	As an average over 1μs duration	–	500	ps
L_{ACC}	Long-term Accuracy	Over 150 ms		300	ppm
CLK					
T_{DC}	CLK Duty Cycle	Measurement at 1.5V	45	55	%
$T_{PERIOD33}$	33MHz CLK Period	Measurement at 1.5V	29.5	30.5	ns
$T_{PERIOD66}$	66MHz CLK Period	Measurement at 1.5V	14.5	15.5	ns
$T_{PERIOD100}$	100MHz CLK Period	Measurement at 1.5V	9.5	10.5	ns
$T_{PERIOD133}$	133MHz CLK Period	Measurement at 1.5V	7.0	8.0	ns
T_R / T_F	CLK Rise and Fall Times	Measured between 0.4V and 2.4V	0.5	2.0	ns
T_{SKEW}	Any CLK to Any CLK Clock Skew	Measurement at 1.5V	–	250	ps
T_{CCJ}	CLK Cycle to Cycle Jitter	Measurement at 1.5V	–	175	ps
REF					
T_{DC}	REF Duty Cycle	Measurement at 1.5V	45	55	%
T_R / T_F	REF Rise and Fall Times	Measured between 0.4V and 2.4V	1.0	4.0	ns
T_{CCJ}	REF Cycle to Cycle Jitter	Measurement at 1.5V	–	750	ps
ENABLE/DISABLE and SET-UP					
tpZL,tpZH	Output Enable Delay (all outputs)		–	10.0	ns
tpLZ,tpZH	Output Disable Delay (all outputs)		–	10.0	ns
T_{STABLE}	Clock Stabilization from Power-up		–	3.0	ms

Test and Measurement Set-up



Lumped Load



LVTTL Signaling

Figure 2. Test and Measurement Set-up

Table 8. Loading

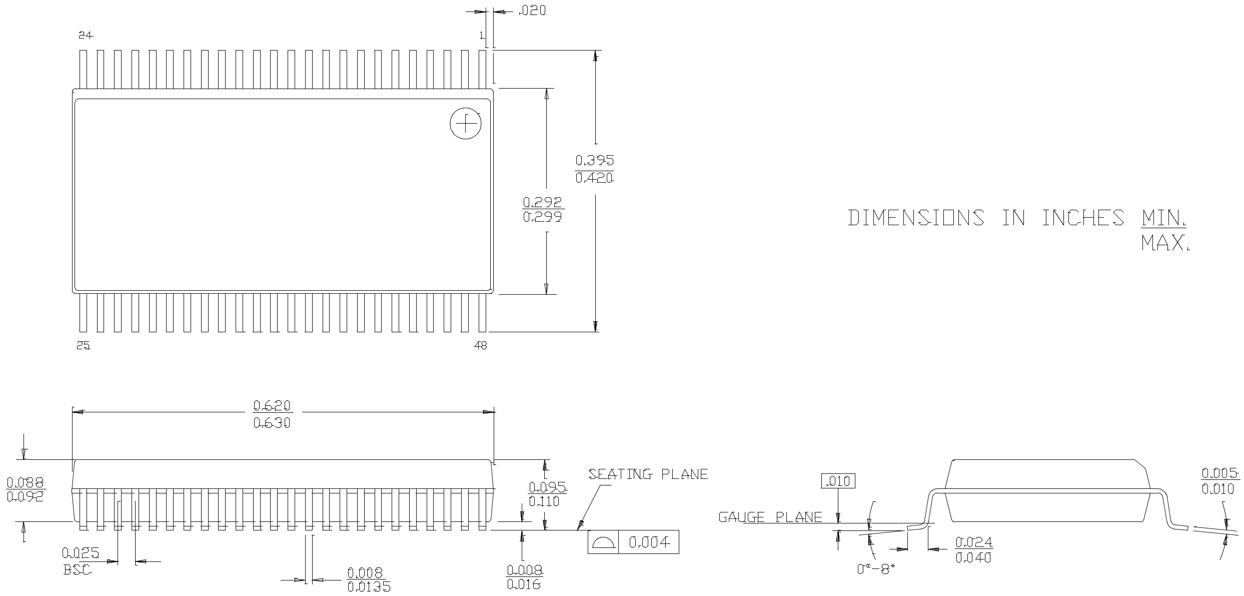
Output Name	Max Load (in pF)
CLK5	30
REF	20

Ordering Information

Part Number	Package Type	Product Flow
IMIC9530CY	48-Pin SSOP	Commercial, 0° to 70°C
IMIC9530CYT	48-Pin SSOP – Tape and Reel	Commercial, 0° to 70°C
IMIC9530CT	48-Pin TSSOP	Commercial, 0° to 70°C
IMIC9530CTT	48-Pin TSSOP – Tape and Reel	Commercial, 0° to 70°C
Lead-free		
CYI9530ZXC	48-Pin TSSOP	Commercial, 0° to 70°C
CYI9530ZXCT	48-Pin TSSOP – Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

48-lead Shrunk Small Outline Package O48



48-lead (240-mil) TSSOP II Z4824