

# BLS9G2731L-400; BLS9G2731LS-400

LDMOS S-band radar power transistor

Rev. 1 — 13 April 2017

AMPLEON

Product data sheet

## 1. Product profile

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### 1.1 General description

400 W LDMOS power transistor for S-band applications in the frequency range from 2700 MHz to 3100 MHz.

**Table 1. Test information**

Typical RF performance at  $T_{case} = 25\text{ °C}$ ;  $t_p = 300\text{ }\mu\text{s}$ ;  $\delta = 10\%$ ;  $I_{Dq} = 400\text{ mA}$ ; in a class-AB demo circuit measured over the entire 2700 MHz to 3100 MHz frequency range.

Test signal	f (MHz)	V <sub>DS</sub> (V)	P <sub>L</sub> (W)	G <sub>p</sub> (dB)	$\eta_D$ (%)
pulsed RF	2700 to 3100	32	425	13	47

### 1.2 Features and benefits

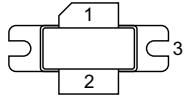
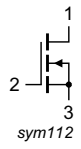
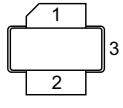
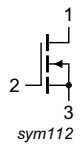
- High efficiency
- Excellent ruggedness
- Designed for S-band radar applications
- Excellent thermal stability
- Easy power control
- Integrated dual sided ESD protection enables excellent off-state isolation
- High flexibility with respect to pulse formats
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- S-band radar applications in the frequency range from 2700 MHz to 3100 MHz

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLS9G2731L-400 (SOT502A)</b>			
1	drain		 sym112
2	gate		
3	source <sup>[1]</sup>		
<b>BLS9G2731LS-400 (SOT502B)</b>			
1	drain		 sym112
2	gate		
3	source <sup>[1]</sup>		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLS9G2731L-400	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A
BLS9G2731LS-400	-	earless flanged ceramic package; 2 leads	SOT502B

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-6	+13	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature	<sup>[1]</sup>	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to case	$T_{case} = 85\text{ °C}; P_L = 400\text{ W}$		
		$t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.11	K/W
		$t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.15	K/W
		$t_p = 500\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.17	K/W
		$t_p = 1000\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.18	K/W

## 6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 4.5\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 450\text{ mA}$	1.5	1.9	2.5	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 32\text{ V}$	-	-	4	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	85	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	400	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 450\text{ mA}$	-	4.2	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 15.75\text{ A}$	-	0.03	-	$\Omega$

Table 7. RF characteristics

Test signal: pulsed RF;  $t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$ ; RF performance at  $V_{DS} = 32\text{ V}; I_{Dq} = 400\text{ mA}$ ;

$T_{case} = 25\text{ °C}$ ; unless otherwise specified; in a class-AB production circuit measured at frequencies of 2700 MHz, 2900 MHz and 3100 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_L = 425\text{ W}$	11	13	-	dB
$RL_{in}$	input return loss	$P_L = 425\text{ W}$	-	-7	-	dB
$\eta_D$	drain efficiency	$P_L = 425\text{ W}$	44	47	-	%
$P_{droop(pulse)}$	pulse droop power	$P_L = 425\text{ W}$	-	0.0	0.3	dB
$t_r$	rise time	$P_L = 425\text{ W}$	-	6	50	ns
$t_f$	fall time	$P_L = 425\text{ W}$	-	6	50	ns
$P_{L(3dB)}$	output power at 3 dB gain compression		400	-	-	W

## 7. Test information

### 7.1 Ruggedness in class-AB operation

The BLS9G2731L-400 and BLS9G2731LS-400 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; P_L = 400\text{ W}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$ .

## 7.2 Impedance information

Table 8. Typical impedance

f (MHz)	Z <sub>S</sub> (Ω)	Z <sub>L</sub> (Ω)
2700	1.6 – j5.8	1.6 – j3.7
2800	2.9 – j6.6	1.8 – j3.6
2900	8.0 – j4.7	2.2 – j3.1
3000	4.4 – j0.3	1.9 – j2.4
3100	1.9 – j0.7	1.5 – j2.1

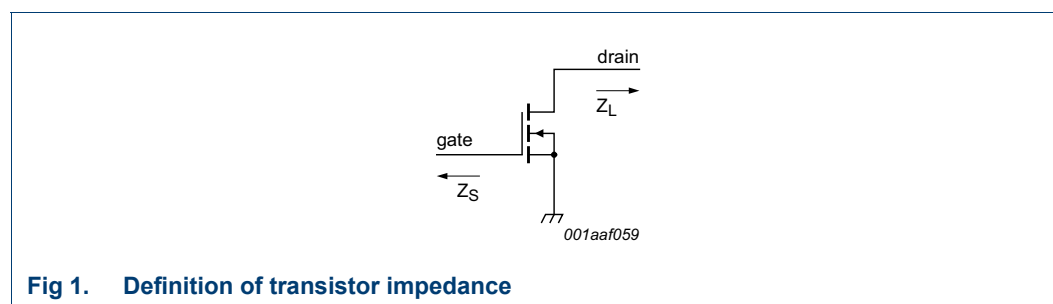
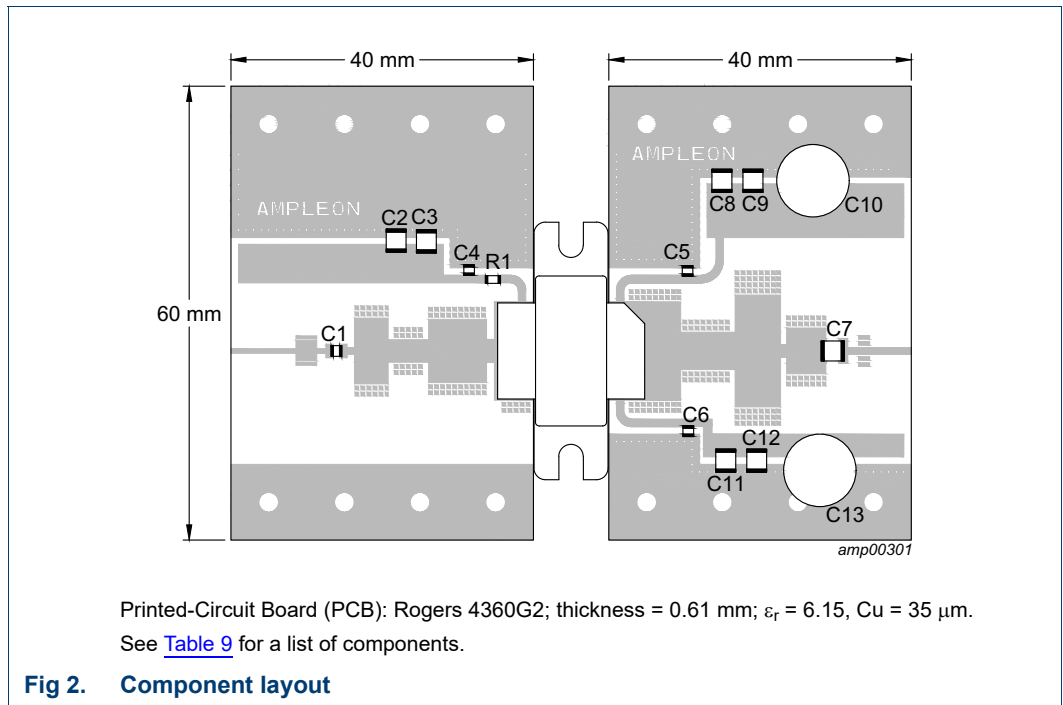


Fig 1. Definition of transistor impedance

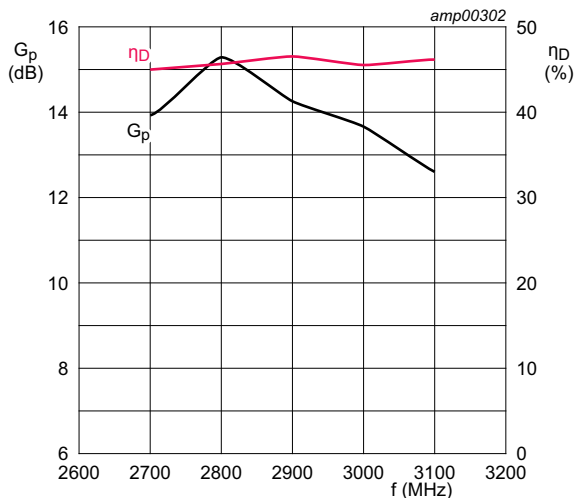
7.3 Test circuit



**Table 9. List of components**  
See [Figure 2](#) for component layout.

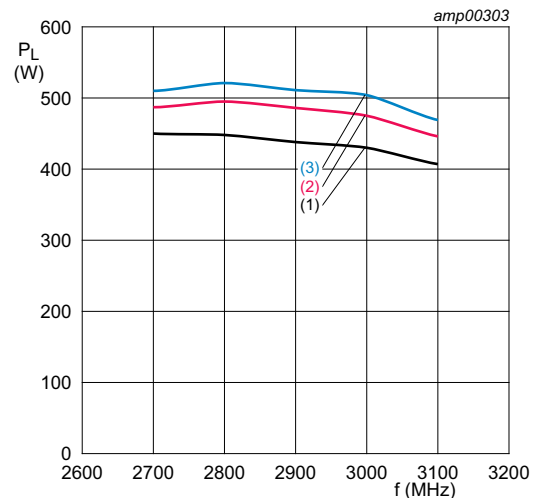
Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	12 pF	ATC 800A
C2, C8, C11	multilayer ceramic chip capacitor	1 nF	ATC 800B
C3, C9, C12	multilayer ceramic chip capacitor	10 $\mu\text{F}$	Murata: GRM55DR61H106KA88L
C4, C5, C6	multilayer ceramic chip capacitor	15 pF	ATC 800A
C7	multilayer ceramic chip capacitor	33 pF	ATC 800B
C10, C13	electrolytic capacitor	100 $\mu\text{F}$ , 63 V	
R1	resistor	5 $\Omega$	SMD 0603

7.4 Graphical data



$V_{DS} = 32\text{ V}$ ;  $I_{Dq} = 400\text{ mA}$ ;  $P_L = 425\text{ W}$ ;  $t_p = 300\text{ }\mu\text{s}$ ;  $\delta = 10\text{ }\%$ .

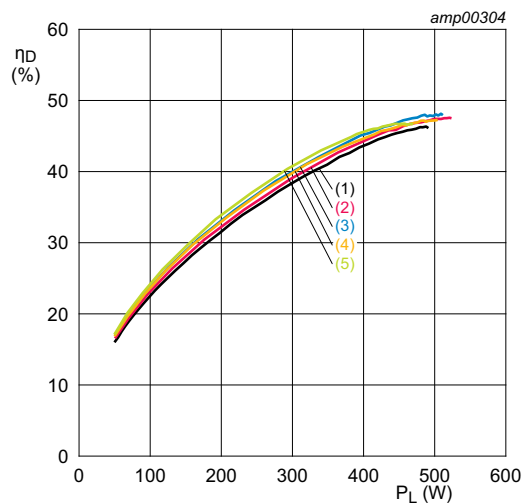
Fig 3. Power gain and drain efficiency as function of frequency; typical values



$V_{DS} = 32\text{ V}$ ;  $I_{Dq} = 400\text{ mA}$ ;  $t_p = 300\text{ }\mu\text{s}$ ;  $\delta = 10\text{ }\%$ .

- (1)  $P_{1dB}$
- (2)  $P_{2dB}$
- (3)  $P_{3dB}$

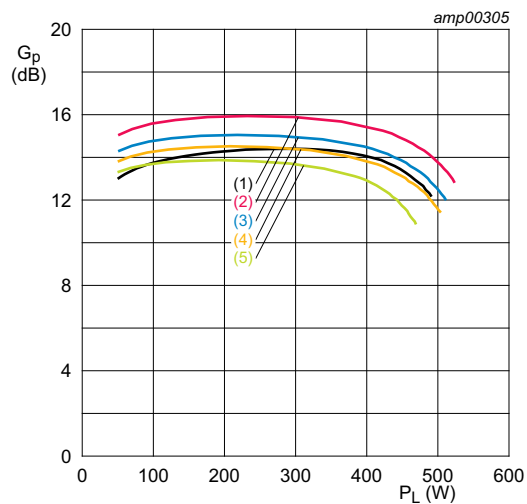
Fig 4. Output power as a function of frequency; typical values



$V_{DS} = 32\text{ V}$ ;  $I_{Dq} = 400\text{ mA}$ ;  $t_p = 300\text{ }\mu\text{s}$ ;  $\delta = 10\text{ }\%$ .

- (1)  $f = 2700\text{ MHz}$
- (2)  $f = 2800\text{ MHz}$
- (3)  $f = 2900\text{ MHz}$
- (4)  $f = 3000\text{ MHz}$
- (5)  $f = 3100\text{ MHz}$

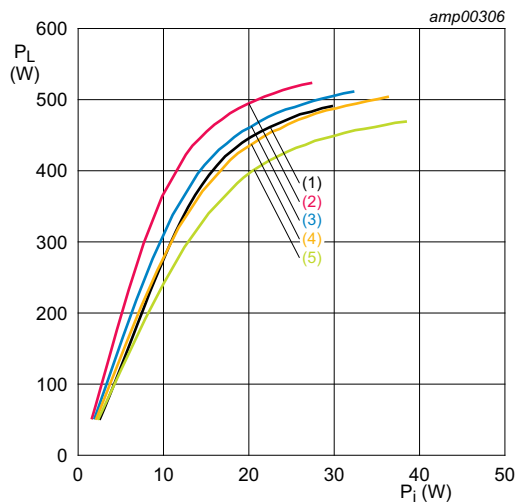
Fig 5. Drain efficiency as a function of output power; typical values



$V_{DS} = 32\text{ V}$ ;  $I_{Dq} = 400\text{ mA}$ ;  $t_p = 300\text{ }\mu\text{s}$ ;  $\delta = 10\text{ }\%$ .

- (1)  $f = 2700\text{ MHz}$
- (2)  $f = 2800\text{ MHz}$
- (3)  $f = 2900\text{ MHz}$
- (4)  $f = 3000\text{ MHz}$
- (5)  $f = 3100\text{ MHz}$

Fig 6. Power gain as a function of output power; typical values



$V_{DS} = 32 \text{ V}$ ;  $I_{Dq} = 400 \text{ mA}$ ;  $t_p = 300 \mu\text{s}$ ;  $\delta = 10 \%$ .

- (1)  $f = 2700 \text{ MHz}$
- (2)  $f = 2800 \text{ MHz}$
- (3)  $f = 2900 \text{ MHz}$
- (4)  $f = 3000 \text{ MHz}$
- (5)  $f = 3100 \text{ MHz}$

**Fig 7. Output power as a function of input power; typical values**

8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads

SOT502A

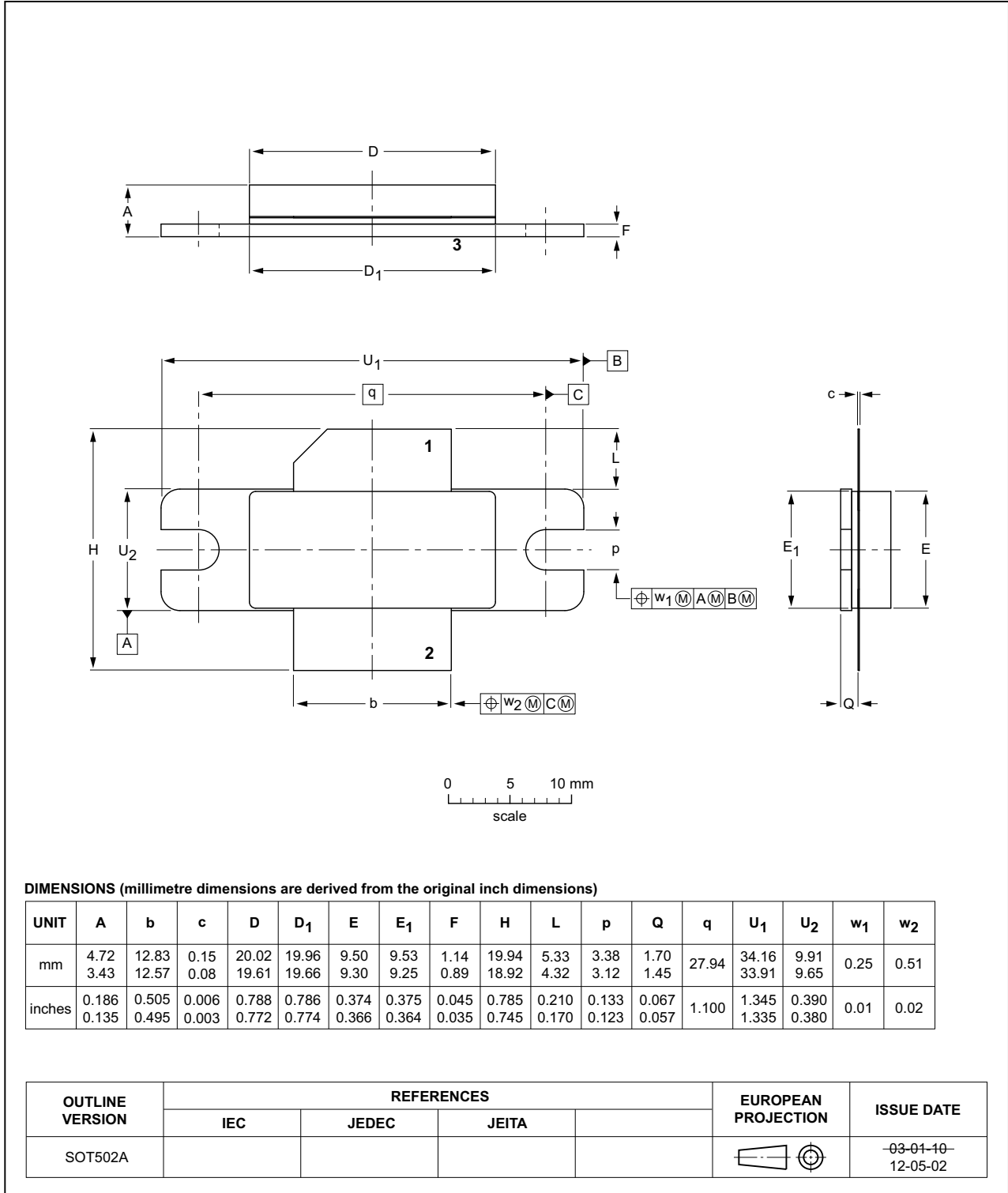


Fig 8. Package outline SOT502A



Earless flanged ceramic package; 2 leads

SOT502B

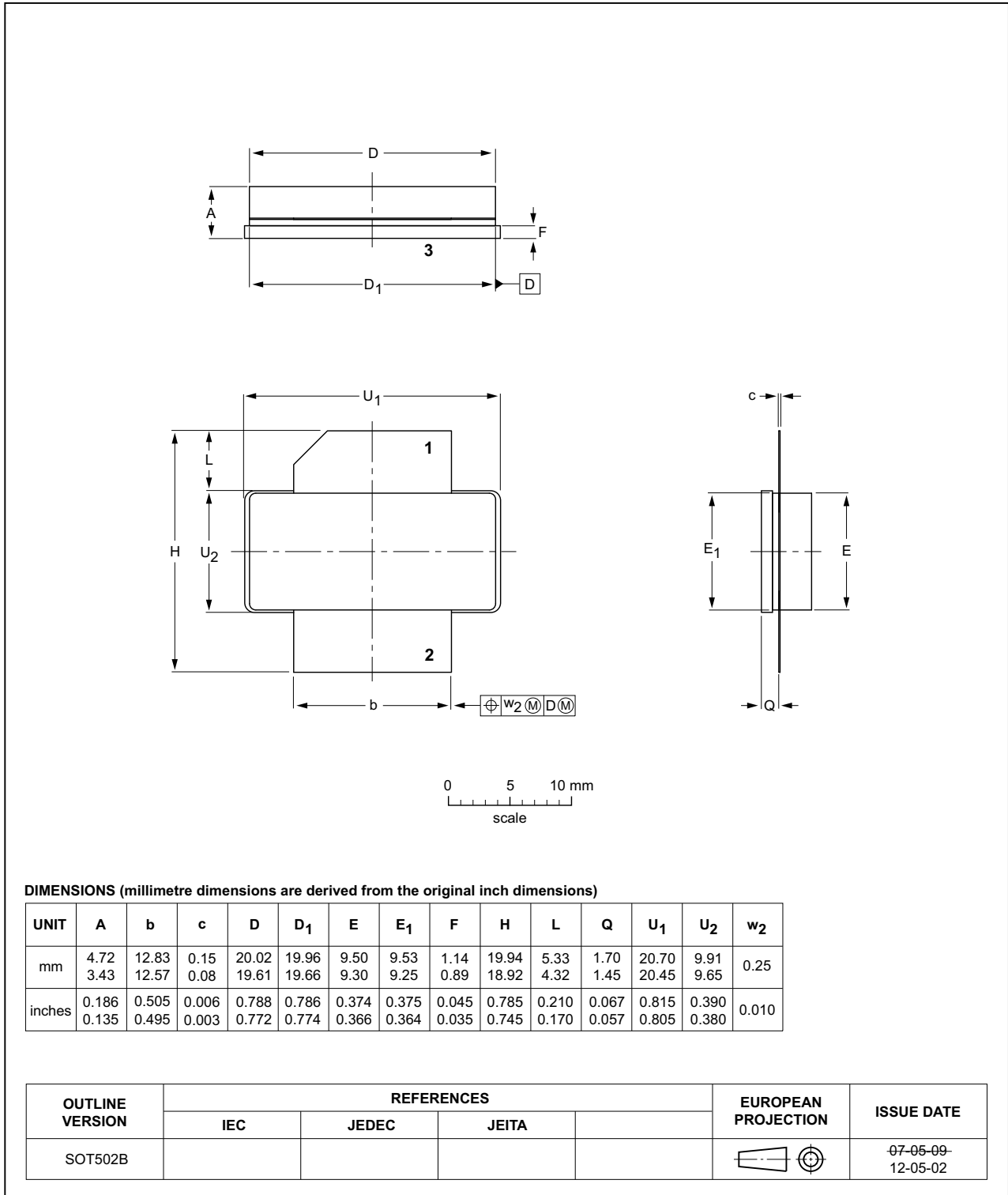


Fig 9. Package outline SOT502B

## 9. Handling information

**CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

**Table 10. ESD sensitivity**

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A <a href="#">[1]</a>
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 <a href="#">[2]</a>

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

## 10. Abbreviations

**Table 11. Abbreviations**

Acronym	Description
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
S-band	Short wave band
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

## 11. Revision history

**Table 12. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLS9G2731L-400_LS-400 v.1	20170413	Product data sheet		-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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