# S-93C46C/56C/66C/76C/86C

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## 3-WIRE SERIAL $E^2$PROM

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Rev.1.1_01

This IC is a high speed, low current consumption, 3-wire serial $E^2$PROM with a wide operating voltage range. This IC has the capacity of 1 K-bit, 2 K-bit, 4 K-bit, 8 K-bit and 16 K-bit, and the organization is 64 words × 16-bit, 128 words × 16-bit, 256 words × 16-bit, 512 words × 16-bit and 1024 words × 16-bit, respectively. Sequential read is available, at which time addresses are automatically incremented in 16-bit blocks. The communication method is by the Microwire bus.

**Caution This product is intended to use in general electronic devices such as consumer electronics, office equipment, and communications devices. Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to ABLIC Inc. is indispensable.**

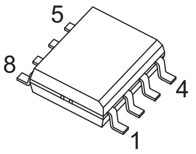
## ■ Features

- Memory capacity
  - S-93C46C: 1 K-bit (64-word × 16-bit)
  - S-93C56C: 2 K-bit (128-word × 16-bit)
  - S-93C66C: 4 K-bit (256-word × 16-bit)
  - S-93C76C: 8 K-bit (512-word × 16-bit)
  - S-93C86C: 16 K-bit (1024-word × 16-bit)
- Operation voltage range
  - Read: 1.6 V to 5.5 V
  - Write: 1.8 V to 5.5 V
- Operation frequency: 2.0 MHz max.
- Write time: 4.0 ms max.
- Sequential read
- Write protect function during the low power supply voltage
- Function to protect against write due to erroneous instruction recognition
- Endurance: $10^6$ cycle / word[*1] (Ta = +85°C)
- Data retention: 100 years (Ta = +25°C)
  50 years (Ta = +85°C)
- Initial delivery state: FFFFh
- Operation temperature range: Ta = −40°C to +85°C
- Lead-free (Sn 100%), halogen-free

***1.** For each address (Word: 16-bit)

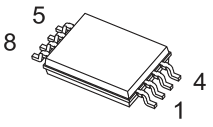
## ■ Packages

- 8-Pin SOP (JEDEC)



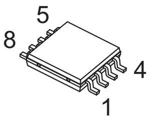
(5.0 × 6.0 × t1.75 mm)

- 8-Pin TSSOP



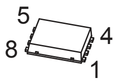
(3.0 × 6.4 × t1.1 mm)

- TMSOP-8



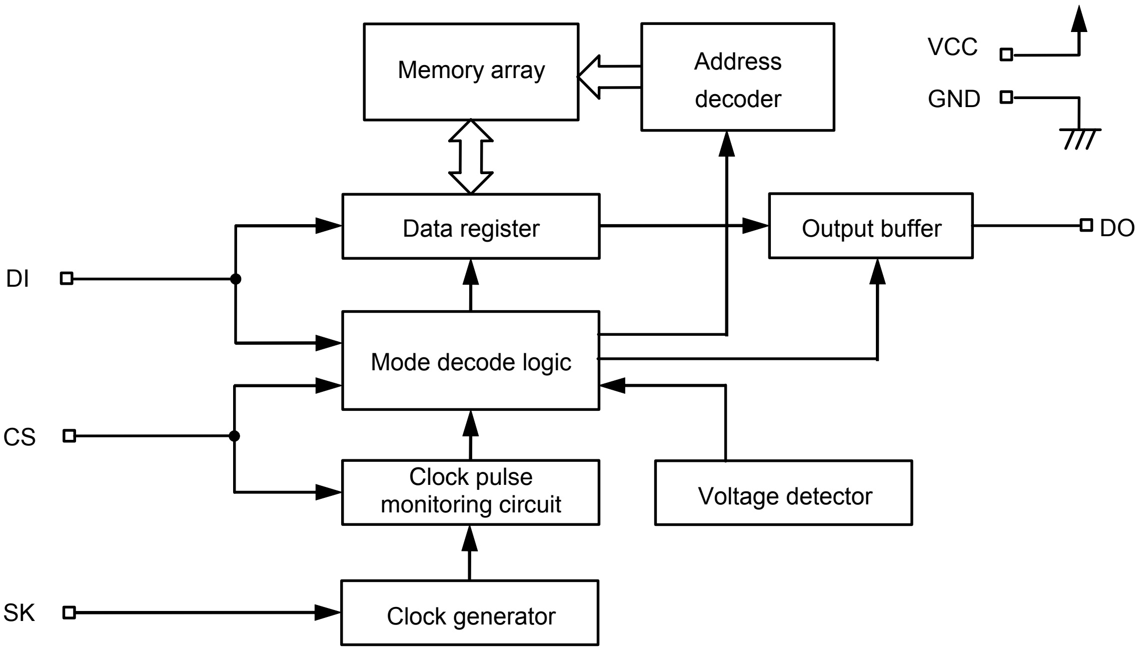
(2.9 × 4.0 × t0.8 mm)

- SNT-8A



(2.5 × 2.0 × t0.5 mm)

## ■ Block Diagram


Memory array
Address decoder
VCC
GND
Data register
Output buffer
DO
DI
Mode decode logic
CS
Clock pulse monitoring circuit
Voltage detector
SK
Clock generator

## ■ Product Name Structure

### 1. Product name

**S-93CxxC x 0 I - xxxx U 3**

Environmental code
U: Lead-free (Sn 100%), halogen-free

Package abbreviation and IC packing specification[*1]

| | |
|---|---|
| J8T1: | 8-Pin SOP (JEDEC), Tape |
| T8T1: | 8-Pin TSSOP, Tape |
| K8T3: | TMSOP-8, Tape |
| I8T1: | SNT-8A, Tape |

Operation temperature
I: Ta = −40°C to +85°C

Fixed

Pin assignment

| | |
|---|---|
| D: | 8-Pin SOP (JEDEC)<br>8-Pin TSSOP<br>TMSOP-8<br>SNT-8A |
| R: | 8-Pin SOP (JEDEC) (Rotated)[*2] |

Product name

| | |
|---|---|
| S-93C46C: | 1 K-bit |
| S-93C56C: | 2 K-bit |
| S-93C66C: | 4 K-bit |
| S-93C76C: | 8 K-bit |
| S-93C86C: | 16 K-bit |

***1.** Refer to the tape drawing
***2.** S-93C46C/56C/66C only

### 2. Packages

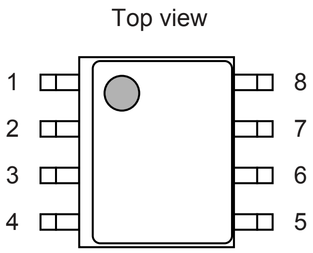
| Package Name | Dimension | Tape | Reel | Land |
|---|---|---|---|---|
| 8-Pin SOP (JEDEC) | FJ008-Z-P-SD | FJ008-Z-C-SD | FJ008-Z-R-SD | − |
| 8-Pin TSSOP | FT008-Z-P-SD | FT008-Z-C-SD | FT008-Z-R-SD | − |
| TMSOP-8 | FM008-A-P-SD | FM008-A-C-SD | FM008-A-R-SD | − |
| SNT-8A | PH008-A-P-SD | PH008-A-C-SD | PH008-A-R-SD | PH008-A-L-SD |

## 3. Product name list

| Product Name | Capacity | Package Name |
|---|---|---|
| S-93C46CD0I-J8T1U3 | 1 K-bit | 8-Pin SOP (JEDEC) |
| S-93C46CR0I-J8T1U3 | 1 K-bit | 8-Pin SOP (JEDEC) (Rotated) |
| S-93C46CD0I-T8T1U3 | 1 K-bit | 8-Pin TSSOP |
| S-93C46CD0I-K8T3U3 | 1 K-bit | TMSOP-8 |
| S-93C46CD0I-I8T1U3 | 1 K-bit | SNT-8A |
| S-93C56CD0I-J8T1U3 | 2 K-bit | 8-Pin SOP (JEDEC) |
| S-93C56CR0I-J8T1U3 | 2 K-bit | 8-Pin SOP (JEDEC) (Rotated) |
| S-93C56CD0I-T8T1U3 | 2 K-bit | 8-Pin TSSOP |
| S-93C56CD0I-K8T3U3 | 2 K-bit | TMSOP-8 |
| S-93C56CD0I-I8T1U3 | 2 K-bit | SNT-8A |
| S-93C66CD0I-J8T1U3 | 4 K-bit | 8-Pin SOP (JEDEC) |
| S-93C66CR0I-J8T1U3 | 4 K-bit | 8-Pin SOP (JEDEC) (Rotated) |
| S-93C66CD0I-T8T1U3 | 4 K-bit | 8-Pin TSSOP |
| S-93C66CD0I-K8T3U3 | 4 K-bit | TMSOP-8 |
| S-93C66CD0I-I8T1U3 | 4 K-bit | SNT-8A |
| S-93C76CD0I-J8T1U3 | 8 K-bit | 8-Pin SOP (JEDEC) |
| S-93C76CD0I-T8T1U3 | 8 K-bit | 8-Pin TSSOP |
| S-93C76CD0I-K8T3U3 | 8 K-bit | TMSOP-8 |
| S-93C76CD0I-I8T1U3 | 8 K-bit | SNT-8A |
| S-93C86CD0I-J8T1U3 | 16 K-bit | 8-Pin SOP (JEDEC) |
| S-93C86CD0I-T8T1U3 | 16 K-bit | 8-Pin TSSOP |
| S-93C86CD0I-K8T3U3 | 16 K-bit | TMSOP-8 |
| S-93C86CD0I-I8T1U3 | 16 K-bit | SNT-8A |

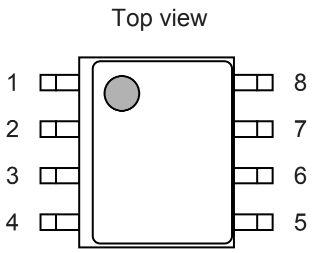
## ■ Pin Configuration

### 1. 8-Pin SOP (JEDEC)



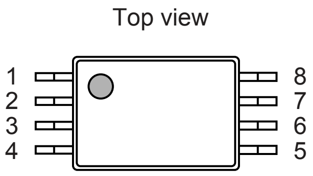
| Pin No. | Symbol | Description |
|---|---|---|
| 1 | CS | Chip select input |
| 2 | SK | Serial clock input |
| 3 | DI | Serial data input |
| 4 | DO | Serial data output |
| 5 | GND | Ground |
| 6 | TEST[*1] | Test |
| 7 | NC | No connection |
| 8 | VCC | Power supply |

### 2. 8-Pin SOP (JEDEC) (Rotated)



| Pin No. | Symbol | Description |
|---|---|---|
| 1 | NC | No connection |
| 2 | VCC | Power supply |
| 3 | CS | Chip select input |
| 4 | SK | Serial clock input |
| 5 | DI | Serial data input |
| 6 | DO | Serial data output |
| 7 | GND | Ground |
| 8 | TEST[*1] | Test |

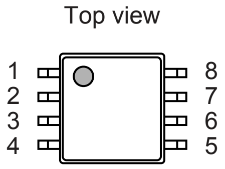
### 3. 8-Pin TSSOP



| Pin No. | Symbol | Description |
|---|---|---|
| 1 | CS | Chip select input |
| 2 | SK | Serial clock input |
| 3 | DI | Serial data input |
| 4 | DO | Serial data output |
| 5 | GND | Ground |
| 6 | TEST[*1] | Test |
| 7 | NC | No connection |
| 8 | VCC | Power supply |

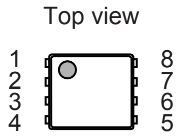
***1.** Connect to GND or the VCC pin, or set to open. Even if this pin is not connected, performance is not affected so long as the absolute maximum rating is not exceeded.

### 4. TMSOP-8



| Pin No. | Symbol | Description |
|---|---|---|
| 1 | CS | Chip select input |
| 2 | SK | Serial clock input |
| 3 | DI | Serial data input |
| 4 | DO | Serial data output |
| 5 | GND | Ground |
| 6 | TEST[*1] | Test |
| 7 | NC | No connection |
| 8 | VCC | Power supply |

### 5. SNT-8A



| Pin No. | Symbol | Description |
|---|---|---|
| 1 | CS | Chip select input |
| 2 | SK | Serial clock input |
| 3 | DI | Serial data input |
| 4 | DO | Serial data output |
| 5 | GND | Ground |
| 6 | TEST[*1] | Test |
| 7 | NC | No connection |
| 8 | VCC | Power supply |

***1.** Connect to GND or the VCC pin, or set to open. Even if this pin is not connected, performance is not affected so long as the absolute maximum rating is not exceeded.

## ■ Absolute Maximum Ratings

**Table 1**

| Item | Symbol | Absolute Maximum Rating | Unit |
|---|---|---|---|
| Power supply voltage | $V_{CC}$ | −0.3 to +6.5 | V |
| Input voltage | $V_{IN}$ | −0.3 to +6.5 | V |
| Output voltage | $V_{OUT}$ | −0.3 to $V_{CC}$ + 0.3 | V |
| Operation ambient temperature | $T_{opr}$ | −40 to +85 | °C |
| Storage temperature | $T_{stg}$ | −65 to +150 | °C |

**Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

## ■ Recommended Operating Conditions

**Table 2**

| Item | Symbol | Condition | Ta = −40°C to +85°C | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| Power supply voltage | $V_{CC}$ | READ, EWDS | 1.6 | 5.5 | V |
| | | WRITE, ERASE,EWEN | 1.8 | 5.5 | V |
| | | WRAL, ERAL | 2.5 | 5.5 | V |
| High level input voltage | $V_{IH}$ | $V_{CC}$ = 4.5 V to 5.5 V | 2.0 | $V_{CC}$ | V |
| | | $V_{CC}$ = 2.7 V to 4.5 V | 0.8 × $V_{CC}$ | $V_{CC}$ | V |
| | | $V_{CC}$ = 1.6 V to 2.7 V | 0.8 × $V_{CC}$ | $V_{CC}$ | V |
| Low level input voltage | $V_{IL}$ | $V_{CC}$ = 4.5 V to 5.5 V | 0.0 | 0.8 | V |
| | | $V_{CC}$ = 2.7 V to 4.5 V | 0.0 | 0.2 × $V_{CC}$ | V |
| | | $V_{CC}$ = 1.6 V to 2.7 V | 0.0 | 0.15 × $V_{CC}$ | V |

## ■ Pin Capacitance

**Table 3**

(Ta = +25°C, f = 1.0 MHz, $V_{CC}$ = 5.0 V)

| Item | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | $V_{IN}$ = 0 V | − | 8 | pF |
| Output capacitance | $C_{OUT}$ | $V_{OUT}$ = 0 V | − | 10 | pF |

## ■ Endurance

**Table 4**

| Item | Symbol | Operation Ambient Temperature | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Endurance | $N_W$ | Ta = −40°C to +85°C | $10^6$ | − | cycle / word*1 |

***1.** For each address (Word: 16-bit)

## ■ Data Retention

**Table 5**

| Item | Symbol | Operation Ambient Temperature | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Data retention | − | Ta = +25°C | 100 | − | year |
| | | Ta = −40°C to +85°C | 50 | − | year |

## ■ DC Electrical Characteristics

**Table 6**

| Item | Symbol | Condition | Ta = −40°C to +85°C | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 1.6 V to 1.8 V, $f_{SK}$ = 0.5 MHz | | $V_{CC}$ = 1.8 V to 2.5 V, $f_{SK}$ = 1.0 MHz | | $V_{CC}$ = 2.5 V to 4.5 V, $f_{SK}$ = 2.0 MHz | | $V_{CC}$ = 4.5 V to 5.5 V, $f_{SK}$ = 2.0 MHz | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Current consumption (read) | $I_{CC1}$ | No load at DO pin | − | 0.4 | − | 0.4 | − | 0.5 | − | 0.8 | mA |

**Table 7**

| Item | Symbol | Condition | Ta = −40°C to +85°C | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 1.8 V to 4.5 V | | $V_{CC}$ = 4.5 V to 5.5 V | | |
| | | | Min. | Max. | Min. | Max. | |
| Current consumption (write) | $I_{CC2}$ | No load at DO pin | − | 2.0 | − | 2.0 | mA |

**Table 8**

| Item | Symbol | Condition | Ta = −40°C to +85°C | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 1.6 V to 2.5 V | | $V_{CC}$ = 2.5 V to 4.5 V | | $V_{CC}$ = 4.5 V to 5.5 V | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Standby current consumption | $I_{SB}$ | CS = GND, DO = Open, Other input pins are $V_{CC}$ or GND | − | 2.0 | − | 2.0 | − | 2.0 | µA |
| Input leakage current | $I_{LI}$ | CS, SK, DI, $V_{IN}$ = GND to $V_{CC}$ | − | 1.0 | − | 1.0 | − | 1.0 | µA |
| Output leakage current | $I_{LO}$ | DO, $V_{OUT}$ = GND to $V_{CC}$ | − | 1.0 | − | 1.0 | − | 1.0 | µA |
| Pull-down current | $I_{PD}$ | TEST, $V_{IN}$ = GND ~ $V_{CC}$ | − | 1.2 | − | 1.2 | − | 1.2 | µA |
| Low level output voltage | $V_{OL}$ | $I_{OL}$ = 2.1 mA | − | − | − | − | − | 0.4 | V |
| | | $I_{OL}$ = 100 µA | − | 0.1 | − | 0.1 | − | 0.1 | V |
| High level output voltage | $V_{OH}$ | $I_{OH}$ = −400 µA | − | − | − | − | 2.4 | − | V |
| | | $I_{OH}$ = −100 µA | − | − | $V_{CC}$ − 0.3 | − | $V_{CC}$ − 0.3 | − | V |
| | | $I_{OH}$ = −10 µA | $V_{CC}$ − 0.2 | − | $V_{CC}$ − 0.2 | − | $V_{CC}$ − 0.2 | − | V |
| Data hold voltage of write enable latch | $V_{DH}$ | Only program disable mode | 1.5 | − | 1.5 | − | 1.5 | − | V |

## ■ AC Electrical Characteristics

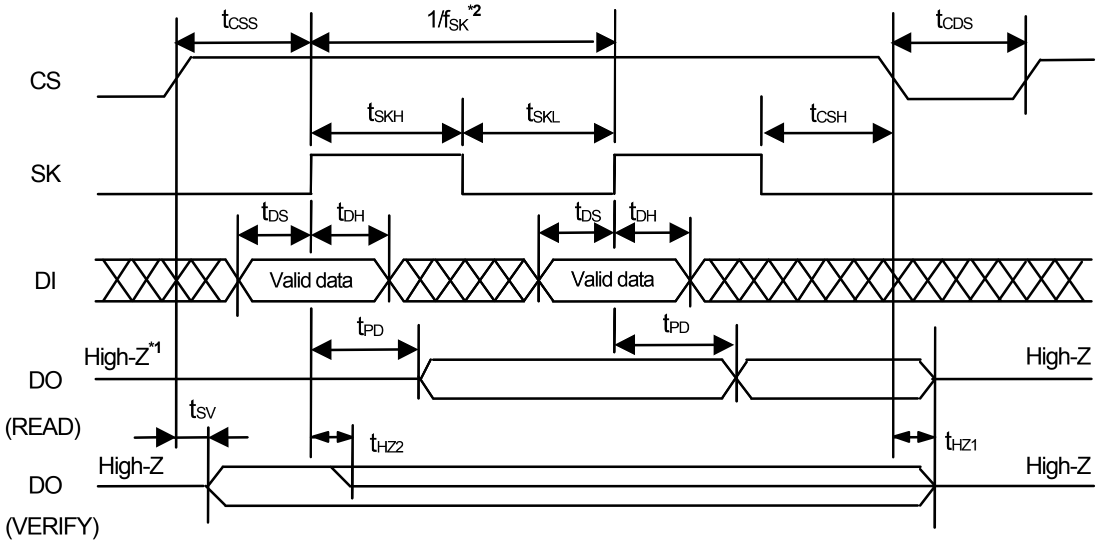
**Table 9 Measurement Conditions**

| | |
|---|---|
| Input pulse voltage | $0.1 \times V_{CC}$ to $0.9 \times V_{CC}$ |
| Output reference voltage | $0.5 \times V_{CC}$ |
| Output load | 100 pF |

**Table 10**

| Item | Symbol | Ta = −40°C to +85°C | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ = 1.6 V to 1.8 V | | $V_{CC}$ = 1.8 V to 2.5 V | | $V_{CC}$ = 2.5 V to 4.5 V | | $V_{CC}$ = 4.5 V to 5.5 V | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| CS pin setup time | $t_{CSS}$ | 0.4 | − | 0.2 | − | 0.15 | − | 0.15 | − | µs |
| CS pin hold time | $t_{CSH}$ | 0 | − | 0 | − | 0 | − | 0 | − | µs |
| CS pin deselect time | $t_{CDS}$ | 0.4 | − | 0.2 | − | 0.2 | − | 0.2 | − | µs |
| Data setup time | $t_{DS}$ | 0.2 | − | 0.1 | − | 0.1 | − | 0.1 | − | µs |
| Data hold time | $t_{DH}$ | 0.2 | − | 0.1 | − | 0.1 | − | 0.1 | − | µs |
| Output delay time | $t_{PD}$ | − | 0.8 | − | 0.6 | − | 0.25 | − | 0.25 | µs |
| Clock frequency[*1] | $f_{SK}$ | 0 | 0.5 | 0 | 1.0 | 0 | 2.0 | 0 | 2.0 | MHz |
| SK clock time "L"[*1] | $t_{SKL}$ | 0.5 | − | 0.2 | − | 0.2 | − | 0.1 | − | µs |
| SK clock time "H"[*1] | $t_{SKH}$ | 0.5 | − | 0.2 | − | 0.2 | − | 0.1 | − | µs |
| Output disable time | $t_{HZ1}$, $t_{HZ2}$ | 0 | 0.5 | 0 | 0.2 | 0 | 0.2 | 0 | 0.15 | µs |
| Output enable time | $t_{SV}$ | 0 | 0.5 | 0 | 0.2 | 0 | 0.2 | 0 | 0.15 | µs |
| Write time | $t_{PR}$ | − | 4.0 | − | 4.0 | − | 4.0 | − | 4.0 | ms |

***1.** The clock cycle of the SK clock (frequency $f_{SK}$) is $1/f_{SK}$ µs. This clock cycle is determined by a combination of several AC characteristics. Note that the clock cycle cannot be set as $(1/f_{SK}) = t_{SKL}$ (min.) + $t_{SKH}$ (min.) by minimizing the SK clock cycle time.



***1.** Indicates high impedance.

***2.** $1/f_{SK}$ is the SK clock cycle. This clock cycle is determined by a combination of several AC characteristics. Note that the clock cycle cannot be set as $(1/f_{SK}) = t_{SKL}$ (min.) + $t_{SKH}$ (min.) by minimizing the SK clock cycle time.

**Figure 1 Timing Chart**

## ■ Pin Functions

### 1. CS (chip select input) pin

This is an input pin to set a chip in the select status. In the "L" input level, this IC is in the non-select status and its output is "High-Z". This IC is in standby as long as it is not in write inside. This IC goes in active by setting the chip select to "H". Input any instruction code after power-on and a rising of chip select.

### 2. SK (serial clock input) pin

This is a clock input pin to set the timing of serial data. A start bit, an operation code, an address and a write data are received at a rising edge of clock. Data is output during rising edge of clock.

### 3. DI (serial data input) pin

This pin is to input serial data. This pin receives a start bit, an operation code, an address and a write data. This pin latches data at rising edge of serial clock.

### 4. SO (serial data output) pin

This pin is to output serial data. The data output changes at rising edge of serial clock.

### 5. TEST (test input) pin

This is an input pin in test mode. Connect to GND or the VCC pin, or set to open. Because this pin has a built-in pull-down element, pull-down current flows when it connected to VCC pin.

## ■ Initial Delivery State

Initial delivery state of all addresses is "FFFFh".

## ■ Instruction Sets

### 1. S-93C46C

**Table 11**

| Instruction | Start Bit | Operation Code | | Address | | | | | | Data |
|---|---|---|---|---|---|---|---|---|---|---|
| SK input clock | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 to 25 |
| READ (Data read) | 1 | 1 | 0 | A5 | A4 | A3 | A2 | A1 | A0 | D15 to D0 output[*1] |
| WRITE (Data write) | 1 | 0 | 1 | A5 | A4 | A3 | A2 | A1 | A0 | D15 to D0 input |
| ERASE (Data erase) | 1 | 1 | 1 | A5 | A4 | A3 | A2 | A1 | A0 | – |
| WRAL (Chip write) | 1 | 0 | 0 | 0 | 1 | x | x | x | x | D15 to D0 input |
| ERAL (Chip erase) | 1 | 0 | 0 | 1 | 0 | x | x | x | x | – |
| EWEN (Write enable) | 1 | 0 | 0 | 1 | 1 | x | x | x | x | – |
| EWDS (Write disable) | 1 | 0 | 0 | 0 | 0 | x | x | x | x | – |

***1.** When the 16-bit data in the specified address has been output, the data in the next address is output.

**Remark** x = Don't care.

### 2. S-93C56C

**Table 12**

| Instruction | Start Bit | Operation Code | | Address | | | | | | | | Data |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SK input clock | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 to 27 |
| READ (Data read) | 1 | 1 | 0 | x | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D15 to D0 output[*1] |
| WRITE (Data write) | 1 | 0 | 1 | x | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D15 to D0 input |
| ERASE (Data erase) | 1 | 1 | 1 | x | A6 | A5 | A4 | A3 | A2 | A1 | A0 | – |
| WRAL (Chip write) | 1 | 0 | 0 | 0 | 1 | x | x | x | x | x | x | D15 to D0 input |
| ERAL (Chip erase) | 1 | 0 | 0 | 1 | 0 | x | x | x | x | x | x | – |
| EWEN (Write enable) | 1 | 0 | 0 | 1 | 1 | x | x | x | x | x | x | – |
| EWDS (Write disable) | 1 | 0 | 0 | 0 | 0 | x | x | x | x | x | x | – |

***1.** When the 16-bit data in the specified address has been output, the data in the next address is output.

**Remark** x = Don't care.

### 3. S-93C66C

**Table 13**

| Instruction | Start Bit | Operation Code | | Address | | | | | | | | Data |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SK input clock | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 to 27 |
| READ (Data read) | 1 | 1 | 0 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D15 to D0 output[*1] |
| WRITE (Data write) | 1 | 0 | 1 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D15 to D0 input |
| ERASE (Data erase) | 1 | 1 | 1 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | – |
| WRAL (Chip write) | 1 | 0 | 0 | 0 | 1 | x | x | x | x | x | x | D15 to D0 input |
| ERAL (Chip erase) | 1 | 0 | 0 | 1 | 0 | x | x | x | x | x | x | – |
| EWEN (Write enable) | 1 | 0 | 0 | 1 | 1 | x | x | x | x | x | x | – |
| EWDS (Write disable) | 1 | 0 | 0 | 0 | 0 | x | x | x | x | x | x | – |

***1.** When the 16-bit data in the specified address has been output, the data in the next address is output.

**Remark** x = Don't care.

## 4. S-93C76C

**Table 14**

| Instruction | Start Bit | Operation Code | | Address | | | | | | | | | | Data |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SK input clock | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 to 29 |
| READ (Data read) | 1 | 1 | 0 | x | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D15 to D0 output[*1] |
| WRITE (Data write) | 1 | 0 | 1 | x | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D15 to D0 input |
| ERASE (Data erase) | 1 | 1 | 1 | x | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | − |
| WRAL (Chip write) | 1 | 0 | 0 | 0 | 1 | x | x | x | x | x | x | x | x | D15 to D0 input |
| ERAL (Chip erase) | 1 | 0 | 0 | 1 | 0 | x | x | x | x | x | x | x | x | − |
| EWEN (Write enable) | 1 | 0 | 0 | 1 | 1 | x | x | x | x | x | x | x | x | − |
| EWDS (Write disable) | 1 | 0 | 0 | 0 | 0 | x | x | x | x | x | x | x | x | − |

***1.** When the 16-bit data in the specified address has been output, the data in the next address is output.

**Remark** x = Don't care.

## 5. S-93C86C

**Table 15**

| Instruction | Start Bit | Operation Code | | Address | | | | | | | | | | Data |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SK input clock | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 to 29 |
| READ (Data read) | 1 | 1 | 0 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D15 to D0 output[*1] |
| WRITE (Data write) | 1 | 0 | 1 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D15 to D0 input |
| ERASE (Data erase) | 1 | 1 | 1 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | − |
| WRAL (Chip write) | 1 | 0 | 0 | 0 | 1 | x | x | x | x | x | x | x | x | D15 to D0 input |
| ERAL (Chip erase) | 1 | 0 | 0 | 1 | 0 | x | x | x | x | x | x | x | x | − |
| EWEN (Write enable) | 1 | 0 | 0 | 1 | 1 | x | x | x | x | x | x | x | x | − |
| EWDS (Write disable) | 1 | 0 | 0 | 0 | 0 | x | x | x | x | x | x | x | x | − |

***1.** When the 16-bit data in the specified address has been output, the data in the next address is output.

**Remark** x = Don't care.

## ■ Operation

All instructions are executed by inputting the DI pin in synchronization with the rising of the SK pulse after the CS pin goes to "H". An instruction set is input in the order of start bit, instruction, address, and data.
Instruction input finishes when the CS pin goes to "L". "L" must be input to the CS pin between commands during $t_{CDS}$. While "L" is being input to the CS pin, this IC is in standby mode, so the SK pin and the DI pin inputs are invalid and no instructions are allowed.

### 1. Start Bit

A start bit is recognized when the DI pin goes to "H" at the rising of the SK pulse after the CS pin goes to "H". After the CS pin goes to "H", a start bit is not recognized even if the SK pulse is input as long as the DI pin is "L".

#### 1. 1 Dummy clock

The SK clocks input while the DI pin is "L" before a start bit is input are called dummy clocks. Dummy clocks are effective when aligning the number of instruction sets (clocks) sent by the CPU with those required for serial memory operation. For example, when the CPU instruction set is 16 bits, the number of instruction set clocks can be adjusted by inserting the 7-bit dummy clock in S-93C46C, the 5-bit dummy clock in S-93C56C/66C and the 3-bit dummy clock in S-93C76C/86C.

#### 1. 2 Start bit input failure

(1) When the output of the DO pin is "H" during the verify period after a write operation, if "H" is input to the DI pin at the rising of the SK pulse, this IC recognizes that a start bit has been input. To prevent this failure, input "L" to the DI pin during the verify operation period (refer to "**3. 1 Verify operation**").

(2) When a 3-wire interface is configured by connecting the DI input pin and the DO output pin, a period in which the data output from the CPU and the serial memory collide may be generated, preventing successful input of the start bit. Take the measures described in "**■ 3-Wire Interface (Direct Connection between DI Pin and DO Pin**)".

### 2. Reading (READ)

The READ instruction reads data from a specified address.
After the CS pin goes to "H", input an instruction in the order of the start bit, read instruction, and address. Since the last input address ($A_0$) has been latched, the output status of the DO pin changes from "High-Z" to "L", which is held until the next rising of the SK pulse. 16-bit data starts to be output in synchronization with the next rising of the SK pulse.

#### 2. 1 Sequential read

After the 16-bit data at the specified address has been output, inputting the SK pulse while the CS pin is "H" automatically increments the address, and causes the 16-bit data at the next address to be output sequentially. The above method makes it possible to read the data in the whole memory space. The last address ($A_n$ ••• $A_1$ $A_0$ = 1 ••• 1 1) rolls over to the top address ($A_n$ ••• $A_1$ $A_0$ = 0 ••• 0 0).

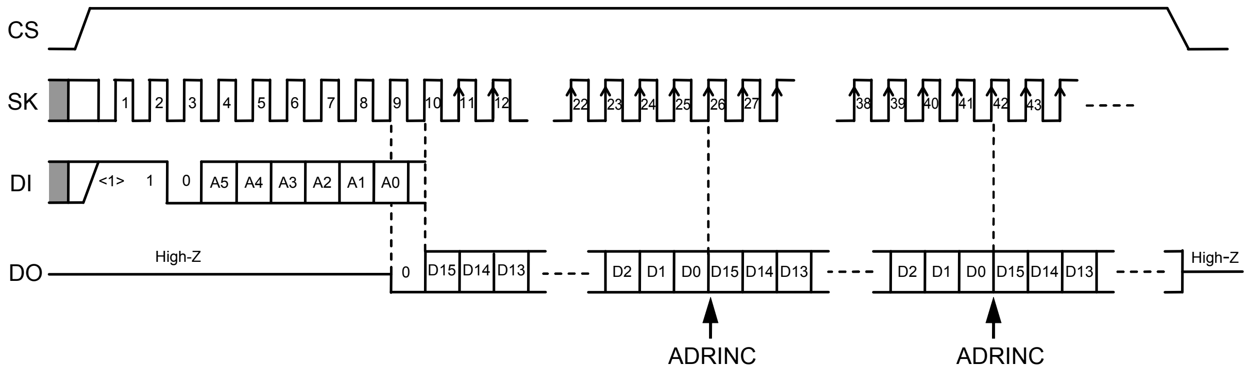

CS
SK
1 2 3 4 5 6 7 8 9 10 11 12
22 23 24 25 26 27
38 39 40 41 42 43
DI
<1>
1
0
A5 A4 A3 A2 A1 A0
DO
High-Z
0
D15 D14 D13
D2 D1 D0 D15 D14 D13
D2 D1 D0 D15 D14 D13
High-Z
ADRINC
ADRINC

Figure 2 Read Timing (S-93C46C)

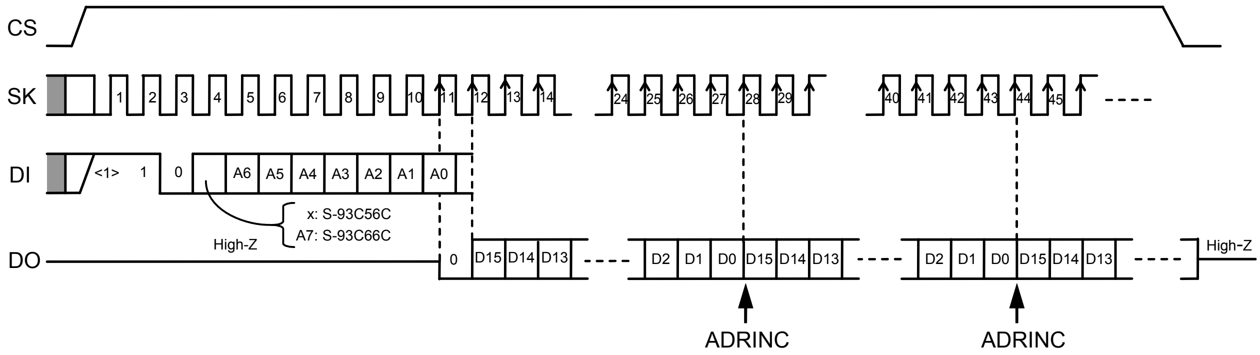

CS
SK
1 2 3 4 5 6 7 8 9 10 11 12 13 14
24 25 26 27 28 29
40 41 42 43 44 45
DI
<1>
1
0
A6 A5 A4 A3 A2 A1 A0
x: S-93C56C
A7: S-93C66C
DO
High-Z
0
D15 D14 D13
D2 D1 D0 D15 D14 D13
D2 D1 D0 D15 D14 D13
High-Z
ADRINC
ADRINC

Figure 3 Read Timing (S-93C56C/66C)

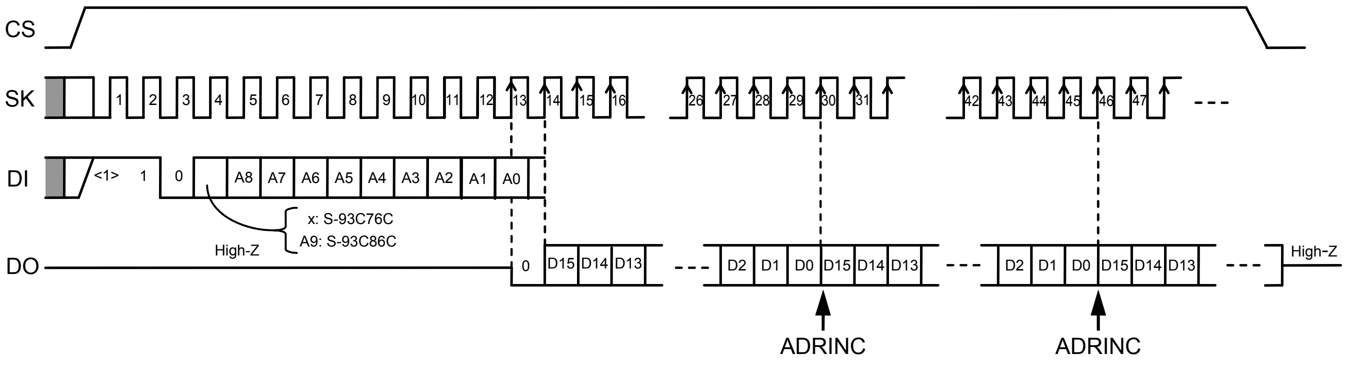

CS
SK
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
26 27 28 29 30 31
42 43 44 45 46 47
DI
<1>
1
0
A8 A7 A6 A5 A4 A3 A2 A1 A0
x: S-93C76C
A9: S-93C86C
DO
High-Z
0
D15 D14 D13
D2 D1 D0 D15 D14 D13
D2 D1 D0 D15 D14 D13
High-Z
ADRINC
ADRINC

Figure 4 Read Timing (S-93C76C/86C)

## 3. Writing (WRITE, ERASE, WRAL, ERAL)

A write operation includes four write instructions: data write (WRITE), data erase (ERASE), chip write (WRAL), and chip erase (ERAL).
A write instruction (WRITE, ERASE, WRAL, ERAL) starts a write operation to the memory cell when "L" is input to the CS pin after a specified number of clocks have been input. The SK pin and the DI pin inputs are invalid during the write period, so do not input an instruction.
Input an instruction while the output status of the DO pin is "H" or "High-Z".
A write operation is valid only in program enable mode (refer to "**4. Write enable (EWEN) / write disable (EWDS)**").

### 3. 1 Verify operation

A write operation executed by any instruction is completed within 4 ms (write time $t_{PR}$), so if the completion of the write operation is recognized, the write cycle can be minimized. A sequential operation to confirm the status of a write operation is called a verify operation.

#### 3. 1. 1 Operation method

After the write operation has started (CS pin = "L"), the status of the write operation can be verified by confirming the output status of the DO pin by inputting "H" to the CS pin again. This sequence is called a verify operation, and the period that "H" is input to the CS pin after the write operation has started is called the verify operation period.
The relationship between the output status of the DO pin and the write operation during the verify operation period is as follows.

(1) DO pin = "L": Writing in progress (busy)
(2) DO pin = "H": Writing completed (ready)

#### 3. 1. 2 Operation example

There are two methods to perform a verify operation: Waiting for a change in the output of the DO pin while keeping the CS pin "H", or suspending the verify operation (CS pin = "L") once and then performing it again to verify the output of the DO pin. The latter method allows the CPU to perform other processing during the wait period, allowing an efficient system to be designed.

**Caution 1. Input "L" to the DI pin during a verify operation.**
**2. If "H" is input to the DI pin at the rising of the SK pulse when the output status of the DO pin is "H", this IC latches the instruction assuming that a start bit has been input. In this case, note that the DO pin immediately enters "High-Z".**

### 3. 2 Writing data (WRITE)

To write 16-bit data to a specified address, change the CS pin to "H" and then input the WRITE instruction, address, and 16-bit data following the start bit. The write operation starts when the CS pin goes to "L". There is no need to set the data to "1" before writing. When the clocks more than the specified number have been input, the clock pulse monitoring circuit cancels the WRITE instruction. For details of the clock pulse monitoring circuit, refer to "**■ Function to Protect Against Write due to Erroneous Instruction Recognition**".

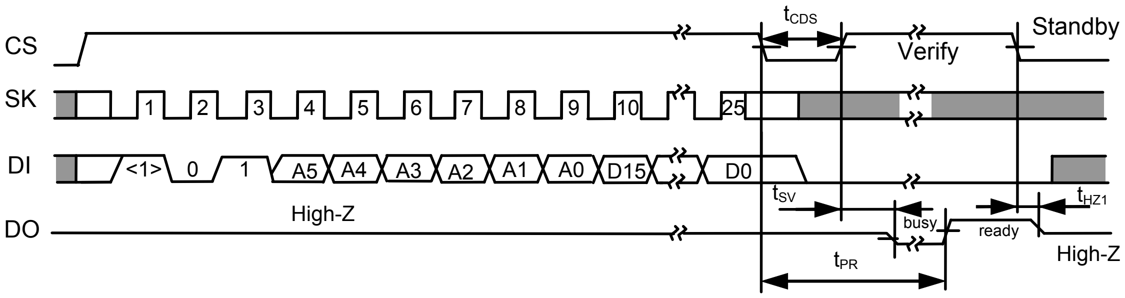

CS
SK
DI
DO
$t_{CDS}$
Standby
Verify
1 2 3 4 5 6 7 8 9 10 25
<1> 0 1 A5 A4 A3 A2 A1 A0 D15 D0
$t_{SV}$
$t_{HZ1}$
High-Z
busy
ready
High-Z
$t_{PR}$

Figure 5 Data Write Timing (S-93C46C)

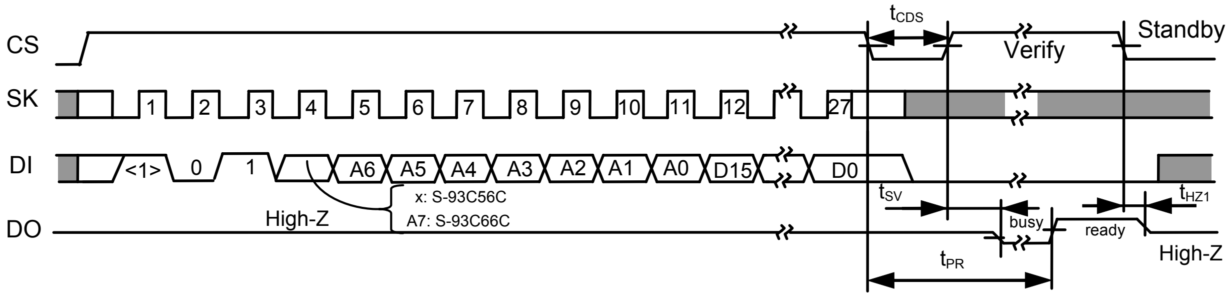

CS
SK
DI
DO
$t_{CDS}$
Standby
Verify
1 2 3 4 5 6 7 8 9 10 11 12 27
<1> 0 1 A6 A5 A4 A3 A2 A1 A0 D15 D0
x: S-93C56C
A7: S-93C66C
High-Z
$t_{SV}$
$t_{HZ1}$
busy
ready
High-Z
$t_{PR}$

Figure 6 Data Write Timing (S-93C56C/66C)

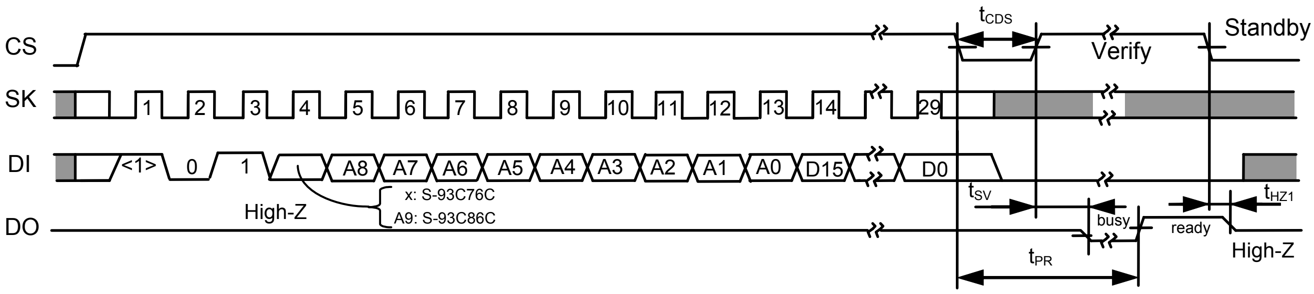

CS
SK
DI
DO
$t_{CDS}$
Standby
Verify
1 2 3 4 5 6 7 8 9 10 11 12 13 14 29
<1> 0 1 A8 A7 A6 A5 A4 A3 A2 A1 A0 D15 D0
x: S-93C76C
A9: S-93C86C
High-Z
$t_{SV}$
$t_{HZ1}$
busy
ready
High-Z
$t_{PR}$

Figure 7 Data Write Timing (S-93C76C/86C)

### 3. 3 Erasing data (ERASE)

To erase 16-bit data at a specified address, set all 16 bits of the data to "1", change the CS pin to "H", and then input the ERASE instruction and address following the start bit. There is no need to input data. The data erase operation starts when the CS pin goes to "L". When the clocks more than the specified number have been input, the clock pulse monitoring circuit cancels the ERASE instruction. For details of the clock pulse monitoring circuit, refer to "**■ Function to Protect Against Write due to Erroneous Instruction Recognition**".

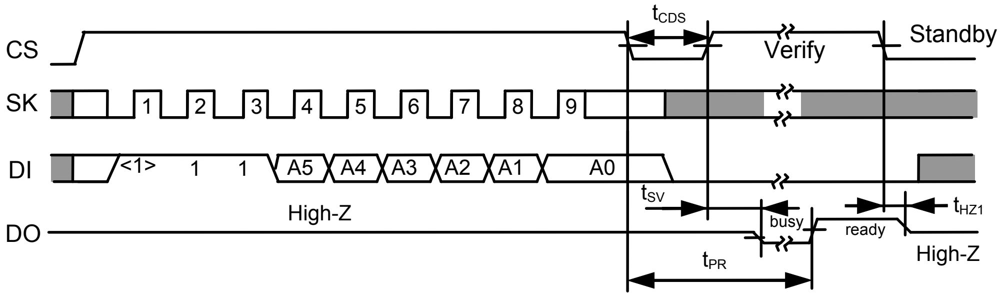

CS
SK
DI
DO
$t_{CDS}$
Verify
Standby
1 2 3 4 5 6 7 8 9
<1> 1 1 A5 A4 A3 A2 A1 A0
High-Z
$t_{SV}$
busy
ready
$t_{HZ1}$
$t_{PR}$
High-Z

Figure 8 Data Erase Timing (S-93C46C)

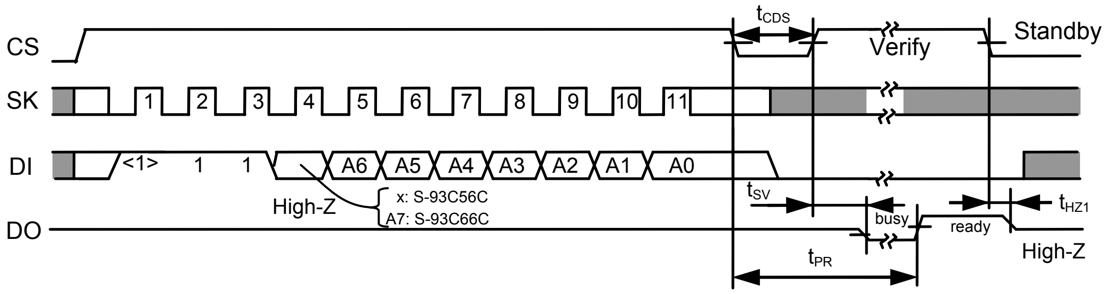

CS
SK
DI
DO
$t_{CDS}$
Verify
Standby
1 2 3 4 5 6 7 8 9 10 11
<1> 1 1 A6 A5 A4 A3 A2 A1 A0
High-Z
x: S-93C56C
A7: S-93C66C
$t_{SV}$
busy
ready
$t_{HZ1}$
$t_{PR}$
High-Z

Figure 9 Data Erase Timing (S-93C56C/66C)

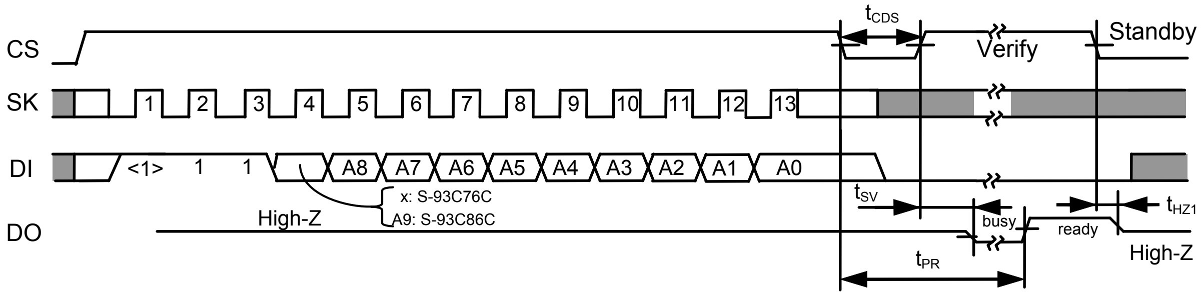

CS
SK
DI
DO
$t_{CDS}$
Verify
Standby
1 2 3 4 5 6 7 8 9 10 11 12 13
<1> 1 1 A8 A7 A6 A5 A4 A3 A2 A1 A0
High-Z
x: S-93C76C
A9: S-93C86C
$t_{SV}$
busy
ready
$t_{HZ1}$
$t_{PR}$
High-Z

Figure 10 Data Erase Timing (S-93C76C/86C)

### 3. 4 Writing to chip (WRAL)

To write the same 16-bit data to the entire memory address space, change the CS pin to "H", and then input the WRAL instruction, an address, and 16-bit data following the start bit. Any address can be input. The write operation starts when the CS pin goes to "L". There is no need to set the data to "1" before writing. When the clocks more than the specified number have been input, the clock pulse monitoring circuit cancels the WRAL instruction. For details of the clock pulse monitoring circuit, refer to "**■ Function to Protect Against Write due to Erroneous Instruction Recognition**".

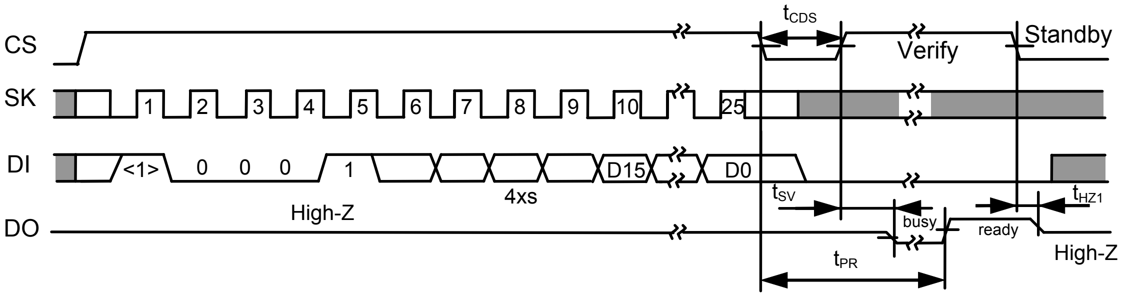

CS
SK
DI
DO
$t_{CDS}$
Verify
Standby
1
2
3
4
5
6
7
8
9
10
25
<1>
0 0 0
1
D15
D0
4xs
High-Z
$t_{SV}$
busy
ready
$t_{HZ1}$
$t_{PR}$
High-Z

**Figure 11 Chip Write Timing (S-93C46C)**

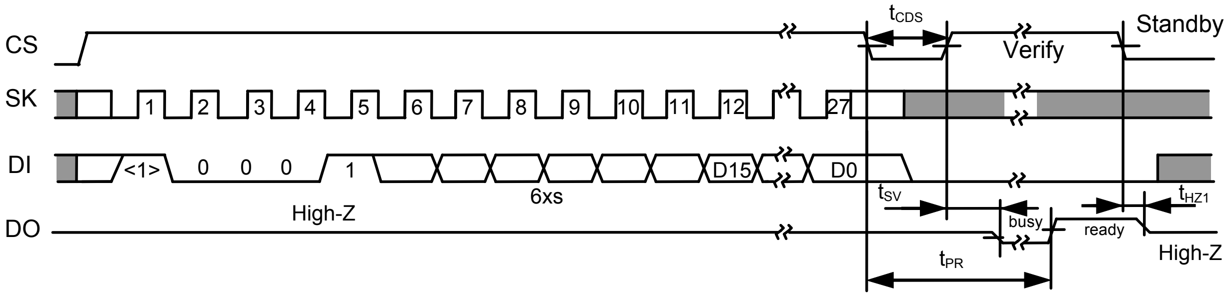

CS
SK
DI
DO
$t_{CDS}$
Verify
Standby
1
2
3
4
5
6
7
8
9
10
11
12
27
<1>
0 0 0
1
D15
D0
6xs
High-Z
$t_{SV}$
busy
ready
$t_{HZ1}$
$t_{PR}$
High-Z

**Figure 12 Chip Write Timing (S-93C56C/66C)**

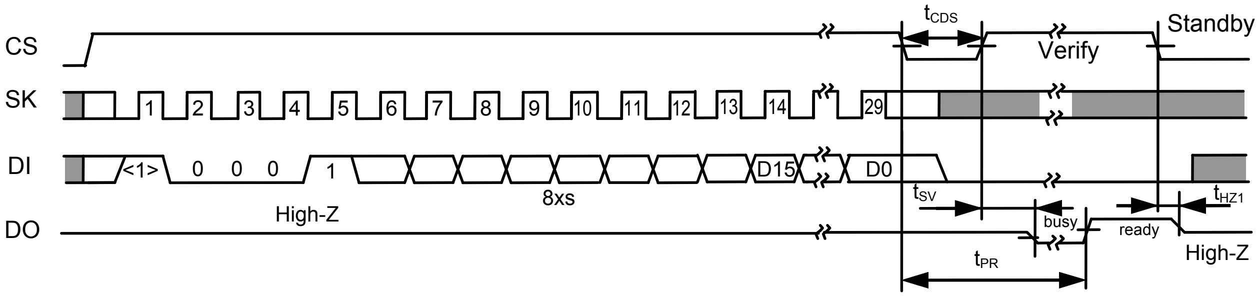

CS
SK
DI
DO
$t_{CDS}$
Verify
Standby
1
2
3
4
5
6
7
8
9
10
11
12
13
14
29
<1>
0 0 0
1
D15
D0
8xs
High-Z
$t_{SV}$
busy
ready
$t_{HZ1}$
$t_{PR}$
High-Z

**Figure 13 Chip Write Timing (S-93C76C/86C)**

### 3. 5 Erasing chip (ERAL)

To erase the data of the entire memory address space, set all the data to "1", change the CS pin to "H", and then input the ERAL instruction and an address following the start bit. Any address can be input. There is no need to input data. The chip erase operation starts when the CS pin goes to "L". When the clocks more than the specified number have been input, the clock pulse monitoring circuit cancels the ERAL instruction. For details of the clock pulse monitoring circuit, refer to "**■ Function to Protect Against Write due to Erroneous Instruction Recognition**".

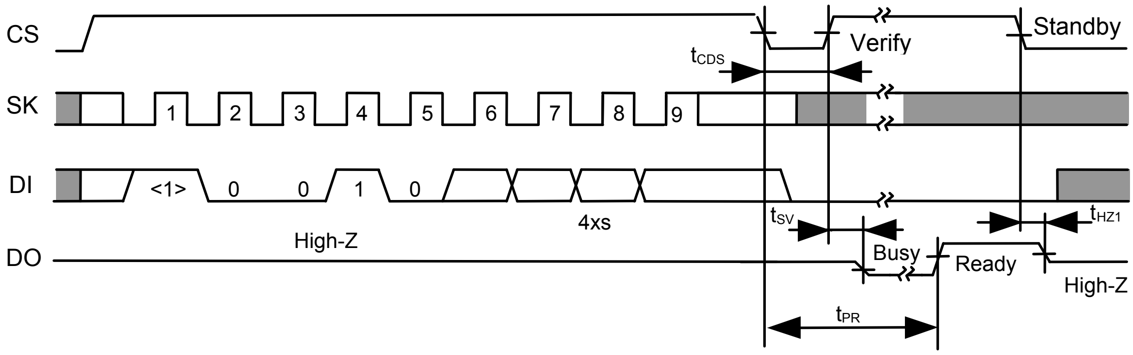

CS
SK
DI
DO
$t_{CDS}$
Verify
Standby
1
2
3
4
5
6
7
8
9
<1>
0
0
1
0
4xs
High-Z
$t_{SV}$
$t_{HZ1}$
Busy
Ready
High-Z
$t_{PR}$

Figure 14 Chip Erase Timing (S-93C46C)

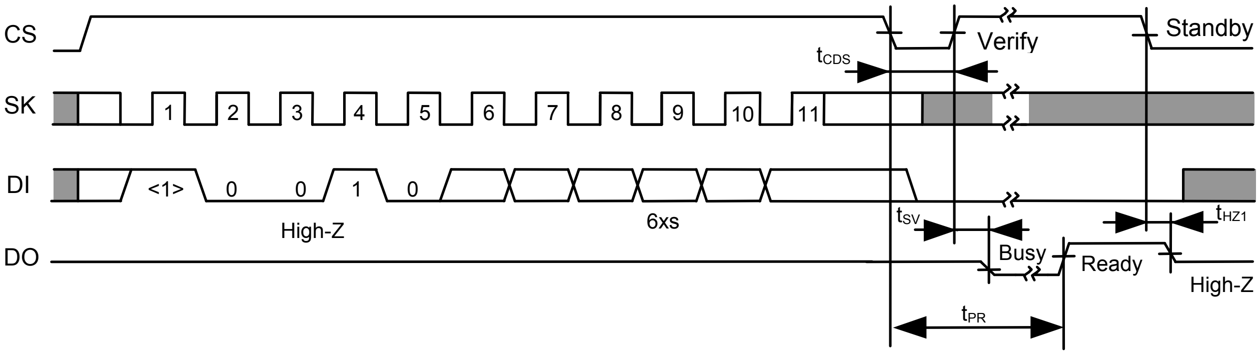

CS
SK
DI
DO
$t_{CDS}$
Verify
Standby
1
2
3
4
5
6
7
8
9
10
11
<1>
0
0
1
0
6xs
High-Z
$t_{SV}$
$t_{HZ1}$
Busy
Ready
High-Z
$t_{PR}$

Figure 15 Chip Erase Timing (S-93C56C/66C)

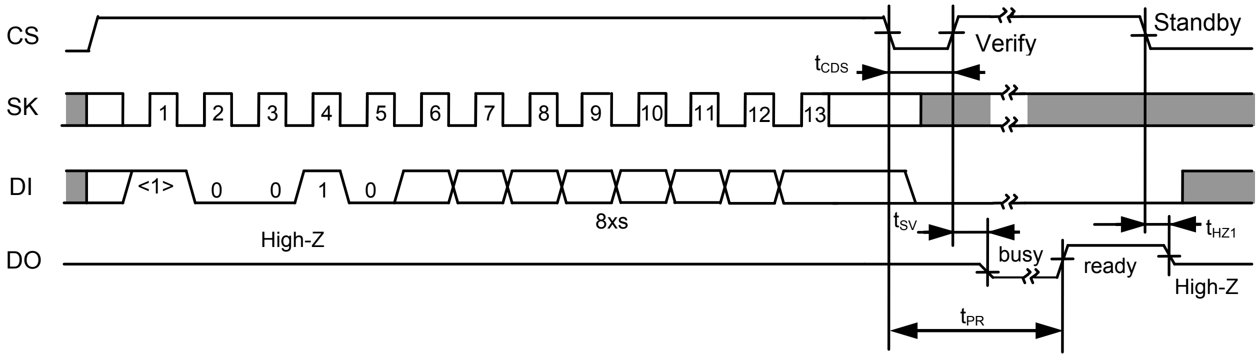

CS
SK
DI
DO
$t_{CDS}$
Verify
Standby
1
2
3
4
5
6
7
8
9
10
11
12
13
<1>
0
0
1
0
8xs
High-Z
$t_{SV}$
$t_{HZ1}$
busy
ready
High-Z
$t_{PR}$

Figure 16 Chip Erase Timing (S-93C76C/86C)

### 4. Write enable (EWEN) / write disable (EWDS)

The EWEN instruction is an instruction that enables a write operation. The status in which a write operation is enabled is called the program enable mode.

The EWDS instruction is an instruction that disables a write operation. The status in which a write operation is disabled is called the program disable mode.

After the CS pin goes to "H", input an instruction in the order of the start bit, EWEN or EWDS instruction, and address (optional). Each mode becomes valid by inputting "L" to the CS pin after the last address (optional) has been input.

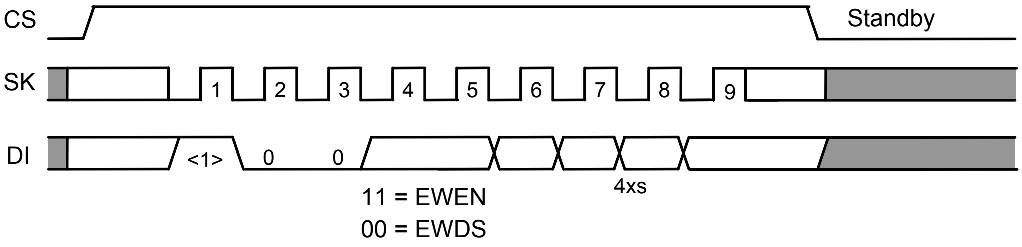

CS
Standby
SK
1
2
3
4
5
6
7
8
9
DI
<1>
0
0
11 = EWEN
00 = EWDS
4xs

**Figure 17 Write Enable / Disable Timing (S-93C46C)**

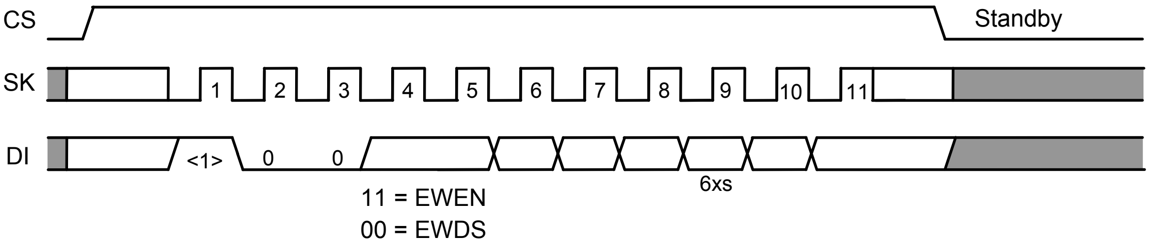

CS
Standby
SK
1
2
3
4
5
6
7
8
9
10
11
DI
<1>
0
0
11 = EWEN
00 = EWDS
6xs

**Figure 18 Write Enable / Disable Timing (S-93C56C/66C)**

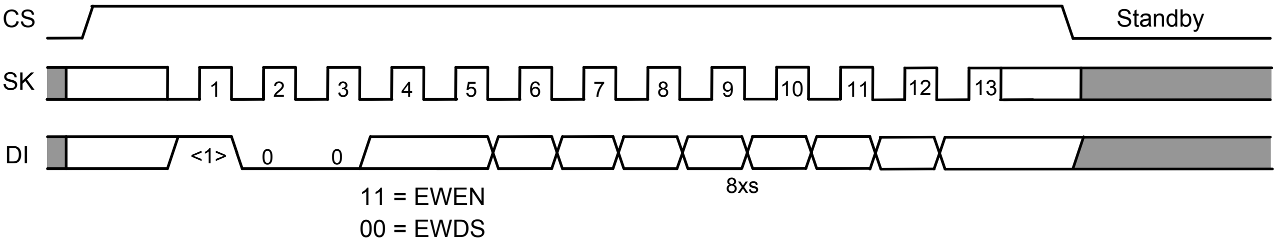

CS
Standby
SK
1
2
3
4
5
6
7
8
9
10
11
12
13
DI
<1>
0
0
11 = EWEN
00 = EWDS
8xs

**Figure 19 Write Enable / Disable Timing (S-93C76C/86C)**

**Remark** It is recommended to execute an EWDS instruction for preventing an incorrect write operation if a write instruction is erroneously recognized when executing instructions other than write instruction, and immediately after power-on and before power-off.

## ■ Write Protect Function during the Low Power Supply Voltage

This IC provides a built-in detection circuit to detect a low power supply voltage. When the power supply voltage is low or at power-on, the write instructions (WRITE, ERASE, WRAL, and ERAL) are cancelled, and the write disable (EWDS) status is automatically set. The detection voltage and the release voltage are 1.2 V typ. (refer to **Figure 20**).

Therefore, when a write operation is performed after the power supply voltage has dropped and then risen again up to the level at which writing is possible, a write enable instruction (EWEN) must be sent before a write instruction (WRITE, ERASE, WRAL, or ERAL) is executed.

When the power supply voltage drops during a write operation, the data being written to an address at that time is not guaranteed.

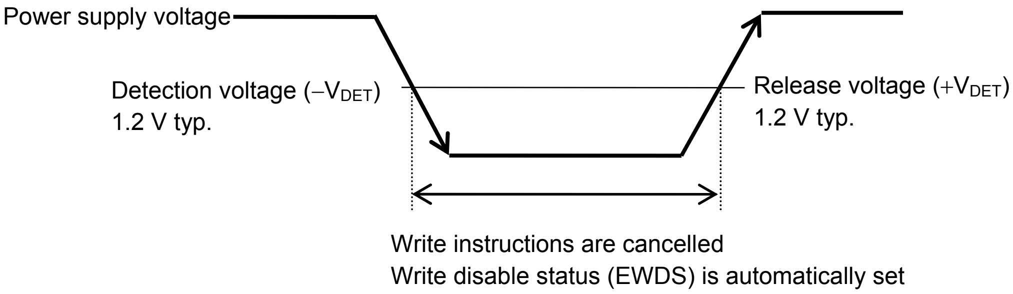
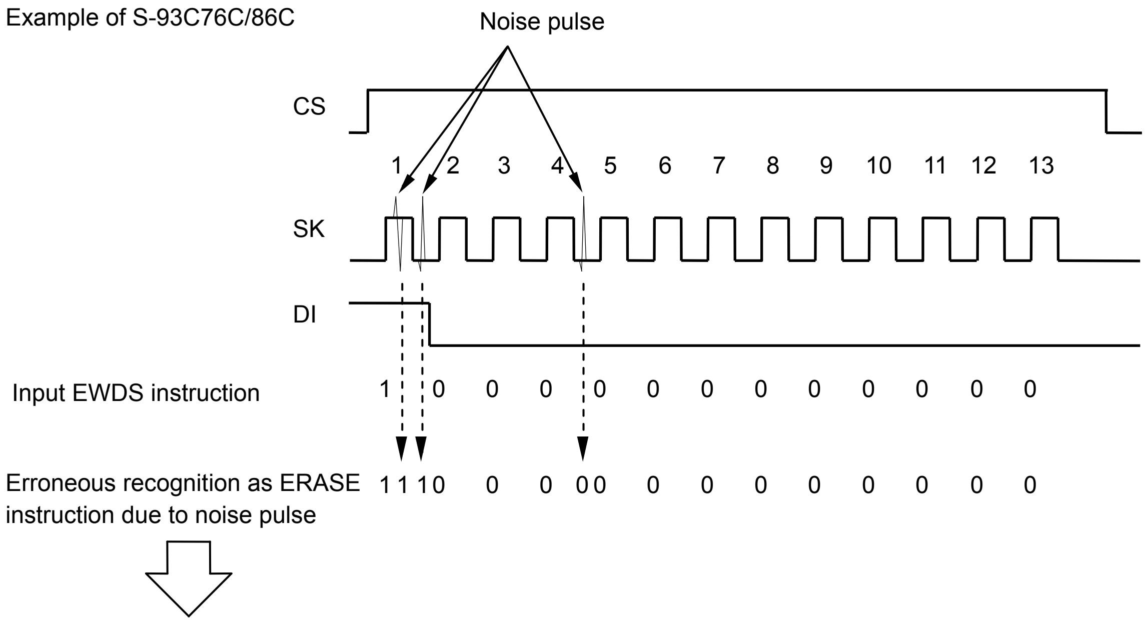

Power supply voltage
Detection voltage ($-V_{DET}$)
1.2 V typ.
Release voltage ($+V_{DET}$)
1.2 V typ.
Write instructions are cancelled
Write disable status (EWDS) is automatically set

**Figure 20 Operation during the Low Power Supply Voltage**

## ■ Function to Protect Against Write due to Erroneous Instruction Recognition

This IC provides a built-in clock pulse monitoring circuit which is used to prevent an erroneous write operation by canceling write instructions (WRITE, ERASE, WRAL, and ERAL) recognized erroneously due to an erroneous clock count caused by the application of noise pulses or double counting of clocks. Instructions are cancelled if a clock pulse whose count other than the one specified for each write instruction (WRITE, ERASE, WRAL, or ERAL) is detected.

**Example: Erroneous Recognition of EWDS as ERASE**


Example of S-93C76C/86C
Noise pulse
CS
1 2 3 4 5 6 7 8 9 10 11 12 13
SK
DI
Input EWDS instruction
1 0 0 0 0 0 0 0 0 0 0 0 0
Erroneous recognition as ERASE instruction due to noise pulse
1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0

In products that do not incorporate a clock pulse monitoring circuit, "FFFFh" is mistakenly written to address 00h. However the S-93C76C/86C detects the overcount and cancels the instruction without performing a write operation.

**Figure 21 Example of Clock Pulse Monitoring Circuit Operation**

## ■ 3-Wire Interface (Direct Connection between DI Pin and DO Pin)

There are two types of serial interface configurations: a 4-wire interface configured using the CS pin, the SK pin, the DI pin and the DO pin and a 3-wire interface that connects the DI pin and the DO pin.
When the 3-wire interface is employed, a period in which the data output from the CPU and the data output from the serial memory collide may occur, causing a malfunction. To prevent such a malfunction, connect the DI pin and the DO pin of this IC via a resistor (10 kΩ to 100 kΩ) so that the data output from the CPU takes precedence in being input to the DI pin (refer to **Figure 22**).

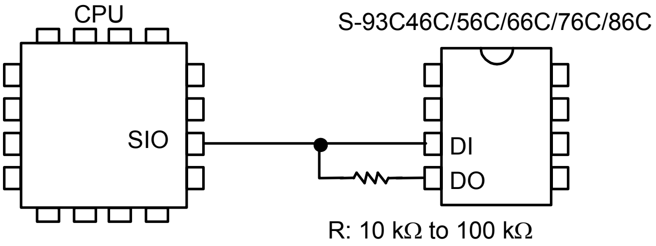


**Figure 22 Connection of 3-Wire Interface**

## ■ Input Pin and Output Pin

### 1. Connection of input pin

All input pins in this IC have the CMOS structure. Do not set these pins in "High-Z" during operation when you design. Especially, set the CS pin to "L" at power-on, power-off, and during standby. The error write does not occur as long as the CS pin is "L". Set the CS pin to GND via a resistor (the pull-down resistor of 10 kΩ to 100 kΩ).
To prevent the error for sure, it is recommended to use equivalent pull-down resistors for input pins other than the CS pin.

### 2. Equivalent circuit of input pin and output pin

**Figure 23**, **Figure 24** and **Figure 25** show the equivalent circuits of input pins in this IC. In **Figure 23** and **Figure 24**, none of the input pins incorporate pull-up and pull-down elements, so special care must be taken when designing to prevent a floating status.
In **Figure 25**, the TEST pin has a built-in pull-down element.
**Figure 26** shows the equivalent circuit of the output pin. This pin has the tri-state output of "H" / "L" / "High-Z".

### 2. 1 Input pin

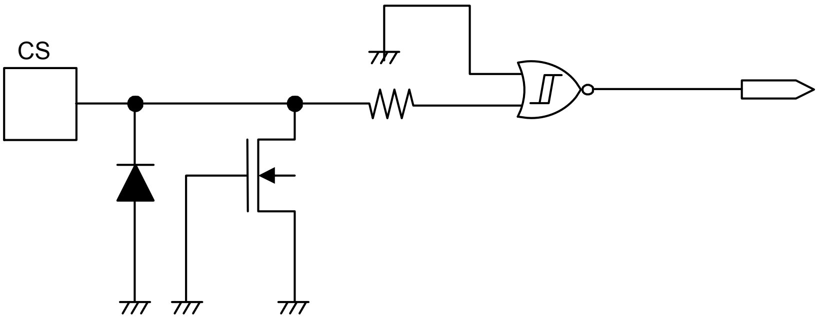


Figure 23 CS Pin

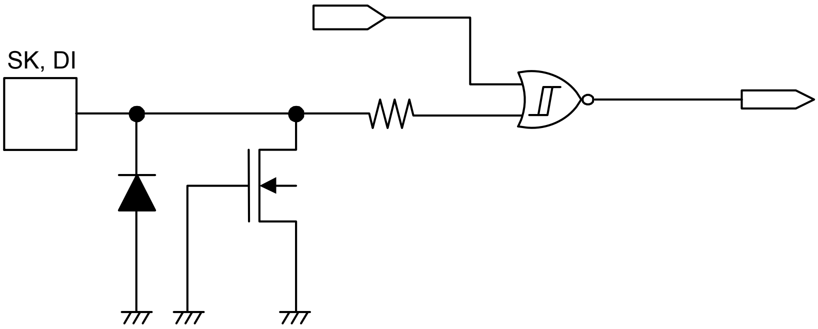


Figure 24 SK, DI Pin

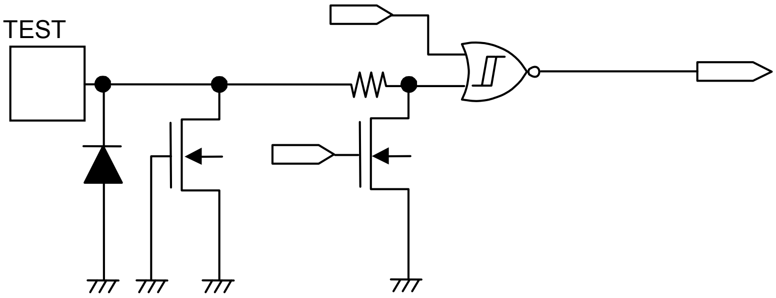


Figure 25 TEST Pin

### 2. 2 Output pin

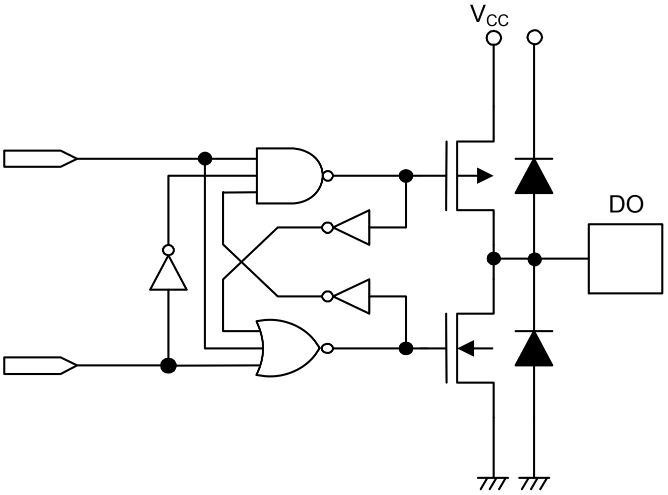


Figure 26 DO Pin

### 3. Input pin noise suppression time

This IC has a built-in low-pass filter at the SK pin, the DI pin and the CS pin to suppress noise. If the supply voltage is 5.0 V, noise with a pulse width of 20 ns or less at room temperature can be suppressed by the low-pass filter.
Note that noise with a pulse width of more than 20 ns is recognized as a pulse since the noise can not be suppressed if the voltage exceeds $V_{IH}$ / $V_{IL}$.

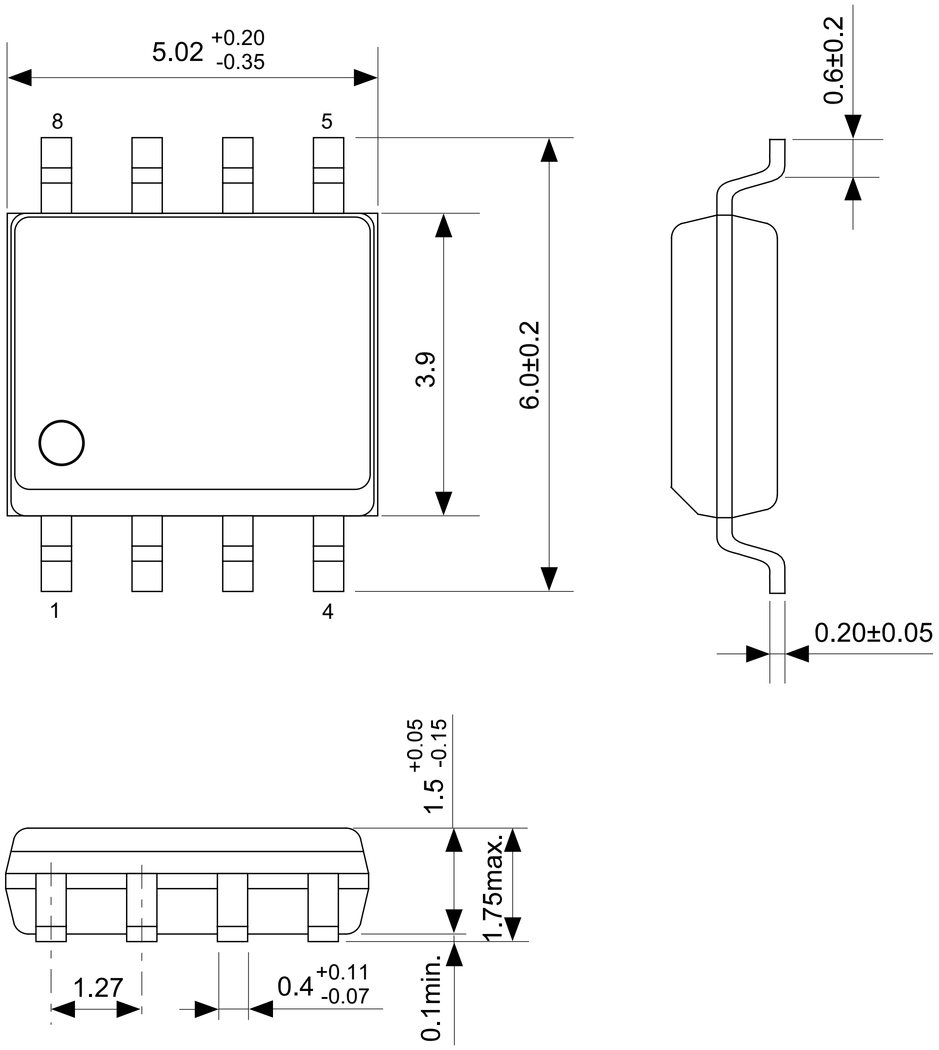
## ■ Precautions

- Do not operate these ICs in excess of the absolute maximum ratings. Attention should be paid to the power supply voltage, especially. The surge voltage which exceeds the absolute maximum ratings can cause latch-up and malfunction. Perform operations after confirming the detailed operation condition in the data sheet.

- Operations with moisture on this IC's pins may occur malfunction by short-circuit between pins. Especially, in occasions like picking this IC up from low temperature tank during the evaluation. Be sure that not remain frost on this IC's pin to prevent malfunction by short-circuit.
  Also attention should be paid in using on environment, which is easy to dew for the same reason.

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

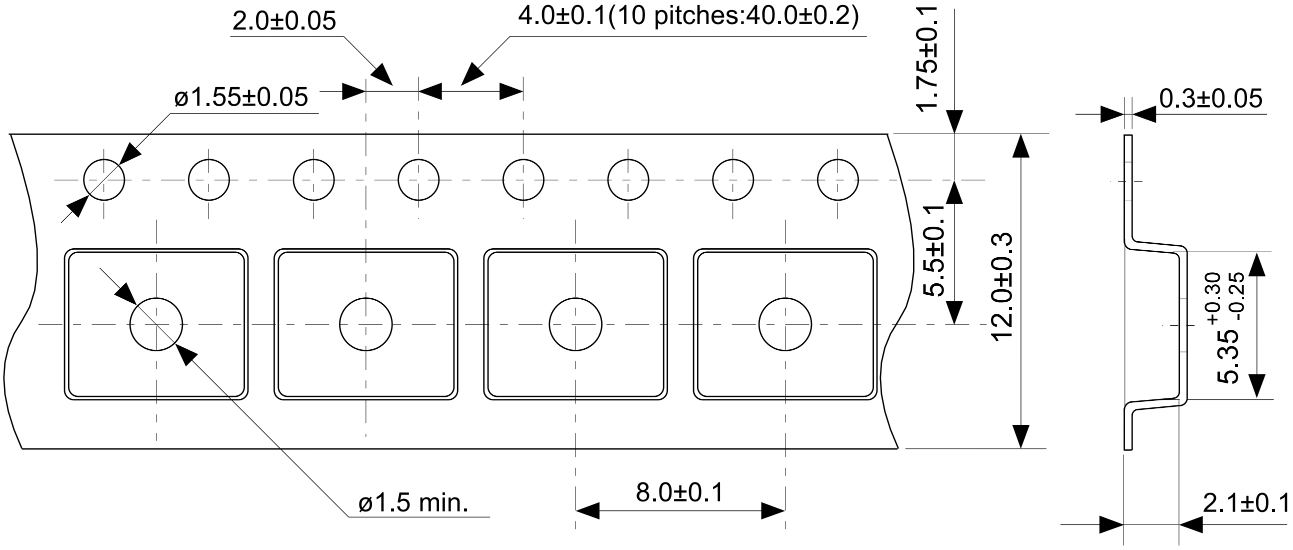


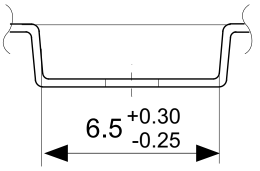
5.02 +0.20 -0.35
8
5
1
4
3.9
6.0±0.2
0.6±0.2
0.20±0.05
1.5 +0.05 -0.15
1.75max.
1.27
0.4 +0.11 -0.07
0.1min.

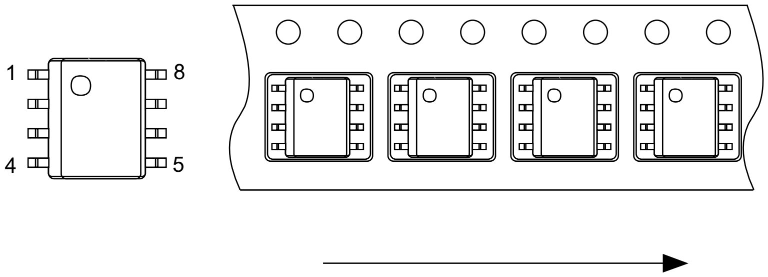
No. FJ008-Z-P-SD-2.1

| | |
|---|---|
| TITLE | SOP8J-Z-PKG Dimensions |
| No. | FJ008-Z-P-SD-2.1 |
| ANGLE | |
| UNIT | mm |
| | |

**ABLIC Inc.**


2.0±0.05
4.0±0.1(10 pitches:40.0±0.2)
ø1.55±0.05
1.75±0.1
5.5±0.1
12.0±0.3
0.3±0.05
5.35 +0.30 -0.25
ø1.5 min.
8.0±0.1
2.1±0.1



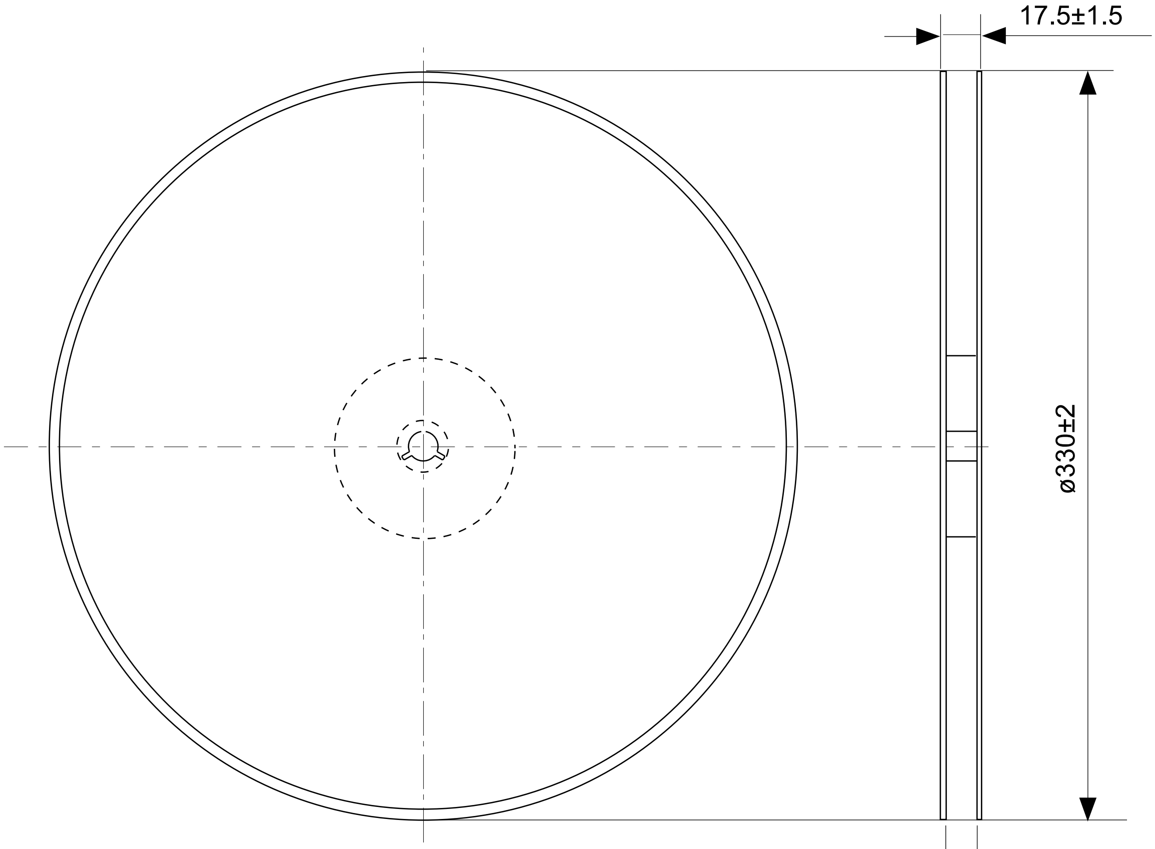


Feed direction

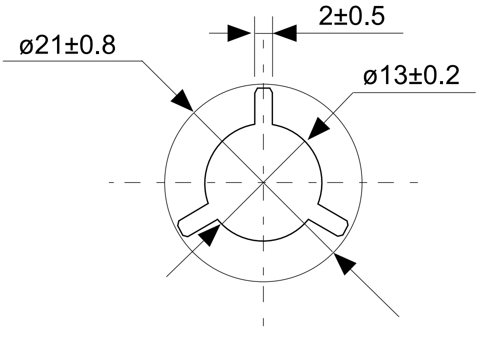
No. FJ008-Z-C-SD-1.0

| | |
|---|---|
| TITLE | SOP8J-Z-Carrier Tape |
| No. | FJ008-Z-C-SD-1.0 |
| ANGLE | |
| UNIT | mm |
| | |

**ABLIC Inc.**

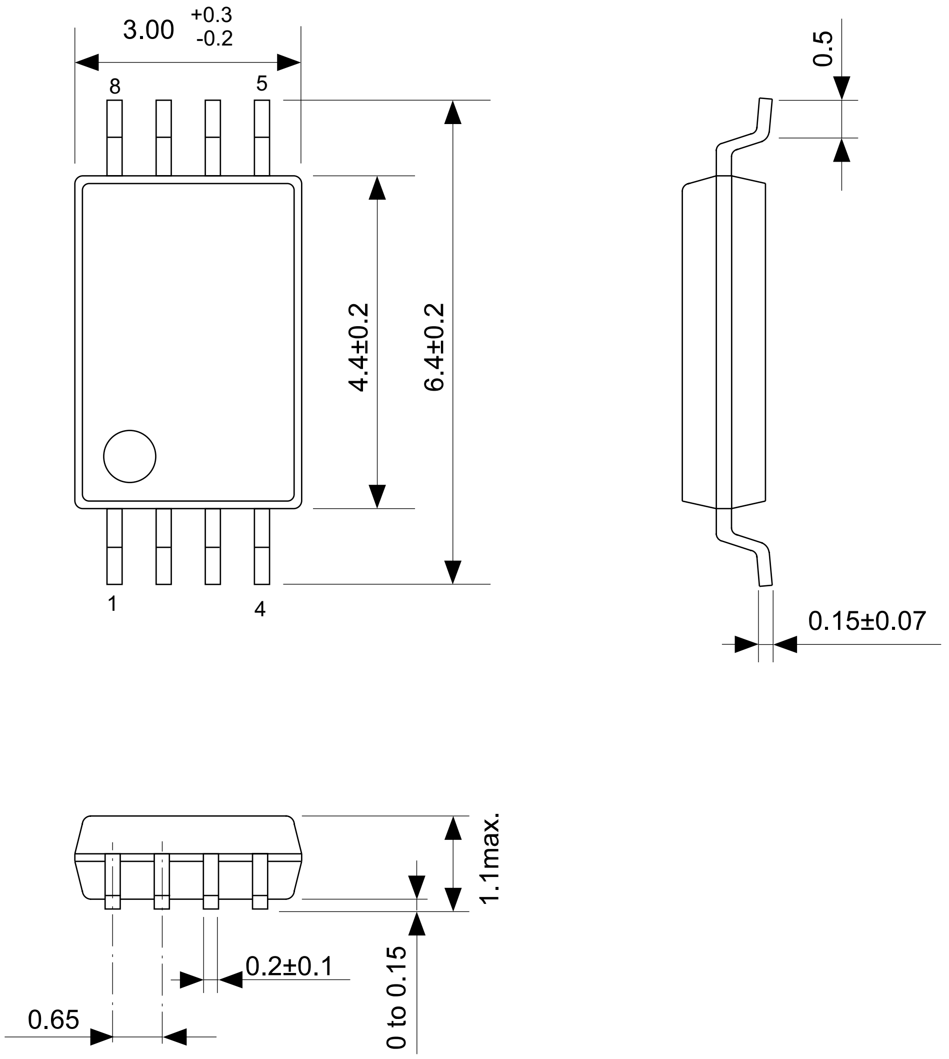

17.5±1.5
ø330±2
13.4±1.0

Enlarged drawing in the central part


2±0.5
ø21±0.8
ø13±0.2

No. FJ008-Z-R-SD-1.0

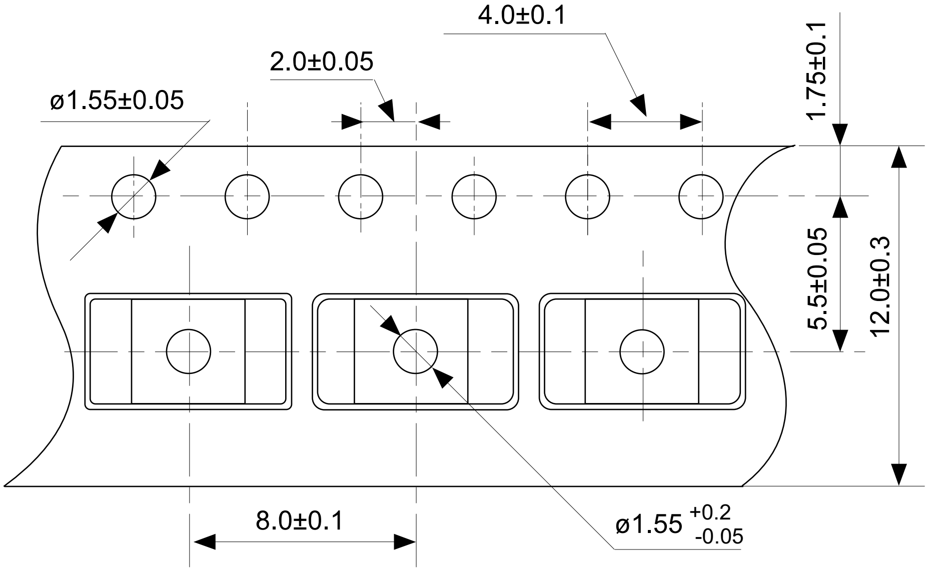
| | | | |
|---|---|---|---|
| TITLE | SOP8J-Z-Reel | | |
| No. | FJ008-Z-R-SD-1.0 | | |
| ANGLE | | QTY. | 4,000 |
| UNIT | mm | | |
| | | | |
| **ABLIC Inc.** | | | |

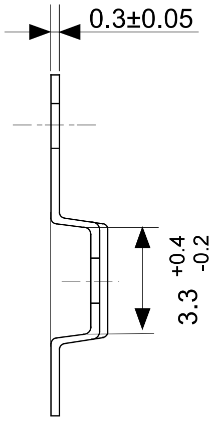

3.00 +0.3 -0.2
8
5
1
4
4.4±0.2
6.4±0.2
0.5
0.15±0.07
1.1max.
0 to 0.15
0.2±0.1
0.65

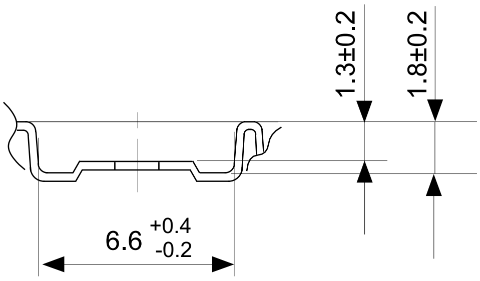
No. FT008-Z-P-SD-1.2

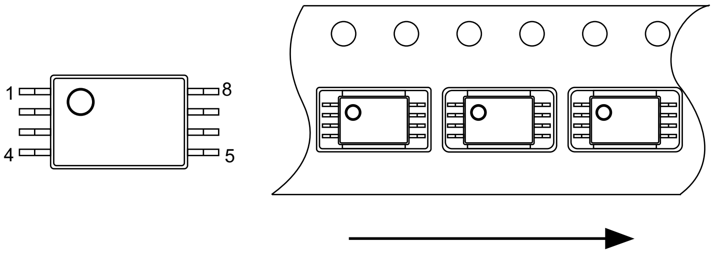
| | |
|---|---|
| TITLE | TSSOP8-Z-PKG Dimensions |
| No. | FT008-Z-P-SD-1.2 |
| ANGLE | |
| UNIT | mm |
| | |

**ABLIC Inc.**


4.0±0.1
2.0±0.05
ø1.55±0.05
1.75±0.1
5.5±0.05
12.0±0.3
8.0±0.1
ø1.55 +0.2 -0.05


0.3±0.05
3.3 +0.4 -0.2


1.3±0.2
1.8±0.2
6.6 +0.4 -0.2

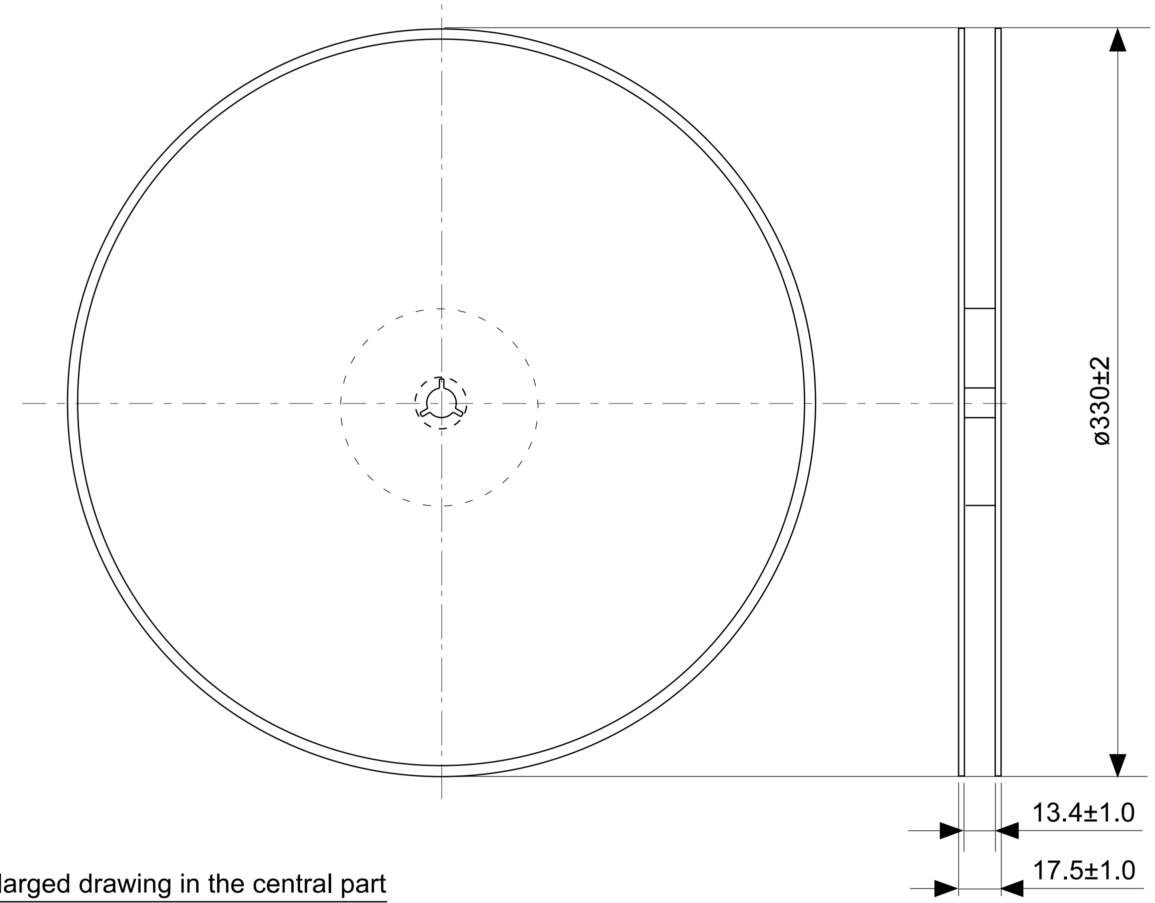


Feed direction

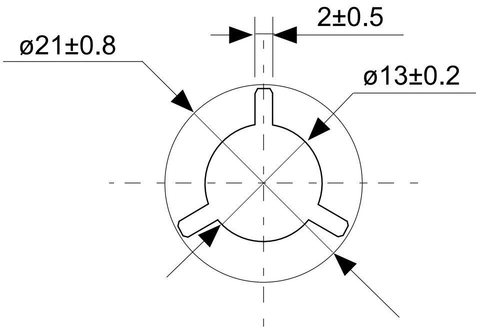
No. FT008-Z-C-SD-1.0

| | |
|---|---|
| TITLE | TSSOP8-Z-Carrier Tape |
| No. | FT008-Z-C-SD-1.0 |
| ANGLE | |
| UNIT | mm |
| | |

**ABLIC Inc.**


ø330±2
13.4±1.0
17.5±1.0

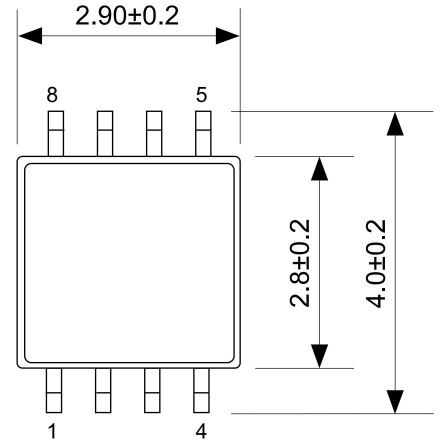
Enlarged drawing in the central part

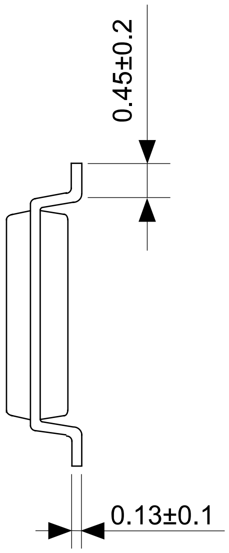

2±0.5
ø21±0.8
ø13±0.2

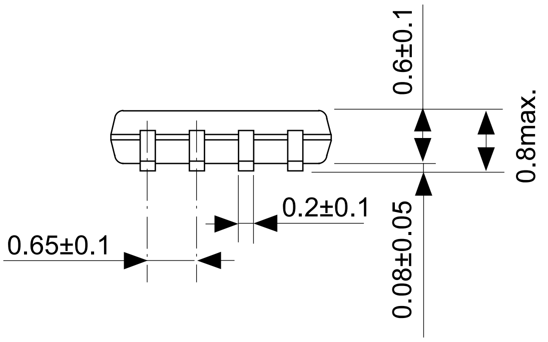
No. FT008-Z-R-SD-1.0

| | | | |
|---|---|---|---|
| TITLE | TSSOP8-Z-Reel | | |
| No. | FT008-Z-R-SD-1.0 | | |
| ANGLE | | QTY. | 4,000 |
| UNIT | mm | | |
| | | | |

**ABLIC Inc.**


2.90±0.2
8
5
1
4
2.8±0.2
4.0±0.2

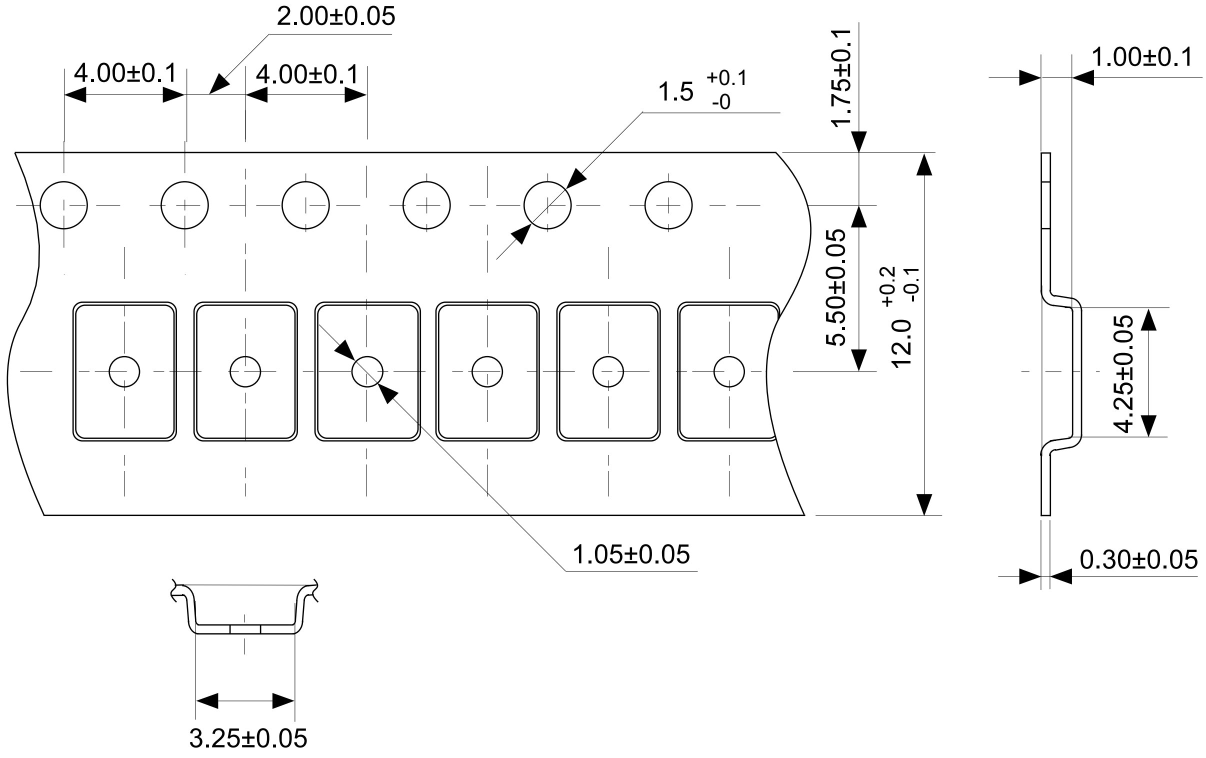

0.45±0.2
0.13±0.1

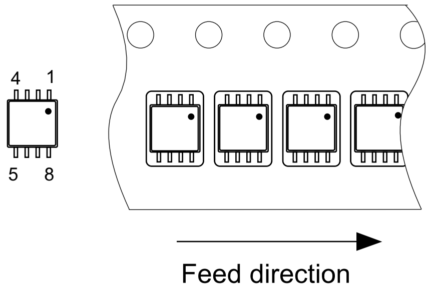

0.6±0.1
0.8max.
0.2±0.1
0.65±0.1
0.08±0.05

No. FM008-A-P-SD-1.2

| | |
|---|---|
| TITLE | TMSOP8-A-PKG Dimensions |
| No. | FM008-A-P-SD-1.2 |
| ANGLE | |
| UNIT | mm |
| | |

**ABLIC Inc.**

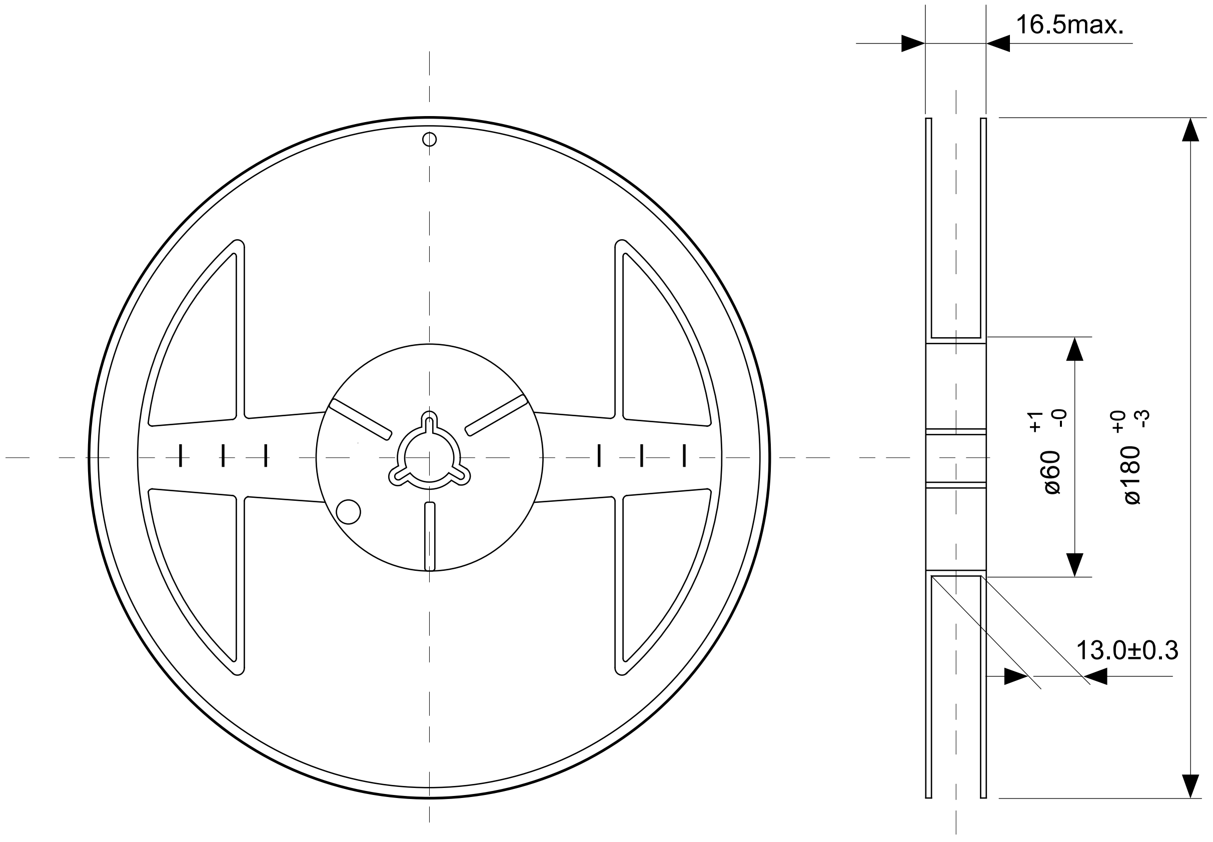

2.00±0.05
4.00±0.1
4.00±0.1
1.5 +0.1 -0
1.75±0.1
5.50±0.05
12.0 +0.2 -0.1
1.00±0.1
4.25±0.05
1.05±0.05
0.30±0.05
3.25±0.05


4
1
5
8
Feed direction

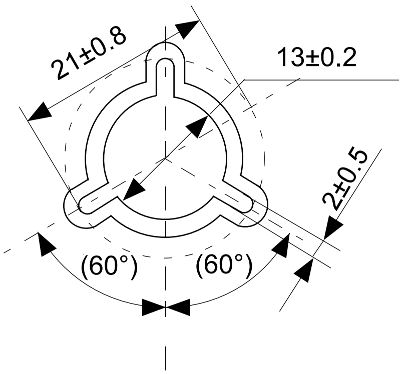
No. FM008-A-C-SD-2.0

| | |
|---|---|
| TITLE | TMSOP8-A-Carrier Tape |
| No. | FM008-A-C-SD-2.0 |
| ANGLE | |
| UNIT | mm |
| | |

**ABLIC Inc.**


16.5max.
ø60 +1 -0
ø180 +0 -3
13.0±0.3

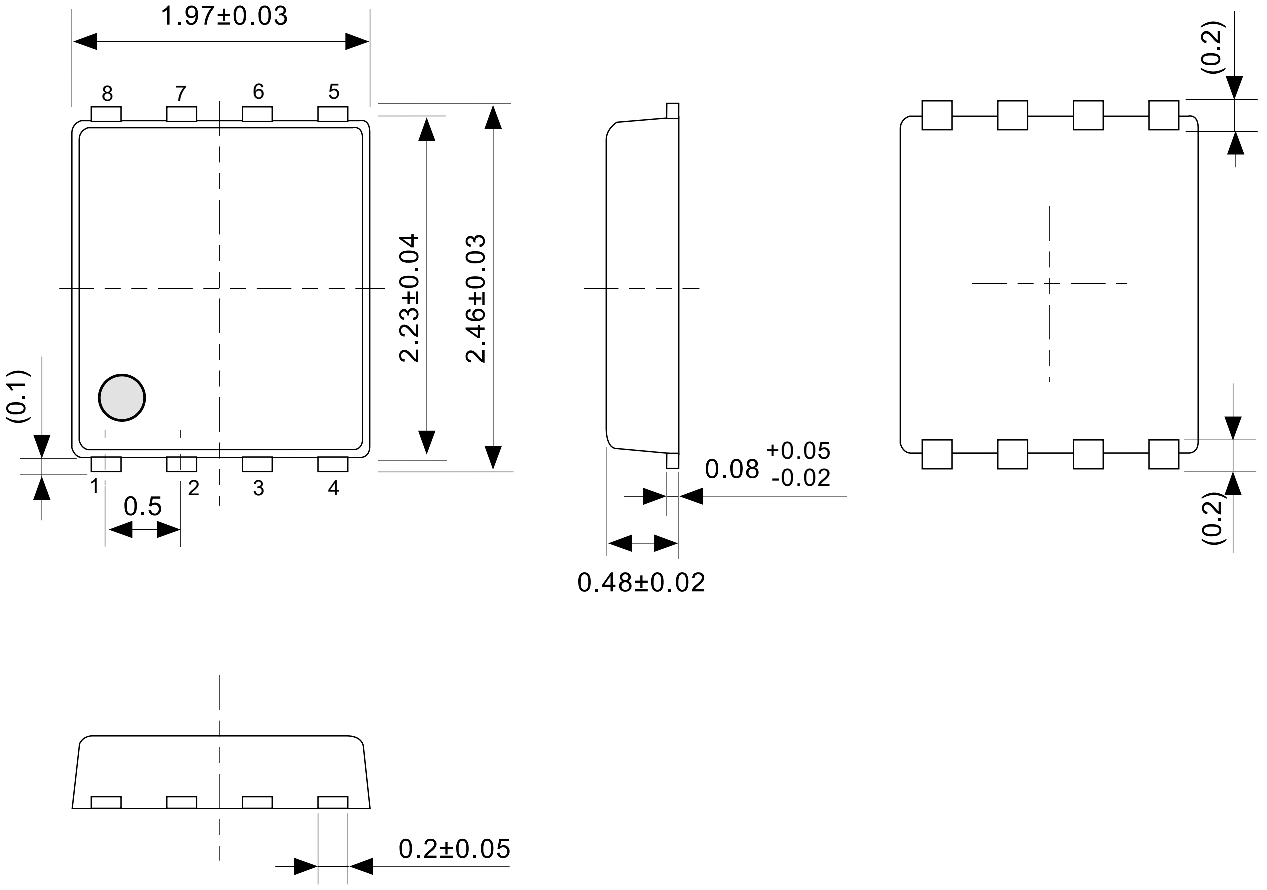
Enlarged drawing in the central part


21±0.8
13±0.2
2±0.5
(60°)
(60°)

No. FM008-A-R-SD-1.0

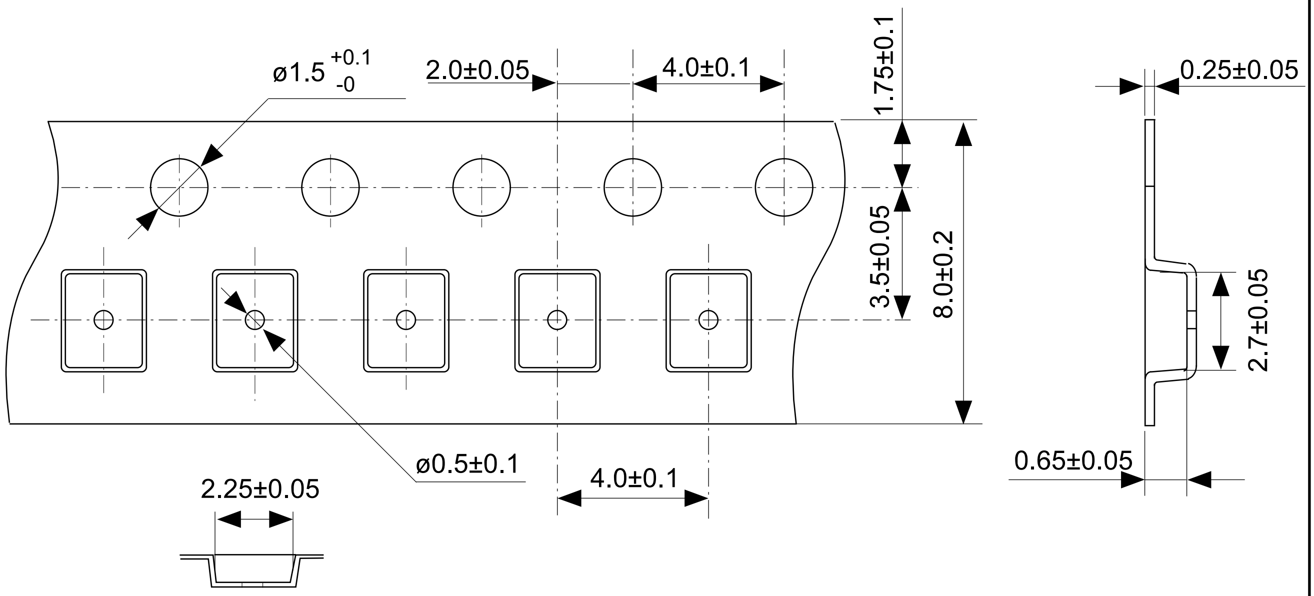
| | | | |
|---|---|---|---|
| TITLE | TMSOP8-A-Reel | | |
| No. | FM008-A-R-SD-1.0 | | |
| ANGLE | | QTY. | 4,000 |
| UNIT | mm | | |
| | | | |

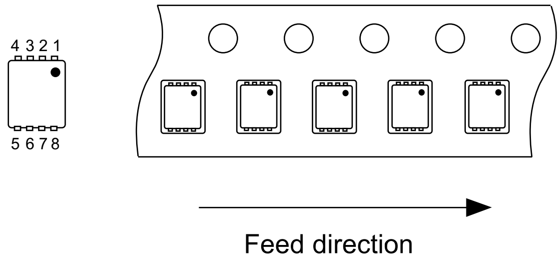
**ABLIC Inc.**


1.97±0.03
8
7
6
5
2.23±0.04
2.46±0.03
(0.1)
1
2
3
4
0.5
0.08 +0.05 -0.02
0.48±0.02
(0.2)
(0.2)
0.2±0.05

No. PH008-A-P-SD-2.1

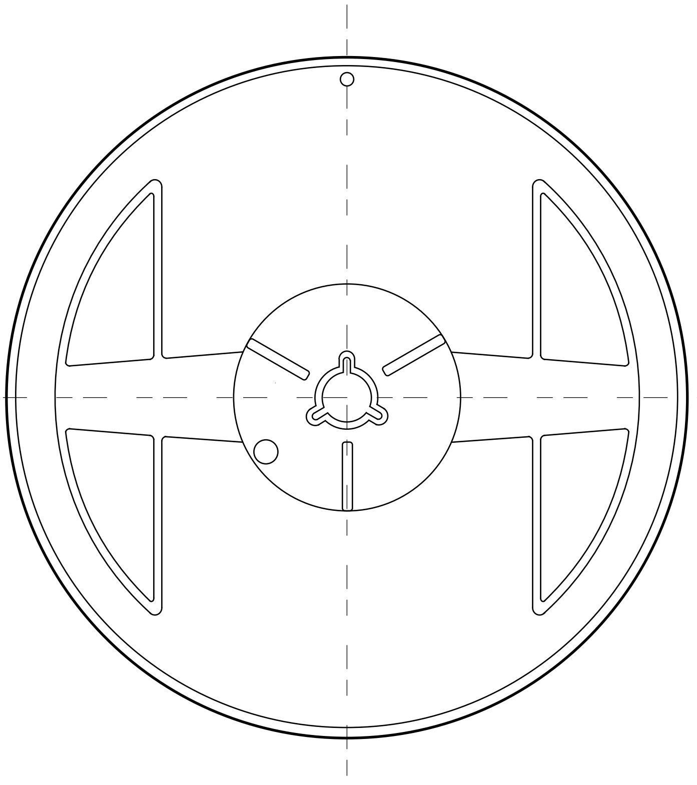
| | |
|---|---|
| TITLE | SNT-8A-A-PKG Dimensions |
| No. | PH008-A-P-SD-2.1 |
| ANGLE | |
| UNIT | mm |
| | |
| **ABLIC Inc.** | |

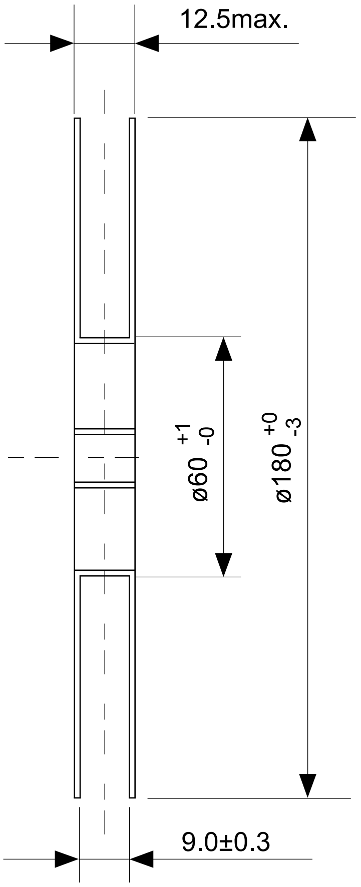

ø1.5 +0.1 -0
2.0±0.05
4.0±0.1
1.75±0.1
0.25±0.05
3.5±0.05
8.0±0.2
2.7±0.05
ø0.5±0.1
0.65±0.05
2.25±0.05
4.0±0.1


4 3 2 1
5 6 7 8
Feed direction

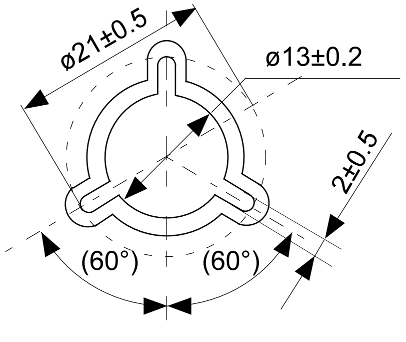
No. PH008-A-C-SD-2.0

| | |
|---|---|
| TITLE | SNT-8A-A-Carrier Tape |
| No. | PH008-A-C-SD-2.0 |
| ANGLE | |
| UNIT | mm |
| | |
| ABLIC Inc. | |



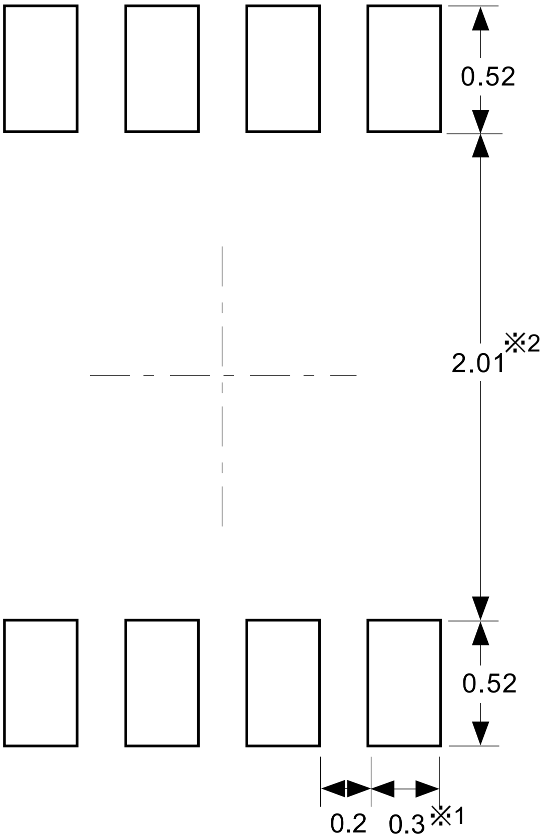

12.5max.
ø60 +1 -0
ø180 +0 -3
9.0±0.3

Enlarged drawing in the central part


ø21±0.5
ø13±0.2
2±0.5
(60°)
(60°)

No. PH008-A-R-SD-1.0

| | | | |
|---|---|---|---|
| TITLE | SNT-8A-A-Reel | | |
| No. | PH008-A-R-SD-1.0 | | |
| ANGLE | | QTY. | 5,000 |
| UNIT | mm | | |
| | | | |
| **ABLIC Inc.** | | | |



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

**注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。**
**2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。**
**3. マスク開口サイズと開口位置はランドパターンと合わせてください。**
**4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。**

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

**Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.**
**2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.**
**3. Match the mask aperture size and aperture position with the land pattern.**
**4. Refer to "SNT Package User's Guide" for details.**

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

**注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。**
**2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。**
**3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。**
**4. 详细内容请参阅 "SNT 封装的应用指南"。**

| | |
|---|---|
| TITLE | SNT-8A-A<br>-Land Recommendation |
| No. | PH008-A-L-SD-4.1 |
| ANGLE | |
| UNIT | mm |
| | |
| **ABLIC Inc.** | |

# Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
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4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
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6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
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   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
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14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

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