XRP6336

Triple µPower Supervisory Circuit with Watchdog and Power Fail

April 2011 Rev. 1.0.0

GENERAL DESCRIPTION

The XRP6336, a triple µPower supervisory circuit, is a microprocessor reset supervisory circuit with multiple reset voltages.

The XRP6336 provides low voltage monitoring ability for up-to three supplies with two precision factory-set thresholds and one user defined custom threshold. This circuit performs a single function: if any of the input supply voltages drops below its associated threshold, reset outputs are asserted. The XRP6336 offers power fail and watchdog functionalities.

The XRP6336 is offered in a RoHS compliant, lead free 8-pin TSOT package and is fully specified over the -40°C to +85°C temperature range.

APPLICATIONS

- **Power Supplies Monitoring**
- **DSPs/FPGAs Supplies Monitoring**

FEATURES

- **Low operating voltage of 1.6V**
- **Low operating current of 20µA typical**
- **Monitors up to 3 supplies simultaneously**
- **Adjustable inputs monitor down to 0.5V**
- **Reset asserted down to 0.9V**
- **4% accuracy over temperature range**
- **Power Fail Input Functionality (PFI)**
- **Power Fail Output function, active low (PFOB)**
- **Open Drain (OD) or CMOS RSTB output**
- **4 Reset Timeout Periods**
  - 50ms, 100ms, 200ms and 400 ms
- **Watch Dog Input Functionality**
- **RoHS Compliant Lead Free 8 pin TSOT Package**

TYPICAL APPLICATION DIAGRAM

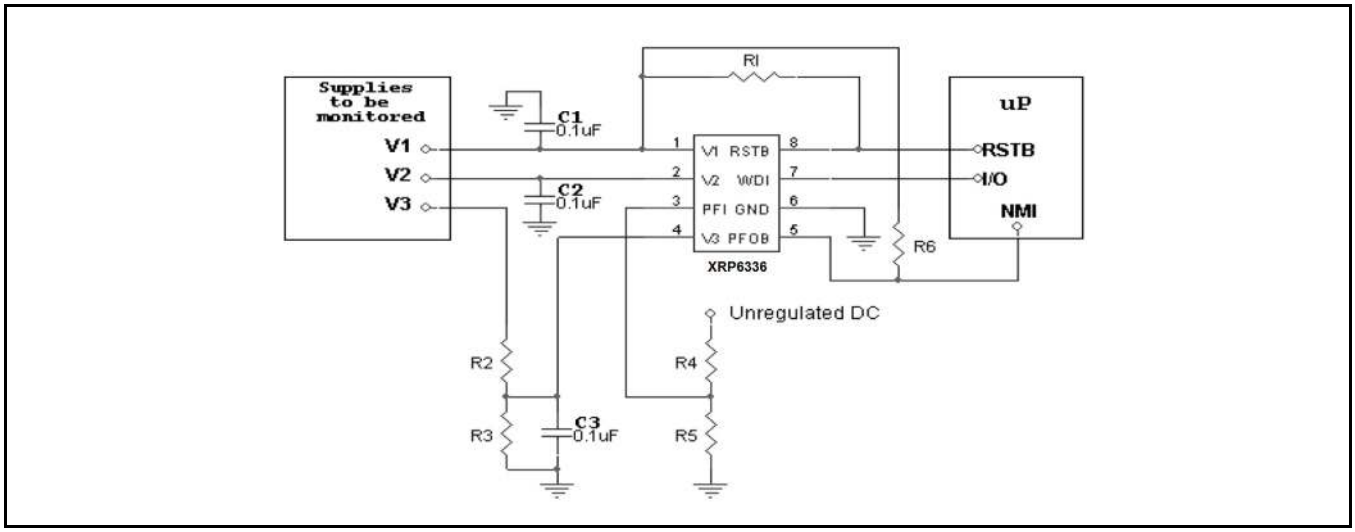


Fig. 1: XRP6336 Application Diagram

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Terminal Voltage (with respect to GND)
V1, V2 ..... -0.3V to 6.0V
Open-Drain RSTB, PFOB ..... -0.3V to 6.0V
CMOS RST, RSTB ..... -0.3V to (V1+0.3V)
Input Current/Output Current 20mA
V3, V4, PFI, WDI ..... -0.3V to (V1+0.3V)
Storage Temperature ..... -65°C to 150°C

Power Dissipation ..... Internally Limited
Lead Temperature (Soldering, 10 sec) ..... 300°C
ESD Rating (HBM - Human Body Model) 2kV
ESD Rating (MM - Machine Model) 500V

OPERATING RATINGS

Input Voltage Range ..... 0.9V to 5.5V
Operating Temperature Range ..... -40°C to 85°C
Thermal Resistance θ_{JA} ..... 134°C/W

ELECTRICAL SPECIFICATIONS

Specifications with standard type are for an Operating Ambient Temperature of T_A = 25°C only; limits applying over the full Operating Ambient Temperature range are denoted by a "•". Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V1 = 1.6V to 5.5V, T_A= –40°C to 85°C.

Parameter	Min.	Typ.	Max.	Units		Conditions
Operating Voltage Range	0.9		5.5	V		T_A=-40°C to +85°C
Supply Current		20	30	µA		V1<5.5V, V2<3.6V, all I/O pins open
		15	25			V1<3.6V, V2<2.75V, all I/O pins open
V1 Reset Threshold	4.532	4.625	4.718	V		Z (valid for V1 falling)
	4.287	4.375	4.463			Y (valid for V1 falling)
	2.900	3.075	3.168			X (valid for V1 falling)
	2.866	2.925	2.984			W (valid for V1 falling)
	2.572	2.625	2.678			V (valid for V1 falling)
	2.273	2.320	2.367			U (valid for V1 falling)
	2.146	2.190	2.234			T (valid for V1 falling)
	1.636	1.670	1.704			S (valid for V1 falling)
	1.548	1.580	1.612			R (valid for V1 falling)
V2 Reset Threshold	2.266	2.313	2.360	V		J (valid for V2 falling)
	2.144	2.188	2.232			I (valid for V2 falling)
	1.631	1.665	1.698			H (valid for V2 falling)
	1.543	1.575	1.607			G (valid for V2 falling)
	1.360	1.388	1.416			F (valid for V2 falling)
	1.286	1.313	1.340			E (valid for V2 falling)
	1.053	1.110	1.152			D (valid for V2 falling)
	1.029	1.050	1.071			C (valid for V2 falling)
	0.816	0.833	0.850			B (valid for V2 falling)
	0.772	0.788	0.804			A (valid for V2 falling)
Threshold 1 tempco		0.06		mV/°C		
Threshold 2 tempco		0.04		mV/°C		
Threshold 1 Hysteresis		0.65		%		Referenced to Vth1 typical
Threshold 2 Hysteresis		0.5		%		Referenced to Vth2 typical

Parameter	Min.	Typ.	Max.	Units		Conditions
V1 to RST/RSTB Delay		50		µs		V1=Vth1 to (Vth1-0.1V), Vth1=3.075V
V2 to RST/RSTB Delay		50		µs		V2=Vth2 to (Vth2-0.1V), Vth1=1.575V
Reset Timeout Period (T1)	37	50	72	ms		TOPT-1
Reset Timeout Period (T2)	74	100	126	ms		TOPT-2
Reset Timeout Period (T3)	148	200	252	ms		TOPT-3
Reset Timeout Period (T4)	296	400	504	ms		TOPT-4
V3 Reset Comparator Input						
V3 Input Threshold	480	500	520	mV		
V3 Input Current	-50		50	nA		T_A=25°C
V3 Threshold Hysteresis		1.5		mV		
WDI – Watchdog Input						
Watchdog Timeout Period	1.2		2.5	sec		
WDI Pulse Width	0.1			µs		
WDI Input Threshold				0.4	V	
	0.8xV1					
WDI Input Current	-500		+500			WDI=0.0V or V1
Reset & Power Fail Outputs RST/RSTB/WDOB/PFOB						
RSTB (CMOS or OD)			0.4	V		V1=Vth1-0.1V, I_{SINK}=1mA, output asserted
PFOB			0.4	V		V_PFI= 0.4V, I_{SINK}=1mA, output not asserted
RSTB (CMOS)	0.8xV1					V1=Vth1-0.1V, I_{SINK}=1mA, output asserted
RST (CMOS)	0.8xV1			V		V1=Vth1-0.1V, I_{SOURCE}=1mA, output asserted
			0.4			V1=Vth1-0.1V, V2>Vth2, V3>0.5V, I_{SOURCE}=1mA, output not asserted
RST/WDOB/PFOB Output Open Drain Leakage Current		2		nA		Output asserted
PFI – Power Fail Input						
PFI Input Threshold	480	500	520	mV		
PFI Input Current	-50		50	nA		
PFI Hysteresis		2.5		mV		
PFI to PFOB Delay		4		µs		

BLOCK DIAGRAM

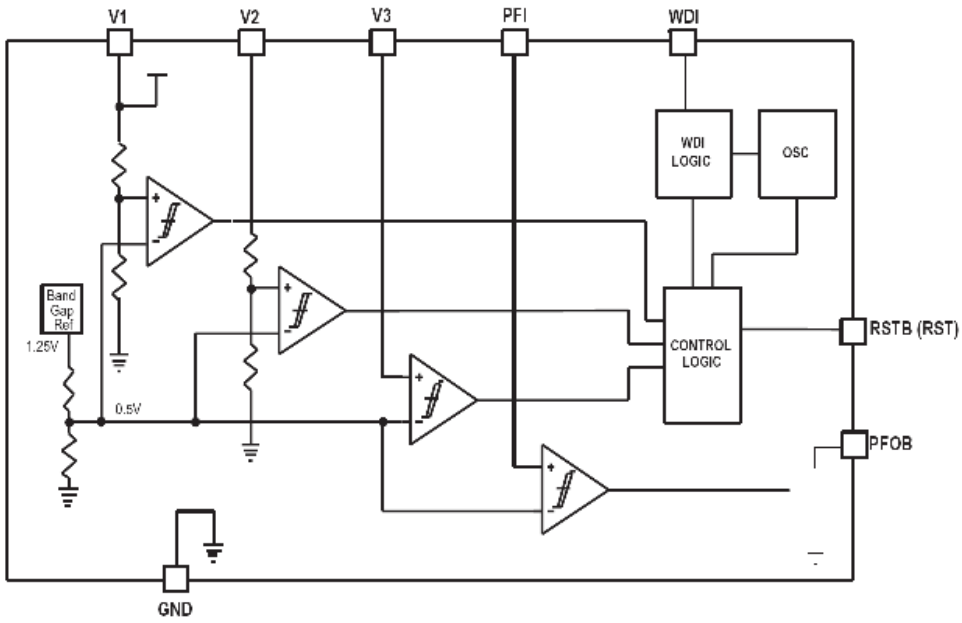


Fig. 2: XRP6336 Block Diagram

PIN ASSIGNMENT

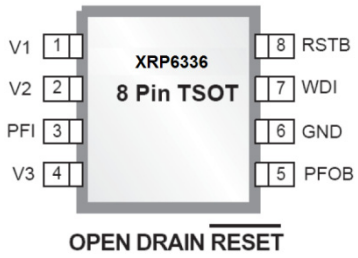
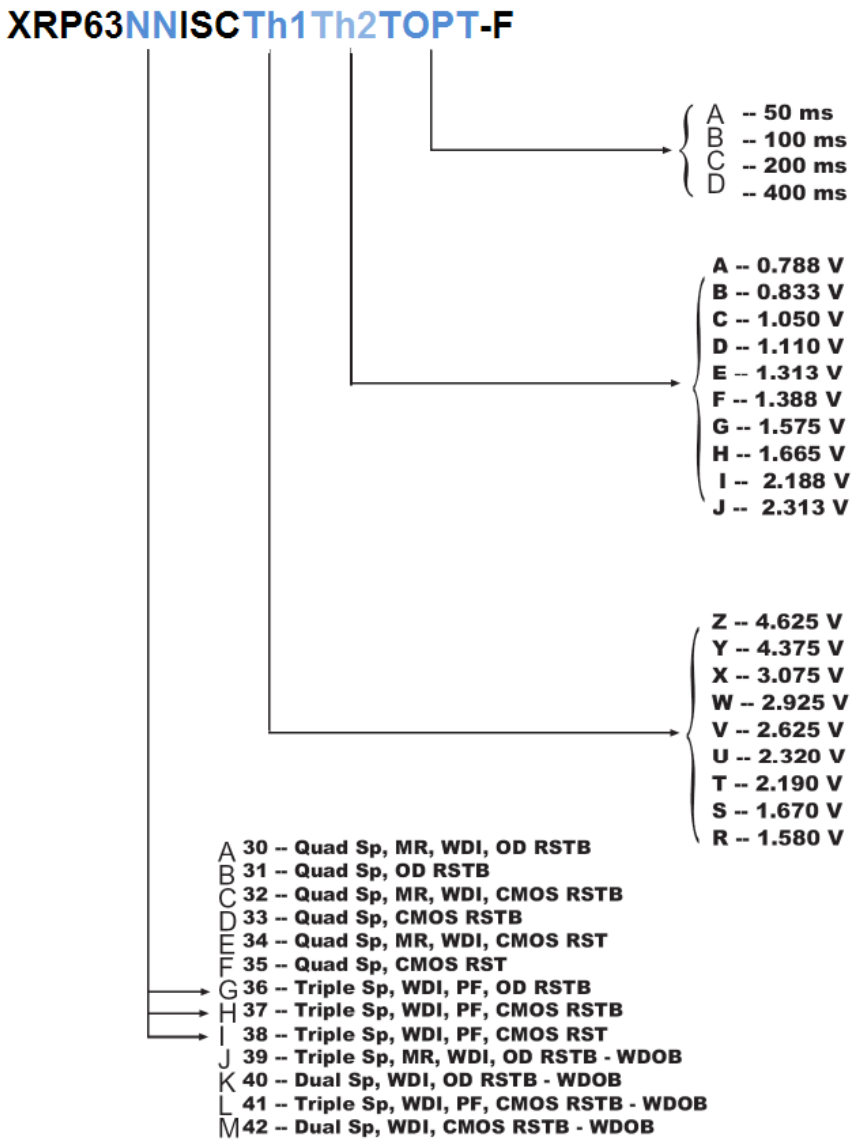


Fig. 3: XRP6336 Pin Assignment

PIN DESCRIPTION

Name	Pin Number	Description
V1	1	First supply voltage input. Also powers internal circuitry. Trip threshold voltage is internally set.
V2	2	Second supply voltage input. Trip threshold voltage internally set.
PFI	3	Power Fail Input pin. Trip threshold is 0.5V. When the input voltage at the PFI pin is <0.5V, PFOB is low. Connect to GND or V1 if not used.
V3	4	Input for the third supply voltage. Trip threshold is 0.5V.
PFOB	5	Power Fail Output pin. Active low open drain output. When the input voltage at the PFI pin is <0.5V, PFOB is low.
GND	6	Common ground reference pin.
WDI	7	Watch-Dog Input pin. When no transition is detected at the WDI pin for the duration of WDI timeout period, reset is asserted. Leave open if not used. RST/RSTB outp4ut is used to signal watchdog timeout overflow, and its output pulses high/low (depending on the active reset polarity) for the reset timeout period after each watchdog timeout overflow. The watchdog timer clears whenever the reset is asserted or manual reset is asserted or a transition is observed at WDI pin. Watchdog timer functionality can be disabled by leaving this input floating.
RST/RSTB	8	Reset output. Open-Drain or CMOS, active high or low. Reset is asserted when any of the three supply inputs is below its trip threshold. It stays asserted for 200 ms (typical / default) after the last supply input traverses its trip threshold. Reset is guaranteed to be in the correct state for V1>0.9V. RST/RSTB asserts when V1 or V2 or V3 drop below their corresponding reset thresholds, or the watchdog timer triggers a reset. RST/RSTB remains asserted for the reset timeout period after V1 and V2 and V3 exceed their corresponding reset thresholds. Open drain outputs require an external pull-up resistor. CMOS outputs are referenced to V1.

PART NAMING NOMENCLATURE



ORDERING INFORMATION

Part Number	Temperature Range	Marking	Package	Packing Quantity	Note 1	Note 2
XRP6336ISCXDA-F	-40°C≤T_A≤+85°C	NXDA	TSOT-8	Bulk	Halogen Free	
XRP6336ISCXDATR-F	-40°C≤T_A≤+85°C	NXDA	TSOT-8	2.5K/Tape & Reel	Halogen Free	

THEORY OF OPERATION

The XRP6336 includes a low-voltage precision bandgap reference, three precision comparators, an oscillator, a digital counter chain, a logic control block, trimmed resistor divider chains and additional supporting circuitry. This device is designed to supervise up to 3 independent supply voltages.

V1 and V2 supply inputs have their resistor dividers on the chip. Their trip thresholds are factory trimmed. V3 input allows users to customize an additional supply threshold to be monitored by means of external resistor dividers. Each part is furnished with power fail indication and watchdog functionalities. The watchdog timer is serviced internally during the watchdog timeout period when WDI is left unconnected. Thus, watchdog functionality can be disabled via leaving the WDI input floating.

APPLICATION INFORMATION

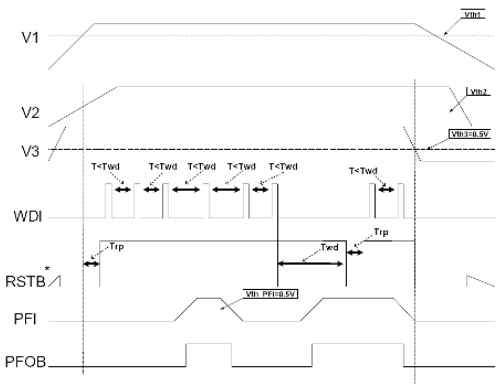


Fig. 4: Timing Diagram for XRP6336

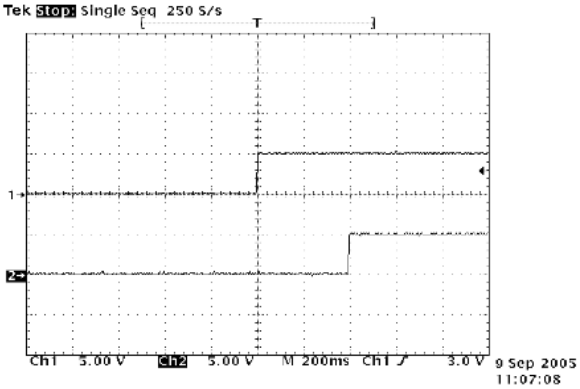


Fig. 5: RESETB Timeout Period (400ms)

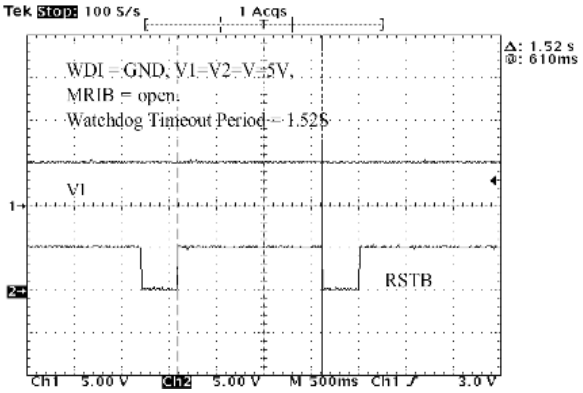


Fig. 6: XRP6336 Watchdog Timeout Period

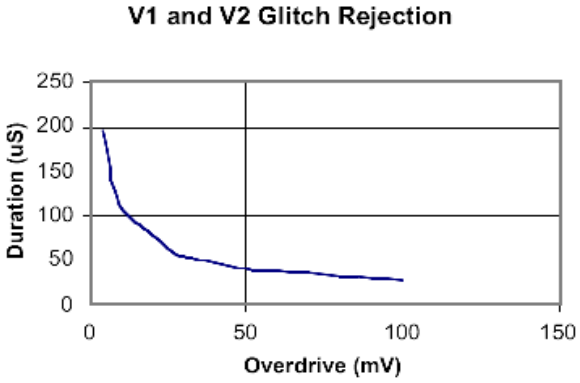


Fig. 7: V1 and V2 Glitch Rejection

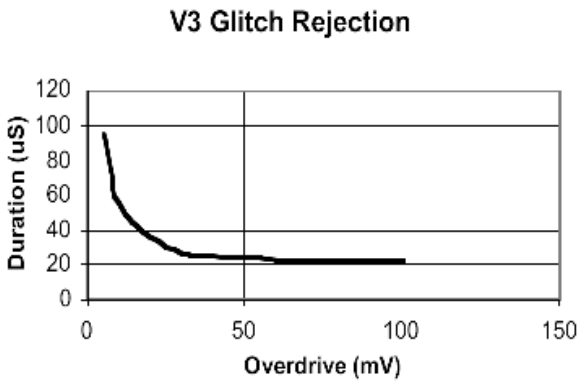


Fig. 8: V3 Glitch Rejection

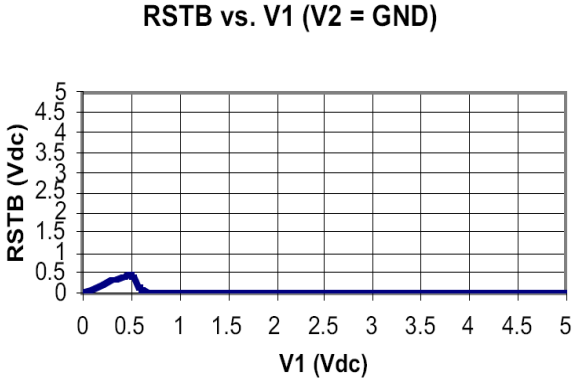


Fig. 9: Reset Good

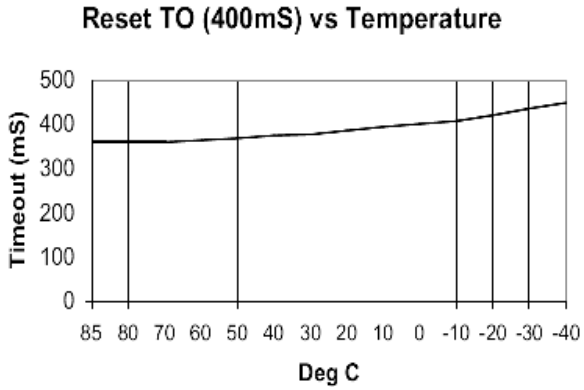
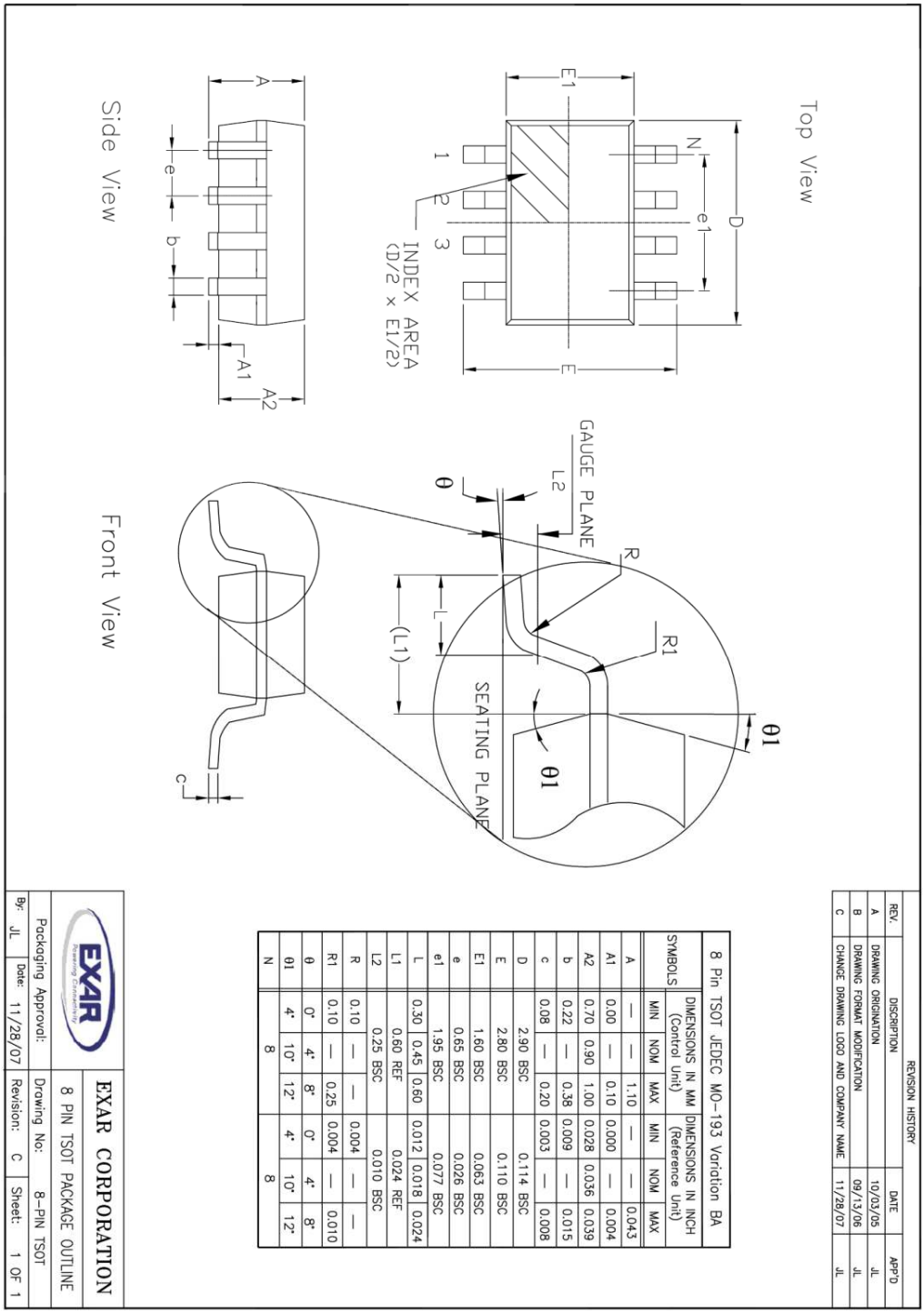


Fig. 10: Reset Timeout versus Temperature

PACKAGE SPECIFICATION

8-PIN TSOT



REVISION HISTORY

Revision	Date	Description
1.0.0	04/02/2011	Initial release of datasheet

FOR FURTHER ASSISTANCE

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