

# Digital Design Using Digilent FPGA Boards — VHDL / Active-HDL Edition

## Table of Contents

<b>1. Introduction</b>	1
1.1 Background	1
1.2 Digital Logic	5
1.3 VHDL	8
<b>2. Basic Logic Gates</b>	9
2.1 Truth Tables and Logic Equations	9
The Three Basic Gates	9
Four New Gates	11
2.2 Positive and Negative Logic: De Morgan's Theorem	13
2.3 Sum of Products Design	15
2.4 Product of Sums Design	16
VHDL Examples	18
Example 1: 2-Input Gates	18
Example 2: Multiple-Input Gates	23
Problems	26
<b>3. Boolean Algebra and Logic Equations</b>	29
3.1 Boolean Theorems	29
One-Variable Theorems	30
Two- and Three-Variable Theorems	30
3.2 Karnaugh Maps	35
Two-Variable K-Maps	35
Three-Variable K-Maps	37
Four-Variable K-Maps	39
3.3 Computer Minimization Techniques	41
Tabular Representations	41
Prime Implicants	42
Essential Prime Implicants	44
VHDL Examples	46
Example 3 – Majority Circuit	46
Example 4 – 2-Bit Comparator	49
Problems	52
<b>4. Implementing Digital Circuits</b>	54
4.1 Implementing Gates	54
4.2 Transistor-Transistor Logic (TTL)	56
4.3 Programmable Logic Devices (PLDs and CPLDs)	58
A 2-Input, 1-Output PLD	58

The GAL 16V8	60
CPLDs	62
4.4 Field Programmable Gate Arrays (FPGAs)	62
VHDL Examples	64
Example 5 – Map Report	64
Problems	65
<b>5. Combinational Logic</b>	<b>66</b>
5.1 Multiplexers	66
2-to-1 Multiplexer	66
4-to-1 Multiplexer	67
Quad 2-to-1 Multiplexer	68
VHDL Examples	69
Example 6 – 2-to-1 Multiplexer: <i>if</i> Statement	69
Example 7 – 4-to-1 Multiplexer: <i>port map</i> Statement	72
Example 8 – 4-to-1 Multiplexer: <i>case</i> Statement	76
Example 9 – A Quad 2-to-1 Multiplexer	77
Example 10 – Generic Multiplexer: Parameters	80
Example 11 – Glitches	82
5.2 7-Segment Displays	85
VHDL Examples	86
Example 12 – 7-Segment Decoder: Logic Equations	86
Example 13 – 7-Segment Decoder: <i>case</i> Statement	88
Example 14 – Multiplexing 7-Segment Displays	91
Example 15 – 7-Segment Displays: <i>x7seg</i> and <i>x7segb</i>	93
5.3 Code Converters	99
Binary-to-BCD Converters	99
Shift and Add 3 Algorithm	100
Gray Code Converters	102
VHDL Examples	102
Example 16 – 4-Bit Binary-to-BCD Converter: Logic Equations	102
Example 17 – 8-Bit Binary-to-BCD Converter: <i>for</i> Loops	103
Example 18 – 4-Bit Binary to Gray Code Converter	107
Example 19 – 4-Bit Gray Code to Binary Converter	108
5.4 Comparators	109
Cascading Comparators	109
TTL Comparators	110
VHDL Examples	111
Example 20 – 4-Bit Comparator Using a VHDL Procedure	111
Example 21 – <i>N</i> -Bit Comparator Using Relational Operators	114
5.5 Decoders and Encoders	115
Decoders	115
TTL Decoders	116
Encoders	117
Priority Encoders	117
TTL Encoders	118
VHDL Examples	118

Example 22 – 3-to-8 Decoder: Logic Equations	118
Example 23 – 3-to-8 Decoder: <i>for</i> Loops	120
Example 24 – 8-to-3 Encoder: Logic Equations	121
Example 25 – 8-to-3 Encoder: <i>for</i> Loops	123
Example 26 – 8-to-3 Priority Encoder	124
Problems	126
<b>6. Arithmetic Circuits</b>	<b>129</b>
6.1 Adders	129
Half Adder	129
Full Adder	129
Carry and Overflow	132
TTL Adder	134
VHDL Examples	134
Example 27 – 4-Bit Adder: Logic Equations	134
Example 28 – 4-Bit Adder: Behavioral Statements	137
Example 29 – <i>N</i> -Bit Adder: Behavioral Statements	138
6.2 Subtractors	139
Half Subtractor	139
Full Subtractor	140
An Adder/Subtractor Circuit	141
VHDL Examples	143
Example 30 – 4-Bit Adder/Subtractor: Logic Equations	143
Example 31 – <i>N</i> -Bit Subtractor: Behavioral Statements	144
6.3 Shifters	145
VHDL Examples	146
Example 32 – 4-Bit Shifter	146
6.4 Multiplication	147
Binary Multiplication	147
Signed Multiplication	150
VHDL Examples	151
Example 33 – Multiplying by a Constant	151
Example 34 – A 4-Bit Multiplier	152
The Multiplication Operator	154
6.5 Division	155
Binary Division	155
VHDL Examples	157
Example 35 – An 8-Bit Divider using a Procedure	157
6.6 Arithmetic Logic Unit (ALU)	159
VHDL Examples	160
Example 36 – 4-Bit ALU	160
Problems	162
<b>7. Sequential Logic</b>	<b>164</b>
7.1 Latches and Flip-Flops	164
SR Latch	164
Clocked SR Latch	166

D Latch	166
Edge-Triggered D Flip-Flop	167
VHDL Examples	169
Example 37 – Edge-Triggered D Flip-Flop	169
Example 38 – Edge-Triggered D Flip-Flop with Set and Clear	170
Example 39 – D Flip-Flops in VHDL	171
Example 40 – D Flip-Flop with Asynchronous Set and Clear	172
Example 41 – Divide-by-2 Counter	173
7.2 Registers	174
VHDL Examples	176
Example 42 – 1-Bit Register	176
Example 43– 4-Bit Register	177
Example 44 – <i>N</i> -Bit Register	179
7.3 Shift Registers	180
4-Bit Ring Counter	180
VHDL Examples	181
Example 45 – Shift Registers	181
Example 46 – Ring Counter	183
Example 47 – Debounce Pushbuttons	184
Example 48 – Clock Pulse	186
7.4 Counters	187
Arbitrary Waveform	189
VHDL Examples	190
Example 49 – 3-Bit Counter	190
Example 50 – Modulo-5 Counter	192
Example 51 – <i>N</i> -Bit Counter	193
Example 52 – Clock Divider: Modulo-10K Counter	195
Example 53 – Arbitrary Waveform	202
7.5 Pulse-Width Modulation (PWM)	203
Controlling the Speed of a DC Motor using PWM	203
Controlling the Position of a Servo using PWM	205
VHDL Examples	206
Example 54 – Pulse-Width Modulation (PWM)	206
Example 55 – PWM Signal for Controlling Servos	208
7.6 BASYS/Nexys-2 Board Examples	210
VHDL Examples	210
Example 56 – Loading Switch Data into a Register	210
Example 57 – Shifting Data into a Shift Register	213
Example 58 – Scrolling the 7-Segment Display	216
Example 59 – Fibonacci Sequence	222
Problems	226
<b>8. Finite State Machines</b>	<b>228</b>
8.1 Mealy and Moore State Machines	228
8.2 A Moore Machine Sequence Detector	229
8.3 Mealy Machine Sequence Detector	231
VHDL Examples	232

Example 60 – Sequence Detector	232
Example 61 – Door Lock Code	238
VHDL Package	243
Example 62 – Traffic Lights	245
Problems	250
<b>9. Datapaths and Control Units</b>	251
9.1 VHDL <i>while</i> Statement	251
Example 63 – GCD Algorithm – Part 1	251
9.2 Datapaths and Control Units	253
Example 64 – GCD Algorithm – Part 2	255
Example 65 – An Integer Square Root Algorithm	266
Square Root Control Unit	270
<b>10. Integrating the Datapath and Control Unit</b>	278
Example 66 –GCD Algorithm – Part 3	280
Example 67 – Integer Square Root– Part 2	284
<b>11. Memory</b>	288
Example 68 – A VHDL ROM	288
Example 69 – Distributed RAM/ROM	292
Example 70 – Block RAM/ROM	297
<b>12. VGA Controller</b>	301
Example 71 – VGA-Stripes	305
Example 72 – VGA-PROM	311
Example 73 – Sprites in Block ROM	316
Example 74 – Screen Saver	322
<b>13. PS/2 Port</b>	328
Example 75 – Keyboard	331
Example 76 – Mouse	338
<b>Appendix A – Aldec Active-HDL Tutorial</b>	348
Part 1: Project Setup	348
Part 2: Design Entry	352
Part 3: Simulation	355
Part 4: Creating a Top-level Design	359
Part 5: Synthesis and Implementation	361
Part 6: Program FPGA Board	365
<b>Appendix B – Number Systems</b>	367
B.1 Counting in Binary and Hexadecimal	367
B.2 Positional Notation	371
B.3 Fractional Numbers	372
B.4 Number System Conversions	372
B.5 Negative Numbers	376
<b>Appendix C – Making a Turnkey System</b>	380

<b>Appendix D</b> – Digilent FPGA Boards Comparison Chart	382
<b>Appendix E</b> – Installing the Xilinx ISE/WebPACK, Aldec Active-HDL, and Digilent Adept2 Software	383
<b>Appendix F</b> – VHDL Quick Reference Guide	385