

# 74AC648

## Octal Transceiver/Register with 3-STATE Outputs

### General Description

The AC648 consists of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental data handling functions available are illustrated in Figure 1, Figure 2, Figure 3, and Figure 4.

### Features

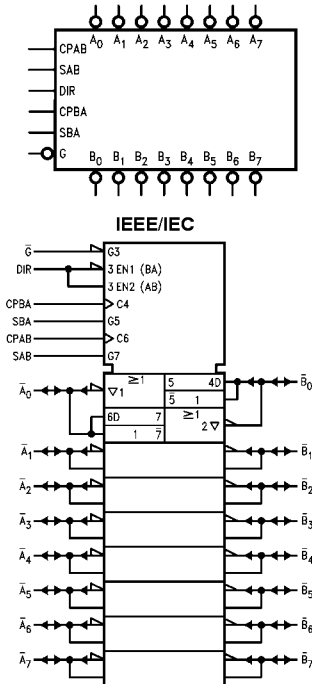
- Independent registers for A and B buses
- Multiplexed real-time and stored data transfers
- 3-STATE outputs
- 300 mil slim dual-in-line package
- Outputs source/sink 24 mA
- Inverted data to output

### Ordering Code:

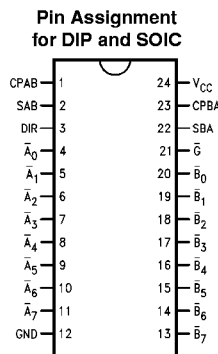
Order Number	Package Number	Package Description
74AC648SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74AC648SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



### Pin Descriptions

Pin Names	Description
$\bar{A}_0$ - $\bar{A}_7$	Data Register A Inputs, Data Register A 3-STATE Outputs
$\bar{B}_0$ - $\bar{B}_7$	Data Register B Inputs, Data Register B 3-STATE Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
DIR, $\bar{G}$	Output Enable Inputs

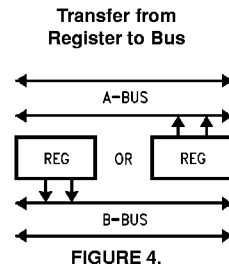
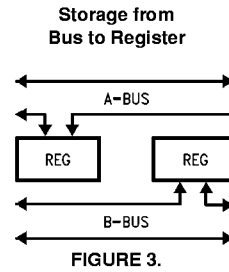
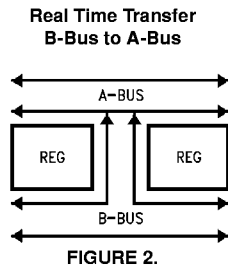
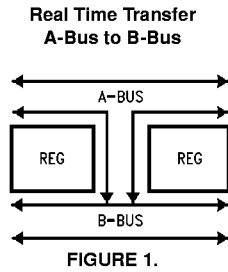
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**Function Table**

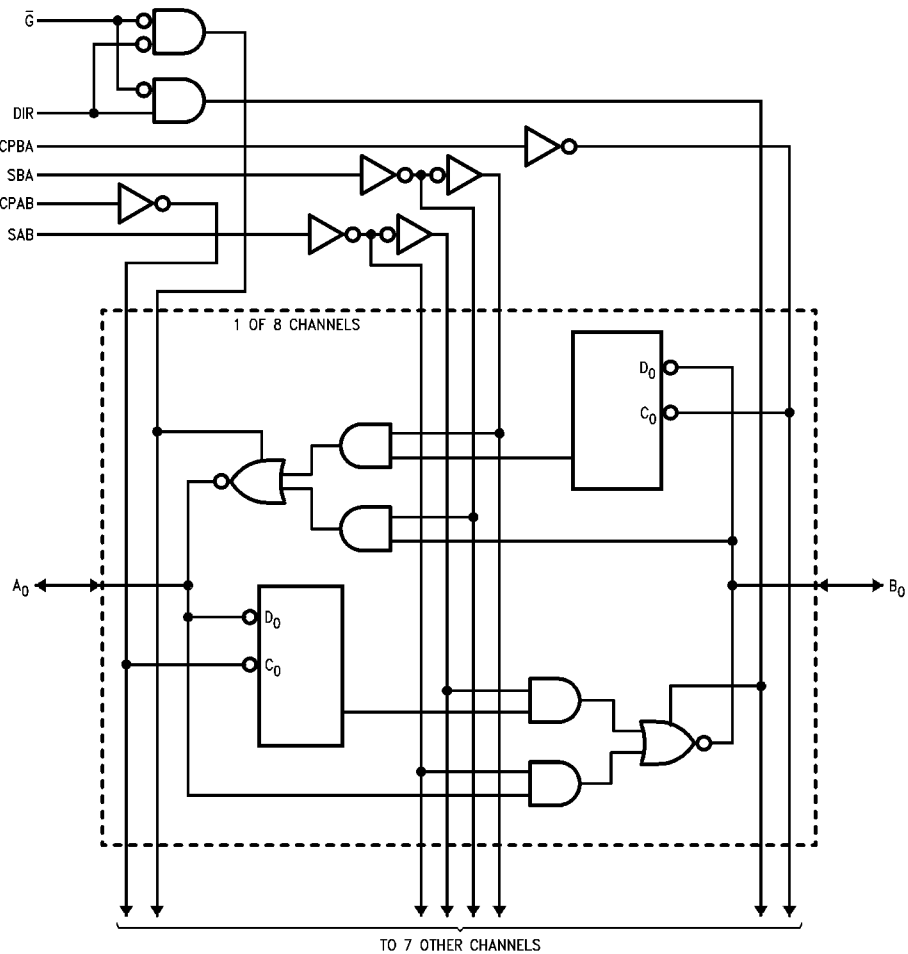
Inputs						Data I/O (Note 1)		Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A <sub>0</sub> -A <sub>7</sub>	B <sub>0</sub> -B <sub>7</sub>	
H	X	H or L	H or L	X	X			Isolation
H	X	↘	X	X	X	Input	Input	Clock A <sub>n</sub> Data into A Register
H	X	X	↘	X	X			Clock B <sub>n</sub> Data into B Register
L	H	X	X	L	X	Input	Output	A <sub>n</sub> to B <sub>n</sub> —Real Time (Transparent Mode)
L	H	↘	X	L	X			Clock A <sub>n</sub> Data into A Register
L	H	H or L	X	H	X			A Register to B <sub>n</sub> (Stored Mode)
L	H	↘	X	H	X			Clock A <sub>n</sub> Data into A Register and Output to B <sub>n</sub>
L	L	X	X	X	L	Output	Input	B <sub>n</sub> to A <sub>n</sub> —Real Time (Transparent Mode)
L	L	X	↘	X	L			Clock B <sub>n</sub> Data into B Register
L	L	X	H or L	X	H			B Register to A <sub>n</sub> (Stored Mode)
L	L	X	↘	X	H			Clock B <sub>n</sub> Data into B Register and Output to A <sub>n</sub>

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Irrelevant  
 ↘ = LOW-to-HIGH Transition

**Note 1:** The data output functions may be enabled or disabled by various signals at the  $\overline{G}$  and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.



**Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)		Junction Temperature ( $T_J$ )
Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V	PDIP 140°C
DC Input Diode Current ( $I_{IK}$ )		
$V_I = -0.5V$	-20 mA	
$V_I = V_{CC} + 0.5V$	+20 mA	
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$	
DC Output Diode Current ( $I_{OK}$ )		
$V_O = -0.5V$	-20 mA	
$V_O = V_{CC} + 0.5V$	+20 mA	
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$	
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA	
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA	
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C	

Recommended Operating Conditions	
Supply Voltage ( $V_{CC}$ )	2.0V to 6.0V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	125 mV/ns
	$V_{IN}$ from 30% to 70% of $V_{CC}$
	$V_{CC}$ @ 3.3V, 4.5V, 5.5V

**Note 2:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

## DC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions	
			Typ	Guaranteed Limits					
$V_{IH}$	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	3.15	3.15				
		5.5	2.75	3.85	3.85				
$V_{IL}$	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	1.35	1.35				
		5.5	2.75	1.65	1.65				
$V_{OH}$	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9		V	$I_{OUT} = -50 \mu\text{A}$	
		4.5	4.49	4.4	4.4				
		5.5	5.49	5.4	5.4				
			3.0		2.56	2.46		V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ (Note 3)
			4.5		3.86	3.76			
			5.5		4.86	4.76			
$V_{OL}$	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1		V	$I_{OUT} = 50 \mu\text{A}$	
		4.5	0.001	0.1	0.1				
		5.5	0.001	0.1	0.1				
			3.0		0.36	0.44		V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ (Note 3)
			4.5		0.36	0.44			
			5.5		0.36	0.44			
$I_{IN}$ (Note 5)	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$		$\mu\text{A}$	$V_I = V_{CC}, \text{GND}$	
$I_{OLD}$	Minimum Dynamic	5.5			75		mA	$V_{OLD} = 1.65V \text{ Max}$	
$I_{OHD}$	Output Current (Note 4)	5.5			-75		mA	$V_{OHD} = 3.85V \text{ Min}$	
$I_{CC}$ (Note 5)	Maximum Quiescent Supply Current	5.5		8.0	80.0		$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND	
$I_{OZT}$	Maximum I/O Leakage Current	5.5		$\pm 0.6$	$\pm 6.0$		$\mu\text{A}$	$V_I$ (OE) = $V_{IL}, V_{IH}$ $V_I = V_{CC}, \text{GND}$ $V_O = V_{CC}, \text{GND}$	

**Note 3:** All outputs loaded; thresholds on input associated with output under test.

**Note 4:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 5:**  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .

AC Electrical Characteristics								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 6)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay Clock to Bus	3.3	1.5	10.0	15.5	1.5	17.0	ns
		5.0	1.5	7.0	11.0	1.5	12.0	
t <sub>PHL</sub>	Propagation Delay Clock to Bus	3.3	1.5	8.5	13.5	1.5	14.5	ns
		5.0	1.5	6.0	10.5	1.5	11.5	
t <sub>PLH</sub>	Propagation Delay Bus to Bus	3.3	1.5	6.0	10.0	1.5	11.0	ns
		5.0	1.5	4.0	7.0	1.0	7.5	
t <sub>PHL</sub>	Propagation Delay Bus to Bus	3.3	1.5	5.5	9.0	1.5	10.0	ns
		5.0	1.5	3.5	7.5	1.0	8.0	
t <sub>PLH</sub>	Propagation Delay SBA or SAB to A <sub>n</sub> or B <sub>n</sub> (with A <sub>n</sub> or B <sub>n</sub> HIGH or LOW)	3.3	1.5	7.5	12.5	1.5	14.0	ns
		5.0	1.5	5.5	9.0	1.5	10.0	
t <sub>PHL</sub>	Propagation Delay SBA or SAB to A <sub>n</sub> or B <sub>n</sub> (with A <sub>n</sub> or B <sub>n</sub> HIGH or LOW)	3.3	1.5	7.5	12.5	1.5	14.0	ns
		5.0	1.5	5.5	9.5	1.5	10.5	
t <sub>PZH</sub>	Enable Time $\bar{G}$ to A <sub>n</sub> or B <sub>n</sub>	3.3	1.5	6.5	11.0	1.0	11.5	ns
		5.0	1.5	5.0	8.0	1.0	9.0	
t <sub>PZL</sub>	Enable Time $\bar{G}$ to A <sub>n</sub> or B <sub>n</sub>	3.3	1.5	7.0	11.0	1.0	12.5	ns
		5.0	1.5	5.0	8.0	1.0	9.0	
t <sub>PHZ</sub>	Disable Time $\bar{G}$ to A <sub>n</sub> or B <sub>n</sub>	3.3	1.5	7.5	12.0	1.0	13.0	ns
		5.0	1.5	6.0	10.0	1.0	11.0	
t <sub>PLZ</sub>	Disable Time $\bar{G}$ to A <sub>n</sub> or B <sub>n</sub>	3.3	1.5	7.0	11.5	1.0	12.5	ns
		5.0	1.5	5.5	9.0	1.0	10.0	
t <sub>PZH</sub>	Enable Time DIR to A <sub>n</sub> or B <sub>n</sub>	3.3	1.5	6.0	12.5	1.0	14.0	ns
		5.0	1.5	4.5	9.5	1.0	10.5	
t <sub>PZL</sub>	Enable Time DIR to A <sub>n</sub> or B <sub>n</sub>	3.3	1.5	6.5	13.0	1.5	14.5	ns
		5.0	1.5	4.5	9.0	1.0	10.5	
t <sub>PHZ</sub>	Disable Time DIR to A <sub>n</sub> or B <sub>n</sub>	3.3	1.5	7.0	11.5	1.0	13.5	ns
		5.0	1.5	5.5	9.0	1.0	10.0	
t <sub>PLZ</sub>	Disable Time DIR to A <sub>n</sub> or B <sub>n</sub>	3.3	1.5	7.0	13.5	1.5	15.0	ns
		5.0	1.5	5.0	9.5	1.0	10.0	

**Note 6:** Voltage Range 3.3 is 3.3V ±0.3V  
Voltage Range 5.0 is 5.0V ±0.5V

### AC Operating Requirements

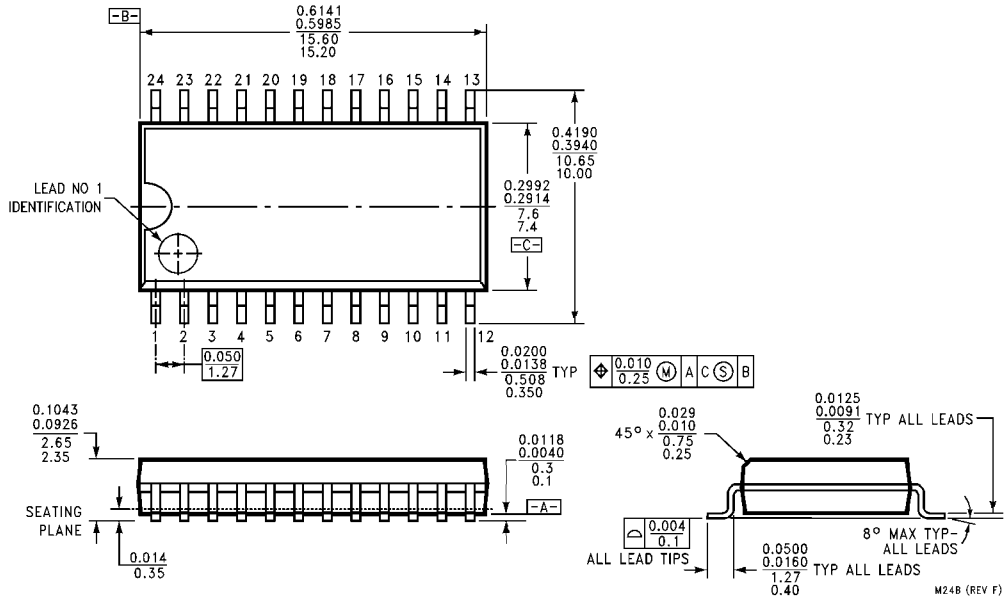
Symbol	Parameter	V <sub>CC</sub> (V) (Note 7)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Typ	Guaranteed Minimum	Guaranteed Minimum		
t <sub>S</sub>	Setup Time, HIGH or LOW, Bus to Clock	3.3	2.0	3.0	3.5		ns
		5.0	1.5	2.0	2.0		
t <sub>H</sub>	Hold Time, HIGH or LOW, Bus to Clock	3.3	-1.5	0	0		ns
		5.0	-0.5	1.0	1.0		
t <sub>W</sub>	Clock Pulse Width HIGH or LOW	3.3	2.0	3.5	4.0		ns
		5.0	2.0	3.0	3.0		

**Note 7:** Voltage Range 3.3 is 3.3V ±0.3V  
Voltage Range 5.0 is 5.0V ±0.5V

### Capacitance

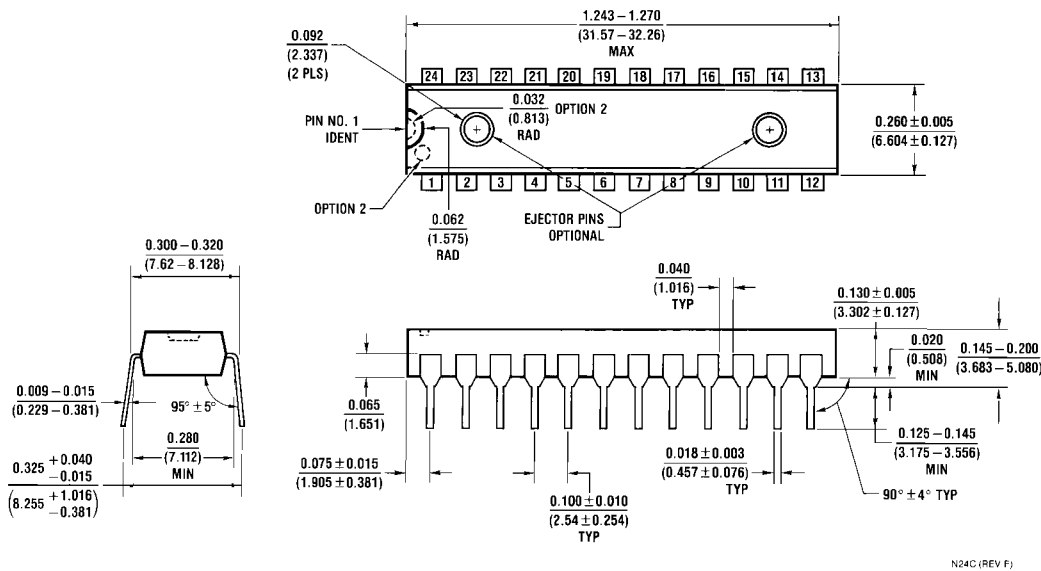
Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	65.0	pF	V <sub>CC</sub> = 5.0V
C <sub>I/O</sub>	Input/Output Capacitance	15.0	pF	V <sub>CC</sub> = 5.0V

**Physical Dimensions** inches (millimeters) unless otherwise noted



**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body  
Package Number M24B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300" Wide Package Number N24C**

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