

## N-channel 100 V, 0.062 $\Omega$ typ., 4 A STripFET™ VII DeepGATE™ Power MOSFET in a PowerFLAT™ 2x2 package

Datasheet - production data

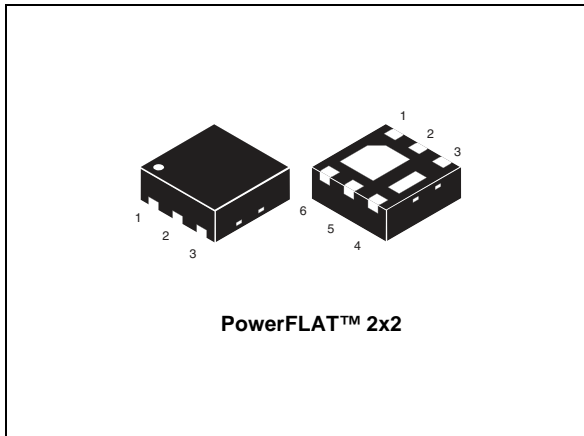
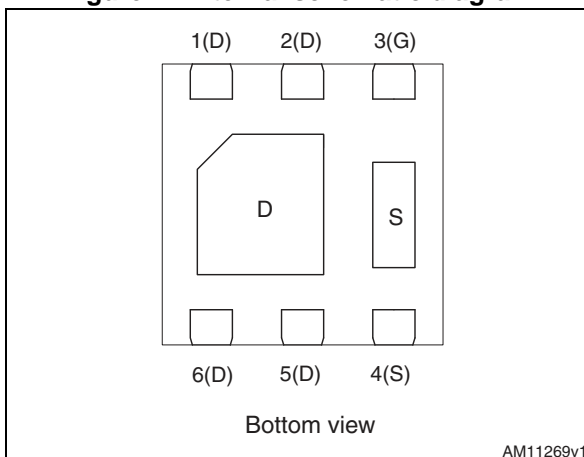


Figure 1. Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STL3N10F7	100 V	0.07 $\Omega$	4 A

- N-channel enhancement mode
- Low gate charge
- 100% avalanche rated

### Applications

- Switching applications

### Description

This device utilizes the 7<sup>th</sup> generation of design rules of ST's proprietary STripFET™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R<sub>DS(on)</sub> in all packages.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STL3N10F7	ST3N	PowerFLAT™ 2x2	Tape and reel

## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>9</b>
<b>5</b>	<b>Revision history</b> .....	<b>12</b>

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	100	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	4	A
$I_D^{(1)}$	Drain current (continuous) at $T_{pcb}=100\text{ }^\circ\text{C}$	2.5	A
$I_{DM}^{(2)}$	Drain current (pulsed)	16	A
$P_{TOT}^{(1)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	2.4	W
$T_J$	Operating junction temperature	-55 to 150	$^\circ\text{C}$
$T_{stg}$	storage temperature		$^\circ\text{C}$

1. The value is rated according  $R_{thj-pcb}$
2. Pulse width limited by safe operating area.

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	52	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ sec}$

## 2 Electrical characteristics

( $T_{CASE}=25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage, $V_{GS}=0$	$I_D = 250\ \mu A$	100			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS}=0$ )	$V_{DS} = 100\text{ V}$			1	$\mu A$
		$V_{DS} = 100\text{ V}$ , $T_C = 125\text{ °C}$			100	$\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS}=0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu A$	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 2\text{ A}$		0.062	0.07	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	408	-	pF
$C_{oss}$	Output capacitance		-	112	-	pF
$C_{rss}$	Reverse transfer capacitance		-	10	-	pF
$Q_g$	Total gate charge	$V_{DD} = 50\text{ V}$ , $I_D = 4\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 14)	-	7.8	-	nC
$Q_{gs}$	Gate-source charge		-	3	-	nC
$Q_{gd}$	Gate-drain charge		-	1.7	-	nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\text{ V}$ , $I_D = 2\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 13)	-	6.3	-	ns
$t_r$	Rise time		-	3	-	ns
$t_{d(off)}$	Turn-off delay time		-	11	-	ns
$t_f$	Fall time		-	4	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		16	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=2\text{ A}$ , $V_{GS}=0$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD}=2\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=80\text{ V}$ , $T_J=150\text{ }^\circ\text{C}$ <i>(see Figure 18)</i>	-	30		ns
$Q_{rr}$	Reverse recovery charge		-	24		nC
$I_{RRM}$	Reverse recovery current		-	1.6		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

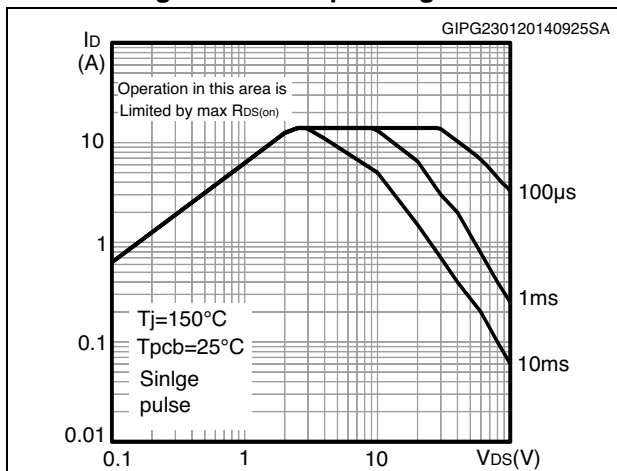


Figure 3. Thermal impedance

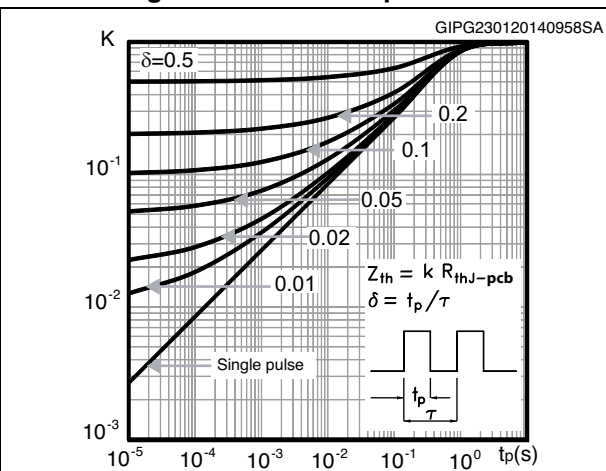


Figure 4. Output characteristics

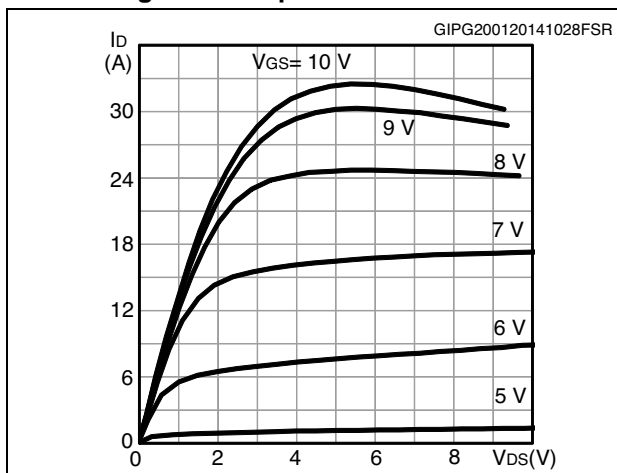


Figure 5. Transfer characteristics

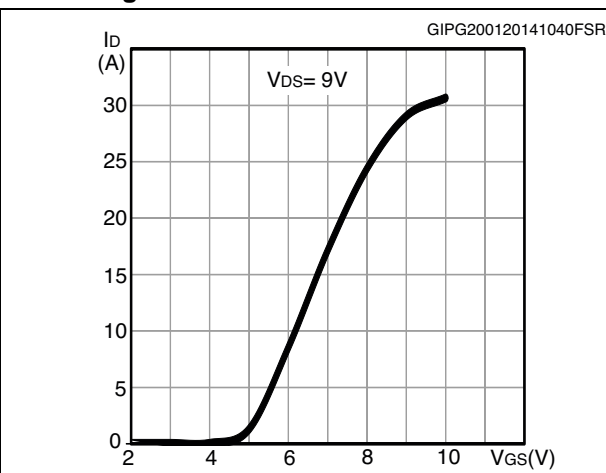


Figure 6. Gate charge vs gate-source voltage

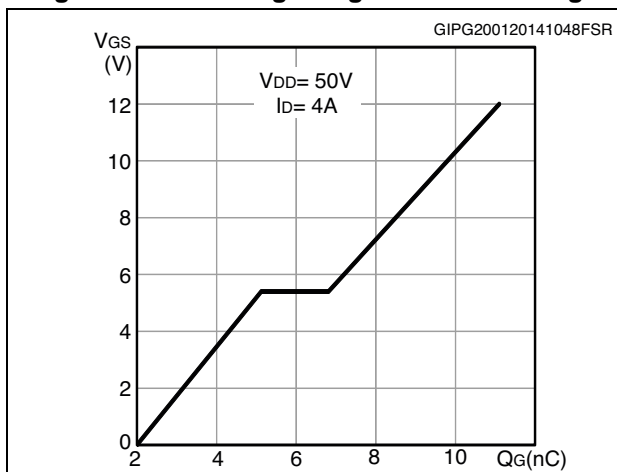


Figure 7. Static drain-source on-resistance

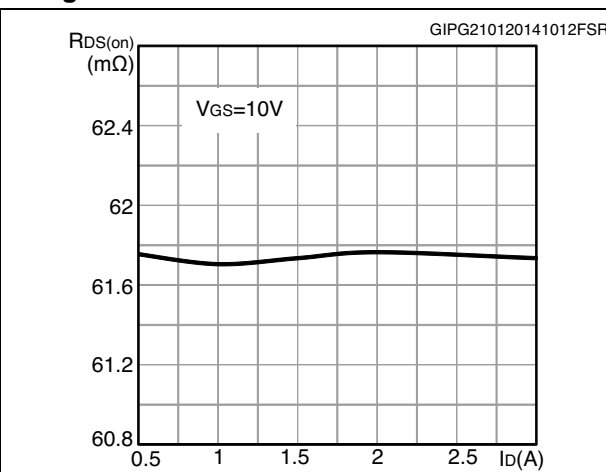


Figure 8. Capacitance variations

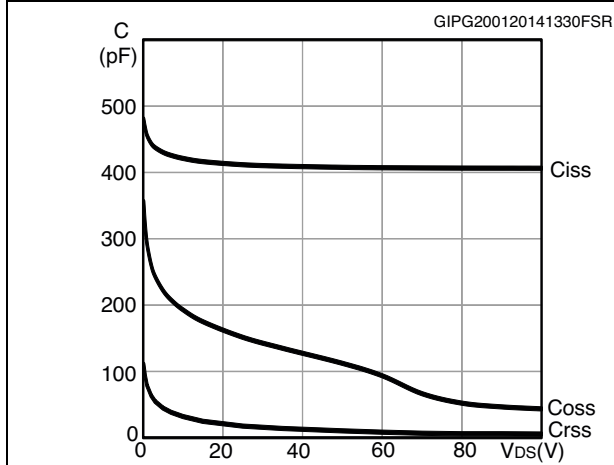


Figure 9. Normalized  $V_{(BR)DSS}$  vs temperature

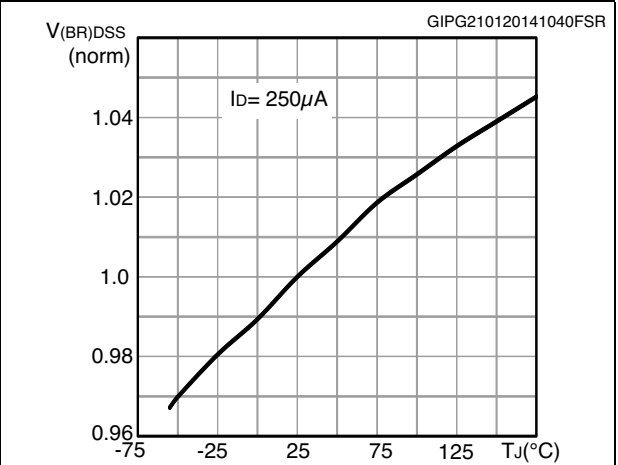


Figure 10. Normalized gate threshold voltage vs temperature

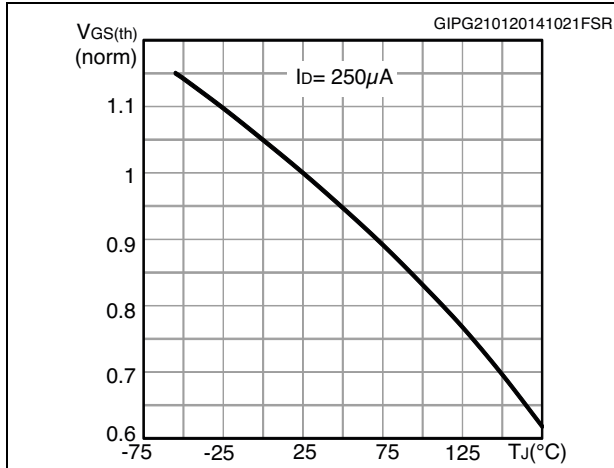


Figure 11. Normalized on-resistance vs temperature

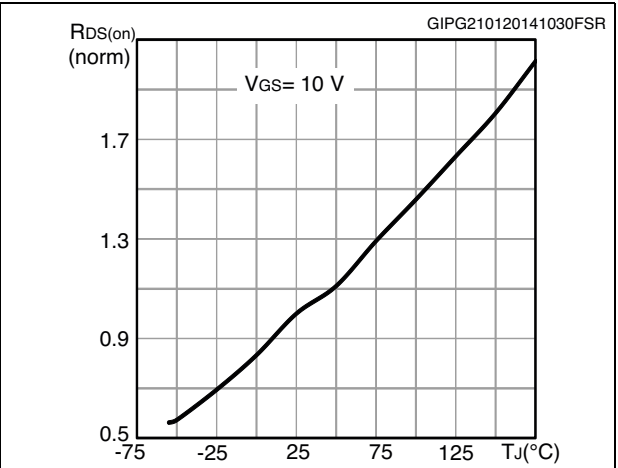
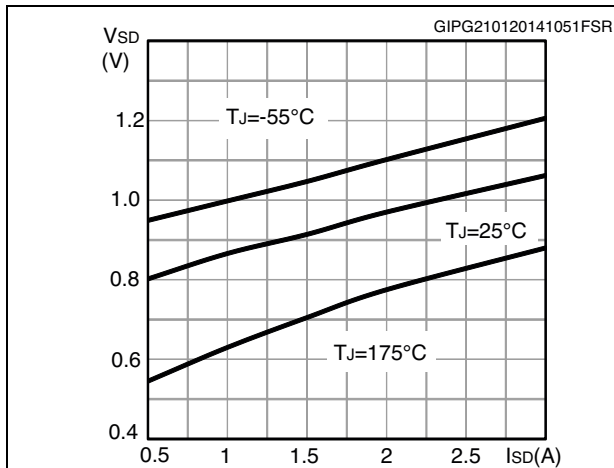
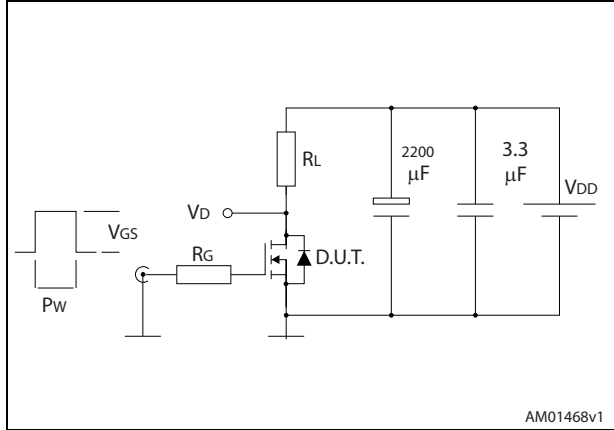


Figure 12. Source-drain diode forward characteristics

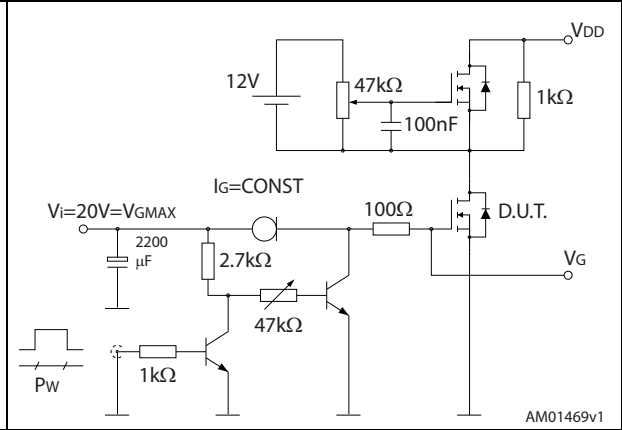


### 3 Test circuits

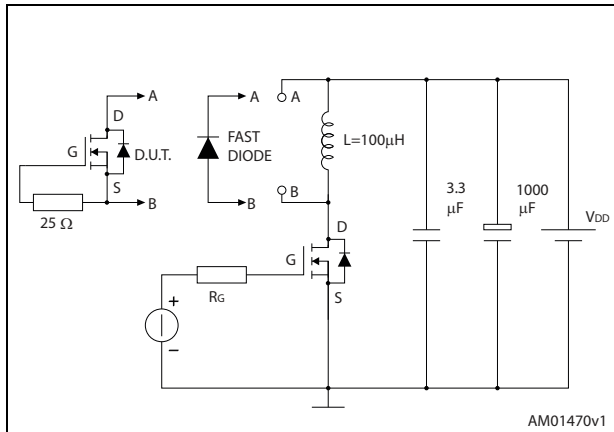
**Figure 13. Switching times test circuit for resistive load**



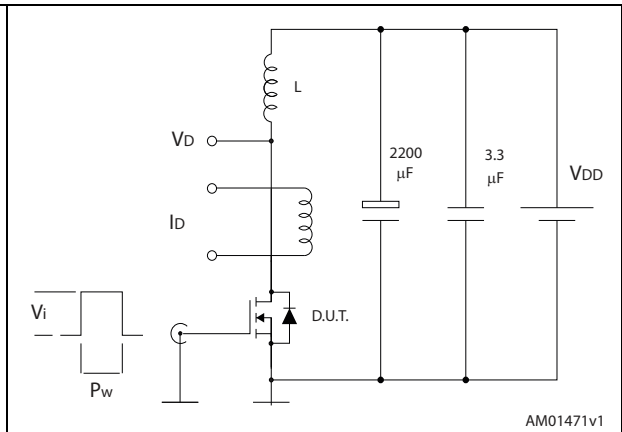
**Figure 14. Gate charge test circuit**



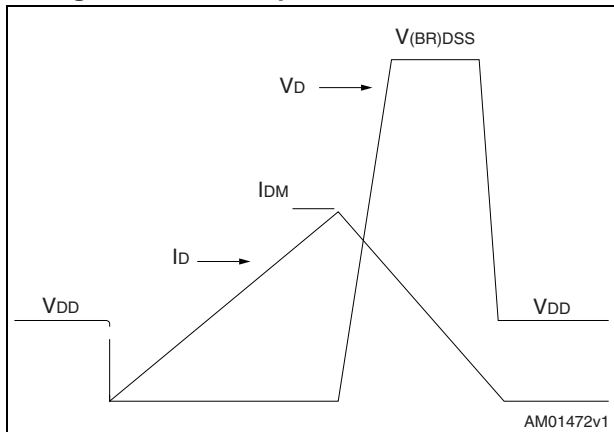
**Figure 15. Test circuit for inductive load switching and diode recovery times**



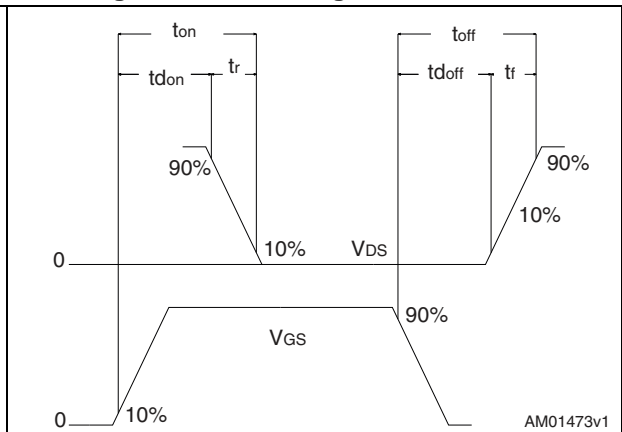
**Figure 16. Unclamped inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



**Figure 18. Switching time waveform**





## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 19. Drawing dimension PowerFLAT™ 2x2

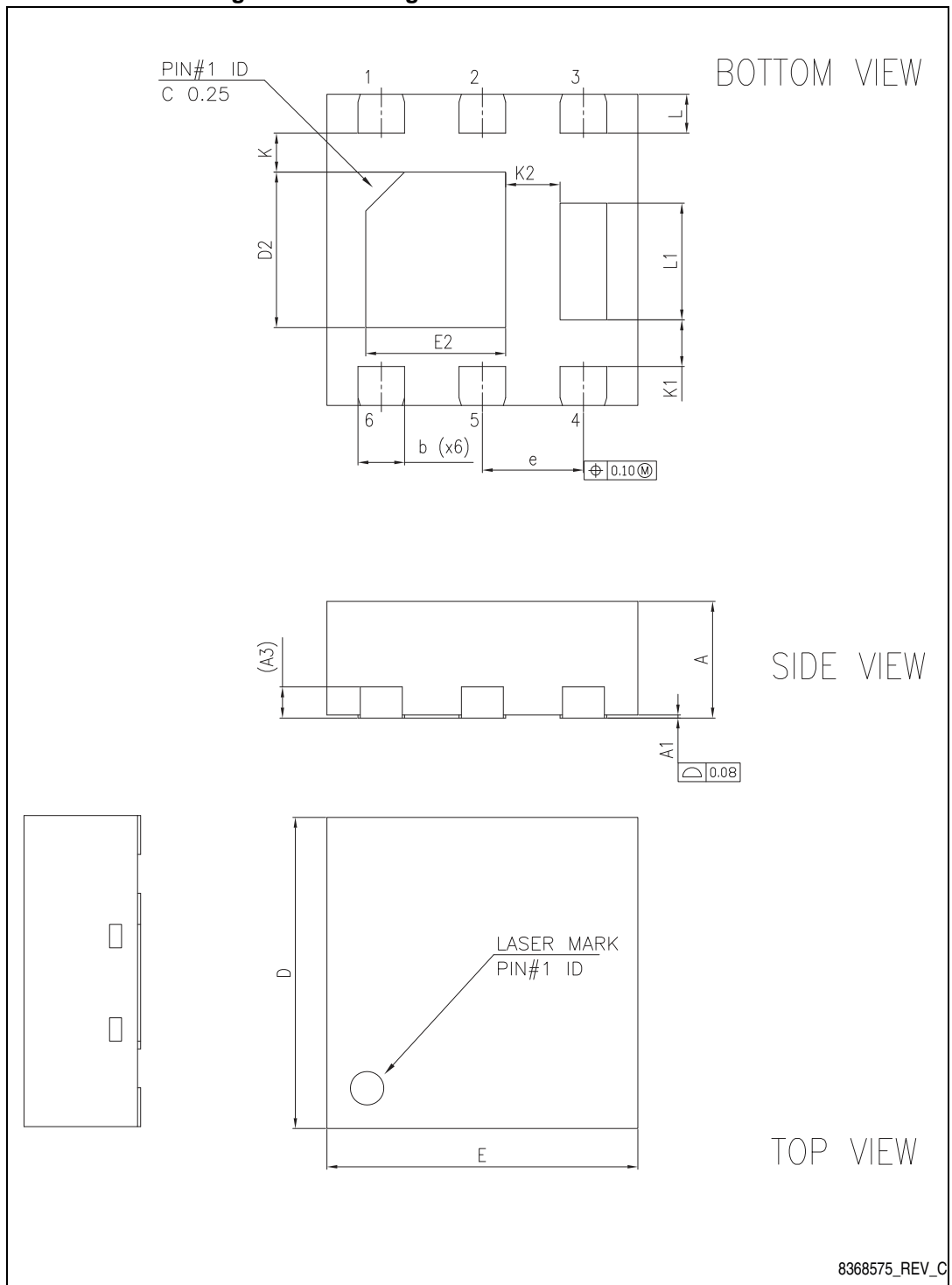
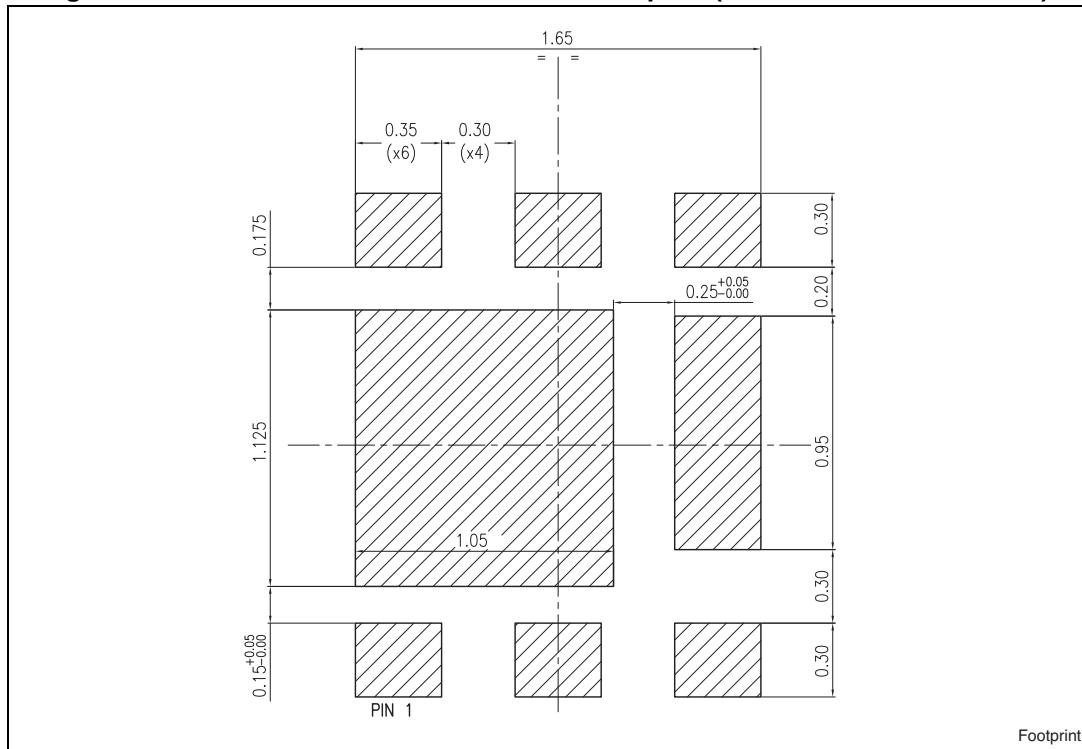


Table 8. PowerFLAT™ 2 x 2 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.90	1.00	1.10
E2	0.80	0.90	1.00
e	0.55	0.65	0.75
K	0.15	0.25	0.35
K1	0.20	0.30	0.40
K2	0.25	0.35	0.45
L	0.20	0.25	0.30
L1	0.65	0.75	0.85

Figure 20. PowerFLAT™ 2x2 recommended footprint (all dimensions are in mm)



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
18-Feb-2014	1	First release.
30-Apr-2014	2	Document status promoted from preliminary to production data

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