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# DS26LS32MQML

## Quad Differential Line Receivers

### General Description

The DS26LS32 and DS26LS32A are quad differential line receivers designed to meet the RS-422, RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26LS32 and DS26LS32A have an input sensitivity of 200 mV over the input voltage range of  $\pm 7V$  and the DS26LS33 have an input sensitivity of 500 mV over the input voltage range of  $\pm 15V$ .

The DS26LS32A differ in function from the popular DS26LS32 and DS26LS33 in that input pull-up and pull-down resistors are included which prevent output oscillation on unused channels.

Each version provides an enable and disable function common to all four receivers and features TRI-STATE<sup>®</sup> outputs with 8 mA sink capability. Constructed using low power

Schottky processing, these devices are available over the full military and commercial operating temperature ranges.

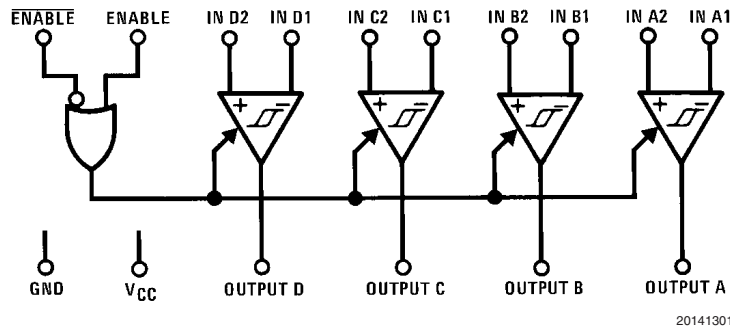
### Features

- High differential or common-mode input voltage ranges of  $\pm 7V$  on the DS26LS32.
- $\pm 0.2V$  sensitivity over the input voltage range on the DS26LS32.
- DS26LS32 meet all requirements of RS-422 and RS-423
- 6k minimum input impedance
- 100 mV input hysteresis on the DS26LS32
- Operation from a single 5V supply
- TRI-STATE outputs, with choice of complementary output enables for receiving directly onto a data bus

### Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Description
DS26LS32ME/883	5962-7802006Q2A	E20A	20LD LEADLESS CHIP CARRIER
DS26LS32MJ/883	5962-7802006QEA	J16A	16LD CERDIP
DS26LS32MW/883	5962-7802006QFA	W16A	16LD CERPACK

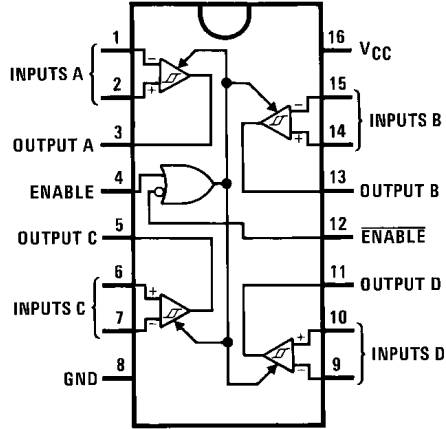
### Logic Diagram



TRI-STATE<sup>®</sup> is a registered trademark of National Semiconductor Corporation.

## Connection Diagrams

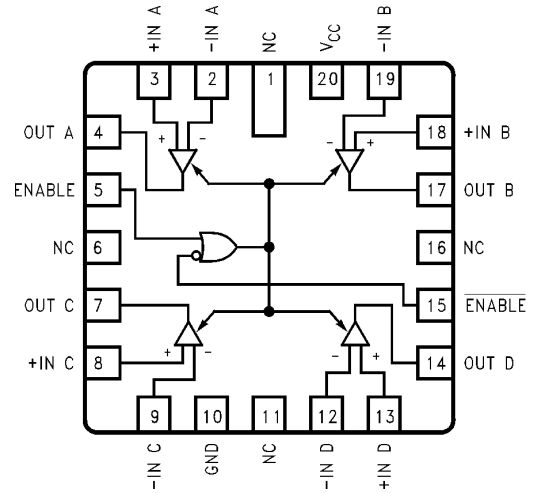
Dual-In-Line Package



20141302

Top View  
See NS Package Number J16A or W16A

20-Lead Ceramic Leadless Chip Carrier



20141312

Top View  
See NS Package Number E20A,

## Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
0	1	X	Hi-Z
See Note Below		$V_{ID} \geq V_{TH} (\text{Max})$	1
		$V_{ID} \leq V_{TH} (\text{Min})$	0

Hi-Z = TRI-STATE®

Note: Input conditions may be any combination not defined for ENABLE and  $\overline{\text{ENABLE}}$ .

## Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Common-Mode Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7V
Output Sink Current	50 mA
Maximum Power Dissipation at 25°C (Note 2)	
J Package	1666.5 mW
E Package	1875 mW
W Package	967.74 mW
Junction Temperature (T <sub>J</sub> )	+150°C
Thermal Resistance, Junction-to-Ambient	
θ <sub>JA</sub>	
J Package	100°C/W
E Package	130°C/W
W Package	140°C/W
Thermal Resistance, Junction-to-Ambient	
θ <sub>JC</sub>	See MIL-STD-1835
Storage Temperature Range	-65°C to +165°C
Lead Temperature (Soldering, 4 seconds)	260°C
ESD Tolerance (Note 3)	500V

## Recommended Operating Conditions

Supply Voltage, V <sub>CC</sub>	4.5 V to 5.5 V
Temperature, T <sub>A</sub>	-55°C to +125°C

## Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

Subgroup	Description	Temp ( °C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

## DS26LS32M 883 Electrical Characteristics

### DC Parameters

The following conditions apply, unless otherwise specified.  $V_{CC} = 5V$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
$I_{IN}$	Input Current	$V_{CC} = 5.5V, V_{IN} = 15V$ (Pin under test), other inputs $-15V, \leq V_{IN} \leq +15V$	(Note 5)		2.3	mA	1, 2, 3
		$V_{CC} = 5.5V, V_{IN} = -15V$ (Pin under test), other inputs $-15V, \leq V_{IN} \leq +15V$	(Note 5)		-2.8	mA	1, 2, 3
$I_{IL}$	Logical "0" ENABLE Current	$V_{CC} = 5.5V, V_{IN} = 0.4V$	(Note 5)		-360	$\mu A$	1, 2, 3
$I_{IH}$	Logical "1" ENABLE Current	$V_{CC} = 5.5V, V_{IN} = 2.7V$	(Note 5)		20	$\mu A$	1, 2, 3
$I_I$	Logical "1" ENABLE Current	$V_{CC} = 5.5V, V_{IN} = 5.5V$	(Note 5)		100	$\mu A$	1, 2, 3
$V_{IC}$	Input Clamp Voltage (ENABLE)	$V_{CC} = 4.5V, I_{IN} = -18mA$	(Note 5)		-1.5	V	1, 2, 3
$V_{OH}$	Logical "1" Output Voltage	$V_{CC} = 4.5V, I_{OH} = -440\mu A, \Delta V_{IN} = 1V, V_{ENABLE} = 0.8V$	(Note 5)	2.5		V	1, 2, 3
$V_{OL}$	Logical "0" Output Voltage	$V_{CC} = 4.5V, I_{OL} = 4mA, \Delta V_{IN} = -1V, V_{ENABLE} = 0.8V$	(Note 5)		.4	V	1, 2, 3
		$V_{CC} = 4.5V, I_{OL} = 8mA, \Delta V_{IN} = -1V, V_{ENABLE} = 0.8V$	(Note 5)		.45	V	1, 2, 3
$I_{OS} (MIN)$	Output Short Circuit Current	$V_{CC} = 5.5V, V_O = 0V, \Delta V_{IN} = 1V$	(Note 5)	-15		mA	1, 2, 3
$I_{OS} (MAX)$	Output Short Circuit Current	$V_{CC} = 5.5V, V_O = 0V, \Delta V_{IN} = 1V$	(Note 5)		-85	mA	1, 2, 3
$I_{CC}$	Supply Current	$V_{CC} = 5.5V, \text{All } V_{IN} = GND, \text{Outputs Disabled}$	(Note 5)		70	mA	1, 2, 3
$I_O$	Off-State Output Current	$V_{CC} = 5.5V, V_O = 0.4V$	(Note 5)		-20	$\mu A$	1, 2, 3
		$V_{CC} = 5.5V, V_O = 2.4V$	(Note 5)		20	$\mu A$	1, 2, 3
$V_{TH}$	Differential Input Voltage	$-7V \leq V_{CM} \leq 7V$	(Notes 4, 5)	-0.2	0.2	V	1, 2, 3
$R_{IN}$	Input Resistance	$-15V \leq V_{CM} \leq 15V$	(Note 5)	6		kohm	1, 2, 3
$V_{IL}$	Logical "0" Input Voltage (ENABLE)	$V_{CC} = 4.5V$	(Notes 4, 5)		0.8	V	1, 2, 3
$V_{IH}$	Logical "1" Input Voltage (ENABLE)	$V_{CC} = 4.5V$	(Notes 4, 5)	2		V	1, 2, 3

## DS26LS32M 883 Electrical Characteristics (Continued)

### AC Parameters - Propagation Delay Time

The following conditions apply, unless otherwise specified.  $V_{CC} = 5V$

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
$t_{PLH}$	Propagation Delay Time	$C_L = 15_pF$	(Note 6)		30	nS	9,11,
$t_{PLH}$	Propagation Delay Time	$C_L = 15_pF$	(Note 6)		120	nS	10
$t_{PHL}$	Propagation Delay Time	$C_L = 15_pF$	(Note 6)		30	nS	9,11,
$t_{PHL}$	Propagation Delay Time	$C_L = 15_pF$	(Note 6)		120	nS	10
$t_{PLZ}$	Enable to Output	$\overline{ENABLE} C_L = 5_pF$	(Note 6)		34	nS	9
		$\overline{ENABLE} C_L = 5_pF$	(Note 6)		64	nS	10
		$\overline{ENABLE} C_L = 5_pF$	(Note 6)		27	nS	11
$t_{PHZ}$	Enable to Output	$\overline{ENABLE} C_L = 5_pF$	(Note 6)		32	nS	9,11,
		$\overline{ENABLE} C_L = 5_pF$	(Note 6)		35	nS	10
$t_{PZL}$	Enable to Output	$\overline{ENABLE} C_L = 15_pF$	(Note 6)		34	nS	9
		$\overline{ENABLE} C_L = 15_pF$	(Note 6)		65	nS	10
		$\overline{ENABLE} C_L = 15_pF$	(Note 6)		27	nS	11
$t_{PZH}$	Enable to Output	$\overline{ENABLE} C_L = 15_pF$	(Note 6)		35	nS	9, 11
		$\overline{ENABLE} C_L = 15_pF$	(Note 6)		65	nS	10

**Note 1:** Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** Derate J package 11.11 mW/°C above 25°C; derate E package 12.5 mW/°C above 25°C; derate W Package 6.4516 mW/°C for above 25°C.

**Note 3:** Human body model, 1.5kΩ in series with 100pF.

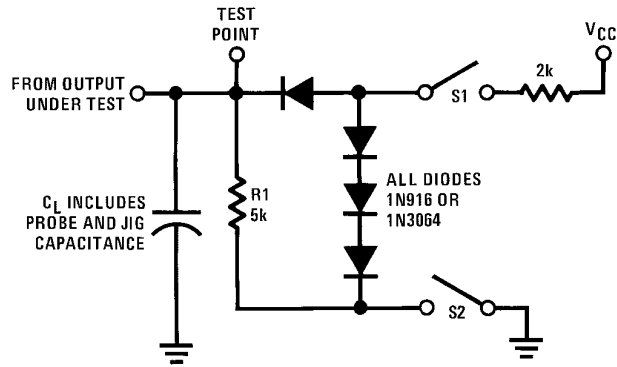
**Note 4:** Parameter tested go-no-go only.

**Note 5:** For Subgroups 1 and 2, power dissipation must be externally controlled at elevated temperatures.

**Note 6:** Tested at 25°C, guaranteed but not tested at +125°C & -55°C

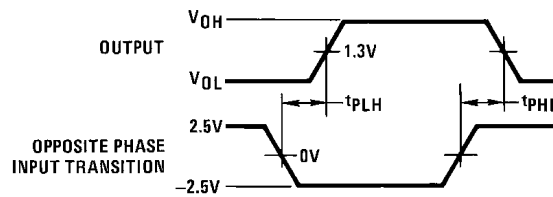
# AC Test Circuit and Switching Time Waveforms

Load Test Circuit for TRI-STATE® Outputs



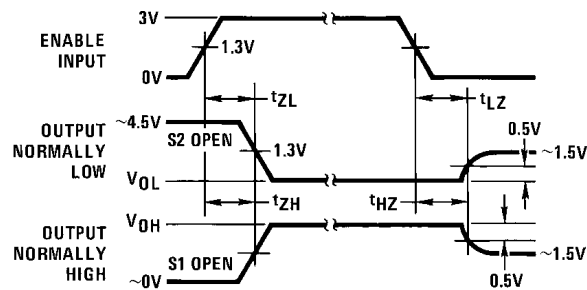
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Propagation Delay (Notes 7, 9)



20141304

Enable and Disable Times (Notes 8, 9)



20141305

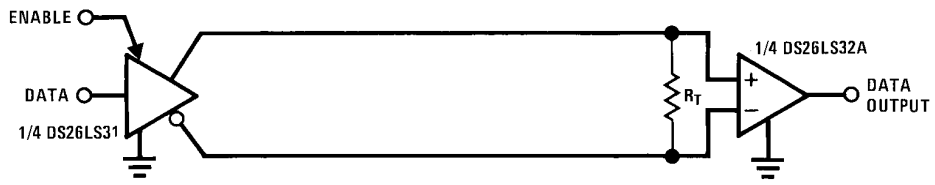
**Note 7:** Diagram shown for  $\overline{\text{ENABLE}}$  low.

**Note 8:** S1 and S2 of load circuit are closed except where shown.

**Note 9:** Pulse generator for all pulses: Rate = 1.0 MHz;  $Z_O = 50\Omega$ ;  $t_r \leq 6 \text{ ns}$ ;  $t_f \leq 6.0 \text{ ns}$ .

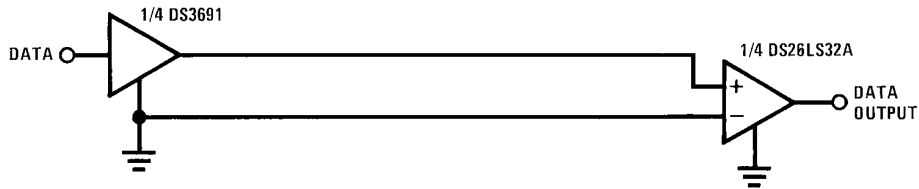
# Typical Applications

### Two-Wire Balanced Interface—RS-422



20141306

### Single Wire with Driver Ground Reference—RS-423



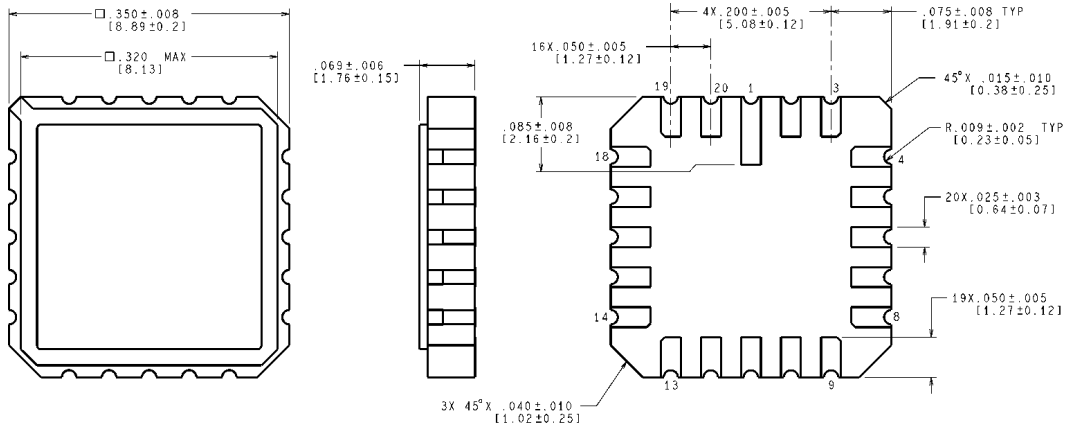
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## Revision History

Date Released	Revision	Section	Originator	Changes
10/20/05	A	New Release, Corporate format. Changes made in conversion: Ordering Info. Table, Absolute Ratings, Maximum Operating Conditions, Typo's in QMLV & RH, 883 AC Electrical Characteristics Parameters Column.	R. Malone	1 MDS data sheet converted into Corporate data sheet format. <b>Added:</b> SMD reference for 883 NSID's, Junction temp., Thermal Resistance $\theta_{JA}$ and $\theta_{JC}$ . <b>Changed:</b> Maximum Operating Conditions to Recommended Operating Conditions, Enable and Disable Time to Enable to Output. Deleted max limit: 27nS for $t_{PZH}$ and added subgroup 11 to max limit 35nS. MDS data sheet MNDS26LS32-X, Rev. 2B0 will be Archived.
10/05/06	B	Ordering Information	R. Malone	Corrected suffix's in the SMD number. Revision A will be Archived.

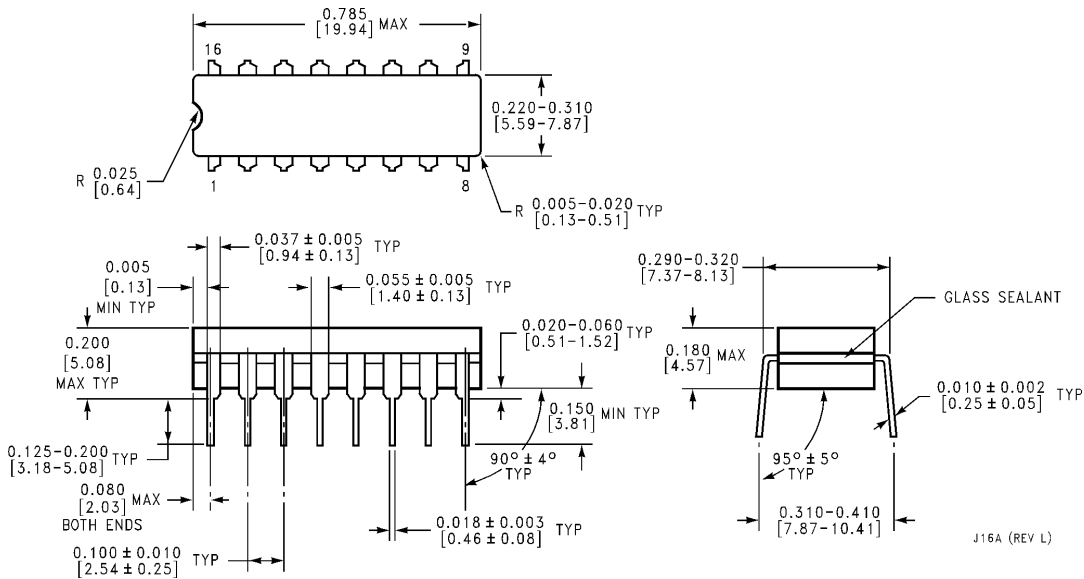
**Physical Dimensions** inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS INCH  
 VALUES IN [ ] ARE MILLIMETERS

E20A (Rev F)

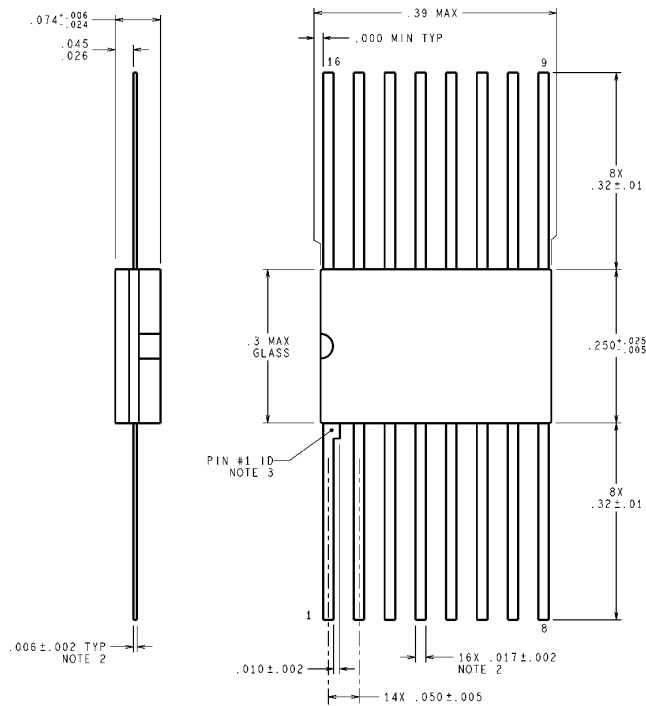
**20 Lead Ceramic Leadless Chip Carrier (E)  
 NS Package Number E20A**



J16A (REV L)

**Ceramic Dual-In-Line Package (J)  
 NS Package Number J16A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN INCHES

W16A (Rev T)

**16 Lead Ceramic Flatpak (W)  
NS Package Number W16A**

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