PGA970EVM User's Guide

User's Guide

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PGA970EVM User's Guide

The PGA970EVM provides a platform to test the PGA970 in the QFN package.

1 Introduction

Figure 1 shows the PGA970EVM and its main sections.

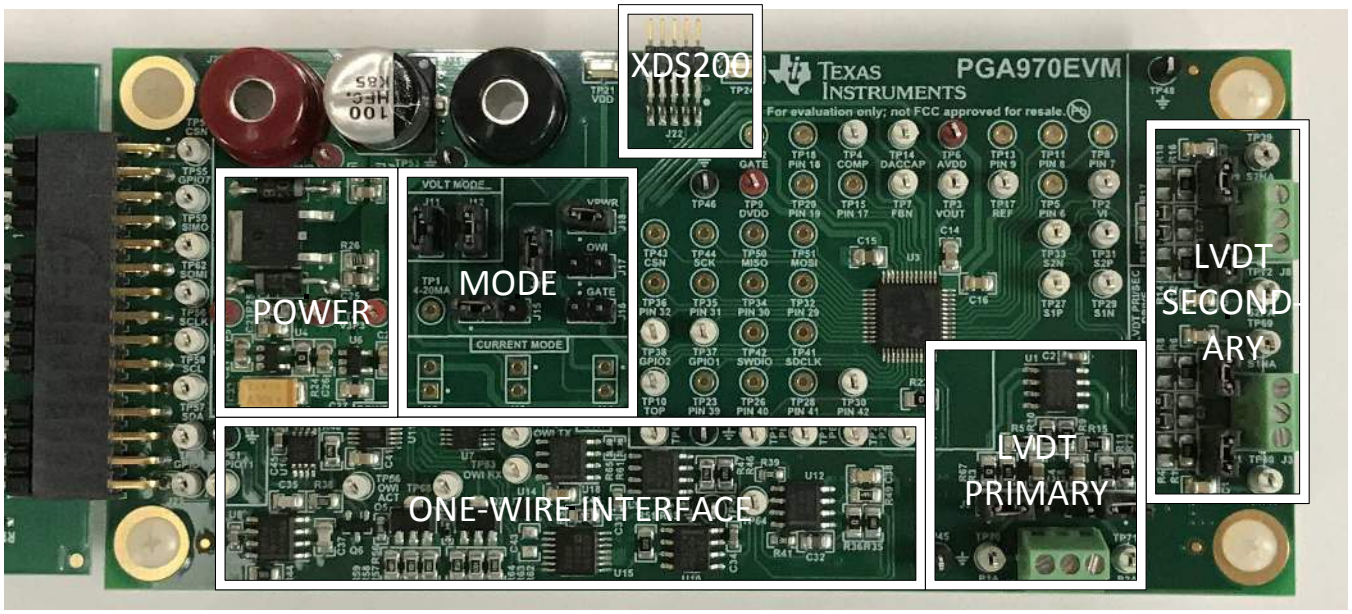

Figure 1. PGA970EVM

The PGA970EVM is divided into six sections:

1. Interface boards and external power:
   (a) USB2ANY connector
   (b) XDS200 connector (single wire debugger)
   (c) Banana connectors to power up EVM
2. Power:
   (a) 7.5-V, 5-V, and 3.3-V regulators
3. Mode selection
   (a) Voltage mode
   (b) 4- to 20-mA loop (3-wire current mode; this section is not placed on the board)
4. OWI circuitry
5. LVDT Primary Driver and Secondary Return

2 Default Configuration

The EVM requires a 10- to 30-V input applied to J11 and J12. Clamp the power supply current to 100 mA. The EVM is shipped configured for voltage mode as shown in Table 1.

Table 1. Default PGA970EVM Jumper Configuration (Voltage Mode)

	JUMPERS	PURPOSE
VDD	J18 closed. J16 and J17 open	PGA970 powered up from VPWR (VDD=VPWR)
LVDT Primary Drive	J2 and J7 tied between pins 1 and 2	External amplifier for P1 and P2 LVDT drive is bypassed
LVDT Secondary Filtering	J1, J4, J6, J9 closed	External filtering and attenuation for secondary inputs to S1 and S2 bypassed
Output	J11, J12 closed	Voltage mode with 100-nF load, with capacitive load compensation
Gate Drive	J19 closed	GATE pin grounded

3 Inputs and Output Configurations

3.1 LVDT Primary and Secondary Drive

The PGA970EVM provides screw terminal connectors J3, J5, and J8 interfacing with the Primary and Secondary of an LVDT. In the default configuration, the Waveform Output Pins of the PGA970, P1 and P2, are tied directly to these terminals. The alternative Jumper configuration allows the user to amplify the waveform for higher voltage LVDT applications. This amplifier provides a gain of 16.1 V/V. In a typical PGA970 Waveform configuration of 0.375 V Amplitude from the Waveform DAC and 1.67 V/V Waveform Gain, this output of this external amplifier will allow the user to have a 20 V peak-to-peak, 7.07 Vrms signal at the terminal connection. If additional current driving capabilities are needed in a resolver or similar, large-load applications, we provided the footprint for an additional drive stage to handle such loads.

The LVDT Secondary side of the PGA970EVM provides footprints to allow for any necessary external filtering or decoupling before being tied to the PGA970 S1 and S2 inputs. In the case that the external amplifier is used on the primary side, the removing jumpers J1, J4, J6, and J9 will provide both decoupling and resistance in the path to attenuate the signal. A resistor divider is created with the internal impedance of these pins, allowing the return signal to be within a measurable amplitude of the ADC.

Figure 2 shows a simple functionality diagram of the Primary and Secondary Drive capabilities on the PGA970EVM.

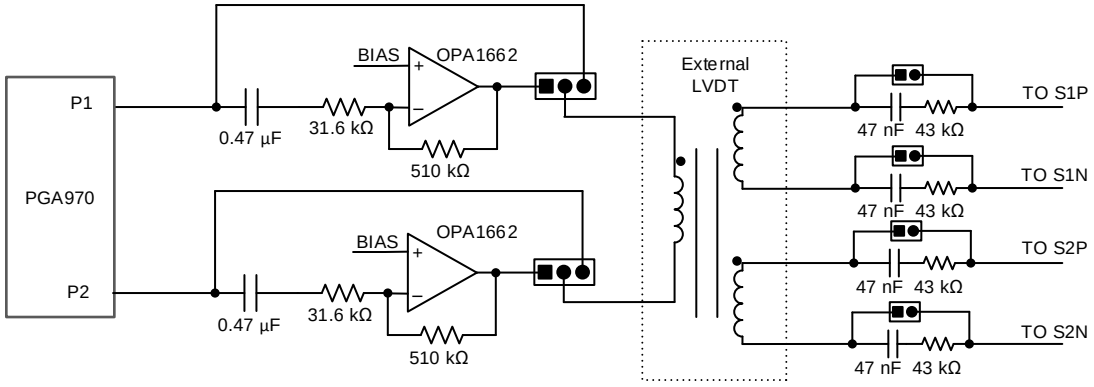

Figure 2. LVDT Primary and Secondary Drive in the PGA970EVM

3.2 Temperature Input

The PGA970EVM does not have on-board stimulus for the temperature inputs of the PGA970. However, the AIN pin, connected to TP2, can be used to provide an external single-ended connection to a temperature sensor.

3.3 Voltage Mode Output

The PGA970EVM is by default configured in voltage mode with a 100-nF load. A compensation capacitor and an isolation resistor are needed for stability. Figure 3 shows the PGA970 schematic for voltage mode and Table 1 shows all the jumpers needed to configure the board in this mode. If the capacitive load is different from 100 nF, then the isolation resistor and compensation capacitor values need to be changed. Refer to application note *PGA900 as a Capacitive Load Driver*, SLDA020, for more information.

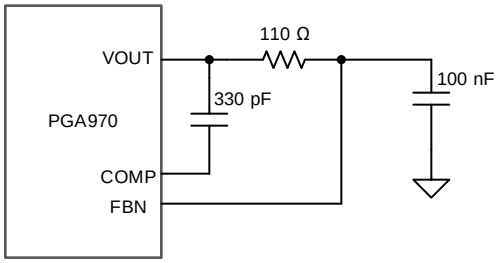

Figure 3. PGA970 in Voltage Mode Configuration

NOTE: Footprints have been provided to put the device into a 3-wire Current Mode Output. Due to the high typical current draw of the PGA970, a two-wire current loop is not possible. Please contact TI through the E2E forums for more details on how to utilize this circuit.

4 OWI

The OWI circuitry in the PGA970EVM allows communicating with the PGA970 by using voltage level translation and current sensing circuitry. The OWI circuitry is mainly based on a summing amplifier using the OPA454.The summing amplifier principle compensates for voltage drops from any potential resistance or diode drops on the VDD supply path so that the OWI logic levels (with respect to PWR_GND) remain always the same regardless of current consumption by the PGA970. The OWI circuitry, shown in Figure 4, consists of four main blocks:

1. OWI write: UART data and activation pulses level translated to OWI voltage logic levels.
2. Offset voltage: Constant offset voltage selected by the user to compensate for constant drops from components such as reverse-protection diodes.
3. Current compensating voltage: This circuit will compensate for voltage drops that occur due to the current drop across any resistive elements in the path to VDD, such as current limiting resistors for ESD protection networks, drain-source resistance of Gate-Drive FETs, etc.
4. OWI read: Current to voltage and voltage level translation to UART voltage logic levels.

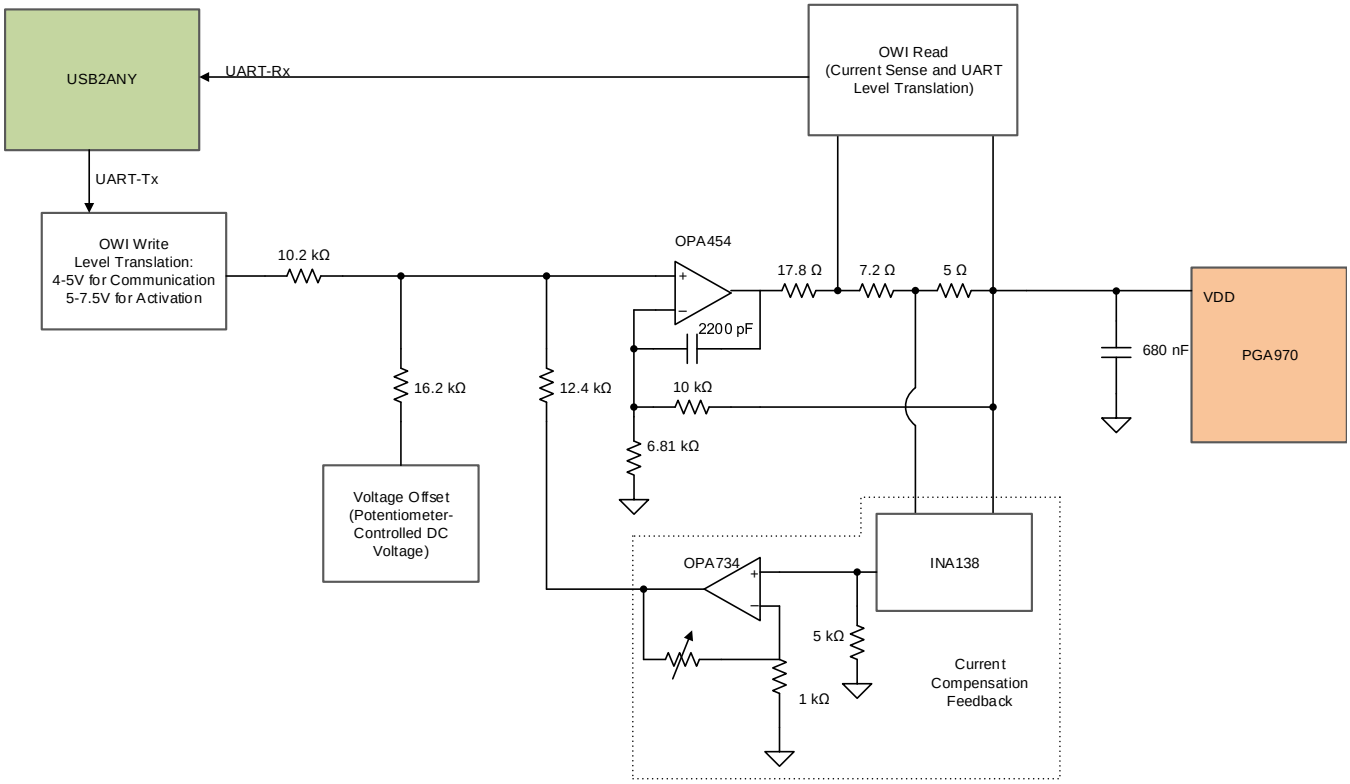

Figure 4. OWI Block Diagram

4.1 Activation Pulse

The activation pulse generated by the PGA970EVM generates the OWI interrupt needed to activate the OWI (with the proper firmware developed by the user). Figure 5 shows the activation pulse from the PGA970EVM. To use this activation pulse, select the “Through Pulse” option from the “OWI Activation Mode” menu and then click “OWI”. The duration of the activation pulse varies due to software delays, but the minimum requirement of 1 or 10 ms is always met.

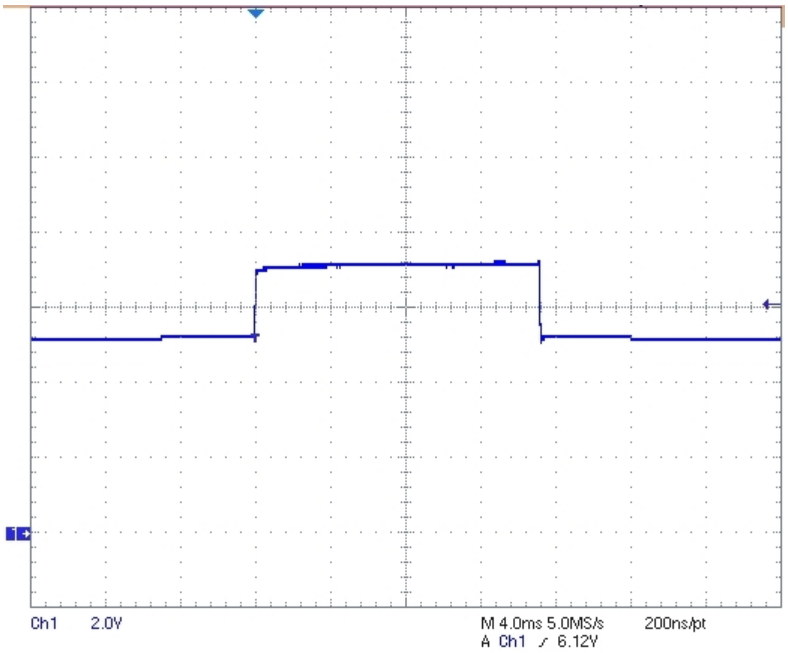

Figure 5. OWI Activation Pulse Generated by the PGA970EVM in Voltage Mode

4.2 Data Sent Through OWI

Data through OWI can be sent to the PGA970 at rates between 320 to 9600 bps. Figure 6 shows data sent at 320 bps.

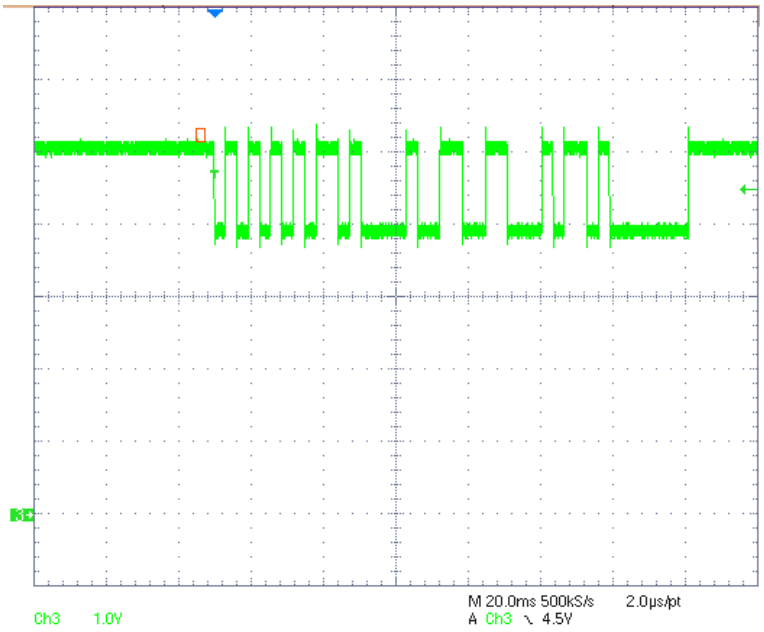

Figure 6. OWI Data at 320 bps; Oscilloscope Probe is Connected at TP21 in the PGA970EVM

5 XDS200 and USB2ANY Connectors

The XDS200 is used for the single-wire debugging (SWD) feature of the PGA970. The designer must use a small breakout board (part of the XDS200 kit) to connect to J13 in the PGA970EVM. No external connections are needed. Figure 7 shows the proper connection for the XDS200 emulator.

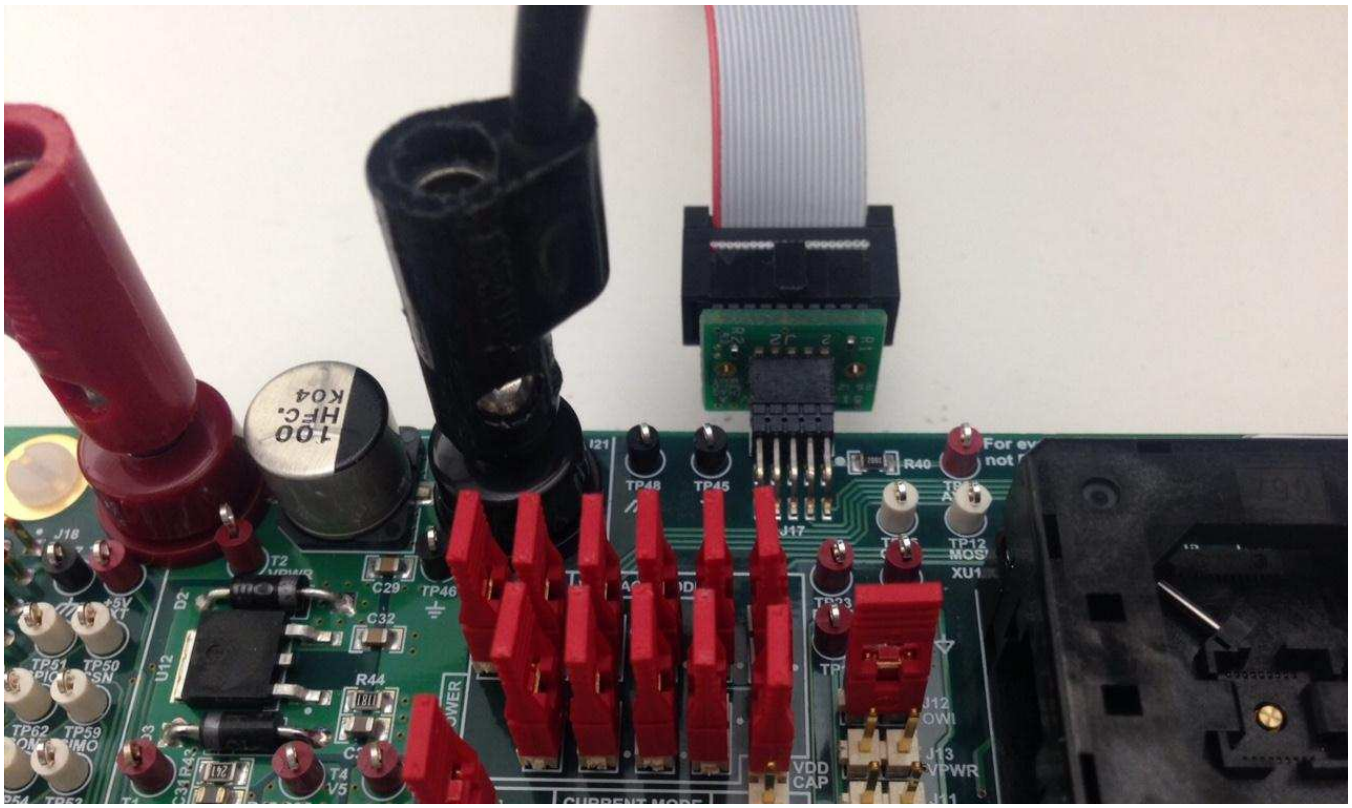

Figure 7. XDS200 Emulator Connection to the PGA970EVM

The USB2ANY is used for the different communication protocols offered by the PGA970. The USB2ANY connects to J18 in the PGA970EVM as shown in Figure 8. The USB2ANY hardware is based on the TI MSP430F5529, 16-bit microcontroller with integrated USB 2.0. The PCB is a two-layer, single-sided board with minimal component count. There are two versions of the USB2ANY, shown in Figure 9, one enclosed and one open. The functionality is exactly the same for both.

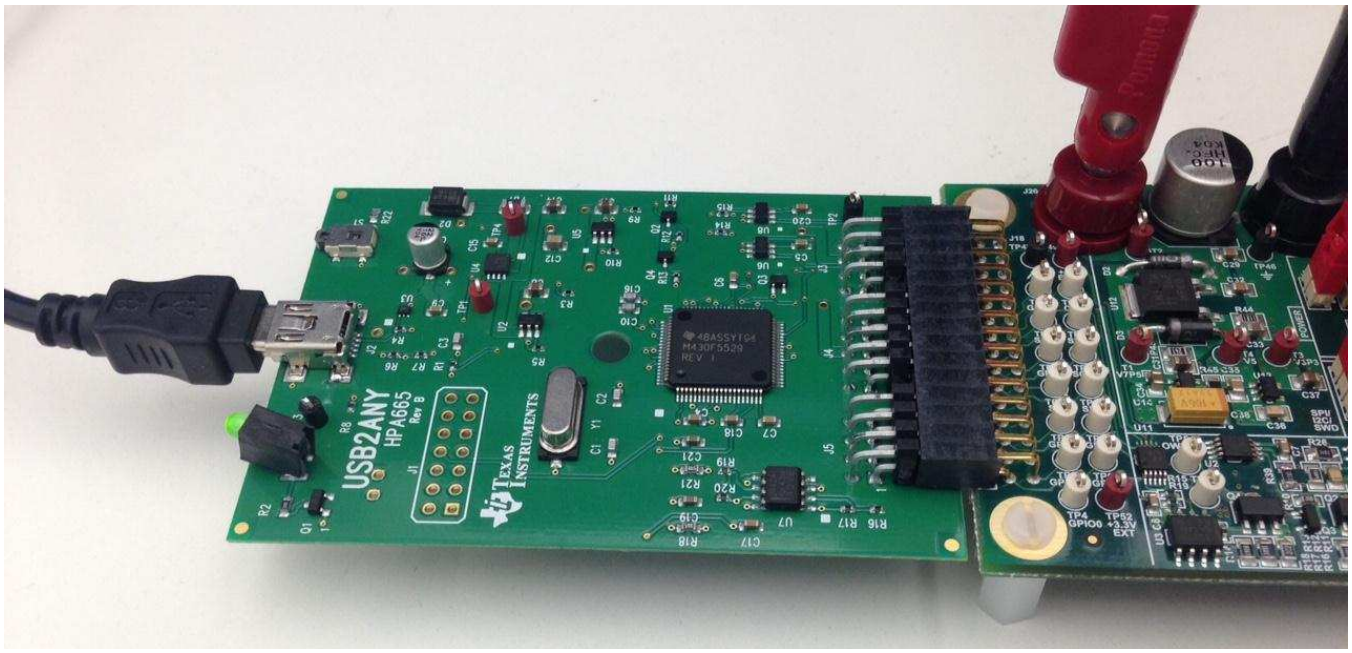

Figure 8. USB2ANY Connection to the PGA970EVM

Figure 9. USB2ANY

Figure 10 shows the pinout of the USB2ANY. The ribbon cable can only be connected one way to the USB2ANY due to a latch present in the cable. A USB cable is included to connect the device to the PC. No external supply is needed.

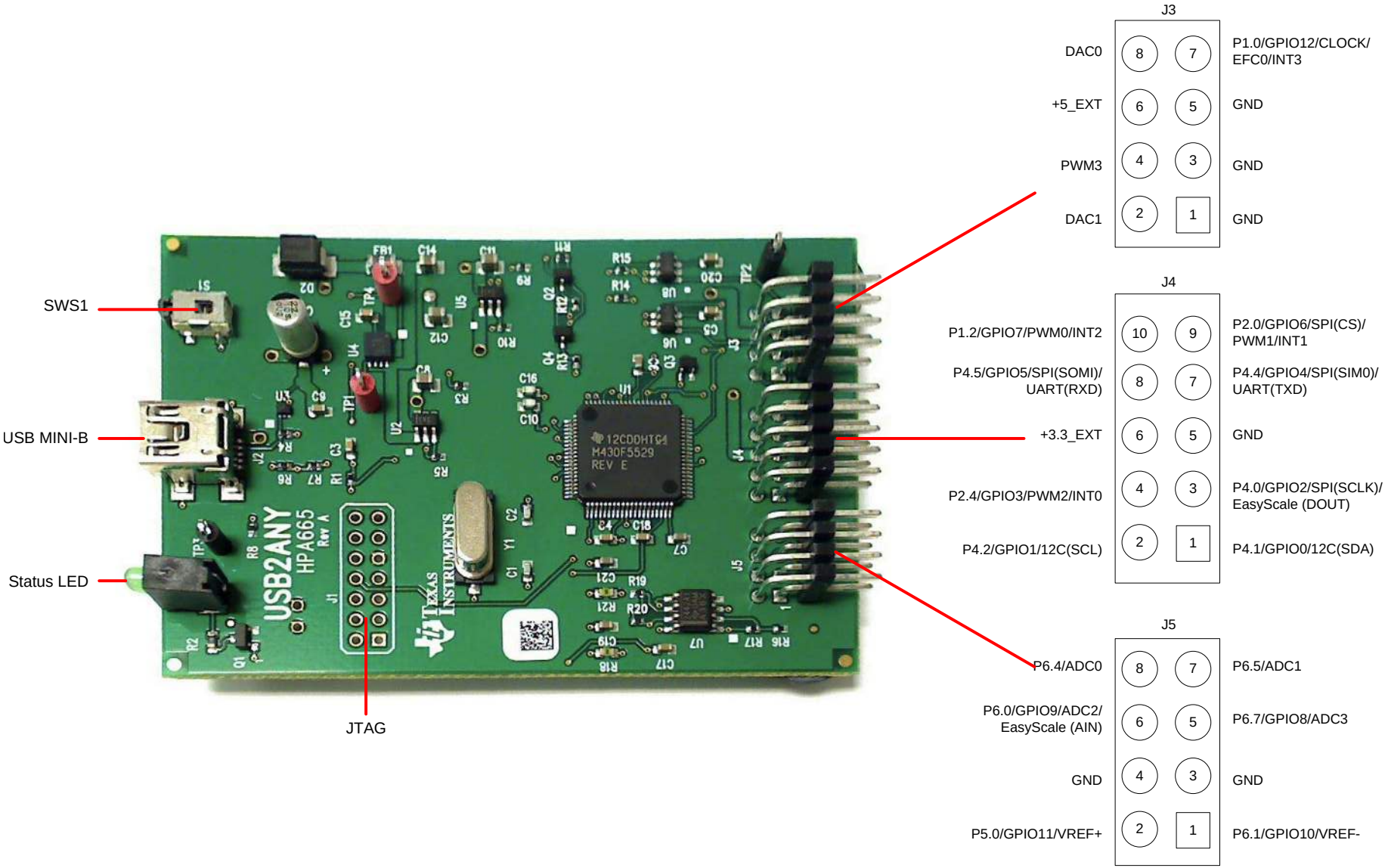

Figure 10. USB2ANY Pinout

6 Schematics

Figure 11 through Figure 16 show the PGA970EVM schematics.

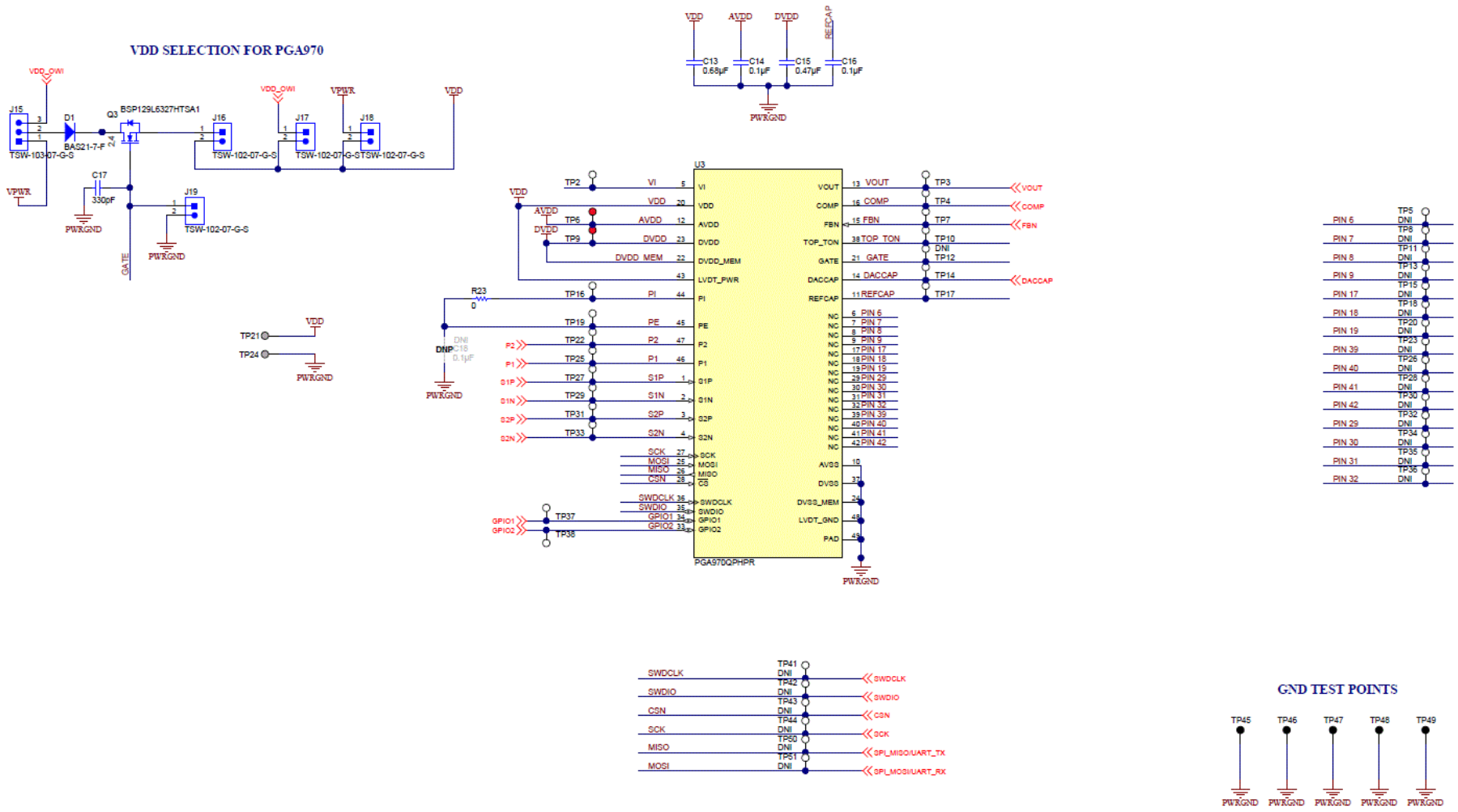

Figure 11. PGA970EVM Main Schematic

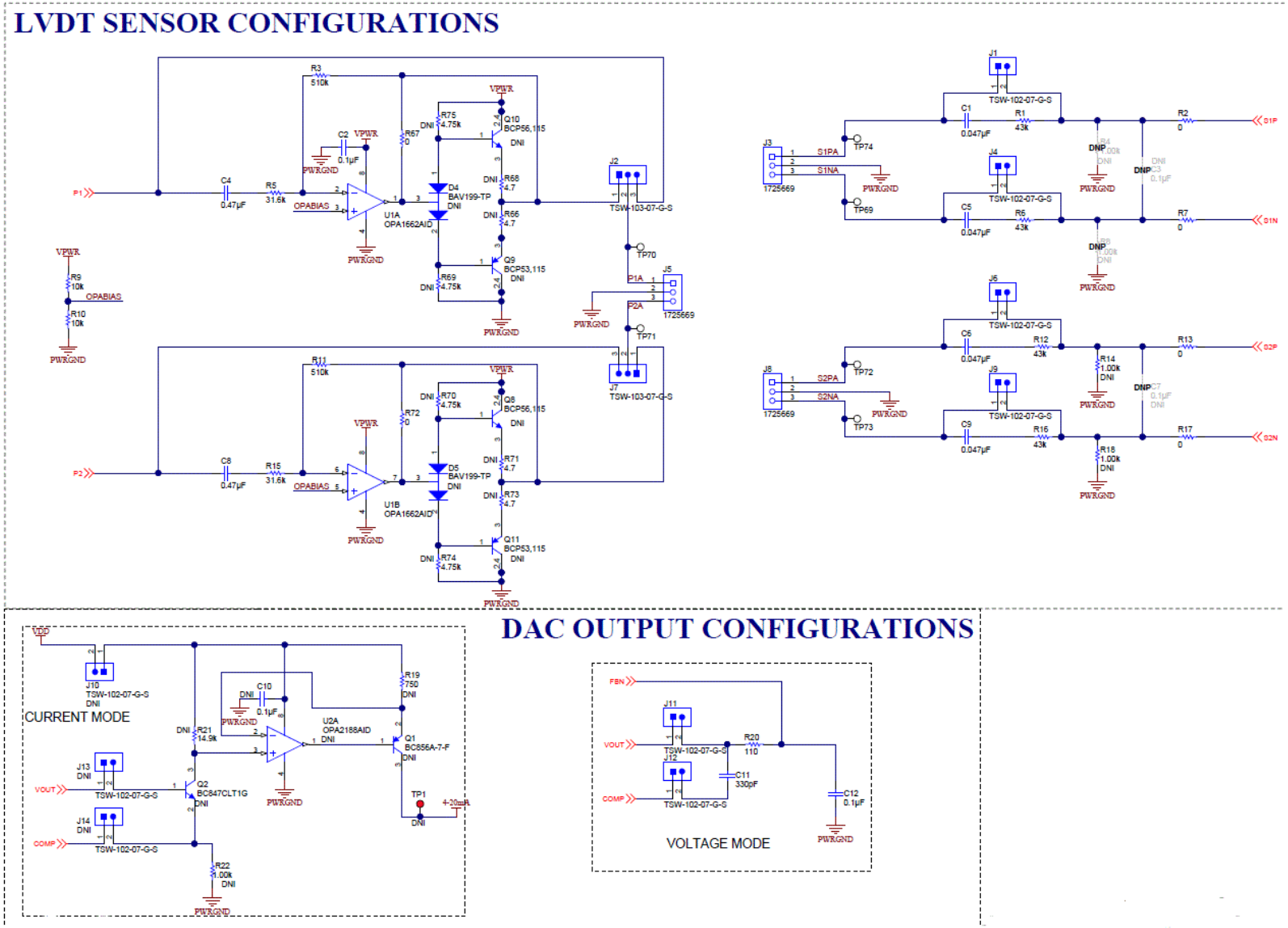

Figure 12. Input and Output Schematic

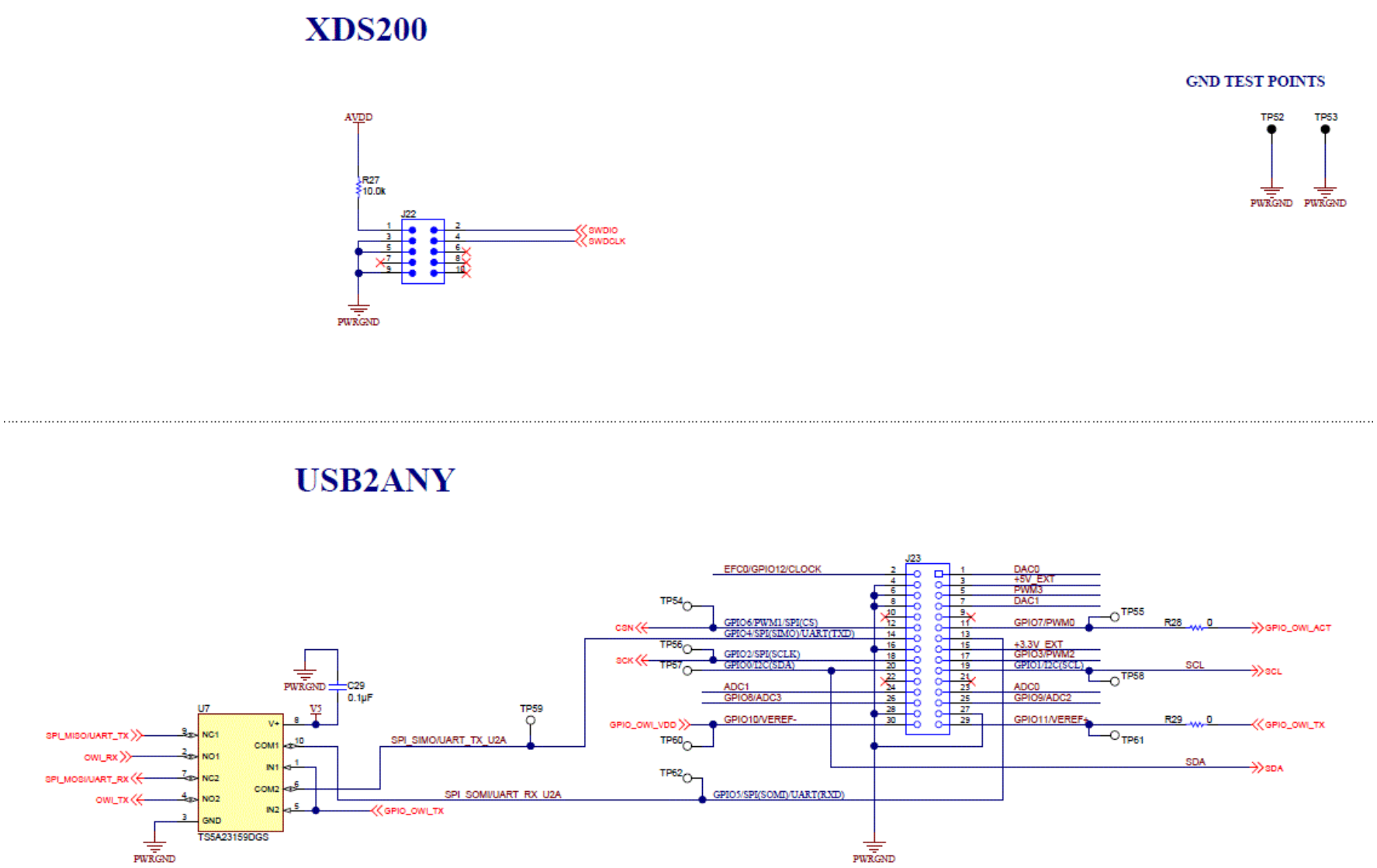

Figure 13. USB2ANY Schematic

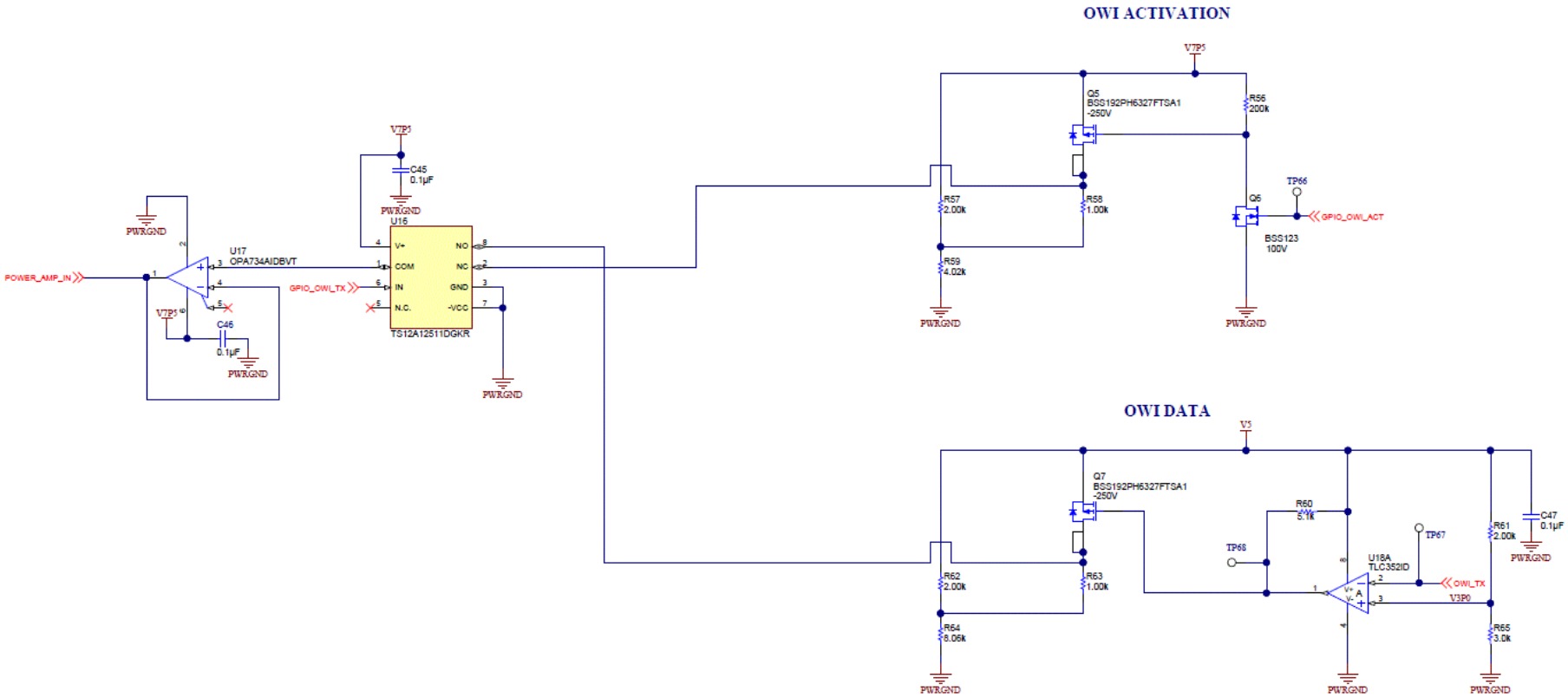

Figure 14. OWI Activation Pulse and Data Schematic

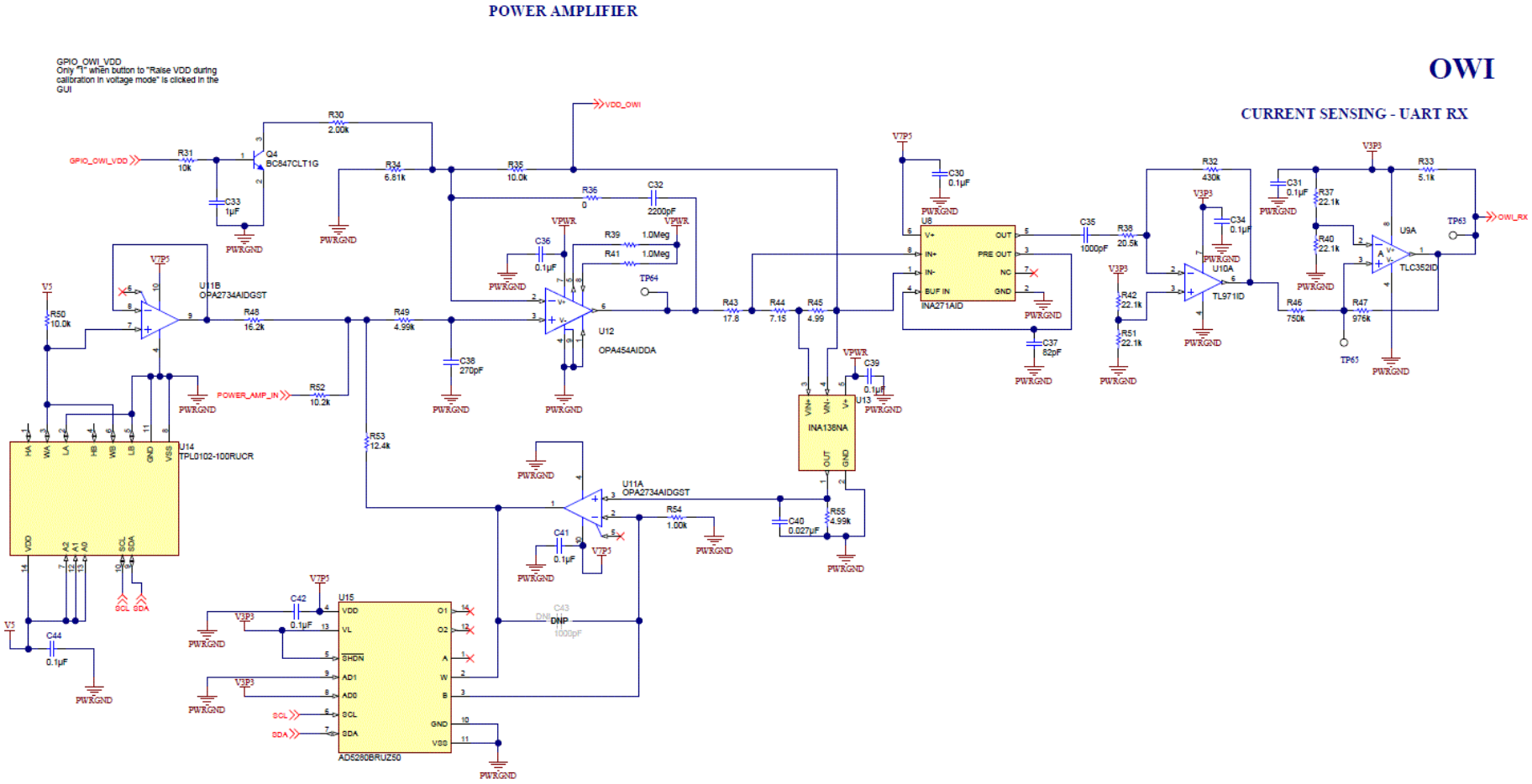

Figure 15. OWI Power Amplifier Schematic

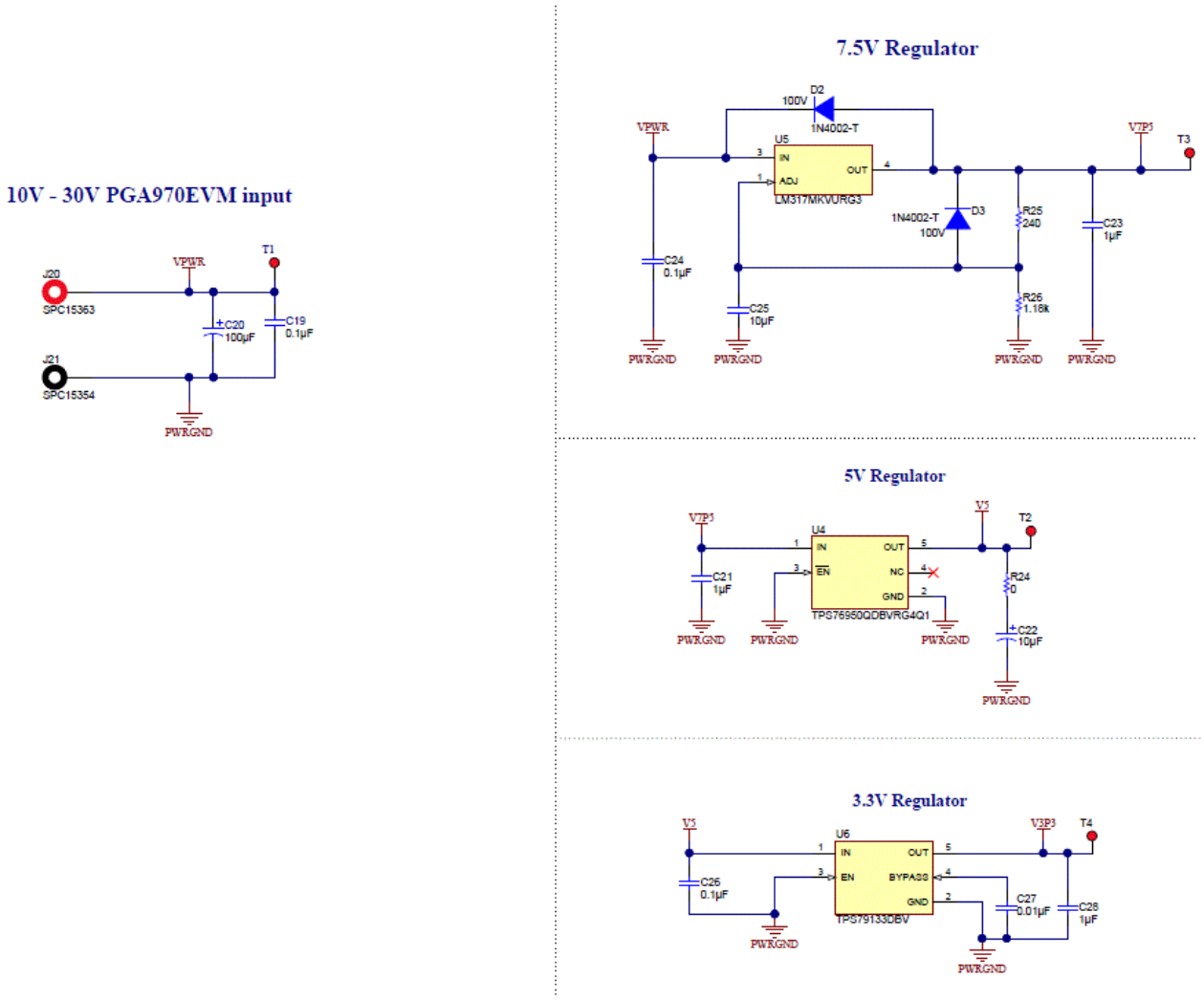

Figure 16. Power Supplies Schematic

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