Vishay Siliconix

Automotive P-Channel 30 V (D-S) 175 °C MOSFET



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Marking Code: QFXXXX

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PRODUCT SUMMARY				
V _{DS} (V)	-30			
$R_{DS(on)}(\Omega)$ at $V_{GS} = -10 V$	0.020			
$R_{DS(on)}(\Omega)$ at V_{GS} = -4.5 V	0.033			
I _D (A)	-10			
Configuration	Single			
Package	PowerPAK SC-70			

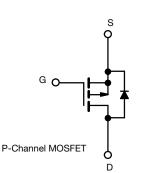
FEATURES

- TrenchFET[®] power MOSFET
- AEC-Q101 qualified ^d
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



COMPLIANT HALOGEN

FREE



ABSOLUTE MAXIMUM RATIN	GS (T _C = 25 °C, unles	s otherwise noted	(k		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage	V _{DS}	-30	V		
Gate-source voltage		V _{GS} ± 20			
Continuous drain current	T _C = 25 °C	1	-10		
	T _C = 125 °C	I _D	-10		
Continuous source current (diode conduction) ^a		IS	10	A	
Pulsed drain current ^b		I _{DM}	-40		
Single pulse avalanche current	L = 0.1 mH	I _{AS}	15		
Single pulse avalanche energy	L = 0.1 IIIn	E _{AS}	11.25	mJ	
Maximum power dissipation ^b	T _C = 25 °C	D	13.6	w	
	T _C = 125 °C	P _D	4.5		
Operating junction and storage temperatu	re range	T _J , T _{stg}	-55 to +175	°C	

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	LIMIT	UNIT		
Junction-to-ambient	PCB mount ^c	R _{thJA}	90	°C/W		
Junction-to-case (drain)		R _{thJF}	11	0/10		

Notes

- a. Package limited
- b. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- c. When mounted on 1" square PCB (FR4 material)

d. Parametric verification ongoing



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static	•	•					1	
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0, I _D = -250 μA		-30	-	-	V	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	$V_{DS} = V_{GS}, I_D = -250 \ \mu A$		-2	-2.5		
Gate-source leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$		-	-	± 100	nA	
		$V_{GS} = 0 V$	V _{DS} = -30 V	-	-	-1		
Zero gate voltage drain current	I _{DSS}	$V_{GS} = 0 V$	V_{DS} = -30 V, T_{J} = 125 °C	-	-	-50	μA	
		$V_{GS} = 0 V$	$V_{DS} = -30 \text{ V}, \text{ T}_{J} = 175 ^{\circ}\text{C}$	-	-	-150		
On-state drain current ^a	I _{D(on)}	$V_{GS} = -10 V$	$V_{DS} \ge 5 V$	-8	-	-	Α	
Drain-source on-state resistance ^a		V _{GS} = -10 V	I _D = -5 A	-	0.016	0.020		
	Б	V _{GS} = -10 V	I _D = -5 A, T _J = 125 °C	-	-	0.029	Ω	
	R _{DS(on)}	V _{GS} = -10 V	I _D = -5 A, T _J = 175 °C	-	-	0.035		
		$V_{GS} = -4.5 V$	I _D = -4 A	-	0.026	0.033		
Forward transconductance ^b	9 _{fs}	V _{DS} = -10 V, I _D = -7 A		-	17	-	S	
Dynamic ^b								
Input capacitance	C _{iss}		V _{GS} = 0 V V _{DS} = -10 V, f = 1 MHz		1505	1880	pF	
Output capacitance	C _{oss}	$V_{GS} = 0 V$			205	260		
Reverse transfer capacitance	C _{rss}			-	181	227		
Total gate charge ^c	Qg			-	26	33		
Gate-source charge ^c	Q _{gs}	V _{GS} = -10 V	10 V V _{DS} = -15 V, I _D = -8 A		4.2	-	nC	
Gate-drain charge ^c	Q _{gd}			-	4.7	-		
Gate resistance	Rg	f = 1 MHz		4.5	7.6	11.2	Ω	
Turn-on delay time ^c	t _{d(on)}			-	20	30		
Rise time ^c	t _r	V_{DD} = -15 V, R _L = 6 Ω I _D \cong -2.5 A, V _{GEN} = -10 V, R _g = 1 Ω		-	18	27	ns	
Turn-off delay time ^c	t _{d(off)}			-	19	28		
Fall time ^c	t _f			-	8	12		
Source-Drain Diode Ratings and Chai	acteristics	•						
Pulsed current ^a	I _{SM}			-	-	-40	Α	
Forward voltage	V _{SD}	$I_{\rm F} = -5$ A, $V_{\rm GS} = 0$		-	-0.8	-1.2	V	

Notes

a. Pulse test; pulse width $\leq 300~\mu s,\,duty~cycle \leq 2~\%$

b. Guaranteed by design, not subject to production testing

c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

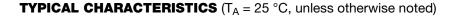
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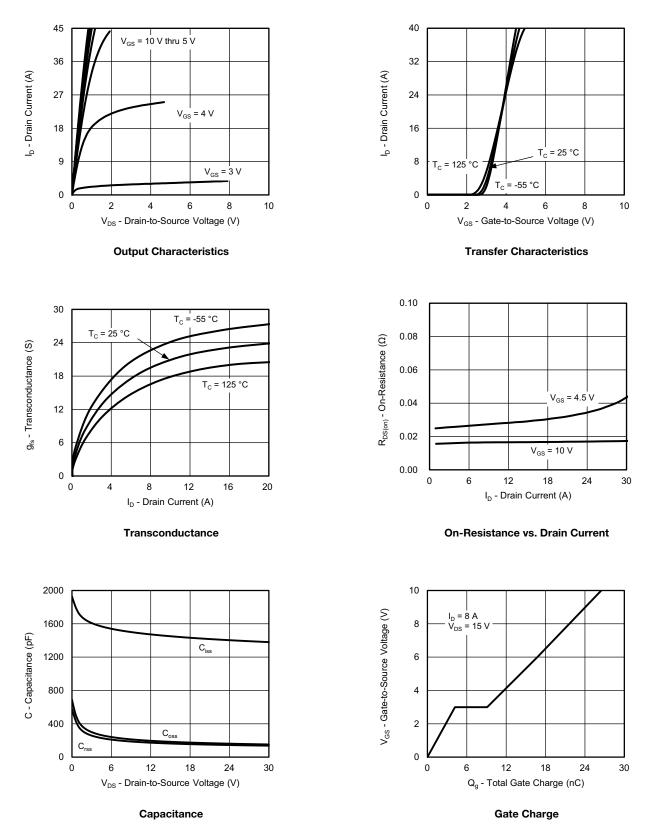
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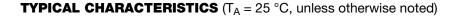
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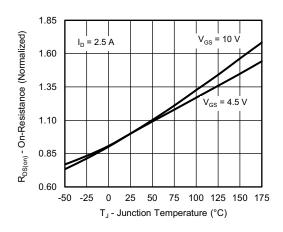
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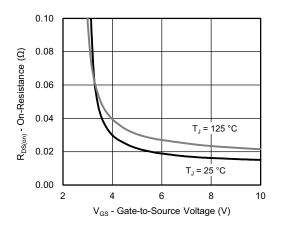
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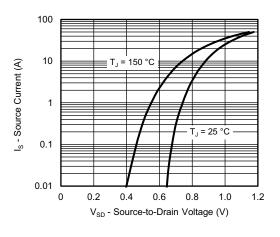




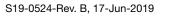
On-Resistance vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage



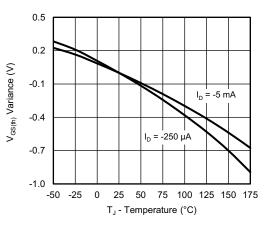
Source-Drain Diode Forward Voltage



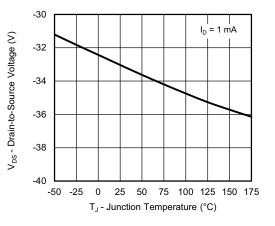
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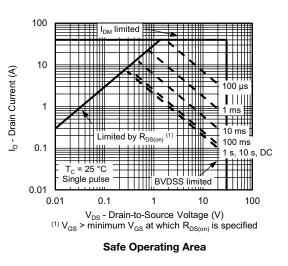
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Threshold Voltage



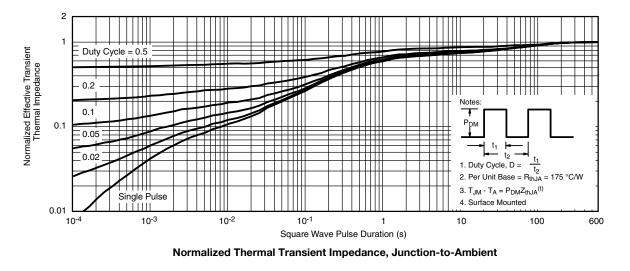
Drain Source Breakdown vs. Junction Temperature

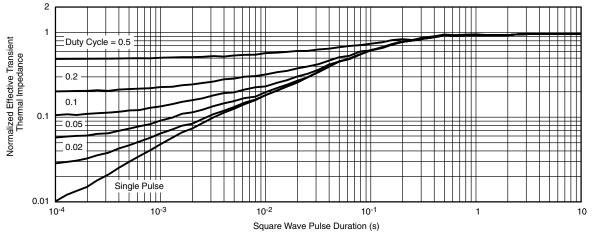




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THERMAL RATINGS ($T_A = 25 \text{ °C}$, unless otherwise noted)





Normalized Thermal Transient Impedance, Junction-to-Foot

Note

The characteristics shown in the two graphs

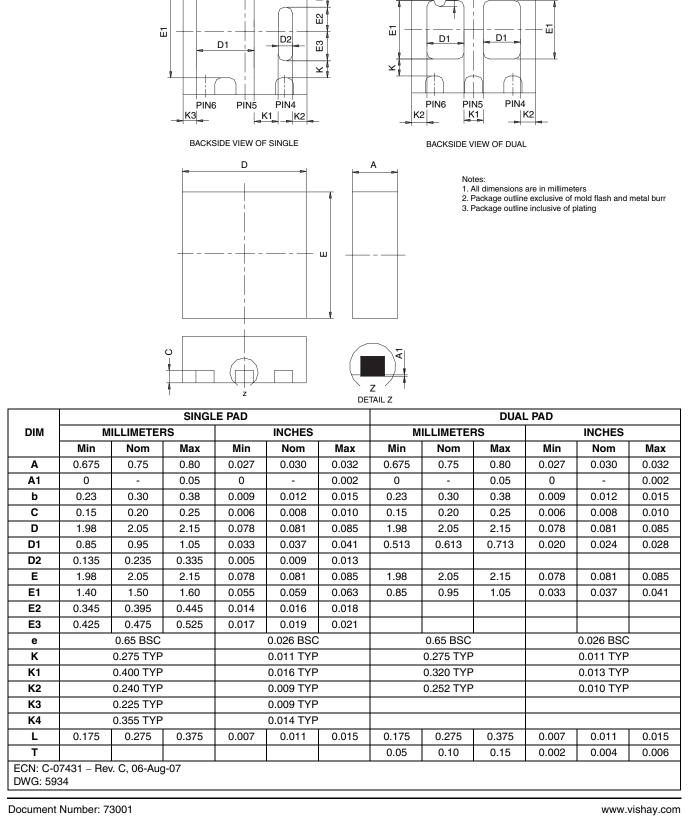
- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

- Normalized Transient Thermal Impedance Junction-to-Foot (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?76242.

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PowerPAK[®] SC70-6L

b PIN2 PIN1 PIN3 _ ₹

Package Information Vishay Siliconix

__ ₿

b

PIN3

PIN2

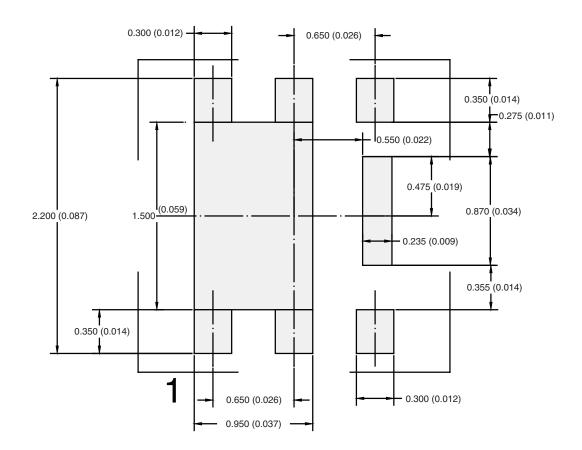
PIN1

¥

VISHA



RECOMMENDED PAD LAYOUT FOR PowerPAK[®] SC70-6L Single



Dimensions in mm/(Inches)

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