# STK11C68-5 (SMD5962-92324)

# 64 Kbit (8 K x 8) SoftStore nvSRAM

## Features

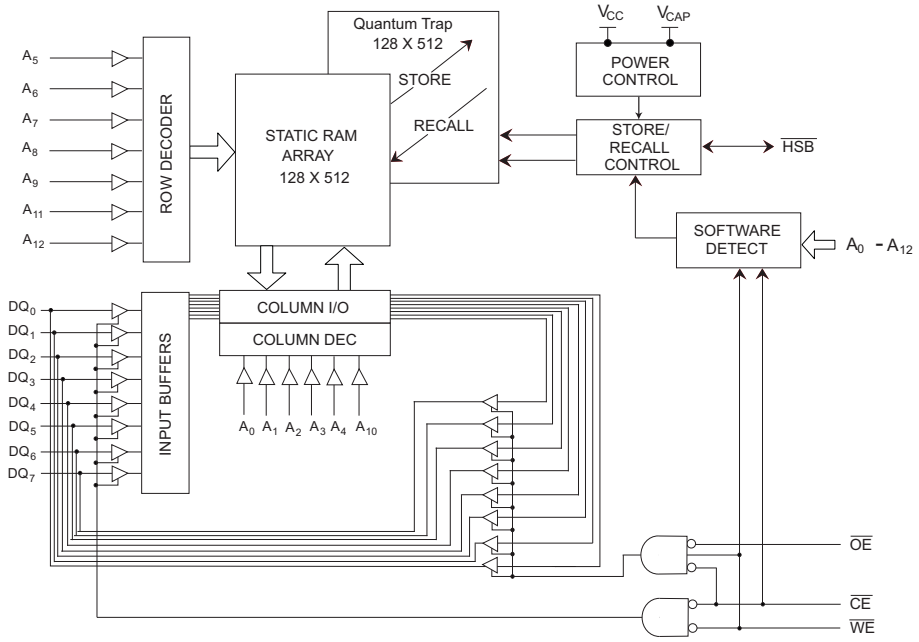
- 35 ns, 45 ns, and 55 ns access times
- Pin compatible with industry standard SRAMs
- Software initiated nonvolatile STORE
- Unlimited Read and Write endurance
- Automatic RECALL to SRAM on power-up
- Unlimited RECALL cycles
- 1,000,000 STORE cycles
- 100 year data retention
- Single 5 V ± 10% operation
- Military temperature
- 28-pin (300 mil) CDIP and 28-pad LCC packages

## Functional Description

The Cypress STK11C68-5 is a 64 Kb fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap technology to produce the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers under software control from SRAM to the nonvolatile elements (the STORE operation). On power-up, data is automatically restored to the SRAM (the RECALL operation) from the nonvolatile memory. RECALL operations are also available under software control.

For a complete list of related documentation, click here.

## Logic Block Diagram



## Contents

## Pinouts

**Figure 1. Pin Diagram - 28-Pin CDIP**

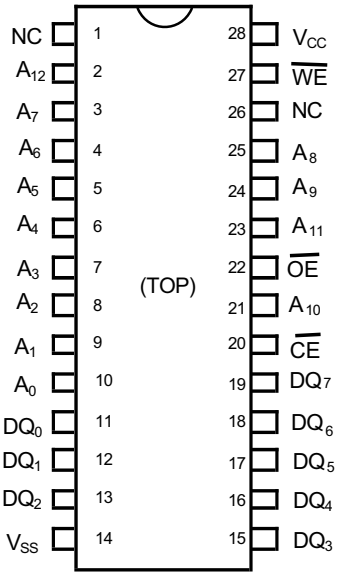
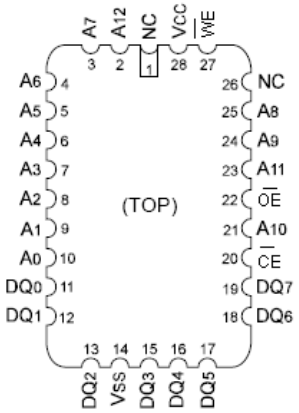



**Figure 2. Pin Diagram - 28-Pin LCC**




## Pin Definitions

| Pin Name | Alt | I/O Type | Description |
|---|---|---|---|
| $A_0$–$A_{12}$ | | Input | **Address Inputs**. Used to select one of the 8,192 bytes of the nvSRAM. |
| $DQ_0$-$DQ_7$ | | Input/Output | **Bidirectional Data I/O Lines**. Used as input or output lines depending on operation. |
| $\overline{WE}$ | $\overline{W}$ | Input | **Write Enable Input, Active LOW**. When the chip is enabled and $\overline{WE}$ is LOW, data on the I/O pins is written to the specific address location. |
| $\overline{CE}$ | $\overline{E}$ | Input | **Chip Enable Input, Active LOW**. When LOW, selects the chip. When HIGH, deselects the chip. |
| $\overline{OE}$ | $\overline{G}$ | Input | **Output Enable, Active LOW**. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the I/O pins to tristate. |
| $V_{SS}$ | | Ground | **Ground for the Device**. The device is connected to ground of the system. |
| $V_{CC}$ | | Power Supply | **Power Supply Inputs to the Device**. |

## Device Operation

The STK11C68-5 (SMD5962-92324) is a versatile memory chip that provides several modes of operation. The STK11C68-5 (SMD5962-92324) can operate as a standard 8K x 8 SRAM. It has an 8K x 8 Nonvolatile Elements shadow to which the SRAM information can be copied or from which the SRAM can be updated in nonvolatile mode.

## SRAM Read

The STK11C68-5 (SMD5962-92324) performs a Read cycle whenever $\overline{CE}$ and $\overline{OE}$ are LOW while $\overline{WE}$ is HIGH. The address specified on pins $A_{0-12}$ determines the 8,192 data bytes accessed. When the Read is initiated by an address transition, the outputs are valid after a delay of $t_{AA}$ (Read cycle 1). If the Read is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at $t_{ACE}$ or at $t_{DOE}$, whichever is later (Read cycle 2). The data outputs repeatedly respond to address changes within the $t_{AA}$ access time without the need for transitions on any control input pins. They remain valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ is brought LOW.

## SRAM Write

A Write cycle is performed whenever $\overline{CE}$ and $\overline{WE}$ are LOW. The address inputs must be stable before entering the Write cycle and must remain stable until either $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common I/O pins $DQ_{0-7}$ are written into the memory if it has valid $t_{SD}$. This is done before the end of a $\overline{WE}$ controlled Write or before the end of an $\overline{CE}$ controlled Write. Keep $\overline{OE}$ HIGH during the entire Write cycle to avoid data bus contention on common I/O lines. If $\overline{OE}$ is left LOW, internal circuitry turns off the output buffers $t_{HZWE}$ after $\overline{WE}$ goes LOW.

## Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. The STK11C68-5 (SMD5962-92324) software STORE cycle is initiated by executing sequential $\overline{CE}$ controlled Read cycles from six specific address locations in exact order. During the STORE cycle, an erase of the previous nonvolatile data is first performed followed by a program of the nonvolatile elements. When a STORE cycle is initiated, input and output are disabled until the cycle is completed.

Because a sequence of Reads from specific addresses is used for STORE initiation, it is important that no other Read or Write accesses intervene in the sequence. If they intervene, the sequence is aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following Read sequence is performed:

1. Read address 0x0000, Valid READ
2. Read address 0x1555, Valid READ
3. Read address 0x0AAA, Valid READ
4. Read address 0x1FFF, Valid READ
5. Read address 0x10F0, Valid READ
6. Read address 0x0F0F, Initiate STORE cycle

The software sequence is clocked with $\overline{CE}$ controlled Reads. When the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. It is important that Read cycles and not Write cycles are used in the sequence. It is not necessary that $\overline{OE}$ is LOW for a valid sequence. After the $t_{STORE}$ cycle time is fulfilled, the SRAM is again activated for Read and Write operation.

## Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of Read operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of $\overline{CE}$ controlled Read operations is performed:

1. Read address 0x0000, Valid READ
2. Read address 0x1555, Valid READ
3. Read address 0x0AAA, Valid READ
4. Read address 0x1FFF, Valid READ
5. Read address 0x10F0, Valid READ
6. Read address 0x0F0E, Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared; then, the nonvolatile information is transferred into the SRAM cells. After the $t_{RECALL}$ cycle time, the SRAM is again ready for Read and Write operations. The RECALL operation does not alter the data in the nonvolatile elements. The nonvolatile data can be recalled for an unlimited number of times.

## Hardware RECALL (Power Up)

During power up or after any low-power condition ($V_{CC}$ < $V_{RESET}$), an internal RECALL request is latched. When $V_{CC}$ once again exceeds the sense voltage of $V_{SWITCH}$, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete.

If the STK11C68-5 (SMD5962-92324) is in a Write state at the end of power-up RECALL, the SRAM data is corrupted. To help avoid this situation, a 10 kΩ resistor is connected either between $\overline{WE}$ and system $V_{CC}$ or between $\overline{CE}$ and system $V_{CC}$.

## Hardware Protect

The STK11C68-5 (SMD5962-92324) offers hardware protection against inadvertent STORE operation and SRAM Writes during low voltage conditions. When $V_{CAP}$ < $V_{SWITCH}$, all externally initiated STORE operations and SRAM Writes are inhibited.

## Noise Considerations

The STK11C68-5 (SMD5962-92324) is a high-speed memory. It must have a high frequency bypass capacitor of approximately 0.1 µF connected between $V_{CC}$ and $V_{SS}$, using leads and traces that are as short as possible. As with all high-speed CMOS ICs, careful routing of power, ground, and signals reduce circuit noise.

## Low Average Active Power

CMOS technology provides the STK11C68-5 (SMD5962-92324) the benefit of drawing significantly less current when it is cycled at times longer than 50 ns. Figure 3 and Figure 4 shows the relationship between $I_{CC}$ and Read or Write cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, $V_{CC}$ = 5.5 V, 100% duty cycle on chip enable). Only standby current is drawn when the chip is disabled. The overall average current drawn by the STK11C68-5 (SMD5962-92324) depends on the following items:

- Duty cycle of chip enable
- Overall cycle rate for accesses
- Ratio of Reads to Writes
- CMOS versus TTL input levels
- Operating temperature
- $V_{CC}$ level
- I/O loading

**Figure 3. Current Versus Cycle Time (Read)**

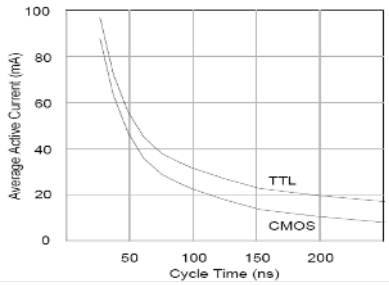
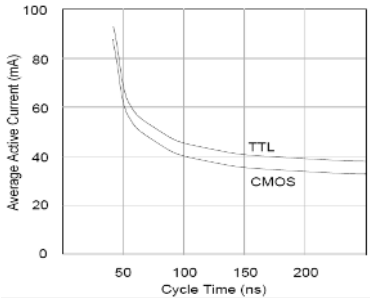



**Figure 4. Current Versus Cycle Time (Write)**




## Best Practices

Cypress nvSRAM products have been used effectively for over 15 years. While ease of use is one of the product's main system values, the experience gained from working with hundreds of applications has resulted in the following suggestions as best practices:

- The nonvolatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprograms these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. The end product's firmware must not assume that an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration.
- Cold or warm boot status, and so on must always program a unique NV pattern (for example, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test. This is to ensure these system routines work consistently.

**Table 1. Hardware Mode Selection**

| $\overline{CE}$ | $\overline{WE}$ | A12–A0 | Mode | I/O | Notes |
|---|---|---|---|---|---|
| L | H | 0x0000<br>0x1555<br>0x0AAA<br>0x1FFF<br>0x10F0<br>0x0F0F | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Nonvolatile STORE | Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output High Z | [1] |
| L | H | 0x0000<br>0x1555<br>0x0AAA<br>0x1FFF<br>0x10F0<br>0x0F0E | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Nonvolatile RECALL | Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output High Z | [1] |

**Note**
1. The six consecutive addresses must be in the order listed. $\overline{WE}$ must be high during all six consecutive $\overline{CE}$ controlled cycles to enable a nonvolatile cycle.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Temperature under bias..... –55 °C to +125 °C

Supply Voltage on $V_{CC}$ Relative to GND .....–0.5 V to 7.0 V

Voltage on Input Relative to $V_{SS}$ .....–0.6 V to $V_{CC}$ + 0.5 V

Voltage on $DQ_{0-7}$ .....–0.5 V to $V_{CC}$ + 0.5 V

Power Dissipation ..... 1.0 W

DC Output Current (1 output at a time, 1s duration).... 15 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Military | -55 °C to +125 °C | 4.5 V to 5.5 V |

## DC Electrical Characteristics

Over the operating range ($V_{CC}$ = 4.5 V to 5.5 V)

| Parameter | Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{CC1}$ | Average $V_{CC}$ current | $t_{RC}$ = 35 ns<br>$t_{RC}$ = 45 ns<br>$t_{RC}$ = 55 ns<br>Dependent on output loading and cycle rate. Values obtained without output loads. $I_{OUT}$ = 0 mA | – | 75<br>65<br>55 | mA<br>mA<br>mA |
| $I_{CC2}$ | Average $V_{CC}$ current during STORE | All Inputs Do Not Care, $V_{CC}$ = Max<br>Average current for duration $t_{STORE}$ | – | 3 | mA |
| $I_{CC3}$ | Average $V_{CC}$ current at $t_{RC}$= 200 ns, 5 V, 25 °C Typical | $\overline{WE} \geq (V_{CC} – 0.2\ V)$. All other inputs cycling.<br>Dependent on output loading and cycle rate. Values obtained without output loads. | – | 10 | mA |
| $I_{SB1}$[2] | $V_{CC}$ standby current (Standby, Cycling TTL Input Levels) | $t_{RC}$ = 35 ns, $\overline{CE} \geq V_{IH}$<br>$t_{RC}$ = 45 ns, $\overline{CE} \geq V_{IH}$<br>$t_{RC}$ = 55 ns, $\overline{CE} \geq V_{IH}$ | – | 24<br>21<br>20 | mA<br>mA<br>mA |
| $I_{SB2}$ [2] | $V_{CC}$ standby current | $\overline{CE} \geq (V_{CC} – 0.2\ V)$. All others $V_{IN} \leq 0.2$ V or $\geq (V_{CC} – 0.2\ V)$. Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz | – | 1500 | µA |
| $I_{IX}$ | Input leakage current | $V_{CC}$ = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$ | –1 | +1 | µA |
| $I_{OZ}$ | Off state output Leakage current | $V_{CC}$ = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$, $\overline{CE}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$ | –5 | +5 | µA |
| $V_{IH}$ | Input HIGH voltage | | 2.2 | $V_{CC}$ + 0.5 | V |
| $V_{IL}$ | Input LOW voltage | | $V_{SS}$ – 0.5 | 0.8 | V |
| $V_{OH}$ | Output HIGH voltage | $I_{OUT}$ = –4 mA | 2.4 | – | V |
| $V_{OL}$ | Output LOW voltage | $I_{OUT}$ = 8 mA | – | 0.4 | V |

## Data Retention and Endurance

| Parameter | Description | Min | Unit |
|---|---|---|---|
| $DATA_R$ | Data retention | 100 | Years |
| $NV_C$ | Nonvolatile STORE operations | 1,000 | K |

## Capacitance

In this table, the capacitance parameters are listed.[3]

| Parameter | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{CC}$ = 0 to 3.0 V | 8 | pF |
| $C_{OUT}$ | Output capacitance | | 7 | pF |

**Note**

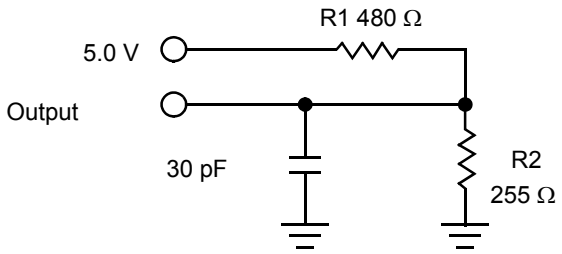
2. $\overline{CE} \geq V_{IH}$ does not produce standby current levels until any nonvolatile cycle in progress has timed out.
3. These parameters are guaranteed by design and are not tested.

## Thermal Resistance

In this table, the thermal resistance parameters are listed.[4]

| Parameter | Description | Test Conditions | 28-CDIP | 28-LCC | Unit |
|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51. | TBD | TBD | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | TBD | TBD | °C/W |

**Figure 5. AC Test Loads**




## AC Test Conditions

Input Pulse Levels ..... 0 V to 3 V
Input Rise and Fall Times (10% to 90%) ..... ≤5 ns
Input and Output Timing Reference Levels ..... 1.5 V

**Note**
4. These parameters are guaranteed by design and are not tested.

## AC Switching Characteristics

### SRAM Read Cycle

| Parameter | | Description | 35 ns | | 45 ns | | 55 ns | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Cypress Parameter | Alt | | Min | Max | Min | Max | Min | Max | |
| $t_{ACE}$ | $t_{ELQV}$ | Chip enable access time | – | 35 | – | 45 | – | 55 | ns |
| $t_{RC}$ [5] | $t_{AVAV}$, $t_{ELEH}$ | Read cycle time | 35 | – | 45 | – | 55 | – | ns |
| $t_{AA}$ [6] | $t_{AVQV}$ | Address access time | – | 35 | – | 45 | – | 55 | ns |
| $t_{DOE}$ | $t_{GLQV}$ | Output enable to data valid | – | 15 | – | 20 | – | 35 | ns |
| $t_{OHA}$ [6] | $t_{AXQX}$ | Output hold after address change | 5 | – | 5 | – | 5 | – | ns |
| $t_{LZCE}$ [7] | $t_{ELQX}$ | Chip enable to output active | 5 | – | 5 | – | 5 | – | ns |
| $t_{HZCE}$ [7] | $t_{EHQZ}$ | Chip disable to output inactive | – | 13 | – | 15 | – | 25 | ns |
| $t_{LZOE}$ [7] | $t_{GLQX}$ | Output enable to output active | 0 | – | 0 | – | 0 | – | ns |
| $t_{HZOE}$ [7] | $t_{GHQZ}$ | Output disable to output inactive | – | 13 | – | 15 | – | 25 | ns |
| $t_{PU}$ [8] | $t_{ELICCH}$ | Chip enable to power active | 0 | – | 0 | – | 0 | – | ns |
| $t_{PD}$ [8] | $t_{EHICCL}$ | Chip disable to power standby | – | 35 | – | 45 | – | 55 | ns |

## Switching Waveforms

**Figure 6. SRAM Read Cycle 1: Address Controlled** [5, 6]

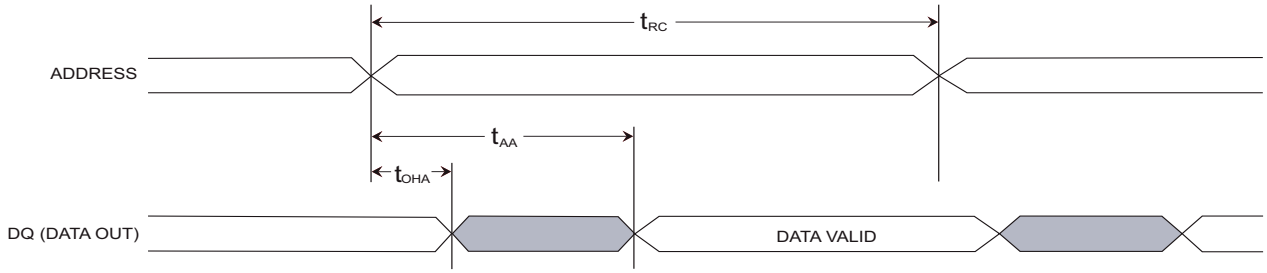
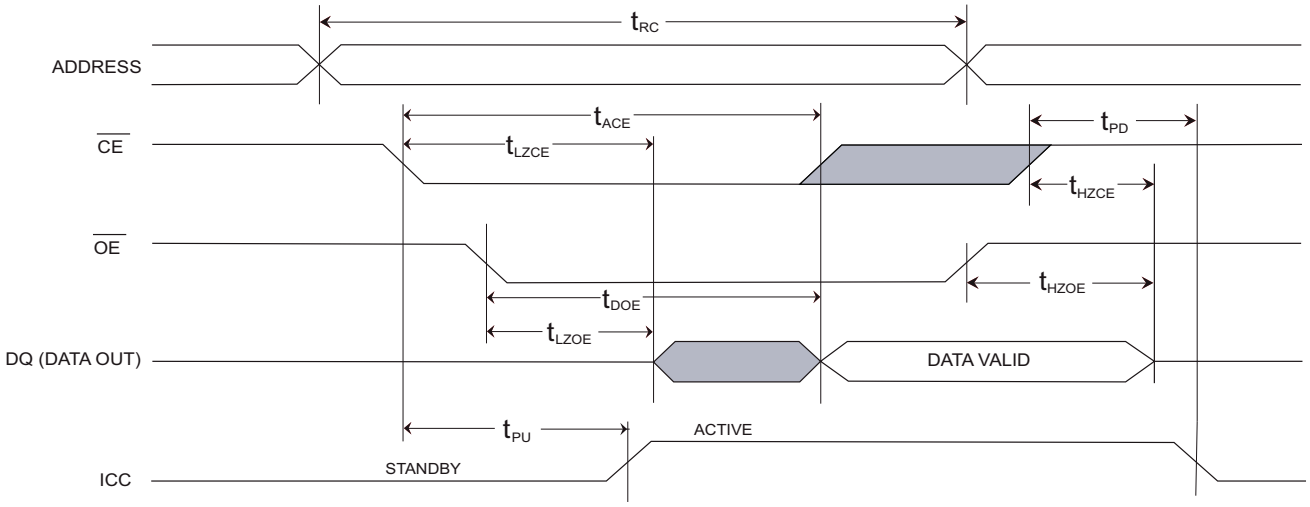



**Figure 7. SRAM Read Cycle 2: $\overline{CE}$ and $\overline{OE}$ Controlled** [5]




**Notes**
5. $\overline{WE}$ must be High during SRAM Read cycles.
6. I/O state assumes $\overline{CE}$ and $\overline{OE} \leq V_{IL}$ and $\overline{WE} \geq V_{IH}$; device is continuously selected.
7. Measured ± 200 mV from steady state output voltage.
8. These parameters are guaranteed by design and are not tested.

### SRAM Write Cycle

| Parameter | | Description | 35 ns | | 45 ns | | 55 ns | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Cypress Parameter | Alt | | Min | Max | Min | Max | Min | Max | |
| $t_{WC}$ | $t_{AVAV}$ | Write cycle time | 35 | – | 45 | – | 55 | – | ns |
| $t_{PWE}$ | $t_{WLWH}$, $t_{WLEH}$ | Write pulse width | 25 | – | 30 | – | 45 | – | ns |
| $t_{SCE}$ | $t_{ELWH}$, $t_{ELEH}$ | Chip enable to end of write | 25 | – | 30 | – | 45 | – | ns |
| $t_{SD}$ | $t_{DVWH}$, $t_{DVEH}$ | Data setup to end of write | 12 | – | 15 | – | 30 | – | ns |
| $t_{HD}$ | $t_{WHDX}$, $t_{EHDX}$ | Data hold after end of write | 0 | – | 0 | – | 0 | – | ns |
| $t_{AW}$ | $t_{AVWH}$, $t_{AVEH}$ | Address setup to end of write | 25 | – | 30 | – | 45 | – | ns |
| $t_{SA}$ | $t_{AVWL}$, $t_{AVEL}$ | Address setup to start of write | 0 | – | 0 | – | 0 | – | ns |
| $t_{HA}$ | $t_{WHAX}$, $t_{EHAX}$ | Address hold after end of write | 0 | – | 0 | – | 0 | – | ns |
| $t_{HZWE}$ [9,10] | $t_{WLQZ}$ | Write enable to output disable | – | 13 | – | 15 | – | 35 | ns |
| $t_{LZWE}$ [9] | $t_{WHQX}$ | Output active after end of write | 5 | – | 5 | – | 5 | – | ns |

## Switching Waveforms

**Figure 8. SRAM Write Cycle 1: $\overline{WE}$ Controlled** [10, 11]

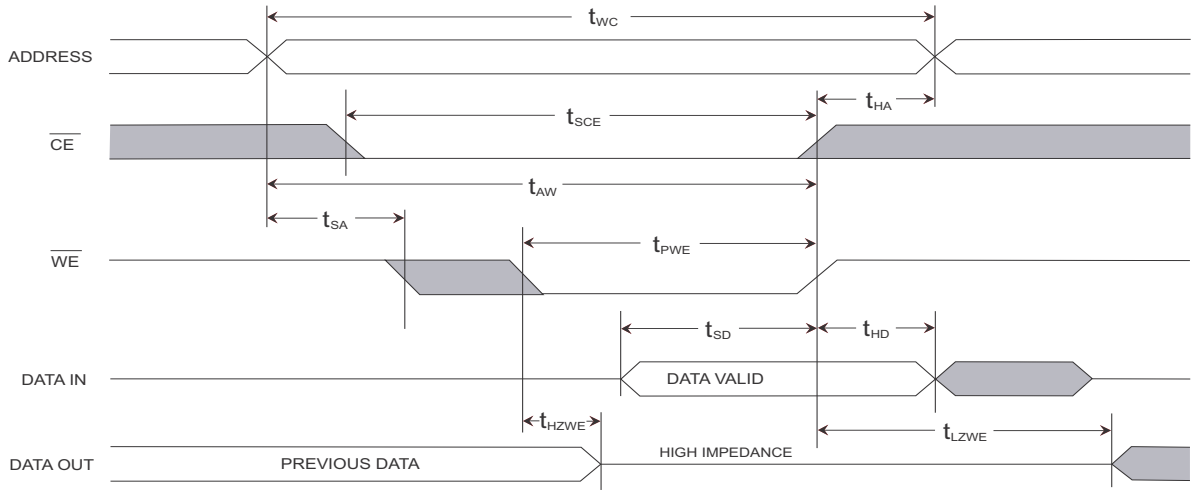
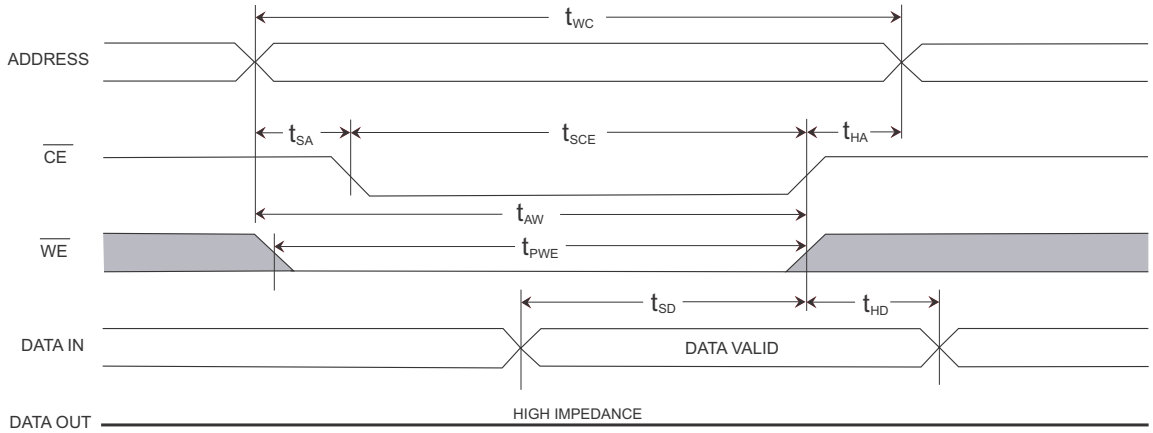



**Figure 9. SRAM Write Cycle 2: $\overline{CE}$ and $\overline{OE}$ Controlled** [10, 11]

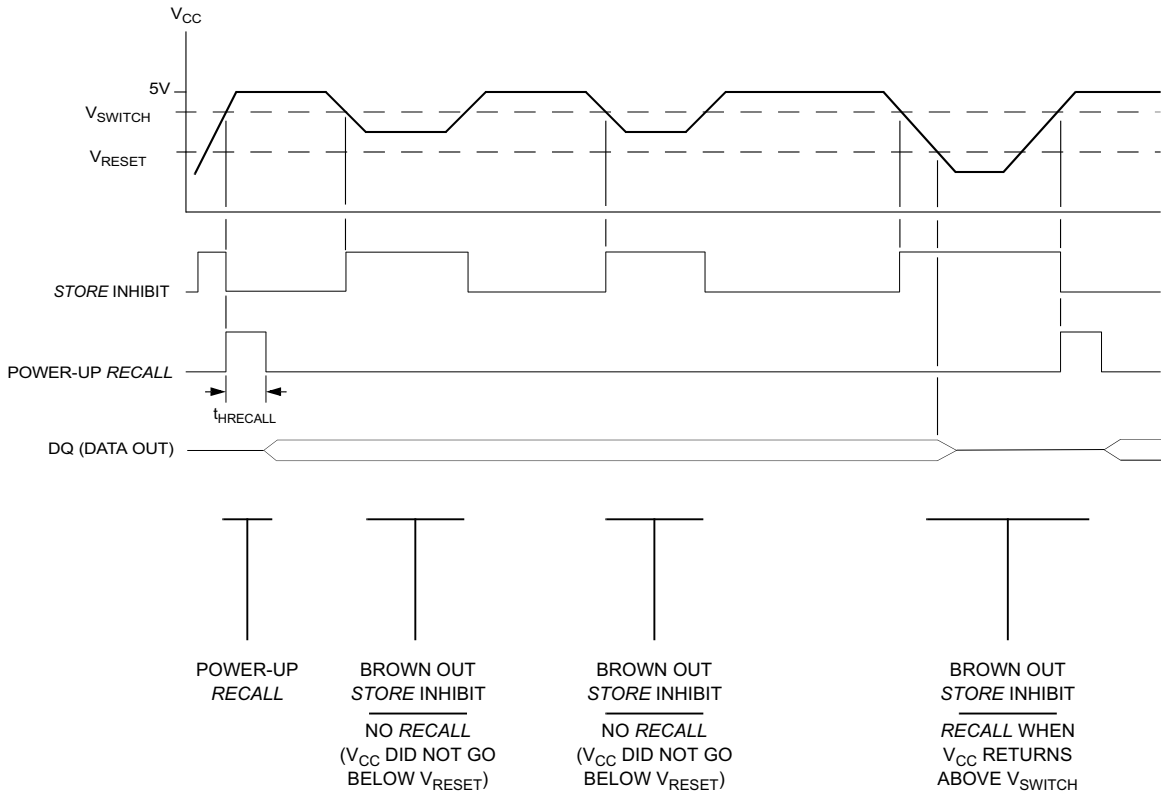



**Notes**
9. Measured ± 200 mV from steady state output voltage.
10. If $\overline{WE}$ is Low when $\overline{CE}$ goes Low, the outputs remain in the high impedance state.
11. $\overline{CE}$ or $\overline{WE}$ must be greater than $V_{IH}$ during address transitions.

## AutoStore INHIBIT or Power Up RECALL

| Parameter | Alt | Description | STK11C68-5 (SMD5962-92324) | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $t_{HRECALL}$ [12] | $t_{RESTORE}$ | Power up RECALL duration | – | 550 | µs |
| $t_{STORE}$ | $t_{HLHZ}$ | STORE cycle duration | – | 10 | ms |
| $V_{SWITCH}$ | | Low voltage trigger level | 4.0 | 4.5 | V |
| $V_{RESET}$ | | Low voltage reset level | – | 3.6 | V |

**Figure 10. AutoStore INHIBIT/Power Up RECALL**




**Notes**

12. $t_{HRECALL}$ starts from the time $V_{CC}$ rises above $V_{SWITCH}$.

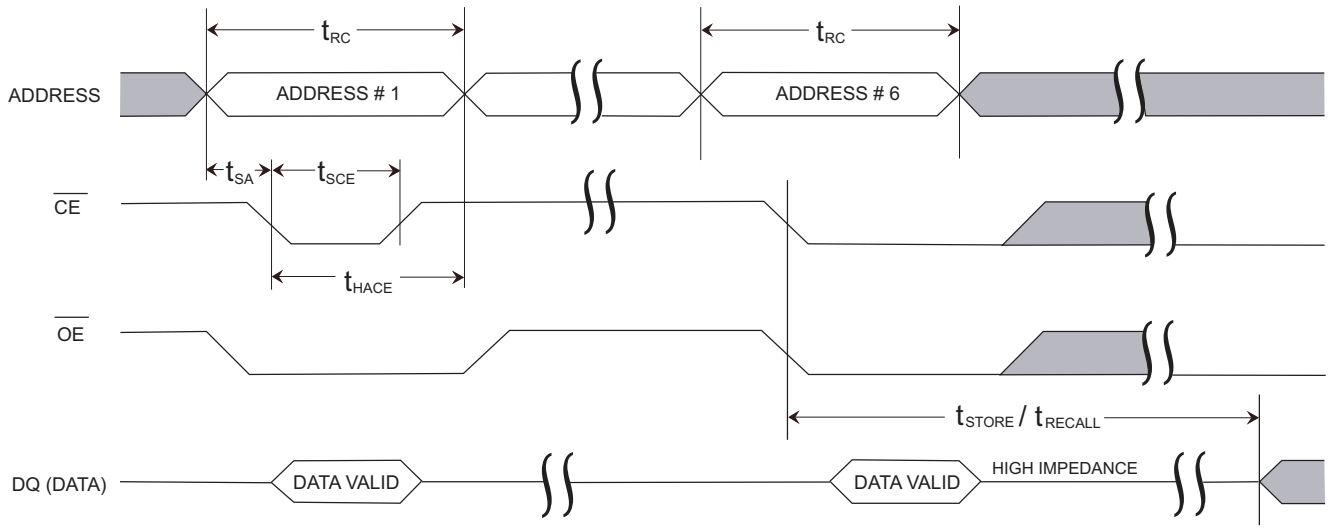
## Software Controlled STORE/RECALL Cycle

The software controlled STORE/RECALL cycle follows. [13, 14]

| Parameter | Alt | Description | 35 ns | | 45 ns | | 55 ns | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{RC}$ | $t_{AVAV}$ | STORE/RECALL initiation cycle time | 35 | – | 45 | – | 55 | – | ns |
| $t_{SA}$[13] | $t_{AVEL}$ | Address setup time | 0 | – | 0 | – | 0 | – | ns |
| $t_{CW}$[13] | $t_{ELEH}$ | Clock pulse width | 25 | – | 30 | – | 35 | – | ns |
| $t_{HACE}$[13] | $t_{ELAX}$ | Address hold time | 20 | – | 20 | – | 20 | – | ns |
| $t_{RECALL}$[13] | | RECALL duration | – | 20 | – | 20 | – | 20 | µs |

## Switching Waveform

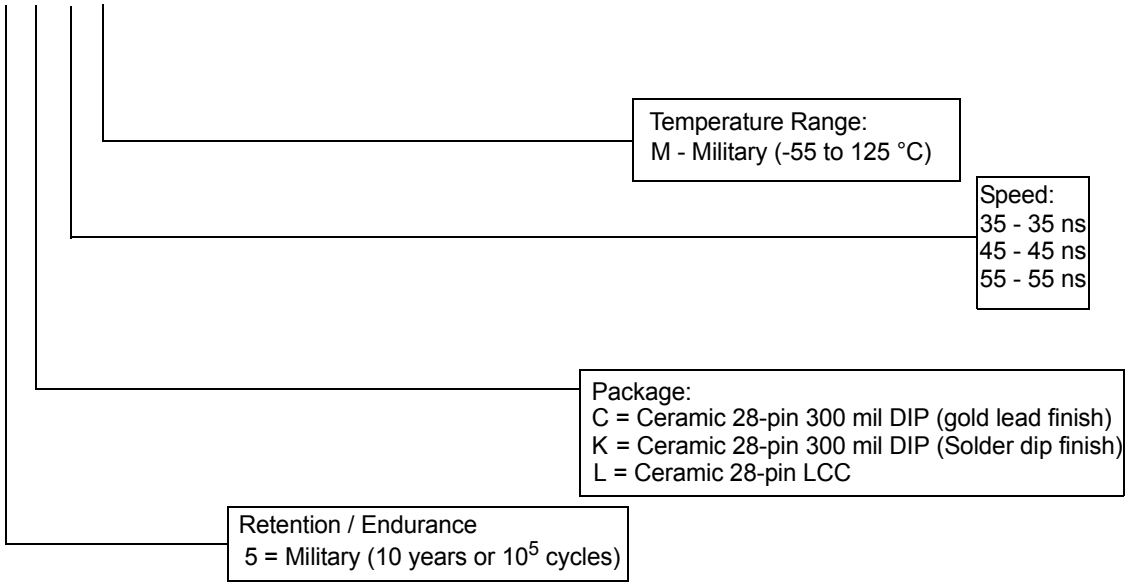
**Figure 11. $\overline{CE}$ Controlled Software STORE/RECALL Cycle [13]**



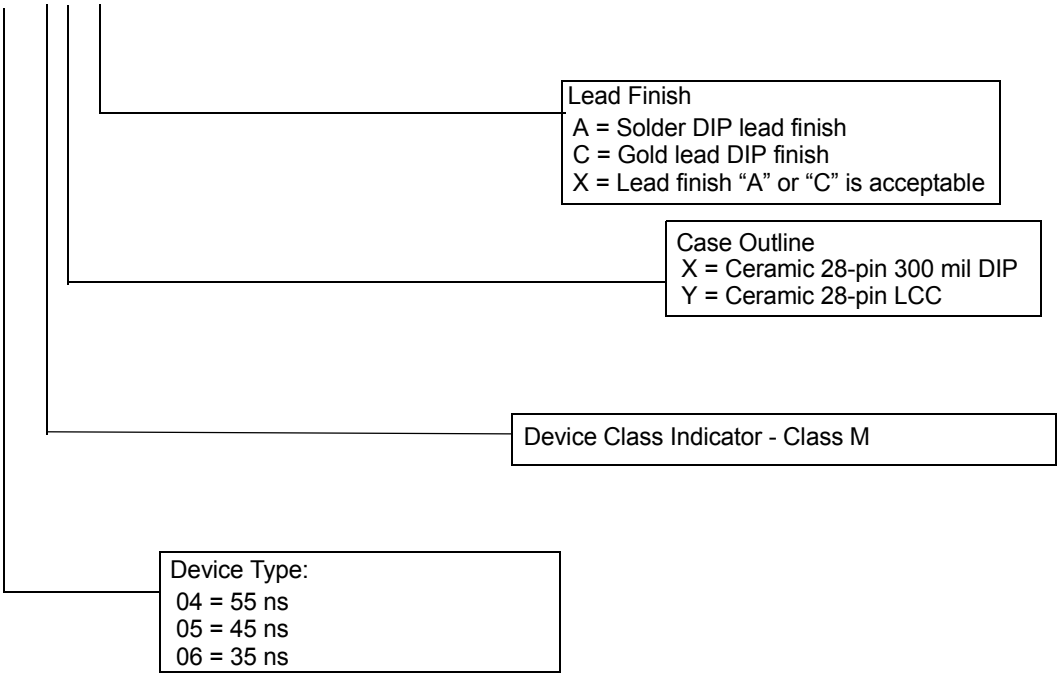

**Notes**
13. The software sequence is clocked on the falling edge of $\overline{CE}$ without involving $\overline{OE}$ (double clocking aborts the sequence).
14. The six consecutive addresses must be read in the order listed in Table 1 on page 5. $\overline{WE}$ must be HIGH during all six consecutive cycles.

## Part Numbering Nomenclature

**STK11C68 - 5 C 45 M**




**SMD5962-92324 04 MX X**



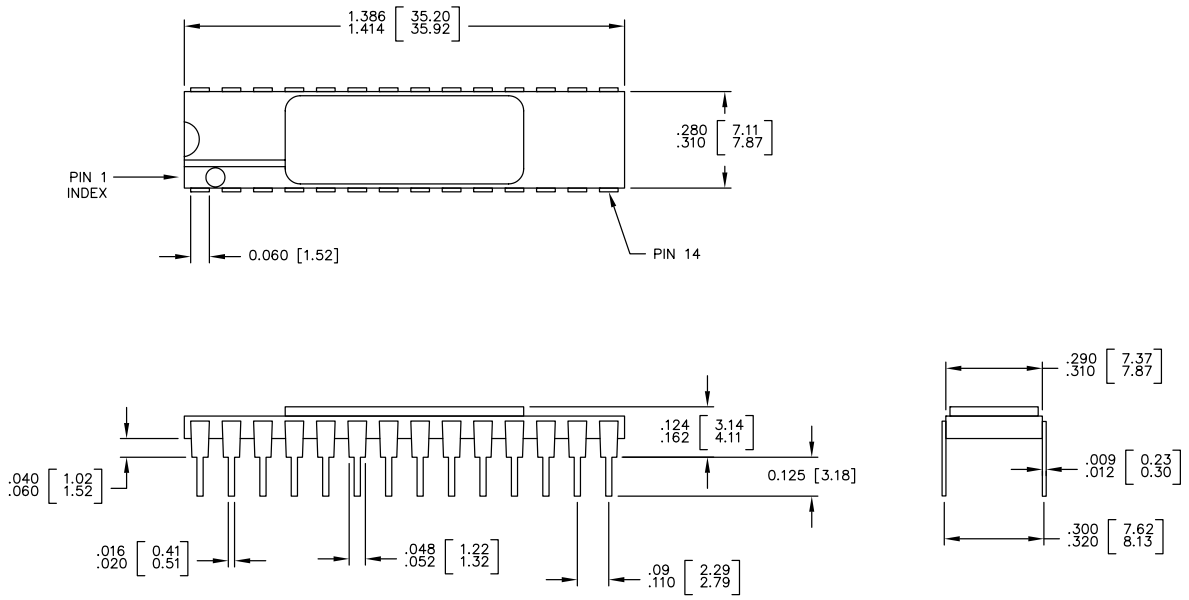
## Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 35 | STK11C68-5L35M | 001-51696 | 28-Pin LCC (350 mil) | Military |
| 55 | STK11C68-5C55M | 001-51695 | 28-Pin CDIP (300 mil) | |

This table contains Final information. Contact your local Cypress sales representative for availability of these parts.

## Package Diagrams

**Figure 12. 28-Pin (300-Mil) Side Braze DIP (001-51695)**

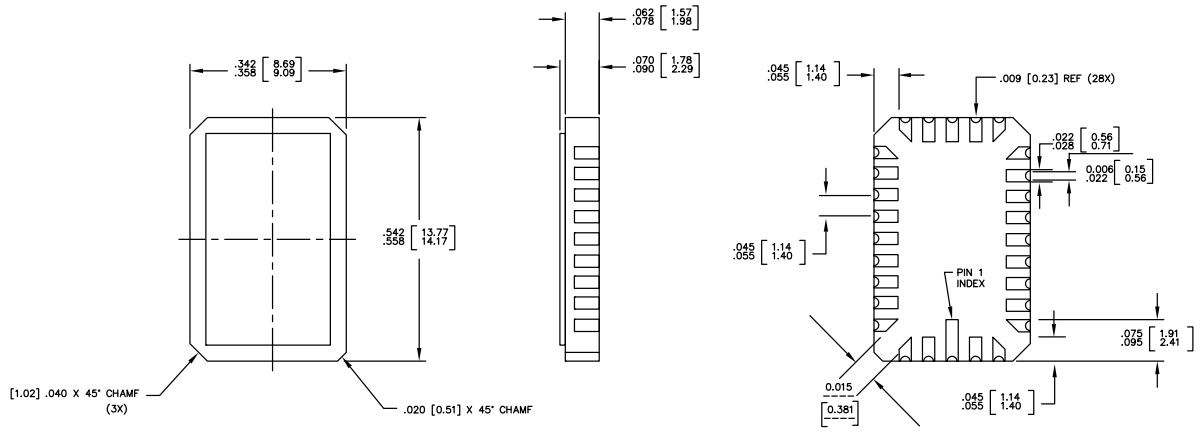



1. ALL DIMENSIONS ARE IN INCHES AND MILLIMETERS [MIN/MAX]
2. PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress Web
3. JEDEC REFERENCE : MO-058

001-51695 *C

## Package Diagrams (continued)

**Figure 13. 28-Pad (350-Mil) LCC (001-51696)**




1. ALL DIMENSION ARE IN INCHES AND MILLIMETERS [MIN/MAX]
2. JEDEC 95 OUTLINE# MO-041
3. PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress Web

001-51696 *C

## Acronyms

| Acronym | Description |
|---|---|
| $\overline{CE}$ | chip enable |
| CMOS | complementary metal oxide semiconductor |
| I/O | input/output |
| I/O | input/output |
| nvSRAM | nonvolatile static random access memory |
| $\overline{OE}$ | output enable |
| SRAM | static random access memory |
| $\overline{TTL}$ | transistor-transistor logic |
| $\overline{WE}$ | write enable |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degrees Celsius |
| kΩ | kilohm |
| μA | microampere |
| mA | milliampere |
| μF | microfarad |
| μs | microsecond |
| ms | millisecond |
| ns | nanosecond |
| pF | picofarad |
| V | volt |
| Ω | ohm |
| W | watt |

## Document History Page

| Document Title: STK11C68-5 (SMD5962-92324) 64 Kbit (8 K x 8) SoftStore nvSRAM<br>Document Number: 001-51001 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 2666844 | GVCH/PYRS | 03/02/2009 | New data sheet |
| *A | 2685053 | GVCH | 04/07/2009 | Added part numbers: STK11C68-5K45M and STK11C68-5K55M |
| *B | 3054310 | GVCH/KEER | 10/1120/10 | Removed inactive parts - STK11C68-5C35M, STK11C68-5K35M, STK11C68-5C45M, STK11C68-5K45M, STK11C68-5L45M from Ordering Code Information table.<br>Updated Package diagrams. |
| *C | 3527665 | GVCH | 02/16/2012 | Added Acronyms, Document Conventions, and Table of Contents.<br>Completing sunset review. |
| *D | 4568935 | GVCH | 11/14/2014 | Added documentation related hyperlink in page 1<br>Removed 02pruned parts - STK11C68-5K55M, STK11C68-5L55M<br>Updated package diagrams from 001-51695*A to 001-51695*B and 001-51696*A to 001-51696*B |
| *E | 4706588 | GVCH | 04/02/2015 | Updated package diagrams from 001-51695*B to 001-51695*C and 001-51696*B to 001-51696*C |

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