



N-Channel 30 V (D-S) MOSFET

| PRODUCT SUMMARY | | | | | |
|---------------------|----------------------------------|------------------------------|-----|--|--|
| V _{DS} (V) | $R_{DS(on)}(\Omega)$ | (on) (Ω) $I_D(A)^a$ | | | |
| 30 | 0.050 at V _{GS} = 10 V | 4.2 | 2.6 | | |
| | 0.079 at V _{GS} = 4.5 V | 3.0 | 2.0 | | |

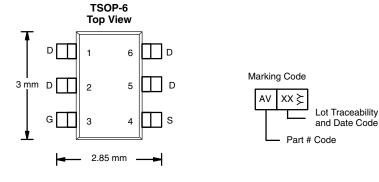
FEATURES

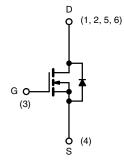
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC



APPLICATIONS

- Load Switch
 - Notebook PC





N-Channel MOSFET

Ordering Information: Si3454CDV-T1-E3 (Lead (Pb)-free)

Si3454CDV-T1-GE3 (Lead (Pb)-free and Halogen-free)

| ABSOLUTE MAXIMUM RATINGS $T_A = 25 ^{\circ}C$, unlet Parameter | | Symbol | Limit | Unit | |
|---|-----------------------------------|-----------------|----------------------|------|--|
| Drain-Source Voltage | V_{DS} | 30 | V | | |
| Gate-Source Voltage | | V_{GS} | ± 20 | | |
| | T _C = 25 °C | | 4.2 | A | |
| Continuous Drain Current (T _{.1} = 150 °C) | T _C = 70 °C | | 3.3 | | |
| Continuous Diain Current (1) = 130 C) | T _A = 25 °C | I _D | 3.8 ^{b, c} | | |
| | T _A = 70 °C | | 3.1 ^{b, c} | | |
| Pulsed Drain Current | | I _{DM} | 20 | | |
| Continuous Source-Drain Diode Current | T _C = 25 °C | I. | 1.25 | | |
| | T _A = 25 °C | I _S | 1.04 ^{b, c} | A | |
| | T _C = 25 °C | | 1.5 | | |
| Maximum Power Dissipation | T _C = 70 °C | D. | 0.9 | W | |
| | T _A = 25 °C | P _D | 1.25 ^{b, c} | | |
| | T _A = 70 °C | | 0.8 ^{b, c} | | |
| Operating Junction and Storage Temperature R | T _J , T _{stg} | - 55 to 150 | °C | | |

| THERMAL RESISTANCE RATINGS | | | | | | |
|---|--------------|-------------------|---------|-----------------|--------------|--|
| Parameter | | Symbol | Typical | Typical Maximum | | |
| Maximum Junction-to-Ambient ^{b, d} | t ≤ 5 s | R _{thJA} | 80 | 100 | °C/W | |
| Maximum Junction-to-Foot (Drain) | Steady State | R_{thJF} | 70 | 85 | G/ VV | |

Notes:

- a. Based on $T_C = 25$ °C.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 5 s
- d. Maximum under Steady State conditions is 145 $^{\circ}\text{C/W}.$

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| Parameter | Symbol | Test Conditions | Min. | Тур. | Max. | Unit | |
|---|-------------------------|--|------|-------|-------|-----------|--|
| Static | | | | | • | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$ | 30 | | | V | |
| V _{DS} Temperature Coefficient | $\Delta V_{DS}/T_{J}$ | I _D = 250 μA | | 27.5 | | m\//°C | |
| V _{GS(th)} Temperature Coefficient | $\Delta V_{GS(th)}/T_J$ | I _D = 250 μA | | - 5.5 | | mV/°C | |
| Gate-Source Threshold Voltage | V _{GS(th)} | $V_{DS} = V_{GS}, I_D = 250 \mu A$ | 1 | | 3 | V | |
| Gate-Source Leakage | I _{GSS} | $V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$ | | | ± 100 | nA | |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = 30 V, V _{GS} = 0 V | | | 1 | | |
| | | $V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 85 ^{\circ}\text{C}$ | | | 10 | μΑ | |
| On-State Drain Current ^a | I _{D(on)} | $V_{DS} = \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$ | 20 | | | Α | |
| Drain-Source On-State Resistance ^a | | $V_{GS} = 10 \text{ V}, I_D = 3.8 \text{ A}$ | | 0.041 | 0.050 | Ω | |
| | R _{DS(on)} | $V_{GS} = 4.5 \text{ V}, I_D = 3.1 \text{ A}$ | | 0.066 | 0.079 | | |
| Forward Transconductance | 9 _{fs} | $V_{DS} = 15 \text{ V}, I_D = 3.8 \text{ A}$ | | 8 | | S | |
| Dynamic ^b | | | | | | | |
| Input Capacitance | C _{iss} | | | 305 | | pF | |
| Output Capacitance | C _{oss} | $V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ | | 52 | | | |
| Reverse Transfer Capacitance | C _{rss} | | | 27 | | | |
| Total Gate Charge | Q _g | $V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 3.8 \text{ A}$ | | 5.3 | 10.6 | 1 | |
| | | | | 2.6 | 5.2 | C | |
| Gate-Source Charge | Q_{gs} | $V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 3.8 \text{ A}$ | | 1.2 | | nC | |
| Gate-Drain Charge | Q _{gd} | | | 0.8 | | | |
| Gate Resistance | R _g | f = 1 MHz | 0.44 | 2.2 | 4.4 | Ω | |
| Turn-On Delay Time | t _{d(on)} | | | 4 | 8 | | |
| Rise Time | t _r | V_{DD} = 15 V, R_L = 4.8 Ω | | 8 | 16 | | |
| Turn-Off DelayTime | t _{d(off)} | $I_D \cong 3.1 \text{ A, V}_{GEN} = 10 \text{ V, R}_g = 1 \Omega$ | | 11 | 18 | | |
| Fall Time | t _f | | | 7 | 14 | | |
| Turn-On Delay Time | t _{d(on)} | | | 15 | 20 | ns | |
| Rise Time | t _r | V_{DD} = 15 V, R_L = 4.8 Ω | | 12 | 18 | | |
| Turn-Off DelayTime | t _{d(off)} | $I_D\cong 3.1$ A, $V_{GEN}=4.5$ V, $R_g=1$ Ω | | 8 | 16 | | |
| Fall Time | t _f | | | 9 | 18 | | |
| Drain-Source Body Diode Characteris | tics | | | | • | | |
| Continous Source-Drain Diode Current | I _S | T _C = 25 °C | | | 1.25 | Λ | |
| Pulse Diode Forward Current ^a | I _{SM} | | | | 20 | A | |
| Body Diode Voltage | V _{SD} | I _S = 3.1 A | | 0.8 | 1.2 | V | |
| Body Diode Reverse Recovery Time | t _{rr} | | | 11.5 | 17.8 | ns | |
| Body Diode Reverse Recovery Charge | Q_{rr} | 1 = 2 1 A dl/d+ = 100 A/va | | 5 | 10 | nC | |
| Reverse Recovery Fall Time | t _a | $I_F = 3.1 \text{ A}, dI/dt = 100 \text{ A/}\mu\text{s}$ | | 7.6 | | ns | |
| Reverse Recovery Rise Time | t _b | | | 3.9 | | | |

Notes:

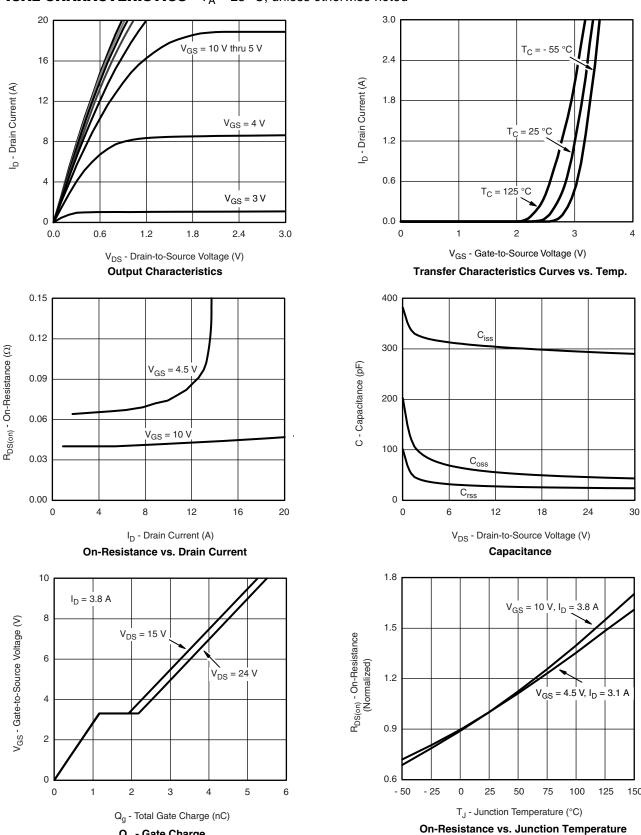
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.



TYPICAL CHARACTERISTICS $T_A = 25$ °C, unless otherwise noted



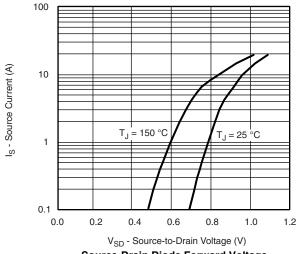
Q_g - Gate Charge

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 $I_D = 3.8 A$

TYPICAL CHARACTERISTICS $T_A = 25$ °C, unless otherwise noted



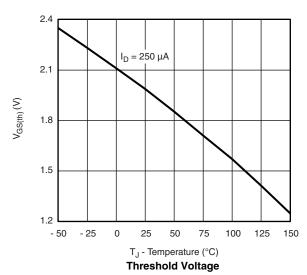
0.08
0.06
T_J = 125 °C
T_J = 25 °C

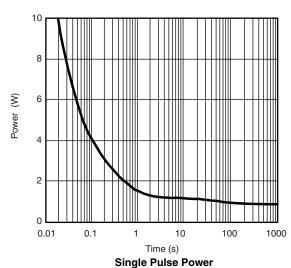
0.00
0 4 8 12 16 20

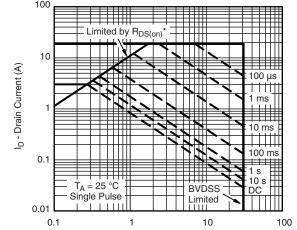
0.10

Source-Drain Diode Forward Voltage

 V_{GS} - Gate-to-Source Voltage (V) **On-Resistance vs. Gate-to-Source Voltage**







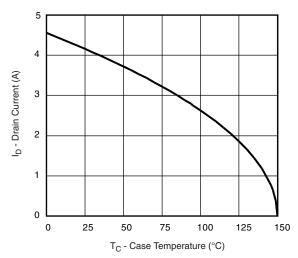
V_{DS} - Drain-to-Source Voltage (V)

* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

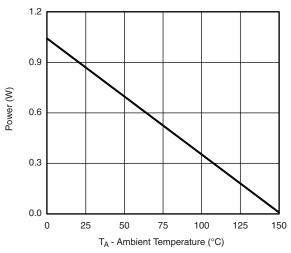
Safe Operating Area, Junction-to-Ambient

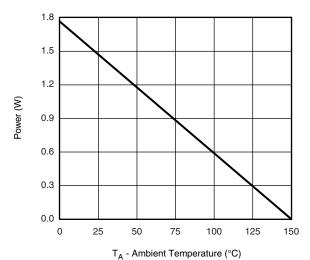


TYPICAL CHARACTERISTICS $T_A = 25 \, ^{\circ}\text{C}$, unless otherwise noted



Current Derating*





Power Derating, Junction-to-Ambient

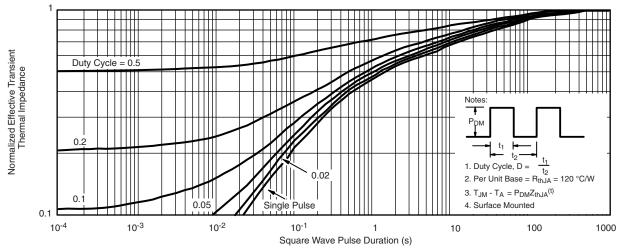
Power Derating, Junction-to-Case

^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

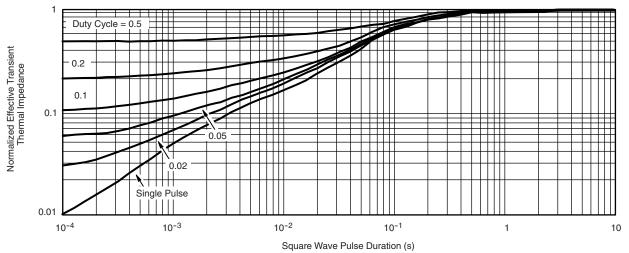
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TYPICAL CHARACTERISTICS $T_A = 25 \, ^{\circ}C$, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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