

High Power Class D Audio Power Amplifier using IR2011S

International **ISR** Rectifier

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Features

- Complete Analog Input Class D Audio Power Amplifier
- 500W + 500W Peak Stereo (2CH) Output
- THD+N=0.008% @1kHz, 100W, 4Ω
- High Efficiency 93% @350W, 1kHz, 4Ω
- Simple Self Oscillating Half-Bridge Topology
- Includes all Local House-keeping Power Supplies
- Protection Functions
- Wide Operating Supply Voltage Range $\pm 25 \sim 60V$
- Immune to Power Supply Fluctuations

Description

The IRAUDAMP1 is an example of a simple complete class D audio power amplifier design using the IR2011S, high speed high voltage gate driver IC. The design contains protection functions and house keeping power supplies for ease of use. This reference design is intended to demonstrate how to use the IR2011S, implement protection circuits, and design an optimum PCB layout.

Specifications

Instructions

Connection Diagram A typical test setup is shown in Fig.1.

Fig.1 Test Setup

Resetting Protection

- 1. Turn off ±50V at the same time
- 2. Wait until supply voltage drops to less than 5V
- 3. Apply ±50V at the same time
- 4. Apply audio signal

Power Supply

The IRAUDAMP1 requires a pair of symmetric dual power supplies ranging from \pm 25V to \pm 60V. A regulated power supply is preferable for performance measurements, but not always necessary. The bus capacitor, C38-41 on the board along with high frequency bypass C31, C32, C35, and C36; are designed to take care only of the high frequency ripple current components from the switching action. A set of bus capacitors having enough capacitance to handle the audio ripple current must be placed outside the board if an unregulated power supply is used.

Bus Pumping

Since the IRAUDAMP1 is a half bridge configuration, the bus pumping phenomenon occurs when the amplifier outputs low frequency signal is below 100Hz. The bus pumping phenomenon is unavoidable; significant bus voltage fluctuations caused by a reverse energy flow coming back to the power supply from the class D amplifier. This might cause an unacceptable instablility condition in the feedback system of a power supply.

The bus pumping becomes worse in the following conditions.

- lower the output frequency
- lower the load impedance
- higher the output voltage
	- smaller the bus capacitance in bus capacitors

If the bus voltage become too high or too low, the IRAUDAMP1 will shutdown the switching operation, and remain in the off condition until resetting the protection using the method described above.

One of the easiest countermeasures is to drive both of the channels out of phase so that the reverse energy from one channel is consumed by the other, and does not return to the power supply.

Input Audio Signal

A proper input signal is an analog signal below 20kHz, up to 5Vrms, having a source impedance of less than 600 Ω. A 30-60KHz input signal can cause LC resonance in the output LPF, resulting in an abnormally large amount of reactive current flowing through the switching stage. The IRAUDAMP1 has a C-R network to dump the resonant energy and protect the board in such a condition. However, these sub-sonic input frequencies should be avoided.

Load Impedance

The IRAUDAMP1 is designed for a load impedance of 4Ω and larger. The frequency response will have a small peak at the corner frequency of the output LC LPF if the loading impedance is higher than 4Ω. The IRAUDAMP1 is stable with capacitive loading, however, it should be realized that the frequency response will be degraded by a heavy capacitive loading of more than 0.1µF.

Adjustments of DC offset and Switching Frequency

Adjustments have to be done at an idling condition with no signal input.

Note: The PWM switching frequency in this type of self oscillating scheme greatly impacts the audio performances, especially in the case where two or more channels are in close proximity.

Thermal Considerations

The IRAUDAMP1 unitlizes a relatively thick aluminum block heatsink for peak power output handling capabilities. It can handle continuous 1/8 of the rated power, which is generally considered to be a normal operating condition in safety standards, for a considerable length of time such as one hour. The size of the heatsink, however, is not sufficient to handle continuous rated power.

Fig.2 shows the relationship between total power dissipation and temperature rise at equilibrium. If testing requires running conditions with continuous power a higher than 1/8 of the rated power, then, attach extensions to the top of the heatsink using three M4 screw taps prepared for this purpose. Please note that the heatsink is electrically connected to the GND pin.

Fig.2 Heatsink Thermal Characteristic at Equilibrium

Functional Description

Fig. 3 Simplified Block Diagram of Amplifier

Self Oscillating PWM modulator

The IRAUDAMP1 class D audio power amplifier is based on a self oscillating type PWM modulator for the lowest component count and a robust design. This topology is basically an analog version of a $2nd$ order sigma delta modulation having a class D switching stage inside the loop. The benefit of the sigma delta modulation in comparison to the carrier signal based modulator is that all the error in the audible frequency range is shifted away into the inaudible upper frequency range by nature of its operation, and it can apply a sufficient amount of correction. Another important benefit of the selfoscillating modulator is that it will cease operation if something interrupts the oscillating sequences. This is generally beneficial in a class D application because it makes the amplifier more robust.

Looking at CH-1 as an example, OP amp U1 forms a front end 2^{nd} order integrator with C17 & C18. This integrator receives a rectangular waveform from the class D switching stage and outputs a quadratic oscillatory waveform as a carrier signal. To create the modulated PWM, the input signal shifts the average value of this quadratic waveform, through R10, so that the duty varies according to the instantaneous value of the analog input signal. The level shift transistor Q1 converts the carrier signal from a voltage form into a current form and sends it to the logic gates sitting on the negative DC bus via the level shift resistor R44, which conerts the signal back into a voltage form. The signal is then quantized by the threshold of the CMOS inverter gate U2. The PWM signal out of the inverter is split into two signals, with opposite polarity, one for high side MOSFET drive signal, the other for the low side MOSFET drive signal. The dual AND gates of U4 are used to implement the shutdown function, a high shutdown signal will ensure the outputs of the AND gates are low which in turn ensures the inputs to the gate driver are low.

Under normal conditions the SD signal is low and the drive signal are passed directly through the AND gates to the IR2011S gate driver.

The IR2011 drives two IRFB23N15D MOSFETs in the power stage to provide the amplified Digital PWM waveform.

The amplified analog output is recreated by demodulating the amplified PWM . This is done by means of the LC Low Pass Filter formed by L1 and C51, which filters out the class D switching signal .

Switching Frequency

The self oscillating frequency is determined by the total delay time inside the loop. The following parameters affect the frequency.

- Delay time in logic circuits
- The gate driver propagation delay
- MOSFET switching speed
- Integration time constant in the front end integrator, e.g. R1, R23, R26, C17, and C18 for CH-1.
- Supply Voltages

Gate Driver

The IRAUDAMP1 uses the IR2011S gate driver IC which is suitable for high speed, high speed switching applications up to 200V. In this design, the difference between ton and toff is used to generate a dead-time (a blanking time in between the on state of the two MOSFETs). Because of this, there is no gate timing adjustment on the board.

MOSFET Gate Resistor

In order to add a little more dead-time and compensate for the finite switching transient time in the MOSFET, a schottky diode is added in parallel with the gate resistor. The gate resistor (R31 and R50 in CH-1) adds about 10nS of delay time at turn on by limiting the gate charging current to the IRFB23N15D. The schottky diode bypasses the gate resistor in the gate discharge path, so that there is no falling edge delay. The delay at the rising edge adds dead time.

Startup Circuit

A self oscillating scheme contains class D switching stage that requires a start-up triggering signal to charge the high side bootstrap capacitor . The starter circuits, Q9 and Q10, detect the rising edge of –Vcc and turn the low side MOSFETs on for about 200mS to charge the bootstrap capacitors C23 and C24, then release the loop allowing the oscillation to start.

Housekeeping Voltage Regulators

The IRAUDAMP1 contains following regulators to accommodate all the necessary functions on the board.

Protection

The IRAUDAMP1 includes protection features for overvoltage (OVP), overcurrent (OCP), and DC current protection. All of the protection uses OR logic so that any of the protection features when activated will disengage the output relay to cut off the load and protect the speakers. OCP and OVP functions are latched, DC protection is unlatched. To reset the protection, the bus voltage has to be reset to zero volts before re-applying power. The protection circuitry will also shutdown the amplifier if a fault condition is detected.

Fig.4 Functional Block Diagram of Protection

DC protection

DC voltage output protection is provided to protect the speakers from DC current. This abnormal condition occurs only when the power amplifier fails and one of the MOSFETs remains in the ON state. DC protection is activated if the output has more than ±3V DC offset. DC protection is unltached, and the amplifier will resume normal operation about 2 seconds after a fault condition has been removed.

Over Current Protection

Over Current Protection will activate and shut down the entire amplifier if the amount of current sensed at the positive power supply in either channel exceeds the preset value. If an overcurrent condition occurs, the voltage generated across a shunt resistor turns on the OCP detection transistors, Q2 and Q4 to send a signal to the protection logic.

Over Voltage Protection

Over Voltage Protection shuts down the amplifier if the bus voltage between $-Vcc$ and $+Vec$ exceeds 126V, the threshold is determined by the sum of the zener voltages of Z1, Z2, and Z3. OVP protects the board from the bus pumping phenomena which occurs at very low audio signal frequencies by shutting down the amplifier.

Power On/Off Sequence Timing

The IRAUDAMP1 is a robust design that can handle any power up/down sequence. However, symmetrical power up is recommended to properly initiate the self oscillation. In order for the unit to startup correctly, the negative power supply has to be initialized from zero volts. Fig.5 shows a preferred power up sequence. At start-up, a DC output voltage appears at the output of the LPF due to the charging of the bootstrap capacitors. To avoid this unwanted DC output signal being to fed to the load, the output relay RLY1 engages approximately 2 seconds after the startup condition is completed. Fig 6 below shows the start-up timing with the audio output not being activated until approximately 2 seconds after the power supplies are stable and the amplifier has reached steady state operation.

 Fig.5 Start-up Timing (BLU: Switching, RED: Audio Output)

Typical Performance

 \pm Vcc= \pm 50V, RL = 4 Ω unless otherwise noted.

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(1kHz, 1V, 4 Ω , f_{SW}=400KHz) (no signal, 4 Ω , f_{SW}=400KHz)

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Fig.10 Spectrum Fig.11 Residual Noise Spectrum

Fig.12 Efficiency v.s. Output Power

Typical Switching Waveforms

(a) 20v/div, 0.5µS/div

(b) 20nS/div, Rising Edge (b) 20nS/div, Falling Edge **Fig.13 Switching Waveform at Output Node (TP5)**

Fig.14 Distortion Waveform

Schematic Diagrams

IRAUDAMP1 Bill of Materials

Inductor Spec

Part number: NPT0104 Inductance: 18uH Rated Current: 10A Core: T106-2, Micrometals Wire: AWG18, magnet wire # of Turns: 37 Finish: Varnished

Mechanical Dimensions:

PCB layout

Functional Allocation

Mechanical Drawings

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