# 2GB DDR3 SDRAM 72bit SO-DIMM

| Part Number | Bandwidth | Speed Grade | Max Frequency | CAS Latency | Density | Organization | Component Composition | Number of Rank |
|---|---|---|---|---|---|---|---|---|
| 75.A73CV.G000C | 10.6GB/sec | 1333Mbps | 666MHz | CL9 | 2GB | 256Mx72 | 128Mx8*18 | 2 |

## Specifications

- Support ECC error detection and correction
- On DIMM Thermal Sensor: YES
- Density: 2GB
- Organization – 256 word x 72 bits, 2rank
- Mounting 18 pieces of 1G bits DDR3 SDRAM sealed FBGA
- Package: 204-pin socket type small outline dual in line memory module (SO-DIMM)

  --- PCB height: 30.0mm

  --- Lead pitch: 0.6mm (pin)

  --- Lead-free (RoHS compliant)
- Power supply: VDD = 1.5V + 0.075V
- Eight internal banks for concurrent operation ( components)
- Interface: SSTL_15
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- /CAS Latency (CL): 6,7,8,9
- /CAS Write latency (CWL): 5,6,7
- Precharge: Auto precharge option for each burst access
- Refresh: Auto-refresh, self-refresh
- Refresh cycles

  --- Average refresh period

  7.8μs at 0℃ < TC < +85℃

  3.9μs at +85℃ ≤ TC ≤ +95℃
- Operating case temperature range

  --- Industrial -40℃≤TC≤+95℃
- Serial presence detect (SPD)
- VDDSPD = 3.0V to 3.6V

### Industrial Temperature

The industrial temperature device requires that the case temperature not exceed –40°C or +95°C. JEDEC specifications require the refresh rate to double when $T_C$ exceeds +85°C; this also requires use of the high-temperature self refresh option.

Notes:
- MAX operating case temperature. $T_C$ is measured in the center of the package.
- A thermal solution must be designed to ensure the DRAM device does not exceed the maximum $T_C$ during operation.
- Device functionality is not guaranteed if the DRAM device exceeds the maximum $T_C$ during operation.
- If $T_C$ exceeds +85°C, the DRAM must be refreshed externally at 2X refresh, which is a 3.9μs interval refresh rate.

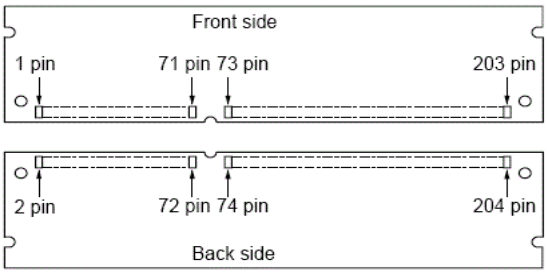
## Features

- Double-data-rate architecture; two data transfers per clock cycle.
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture.
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver.
- DQS is edge-aligned with data for READs; center aligned with data for WRITEs.
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS.
- Data mask (DM) for write data.
- Posted /CAS by programmable additive latency for better command and data bus efficiency.
- On-Die-Termination (ODT) for better signal quality
  --- Synchronous ODT
  --- Dynamic ODT
  --- Asynchronous ODT
- Multi Purpose Register (MPR) for temperature read out.
- ZQ calibration for DQ drive and ODT.
- Programmable Partial Array Self-Refresh (PASR)
- /RESET pin for Power-up sequence and reset function.
- SRT range:
  --- Normal/extended
  --- Auto/manual self-refresh
- Programmable Output driver impedance control

## Description

The 75.A73CV.G000C is a 256MX72 DDR3 SDRAM high density SO-UDIMM. This memory module consists of eighteen CMOS 128MX8 bits with 8 banks DDR3 synchronous DRAMs in BGA packages and a 2K EEPROM in an 8-pin MLF package. This module is a 204-pin small outline dual in line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR3 SDRAM.

# Pin Configurations




| 204-PIN DDR3 SO-UDIMM FRONT | | | | | | | | 204-PIN DDR3 SO-UDIMM BACK | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
| 1 | VREFDQ | 53 | VSS | 105 | A1 | 157 | DM5 | 2 | VSS | 54 | DQ28 | 106 | A2 | 158 | VSS |
| 3 | VSS | 55 | DQ24 | 107 | A0 | 159 | DQ42 | 4 | DQ4 | 56 | DQ29 | 108 | BA1 | 160 | DQ46 |
| 5 | DQ0 | 57 | DQ25 | 109 | VDD | 161 | DQ43 | 6 | DQ5 | 58 | VSS | 110 | VDD | 162 | DQ47 |
| 7 | DQ1 | 59 | DM3 | 111 | CK0 | 163 | VSS | 8 | VSS | 60 | DQS3# | 112 | CK1 | 164 | VSS |
| 9 | VSS | 61 | VSS | 113 | CK0# | 165 | DQ48 | 10 | DQS0# | 62 | DQS3 | 114 | CK1# | 166 | DQ52 |
| 11 | DM0 | 63 | DQ26 | 115 | VDD | 167 | DQ49 | 12 | DQS0 | 64 | VSS | 116 | VDD | 168 | DQ53 |
| 13 | DQ2 | 65 | DQ27 | 117 | A10/AP | 169 | VSS | 14 | VSS | 66 | DQ30 | 118 | NC/CS3# | 170 | VSS |
| 15 | DQ3 | 67 | VSS | 119 | BA0 | 171 | DQS6# | 16 | DQ6 | 68 | DQ31 | 120 | NC/CS2# | 172 | DM6 |
| 17 | VSS | 69 | CB0 | 121 | WE# | 173 | DQS6 | 18 | DQ7 | 70 | VSS | 122 | RAS# | 174 | DQ54 |
| 19 | DQ8 | 71 | CB1 | 123 | VDD | 175 | VSS | 20 | VSS | 72 | CB4 | 124 | VDD | 176 | DQ55 |
| 21 | DQ9 | 73 | VSS | 125 | CAS# | 177 | DQ50 | 22 | DQ12 | 74 | CB5 | 126 | ODT0 | 178 | VSS |
| 23 | VSS | 75 | DQS8# | 127 | CS0# | 179 | DQ51 | 24 | DQ13 | 76 | DM8 | 128 | ODT1 | 180 | DQ60 |
| 25 | DQS1# | 77 | DQS8 | 129 | CS1# | 181 | VSS | 26 | VSS | 78 | VSS | 130 | A13 | 182 | DQ61 |
| 27 | DQS1 | 79 | VSS | 131 | VDD | 183 | DQ56 | 28 | DM1 | 80 | CB6 | 132 | VDD | 184 | VSS |
| 29 | VSS | 81 | CB2 | 133 | DQ32 | 185 | DQ57 | 30 | RESET# | 82 | CB7 | 134 | DQ36 | 186 | DQS7# |
| 31 | DQ10 | 83 | CB3 | 135 | DQ33 | 187 | VSS | 32 | VSS | 84 | VREFCA | 136 | DQ37 | 188 | DQS7 |
| 33 | DQ11 | 85 | VDD | 137 | VSS | 189 | DM7 | 34 | DQ14 | 86 | VDD | 138 | VSS | 190 | VSS |
| 35 | VSS | 87 | CKE0 | 139 | DQS4# | 191 | DQ58 | 36 | DQ15 | 88 | A15/NC* | 140 | DM4 | 192 | DQ62 |
| 37 | DQ16 | 89 | CKE1 | 141 | DQS4 | 193 | DQ59 | 38 | VSS | 90 | A14/NC* | 142 | DQ38 | 194 | DQ63 |
| 39 | DQ17 | 91 | BA2 | 143 | VSS | 195 | VSS | 40 | DQ20 | 92 | A9 | 144 | DQ39 | 196 | VSS |
| 41 | VSS | 93 | VDD | 145 | DQ34 | 197 | SA0 | 42 | DQ21 | 94 | VDD | 146 | VSS | 198 | EVENT#* |
| 43 | DQS2# | 95 | A12/BC# | 147 | DQ35 | 199 | VDDSPD | 44 | DM2 | 96 | A11 | 148 | DQ44 | 200 | SDA |
| 45 | DQS2 | 97 | A8 | 149 | VSS | 201 | SA1 | 46 | VSS | 98 | A7 | 150 | DQ45 | 202 | SCL |
| 47 | VSS | 99 | A5 | 151 | DQ40 | 203 | VTT | 48 | DQ22 | 100 | A6 | 152 | VSS | 204 | VTT |
| 49 | DQ18 | 101 | VDD | 153 | DQ41 | | | 50 | DQ23 | 102 | VDD | 154 | DQS5# | | |
| 51 | DQ19 | 103 | A3 | 155 | VSS | | | 52 | VSS | 104 | A4 | 156 | DQS5 | | |

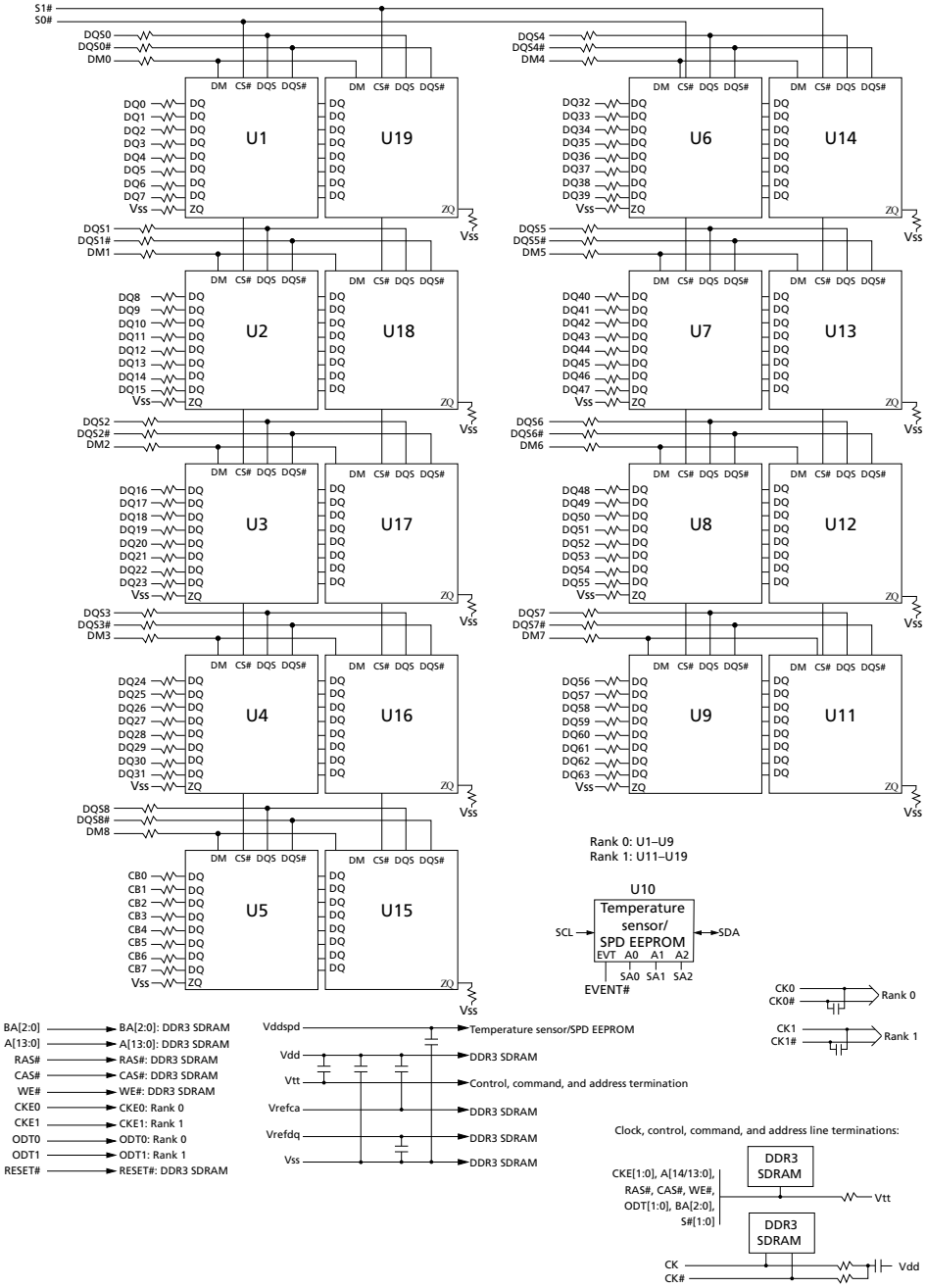
*IC Componet Compositio
256Mx8 A0~A14
512Mx8 A0~A15
1024Mx8 A0~A15

## Pin Description

| Pin name | Function | |
|---|---|---|
| A0 to A13 | Address input<br>Row address<br>Column address | <br>A0 to A13<br>A0 to A9 |
| A10 (AP) | Auto precharge | |
| A12 (/BC) | Burst chop | |
| BA0,BA1,BA2 | Bank select address | |
| DQ0 to DQ63 | Data input/output | |
| /RAS | Row address strobe command | |
| /CAS | Column address strobe command | |
| /WE | Write enable | |
| /CS0,/CS1 | Chip select | |
| CKE0,CKE1 | Clock enable | |
| CK0,CK1 | Clock input | |
| /CK0,/CK1 | Differential clock input | |
| DQS0 to DQS7,/DQS0 to /DQS7 | Input and output data strobe | |
| DM0 to DM7 | Input mask | |
| SCL | Clock input for serial PD | |
| SDA | Data input/output for serial PD | |
| SA0,SA1 | Serial address input | |
| VDD | Power for internal circuit | |
| VDDSPD | Power for serial EEPROM | |
| VREFCA | Reference voltage for CA | |
| VREFDQ | Reference voltage for DQ | |
| VSS | Ground | |
| VTT | I/O termination supply for SDRAM | |
| /RESET | Set DRAM to known state | |
| ODT0,ODT1 | ODT control | |
| /EVENT | Temperature event pin | |
| NC | No connection | |

# Functional Block Diagram

### Figure 2: Functional Block Diagram

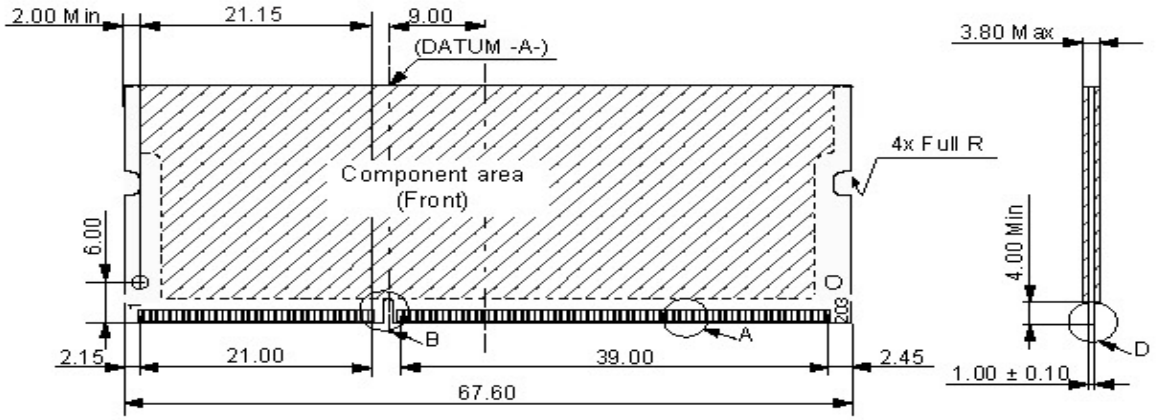



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

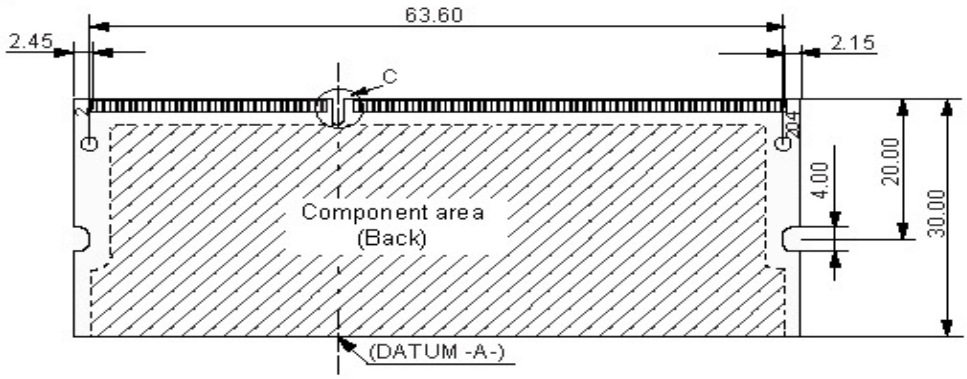
# Dimensions

Unit: mm

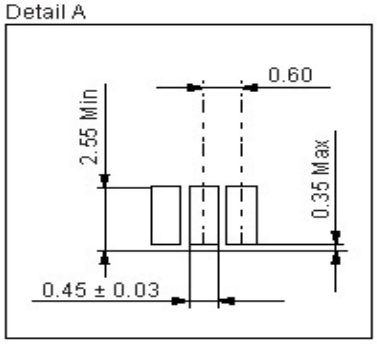
Front side



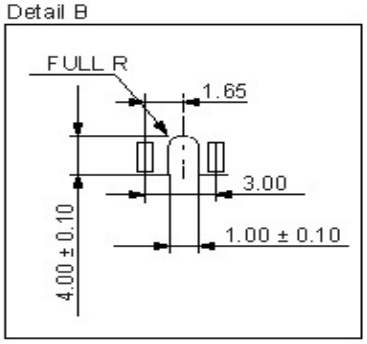

Back side



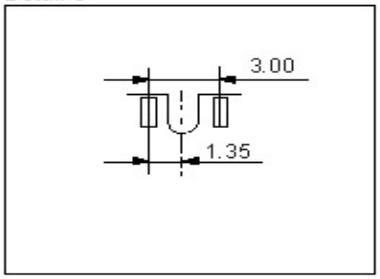

Detail A



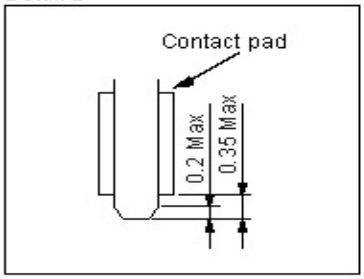

Detail B




Detail C




Detail D




(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)