19-1649; Rev 0; 4/00

MAXIM

Low-Cost, Low-Voltage, Rail-to-Rail, Input/Output, SOT23 5MHz Op Amp

General Description

The MAX4321 operational amplifier (op amp) combines a 5MHz gain-bandwidth product and excellent DC accuracy with Rail-to-Rail® operation at both the inputs and the output. This device requires only 650µA and operates from either a single +2.4V to +6.5V supply or dual ±1.2V to ±3.25V supplies, although the MAX4321 typically operates down to +1.8V (±0.9V). The MAX4321 remains unity-gain stable with capacitive loads up to 500pF and is capable of driving 250Ω loads to within 200mV of either rail.

With rail-to-rail input common-mode range and output swing, the MAX4321 is ideal for low-voltage, single-supply applications. In addition, low ±1.2mV input offset voltage and high 2V/µs slew rate make this device ideal for signal-conditioning stages for precision, low-voltage data-acquisition systems. The MAX4321 comes in a space-saving 5-pin SOT23 package and is guaranteed over the extended (-40°C to +85°C) temperature range.

The MAX4321 is a low-voltage, pin-for-pin compatible upgrade for the LMC7101 that offers five-times higher bandwidth, two-times faster slew rate, and about half the input voltage noise density.

Applications

Battery-Powered Instruments

Portable Equipment

Data-Acquisition Systems

Sensor and Signal Conditioning

Low-Power, Low-Voltage Applications

General-Purpose Low-Voltage Applications

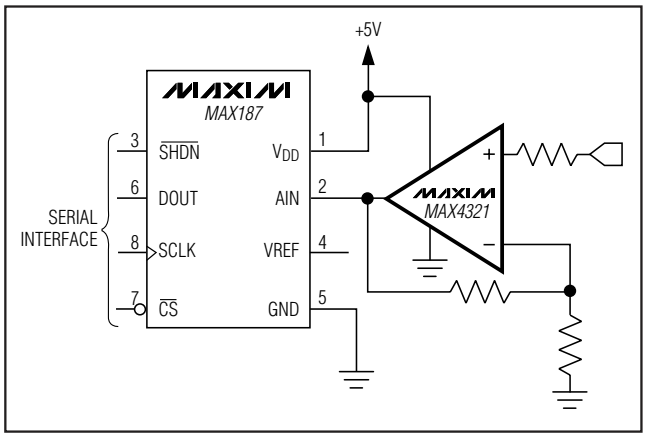
Features

- ♦ **Low-Voltage, Pin-for-Pin Upgrade for LMC7101**
- ♦ **Guaranteed +2.4V to +6.5V Single-Supply Operation**
- ♦ **Typically Operates Down to +1.8V**
- ♦ **5MHz Gain-Bandwidth Product**
- ♦ **650µA Quiescent Current**
- ♦ **Rail-to-Rail Common-Mode Input Voltage Range**
- ♦ **Rail-to-Rail Output Voltage Range**
- ♦ **Drives 250Ω Loads**
- ♦ **Unity-Gain Stable for Capacitive Loads up to 500pF**
- ♦ **No Phase Reversal for Overdriven Inputs**
- ♦ **Low-Cost Solution in SOT23-5 Package**

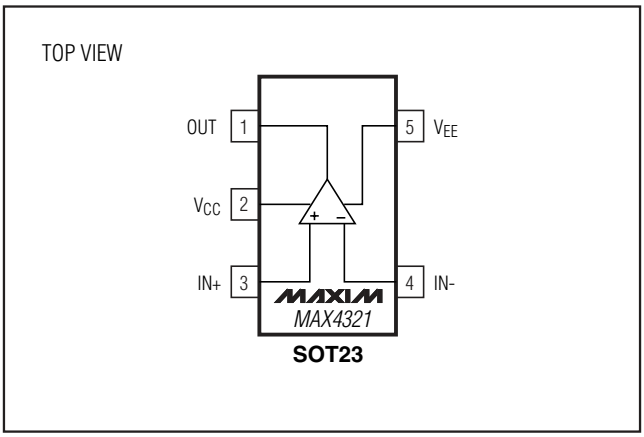
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	TOP MARK
MAX4321EUK-T	-40°C to +85°C	5 SOT23-5	ADOA

Typical Operating Circuit



Pin Configuration/ Functional Diagram



Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Low-Cost, Low-Voltage, Rail-to-Rail, Input/Output, SOT23 5MHz Op Amp

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}) .....-0.3V to +7V
All Other Pins .....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Output Short-Circuit Duration.....Continuous
(short to either supply)
Continuous Power Dissipation (T_A = +70°C)
5-pin SOT23 (derate 7.1mW/°C above +70°C).....571mW

Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V, V_{EE} = 0, V_{CM} = 0, V_{OUT} = V_{CC}/2, R_L = ∞ connected to V_{CC}/2, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC} - V_{EE}			2.4		6.5	V
Supply Current		V_{CM} = V_{OUT} = V_{CC}/2	V_{CC} = +2.4V		650		µA
			V_{CC} = +6.5V		725		
Input Offset Voltage	V_{OS}	V_{CM} = V_{EE} or V_{CC}			±1.2	±3.5	mV
Input Bias Current	I_{BIAS}	V_{CM} = V_{EE} or V_{CC}			±50	±150	nA
Input Offset Current	I_{OFFSET}	V_{CM} = V_{EE} or V_{CC}			±4	±25	nA
Differential Input Resistance	R_{IN}	-1.5V < V_{DIFF} <+1.5V			500		kΩ
Common-Mode Input Voltage Range	V_{CM}	Inferred from CMRR test		V_{EE}		V_{CC}	V
Common-Mode Rejection Ratio	CMRR	V_{EE} ≤ V_{CM} ≤ V_{CC}		60	91		dB
Power-Supply Rejection Ratio	PSRR	2.4V < V_{CC} < 6.5V		66	100		dB
Output Resistance	R_{OUT}	A_V = +1V/V			0.1		Ω
Large-Signal Voltage Gain	A_V	V_{OUT} = 0.25V to 4.75V, R_L = 100kΩ			103		dB
		V_{OUT} = 0.40V to 4.60V, R_L = 600Ω			100		
		V_{OUT} = 0.40V to 4.60V, R_L = 250Ω		70	86		
Output Voltage Swing	V_{OUT}	R_L = 100kΩ	V_{CC} - V_{OH}		25		mV
			V_{OL} - V_{EE}		20		
		R_L = 600Ω	V_{CC} - V_{OH}		135		
			V_{OL} - V_{EE}		60		
		R_L = 250Ω	V_{CC} - V_{OH}		200	300	
			V_{OL} - V_{EE}		100	200	
Output Short-Circuit Current					50		mA

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V, V_{EE} = 0, V_{CM} = 0, V_{OUT} = V_{CC}/2, R_L = ∞ connected to V_{CC}/2, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC} - V_{EE}			2.4		6.5	V
Supply Current	I_{CC}	V_{CM} = V_{OUT} = V_{CC}/2				1200	µA
Input Offset Voltage	V_{OS}	V_{CM} = V_{EE} or V_{CC}				±6	mV
Input Offset Voltage Temperature Coefficient					±2		µV/°C
Input Bias Current	I_{BIAS}	V_{CM} = V_{EE} or V_{CC}				±180	nA
Input Offset Current	I_{OFFSET}	V_{CM} = V_{EE} or V_{CC}				±50	nA
Common-Mode Input Voltage Range	V_{CM}	Inferred from CMRR test		V_{EE}		V_{CC}	V
Common-Mode Rejection Ratio	CMRR	V_{EE} ≤ V_{CM} ≤ V_{CC}		54			dB
Power-Supply Rejection Ratio	PSRR	2.4V < V_{CC} < 6.5V		62			dB
Large-Signal Voltage Gain	A_V	V_{OUT} = 0.40V to 4.60V, R_L = 250Ω		66			dB
Output Voltage Swing	V_{OUT}	R = 250Ω	V_{CC} - V_{OH}			350	mV
			V_{OL} - V_{EE}			250	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V, V_{EE} = 0, V_{CM} = 0, V_{OUT} = V_{CC}/2, R_L = 250Ω connected to V_{CC}/2, **T_A = +25°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	GBP			5		MHz
Phase Margin				64		degrees
Gain Margin				12		dB
Total Harmonic Distortion and Noise	THD+N	10kHz tone, V_{OUT} = 2Vpp, A_V = +1V/V		0.003		%
Slew Rate	SR	V_{OUT} = 1V step		2		V/µs
Settling Time to 0.01%	t_{SETTLE}	V_{OUT} = 2V step, A_V = +1V/V		2		µs
Turn-On Time	t_{ON}	V_{CC} = 0 to 3V step		1		µs
Input Capacitance	C_{IN}			3		pF
Input Noise Voltage Density		f = 1kHz		22		nV/√Hz
Input Noise Current Density		f = 1kHz		0.4		pA/√Hz

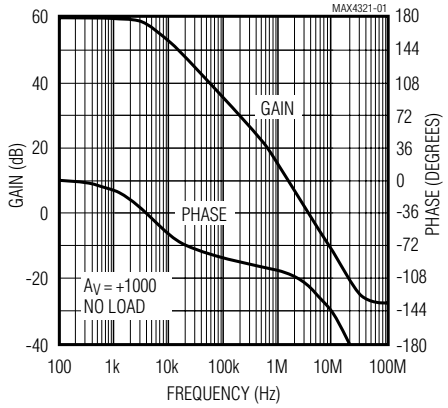
Note 1: All devices are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design and characterization.

Low-Cost, Low-Voltage, Rail-to-Rail, Input/Output, SOT23 5MHz Op Amp

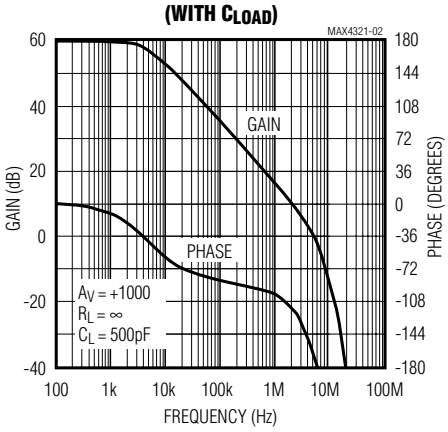
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = 0, V_{CM} = V_{CC}/2, T_A = +25°C, unless otherwise noted.)

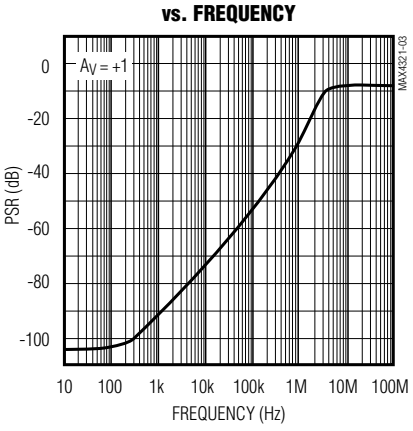
GAIN AND PHASE vs. FREQUENCY



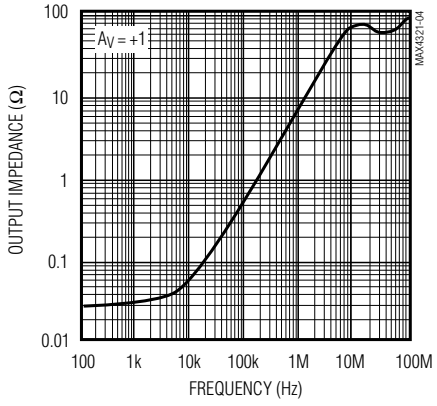
GAIN AND PHASE vs. FREQUENCY (WITH C_{LOAD})



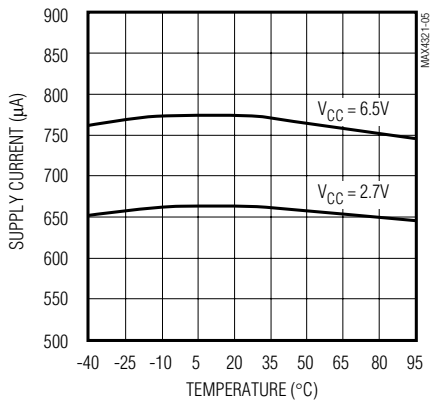
POWER-SUPPLY REJECTION vs. FREQUENCY



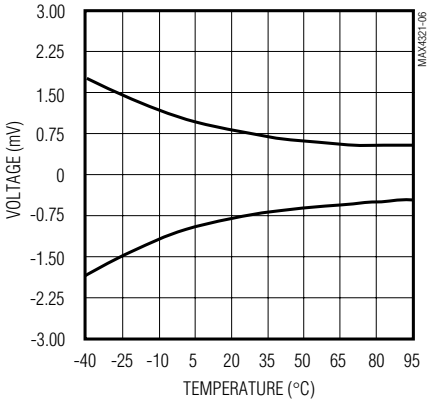
OUTPUT IMPEDANCE vs. FREQUENCY



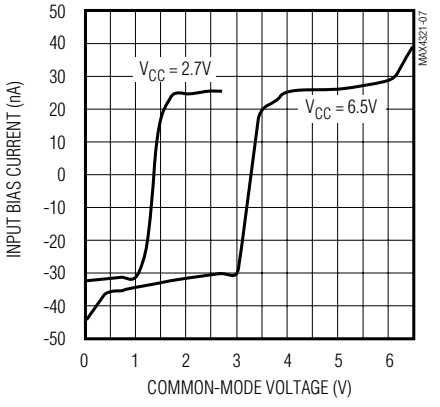
SUPPLY CURRENT vs. TEMPERATURE



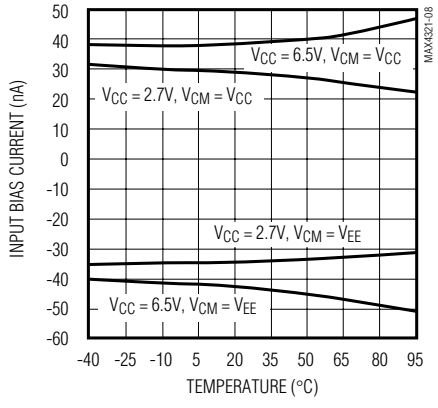
INPUT OFFSET VOLTAGE vs. TEMPERATURE



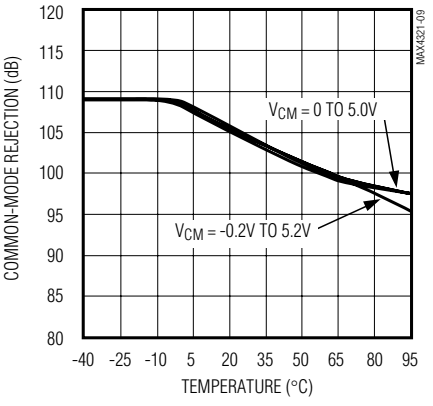
INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE



INPUT BIAS CURRENT vs. TEMPERATURE



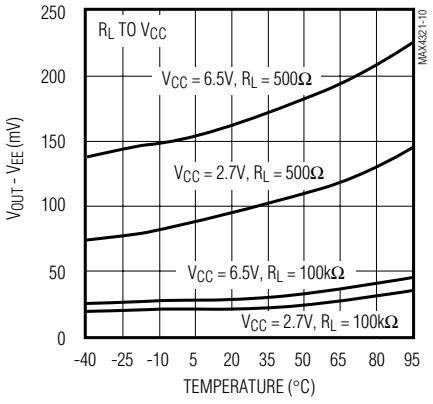
COMMON-MODE REJECTION vs. TEMPERATURE



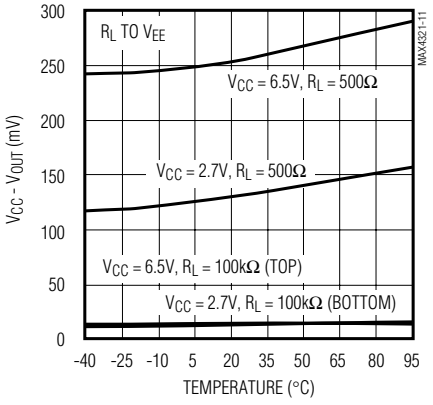
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0, V_{CM} = V_{CC}/2, T_A = +25°C, unless otherwise noted.)

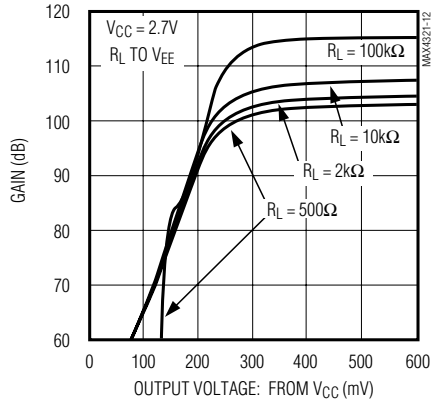
MINIMUM OUTPUT VOLTAGE vs. TEMPERATURE



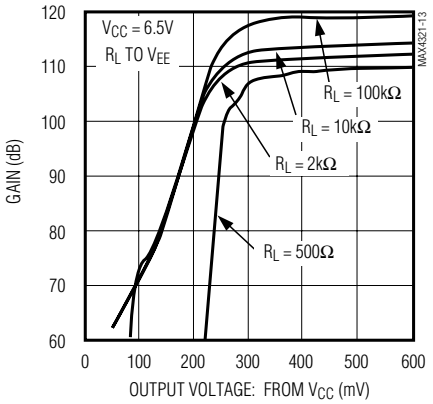
MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE



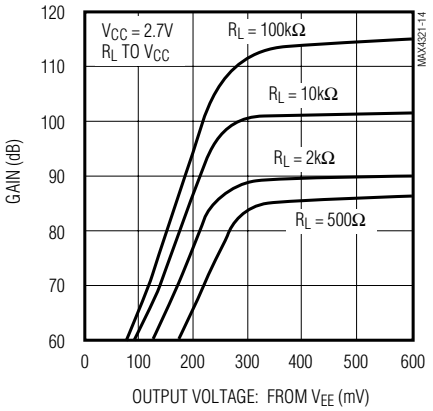
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



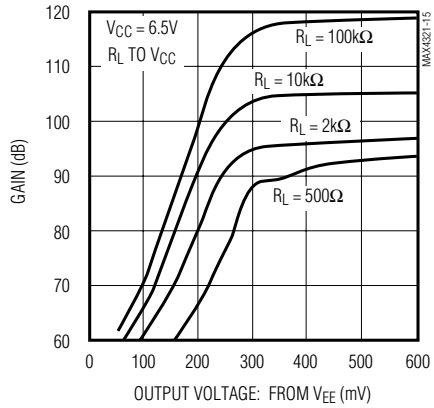
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



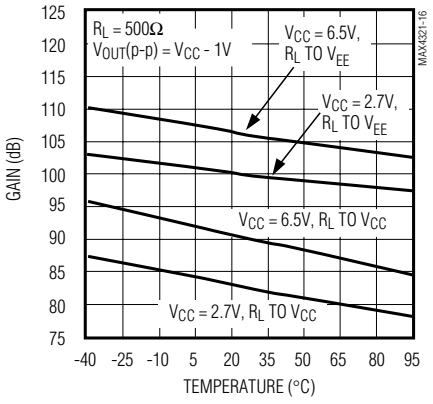
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



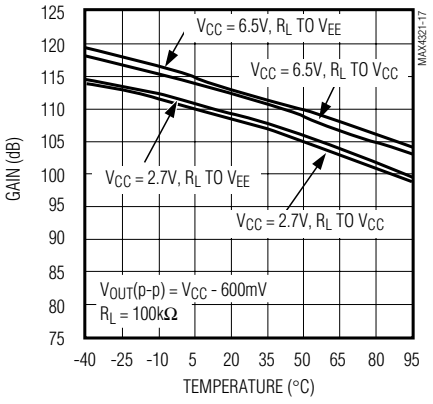
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



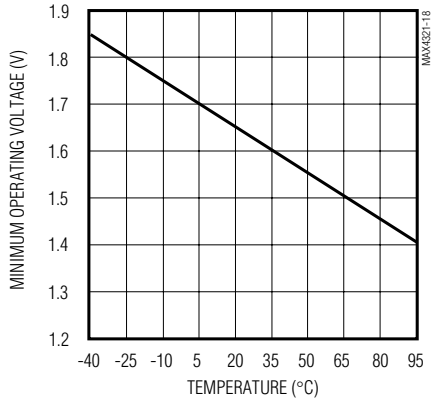
LARGE-SIGNAL GAIN vs. TEMPERATURE



LARGE-SIGNAL GAIN vs. TEMPERATURE



MINIMUM OPERATING VOLTAGE vs. TEMPERATURE

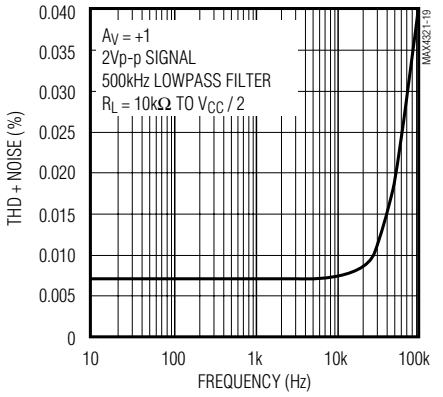


Low-Cost, Low-Voltage, Rail-to-Rail, Input/Output, SOT23 5MHz Op Amp

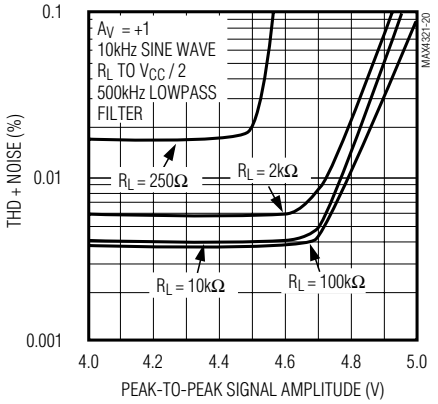
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0, V_{CM} = V_{CC}/2, T_A = +25°C, unless otherwise noted.)

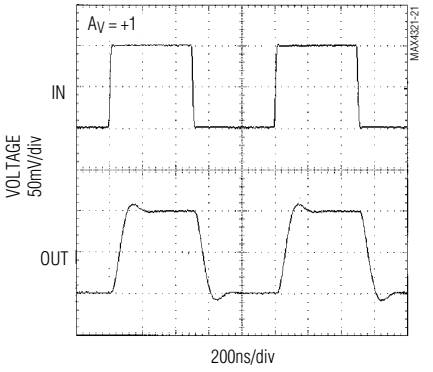
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



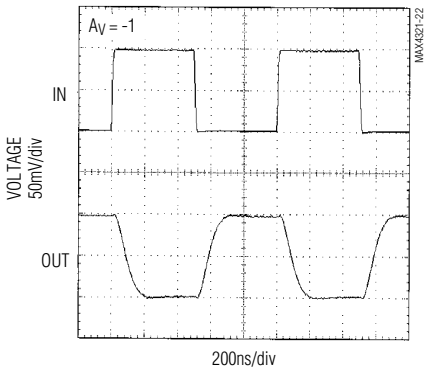
TOTAL HARMONIC DISTORTION PLUS NOISE vs. PEAK-TO-PEAK SIGNAL AMPLITUDE



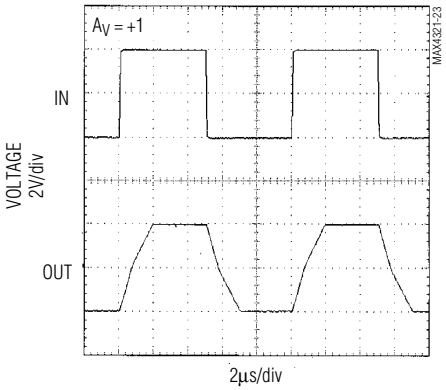
SMALL-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



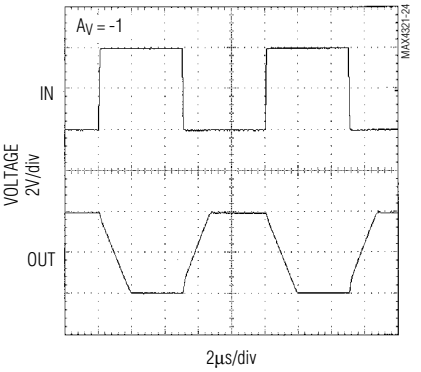
SMALL-SIGNAL TRANSIENT RESPONSE (INVERTING)



LARGE-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



LARGE-SIGNAL TRANSIENT RESPONSE (INVERTING)



Pin Description

PIN	NAME	FUNCTION
1	OUT	Output
2	V_{CC}	Positive Supply
3	IN+	Noninverting Input
4	IN-	Inverting Input
5	V_{EE}	Negative Supply. Connect to ground for single-supply operation.

Applications Information

Rail-to-Rail Input Stage

The MAX4321 high-speed amplifier has rail-to-rail input and output stages designed for low-voltage, single-supply operation. The input stage consists of separate NPN and PNP differential stages, which combine to provide an input common-mode range extending to the supply rails. The PNP stage is active for input voltages close to the negative rail, and the NPN stage is active for input voltages near the positive rail. The switchover transition region, which occurs near V_{CC} / 2, has been extended to minimize the slight degradation in CMRR caused by the mismatch of the input pairs. Its low offset voltage, high bandwidth, and rail-to-rail common-mode range makes this op amp an excellent choice for precision, low-voltage, data-acquisition systems.

Since the input stage switches between the NPN and PNP pairs, the input bias current changes polarity as the input voltage passes through the transition region. To reduce the offset error caused by input bias currents flowing through external source impedances, match the effective impedance seen by each input (Figures 1a, 1b). High source impedances, together with the input capacitance, can create a parasitic pole that produces an underdamped signal response. Reducing the input impedance or placing a small (2pF to 10pF) capacitor across the feedback resistor improves the response.

The MAX4321's inputs are protected from large differential input voltages by 1kΩ series resistors and back-to-back triple diodes across the inputs (Figure 2). For differential input voltages less than 1.8V, the input resistance is typically 500kΩ. For differential input voltages greater than 1.8V, the input resistance is approximately 2kΩ, and the input bias current is determined by the following equation:

$$I_{BIAS} = \frac{V_{DIFF} - 1.8V}{2k\Omega}$$

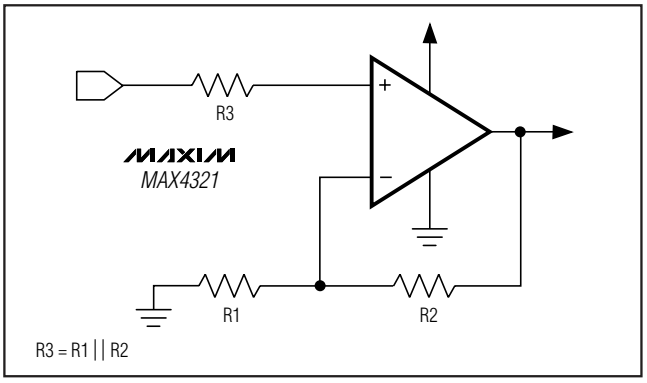


Figure 1a. Reducing Offset Error Due to Bias Current (Noninverting)

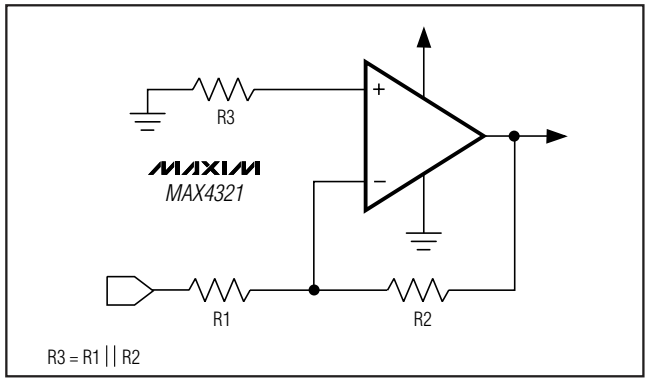


Figure 1b. Reducing Offset Error Due to Bias Current (Inverting)

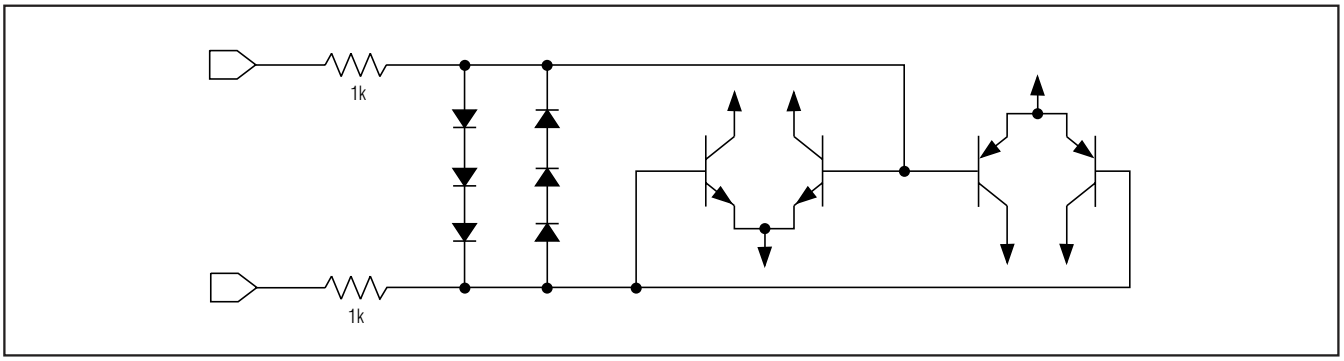


Figure 2. Input Protection Circuit

Low-Cost, Low-Voltage, Rail-to-Rail, Input/Output, SOT23 5MHz Op Amp

Rail-to-Rail Output Stage

The minimum output voltage will be within millivolts of ground for single-supply operation where the load is referenced to ground (V_{EE}). Figure 3 shows the input voltage range and output voltage swing of a MAX4321 connected as a voltage follower. With a +3V supply and the 100kΩ load tied to ground, the output swings from 0.02V to 2.97V. The maximum output voltage swing depends on the load but will be within 300mV of a +5V supply, even with the maximum load (250Ω to ground).

Driving a capacitive load can cause instability in most high-speed op amps, especially those with low quiescent current. The MAX4321 has a high tolerance for capacitive loads. It is stable with capacitive loads up to 500pF. Figure 4 gives the stable operating region for capacitive loads. Figures 5 and 6 show the response with capacitive loads and the results of adding an isolation resistor in series with the output (Figure 7). The resistor improves the circuit's phase margin by isolating the load capacitor from the op amp's output.

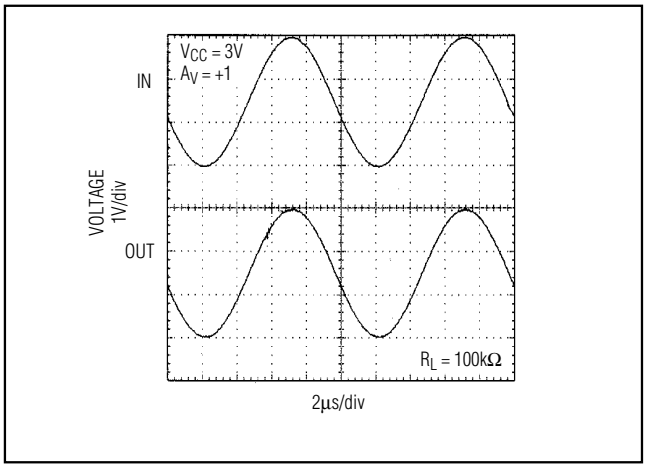


Figure 3. Rail-to-Rail Input /Output Voltage Range

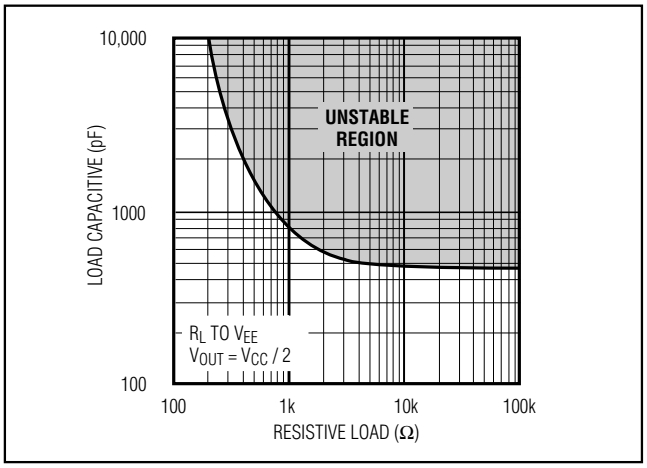


Figure 4. Capacitive-Load Stability

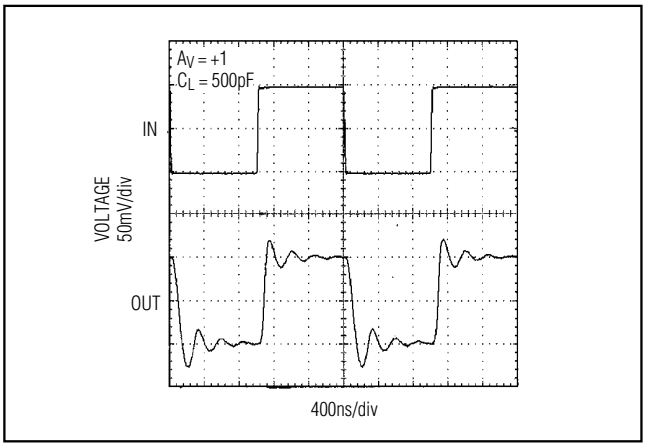


Figure 5. Small-Signal Transient Response with Capacitive Load

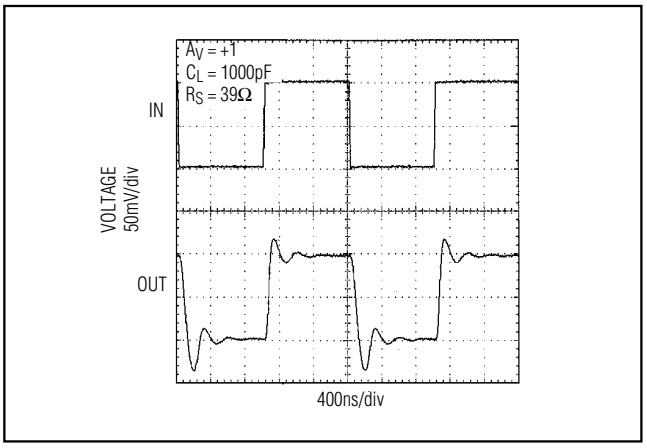


Figure 6. Transient Response to Capacitive Load with Isolation Resistor

Power-Up

The MAX4321 typically settles within 1µs after power-up. Using the test circuit of Figure 8, Figures 9 and 10 show the output voltage and supply current on power-up.

Power Supplies and Layout

The MAX4321 operates from single +2.4V to +6.5V or dual ±1.2V to ±3.25V supplies, though it typically operates down to +1.8V (±0.9V). For single-supply operation, bypass the power supply with a 0.1µF ceramic capacitor in parallel with at least 1µF. For dual supplies, bypass each supply to ground.

Good layout improves performance by decreasing the amount of stray capacitance at the op amp's inputs and outputs. To decrease stray capacitance, minimize trace lengths and resistor leads by placing external components close to the op amp's pins.

Package Information

TRANSISTOR COUNT: 84

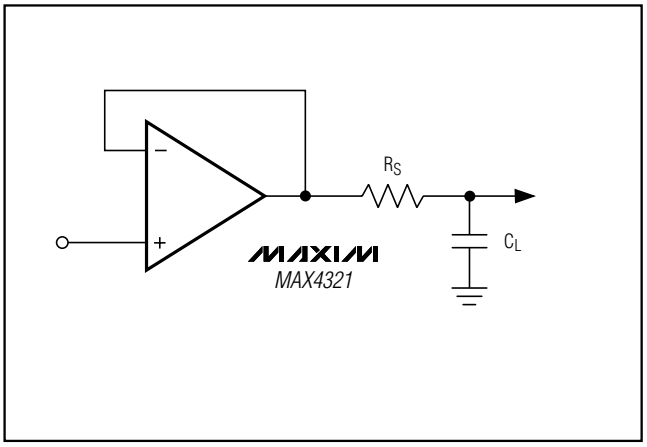


Figure 7. Capacitive-Load-Driving Circuit

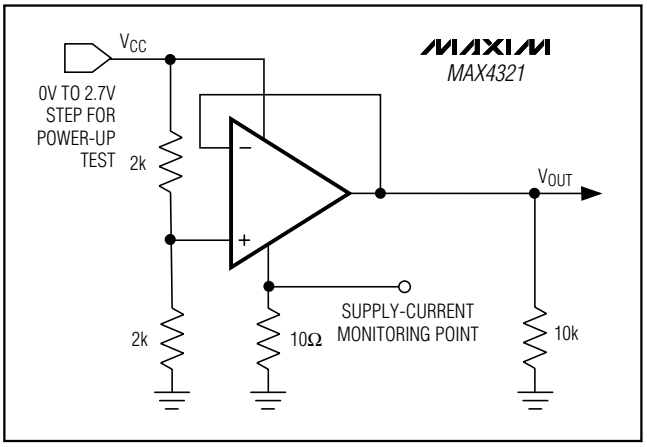


Figure 8. Power-Up Test Circuit

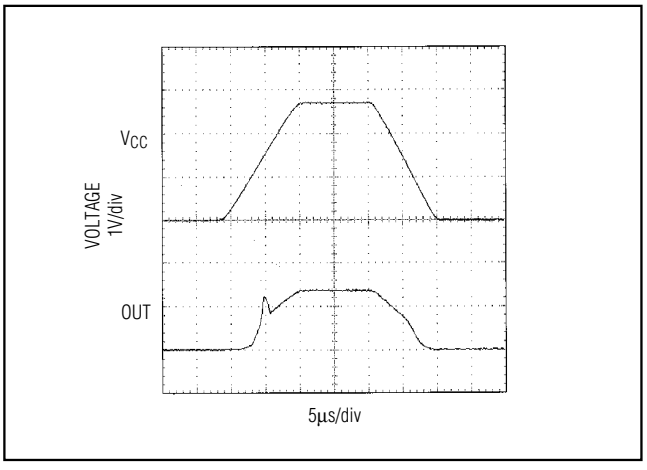


Figure 9. Power-Up Output Voltage

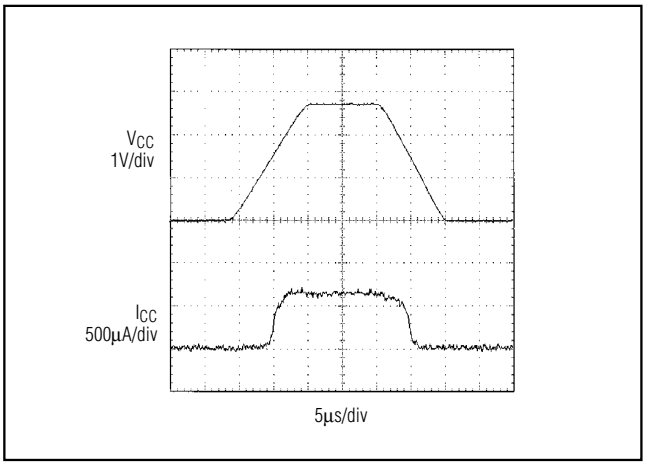
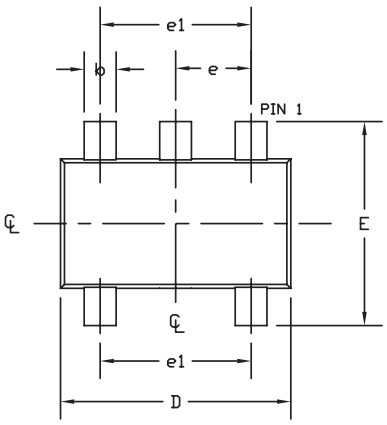


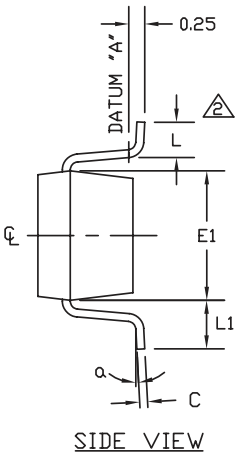
Figure 10. Power-Up Supply Current

Low-Cost, Low-Voltage, Rail-to-Rail, Input/Output, SOT23 5MHz Op Amp

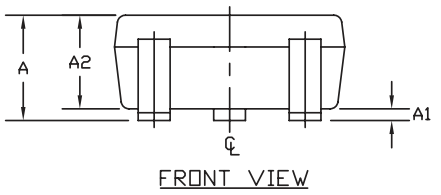
Package Information

SOT-23 5L.EPS





SYMBOL	MIN	NOM	MAX
A	0.90	1.25	1.45
A1	0.00	0.05	0.15
A2	0.90	1.10	1.30
b	0.35	0.40	0.50
C	0.08	0.15	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.35	0.45	0.60
L1	0.60 REF		
e	0.95 BSC.		
e1	1.90 BSC.		
a	0°	2.5°	8°
PKG CODES: U5-1, U5-2			



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25 MM.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. MEETS JEDEC MO178, VARIATION AA.
6. LEADS TO BE COPLANAR WITHIN 0.10 mm.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SOT-23, 5L

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0057	F	1/1

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