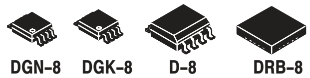


THS4271
THS4275

LOW NOISE, HIGH SLEW RATE, UNITY GAIN STABLE VOLTAGE FEEDBACK AMPLIFIER

Check for Samples: THS4271 THS4275

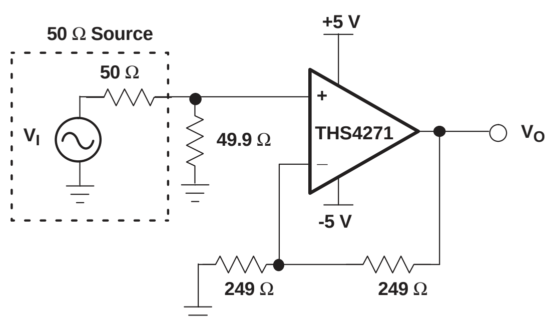
FEATURES

- **Unity Gain Stability**
- **Low Voltage Noise**
  - **3 nV/√Hz**
- **High Slew Rate: 1000 V/μs**
- **Low Distortion**
  - **–92 dBc THD at 30 MHz**
- **Wide Bandwidth: 1.4 GHz**
- **Supply Voltages**
  - **+5 V, ±5 V**
- **Power Down Functionality (THS4275)**
- **Evaluation Module Available**

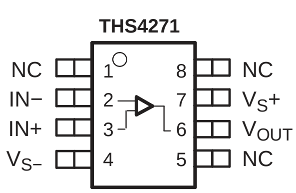
APPLICATIONS

- **High Linearity ADC Preamplifier**
- **Wireless Communication Receivers**
- **Differential to Single-Ended Conversion**
- **DAC Output Buffer**
- **Active Filtering**

Low-Noise, Low-Distortion, Wideband Application Circuit



NOTE: Power supply decoupling capacitors not shown



DESCRIPTION

The THS4271 and THS4275 are low-noise, high slew rate, unity gain stable voltage-feedback amplifiers designed to run from supply voltages as low as 5 V and as high as ±5 V. The THS4275 offers the same performance as the THS4271 with the addition of a power-down capability. The combination of low-noise, high slew rate, wide bandwidth, low distortion, and unity gain stability make the THS4271 and THS4275 high performance devices across multiple ac specifications.

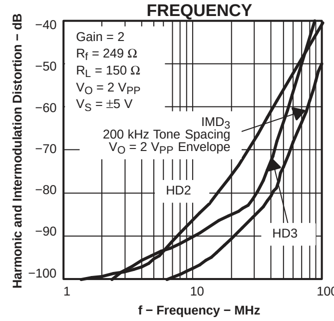
Designers using the THS4271 are rewarded with higher dynamic range over a wider frequency band without the stability concerns of decompensated amplifiers. The devices are available in SOIC, MSOP with PowerPAD™, and leadless MSOP with PowerPAD™ packages.

The THS4271 and THS4275 may have low-level oscillation when the die temperature (also known as the *junction temperature*) exceeds +60°C. For more information, see Maximum Die Temperature to Prevent Oscillation.

RELATED DEVICES

DEVICE	DESCRIPTION
THS4211	1-GHz voltage-feedback amplifier
THS4503	Wideband, fully-differential amplifier
THS3202	Dual, wideband current feedback amplifier

HARMONIC AND INTERMODULATION DISTORTION vs FREQUENCY



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION[1]

ORDERABLE PACKAGE AND NUMBER					
PLASTIC SMALL OUTLINE (D) [2]	LEADLESS MSOP 8 [3]	PLASTIC MSOP [2] PowerPAD		PLASTIC MSOP [2]	
	(DRB)	(DGN)	PACKAGE MARKING	(DGK)	PACKAGE MARKING
THS4271D	THS4271DRBT	THS4271DGN	BFQ	THS4271DGK	BEY
THS4271DR	THS4271DRBR	THS4271DGNR		THS4271DGKR	
THS4275D	THS4275DRBT	THS4275DGN	BFR	THS4275DGK	BJD
THS4275DR	THS4275DRBR	THS4275DGNR		THS4275DGKR	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) All packages are available taped and reeled. The **R** suffix standard quantity is 2500 (for example, THS4271DGNR).
(3) All packages are available taped and reeled. The **R** suffix standard quantity is 3000. The **T** suffix standard quantity is 250 (for example, THS4271DRBT).

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted[1]

			UNIT
V_S	Supply voltage		16.5 V
V_I	Input voltage		$\pm V_S$
I_O [2]	Output current		100 mA
	Continuous power dissipation		See Dissipation Ratings Table
T_J	Maximum junction temperature		+150°C
T_J [2]	Maximum junction temperature, continuous operation long term reliability		+125°C
T_J [3]	Maximum junction temperature to prevent oscillation		+60°C
T_{stg}	Storage temperature range		–65°C to +150°C
	ESD ratings	HBM	3000 V
		CDM	1500 V
		MM	1000 V

(1) The absolute maximum temperature under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.
(3) See *Maximum Die Temperature to Prevent Oscillation* section in the *Application Information* of this data sheet.

PACKAGE DISSIPATION RATINGS

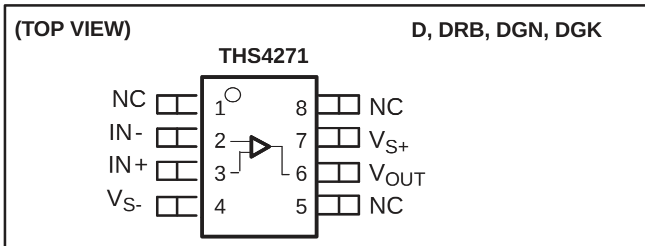
PACKAGE	θ_{JC} (°C/W)	θ_{JA} [1] (°C/W)
D (8 pin)	38.3	97.5
DGN (8 pin)[2]	4.7	58.4
DGK (8 pin)	54.2	260
DRB (8 pin)[2]	5	45.8

(1) These data were taken using the JEDEC standard High-K test PCB.
(2) The THS4271/5 may incorporate a PowerPAD™ on the underside of the chip. This feature acts as a heat sink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical briefs SLMA002 and SLMA004 for more information about utilizing the PowerPAD thermally enhanced package.

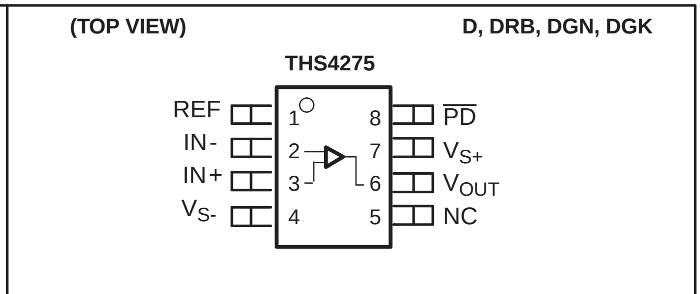
RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage (V_{S+} and $V_{S–}$)	Dual supply	±2.5	±5	V
	Single supply	5	10	
Input common-mode voltage range		V_{S-} + 1.4	V_{S+} – 1.4	V

PIN ASSIGNMENTS



NC - No internal connection



ELECTRICAL CHARACTERISTICS: V_S = ±5 V

At R_F = 249 Ω, R_L = 499 Ω, G = +2, unless otherwise noted.

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE (1)				MIN/ TYP/ MAX
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	
AC PERFORMANCE							
Small-signal bandwidth	G = 1, V_O = 100 mV_{PP}, R_L = 150 Ω	1.4				GHz	Typ
	G = –1, V_O = 100 mV_{PP}	400				MHz	Typ
	G = 2, V_O = 100 mV_{PP}	390				MHz	Typ
	G = 5, V_O = 100 mV_{PP}	85				MHz	Typ
	G = 10, V_O = 100 mV_{PP}	40				MHz	Typ
0.1-dB flat bandwidth	G = 1, V_O = 100 mV_{PP}, R_L = 150 Ω	200				MHz	Typ
Gain bandwidth product	G > 10, f = 1 MHz	400				MHz	Typ
Full-power bandwidth	G = –1, V_O = 2 V_p	80				MHz	Typ
Slew rate	G = 1, V_O = 2 V Step	950				V/µs	Typ
	G = –1, V_O = 2 V Step	1000				V/µs	Typ
Settling time to 0.1%	G = –1, V_O = 4 V Step	25				ns	Typ
Settling time to 0.01%	G = –1, V_O = 4 V Step	38				ns	Typ
Harmonic distortion	G = 1, V_O = 1 V_{PP}, f = 30 MHz						
Second harmonic distortion	R_L = 150 Ω	-92				dBc	Typ
	R_L = 499 Ω	-80				dBc	Typ
Third harmonic distortion	R_L = 150 Ω	-95				dBc	Typ
	R_L = 499 Ω	-95				dBc	Typ
Harmonic distortion	G = 2, V_O = 2 V_{PP}, f = 30 MHz						
Second harmonic distortion	R_L = 150 Ω	-65				dBc	Typ
	R_L = 499 Ω	-70				dBc	Typ
Third harmonic distortion	R_L = 150 Ω	-80				dBc	Typ
	R_L = 499 Ω	-90				dBc	Typ
Third-order intermodulation (IMD_3)	G = 2, V_O = 2 V_{PP}, R_L = 150 Ω, f = 70 MHz	-60				dBc	Typ
Third-order output intercept (OIP_3)	G = 2, V_O = 2 V_{PP}, R_L = 150Ω, f = 70 MHz	35				dBm	Typ
Differential gain (NTSC, PAL)	G = 2, R_L = 150 Ω	0.007%					Typ
Differential phase (NTSC, PAL)	G = 2, R_L = 150 Ω	0.004				°	Typ
Input voltage noise	f = 1 MHz	3				nV/√Hz	Typ
Input current noise	f = 1 MHz	3				pA√Hz	Typ
DC PERFORMANCE							
Open-loop voltage gain (A_{OL})	V_O = ± 50 mV, R_L = 499 Ω	75	65	60	60	dB	Min
Input offset voltage	V_{CM} = 0 V	5	10	12	12	mV	Max
Average offset voltage drift	V_{CM} = 0 V			±10	±10	µV/°C	Typ
Input bias current	V_{CM} = 0 V	6	15	18	18	µA	Max
Average bias current drift	V_{CM} = 0 V			±10	±10	nA/°C	Typ
Input offset current	V_{CM} = 0 V	1	6	8	8	µA	Max
Average offset current drift	V_{CM} = 0 V			±10	±10	nA/°C	Typ
INPUT CHARACTERISTICS							
Common-mode input range		±4	±3.6	±3.5	±3.5	V	Min
Common-mode rejection ratio	V_{CM} = ± 2 V	72	67	65	65	dB	Min
Input resistance	Common-mode	5				MΩ	Typ
Input capacitance	Common-mode / differential	0.4/0.8				pF	Typ

(1) See *Maximum Die Temperature to Prevent Oscillation* section in the *Application Information* of this data sheet.

ELECTRICAL CHARACTERISTICS: V_S = ±5 V (continued)

At R_F = 249 Ω, R_L = 499 Ω, G = +2, unless otherwise noted.

PARAMETER	TEST CONDITIONS		TYP	OVER TEMPERATURE (1)				MIN/ TYP/ MAX
			+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	
OUTPUT CHARACTERISTICS								
Output voltage swing	G = +2		±4	±3.8	±3.7	±3.7	V	Min
Output current (sourcing)	R_L = 10 Ω		160	120	110	110	mA	Min
Output current (sinking)	R_L = 10 Ω		80	60	50	50	mA	Min
Output impedance	f = 1 MHz		0.1				Ω	Typ
POWER SUPPLY								
Specified operating voltage			±5	±5	±5	±5	V	Max
Maximum quiescent current			22	24	27	28	mA	Max
Minimum quiescent current			22	20	18	15	mA	Min
Power-supply rejection (+PSRR)	V_{S+} = 5.5 V to 4.5 V, V_{S-} = 5 V		85	75	70	70	dB	Min
Power-supply rejection (-PSRR)	V_{S+} = 5 V, V_{S-} = -5.5 V to -4.5 V		75	65	60	60	dB	Min
POWER-DOWN CHARACTERISTICS (THS4275 Only)								
Power-down voltage level (2)	REF = 0 V or V_{S-}	Enable		REF+1.8			V	Min
		Power down		REF+1			V	Max
	REF = V_{S+} or Floating	Enable		REF–1			V	Min
		Power down		REF–1.7			V	Max
Power-down quiescent current	PD = Ref +1.0 V,	Ref = 0 V	875	1000	1100	1200	µA	Max
	PD = Ref –1.7 V,	Ref = V_{S+}	650	800	900	1000	µA	Max
Turn-on time delay [$t_{(ON)}$]	50% of final supply current value		4				µs	Typ
Turn-off time delay [$t_{(OFF)}$]	50% of final supply current value		3				µs	Typ
Input impedance	f = 1 MHz		4				GΩ	Typ
Output impedance			200				kΩ	Typ

(2) For detailed information on the power-down circuit, see the *Power-Down* section in the *Application Information* of this data sheet.

ELECTRICAL CHARACTERISTICS: V_S = 5 V

At R_F = 249 Ω, R_L = 499 Ω, G = +2, unless otherwise noted.

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE (1)				MIN/ TYP/ MAX
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	
AC PERFORMANCE							
Small-signal bandwidth	G = 1, V_O = 100 mV_{PP}, R_L = 150 Ω	1.2				GHz	Typ
	G = –1, V_O = 100 mV_{PP}	380				MHz	Typ
	G = 2, V_O = 100 mV_{PP}	360				MHz	Typ
	G = 5, V_O = 100 mV_{PP}	80				MHz	Typ
	G = 10, V_O = 100 mV_{PP}	35				MHz	Typ
0.1-dB flat bandwidth	G = 1, V_O = 100 mV_{PP}, R_L = 150 Ω	120				MHz	Typ
Gain bandwidth product	G > 10, f = 1 MHz	350				MHz	Typ
Full-power bandwidth	G = –1, V_O = 2 V_p	60				MHz	Typ
Slew rate	G = 1, V_O = 2 V Step	700				V/μs	Typ
	G = –1, V_O = 2 V Step	750				V/μs	Typ
Settling time to 0.1%	G = –1, V_O = 2 V Step	18				ns	Typ
Settling time to 0.01%	G = –1, V_O = 2 V Step	66				ns	Typ
Harmonic distortion	G = 1, V_O = 1 V_{PP}, f = 30 MHz						
Second harmonic distortion	R_L = 150 Ω	75				dBc	Typ
	R_L = 499 Ω	72				dBc	Typ
Third harmonic distortion	R_L = 150 Ω	-70				dBc	Typ
	R_L = 499 Ω	70				dBc	Typ
Third-order intermodulation (IMD_3)	G = 2, V_O = 1 V_{PP}, R_L = 150Ω, f = 70 MHz	-65				dBc	Typ
Third-order output intercept (OIP_3)	G = 2, V_O = 1 V_{PP}, R_L = 150Ω, f = 70 MHz	32				dBm	Typ
Input voltage noise	f = 1 MHz	3				nV/√Hz	Typ
Input current noise	f = 10 MHz	3				pA/√Hz	Typ
DC PERFORMANCE							
Open-loop voltage gain (A_{OL})	V_O = ± 50 mV, R_L = 499 Ω	68	63	60	60	dB	Min
Input offset voltage	V_{CM} = V_S/2	5	10	12	12	mV	Max
Average offset voltage drift	V_{CM} = V_S/2			±10	±10	μV/°C	Typ
Input bias current	V_{CM} = V_S/2	6	15	18	18	μA	Max
Average bias current drift	V_{CM} = V_S/2			±10	±10	nA/°C	Typ
Input offset current	V_{CM} = V_S/2	1	6	8	8	μA	Max
Average offset current drift	V_{CM} = V_S/2			±10	±10	nA/°C	Typ
INPUT CHARACTERISTICS							
Common-mode input range		1/4	1.3/3.7	1.4/3.6	1.5/3.5	V	Min
Common-mode rejection ratio	V_{CM} = ± 0.5 V, V_O = 2.5 V	72	67	65	65	dB	Min
Input resistance	Common-mode	5				MΩ	Typ
Input capacitance	Common-mode / differential	0.4/0.8				pF	Typ
OUTPUT CHARACTERISTICS							
Output voltage swing	G = +2	1.2/3.8	1.4/3.6	1.5/3.5	1.5/3.5	V	Min
Output current (sourcing)	R_L = 10 Ω	120	100	90	90	mA	Min
Output current (sinking)	R_L = 10 Ω	65	50	40	40	mA	Min
Output impedance	f = 1 MHz	0.1				Ω	Typ

(1) See *Maximum Die Temperature to Prevent Oscillation* section in the *Application Information* of this data sheet.

ELECTRICAL CHARACTERISTICS: V_S = 5 V (continued)

At R_F = 249 Ω, R_L = 499 Ω, G = +2, unless otherwise noted.

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE (1)				MIN/ TYP/ MAX
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	
POWER SUPPLY							
Specified operating voltage		5	10	10	10	V	Max
Maximum quiescent current		20	22	25	27	mA	Max
Minimum quiescent current		20	18	16	14	mA	Min
Power-supply rejection (+PSRR)	V_{S+} = 5.5 V to 4.5 V, V_{S-} = 0 V	85	75	62	62	dB	Min
Power-supply rejection (-PSRR)	V_{S+} = 5 V, V_{S-} = –0.5 V to 0.5 V	75	65	60	60	dB	Min
POWER-DOWN CHARACTERISTICS (THS4275 Only)							
Power-down voltage level (2)	REF = 0 V, or V_{S-}: Enable		REF+1.8			V	Min
	REF = 0 V, or V_{S-}: Power-down		REF+1			V	Max
	REF = V_{S+} or Floating: Enable		REF–1			V	Min
	REF = V_{S+} or Floating: Power-down		REF–1.7			V	Max
Power-down quiescent current	PD = Ref +1.0 V, Ref = 0 V	650	800	900	1000	µA	Max
	PD = Ref –1.7 V, Ref = V_{S+}	650	800	900	1000	µA	Max
Turn-on time delay [$t_{(ON)}$]	50% of final value	4				µs	Typ
Turn-off time delay [$t_{(OFF)}$]	50% of final value	3				µs	Typ
Input impedance	f = 1 MHz	6				GΩ	Typ
Output impedance		100				kΩ	Typ

(2) For detail information on the power-down circuit, see the *Power-Down* section in the *Application Information* of this data sheet.

TYPICAL CHARACTERISTICS

Table of Graphs (±5 V)

		FIGURE
Small-signal unity gain frequency response		1
Small-signal frequency response		2
0.1-dB gain flatness frequency response		3
Large-signal frequency response		4
Slew rate	vs Output voltage	5
Harmonic distortion	vs Frequency	6, 7, 8, 9
Harmonic distortion	vs Output voltage swing	10, 11, 12, 13
Third-order intermodulation distortion	vs Frequency	14, 16
Third-order intercept point	vs Frequency	15, 17
Voltage and current noise	vs Frequency	18
Differential gain	vs Number of loads	19
Differential phase	vs Number of loads	20
Settling time		21
Quiescent current	vs Supply voltage	22
Output voltage	vs Load resistance	23
Frequency response	vs Capacitive load	24
Open-loop gain and phase	vs Frequency	25
Open-loop gain	vs Supply voltage	26
Rejection ratios	vs Frequency	27
Rejection ratios	vs Case temperature	28
Common-mode rejection ratio	vs Input common-mode range	29
Input offset voltage	vs Case temperature	30
Input bias and offset current	vs Case temperature	31
Small-signal transient response		32
Large-signal transient response		33
Overdrive recovery		34
Closed-loop output impedance	vs Frequency	35
Power-down quiescent current	vs Supply voltage	36
Power-down output impedance	vs Frequency	37
Turn-on and turn-off delay times		38

Table of Graphs (5 V)

		FIGURE
Small-signal unity gain frequency response		39
Small-signal frequency response		40
0.1-dB gain flatness frequency response		41
Large-signal frequency response		42
Slew rate	vs Output voltage	43
Harmonic distortion	vs Frequency	44, 45, 46, 47
Harmonic distortion	vs Output voltage swing	48, 49, 50, 51
Third-order intermodulation distortion	vs Frequency	52, 54
Third-order intercept point	vs Frequency	53, 55
Voltage and current noise	vs Frequency	56
Settling time		57
Quiescent current	vs Supply voltage	58
Output voltage	vs Load resistance	59
Frequency response	vs Capacitive load	60
Open-loop gain and phase	vs Frequency	61
Open-loop gain	vs Case temperature	62
Rejection ratios	vs Frequency	63
Rejection ratios	vs Case temperature	64
Common-mode rejection ratio	vs Input common-mode range	65
Input offset voltage	vs Case temperature	66
Input bias and offset current	vs Case temperature	67
Small-signal transient response		68
Large-signal transient response		69
Overdrive recovery		70
Closed-loop output impedance	vs Frequency	71
Power-down quiescent current	vs Supply voltage	72
Power-down output impedance	vs Frequency	73
Turn-on and turn-off delay times		74

TYPICAL CHARACTERISTICS: ±5 V

SMALL-SIGNAL UNIT GAIN FREQUENCY RESPONSE

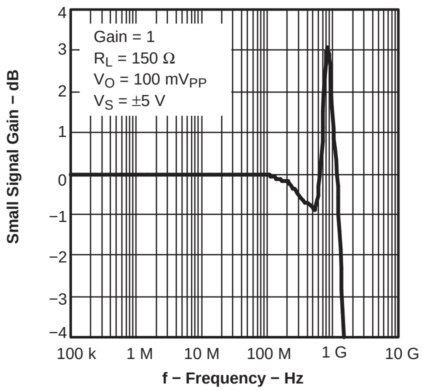


Figure 1.

SMALL-SIGNAL FREQUENCY RESPONSE

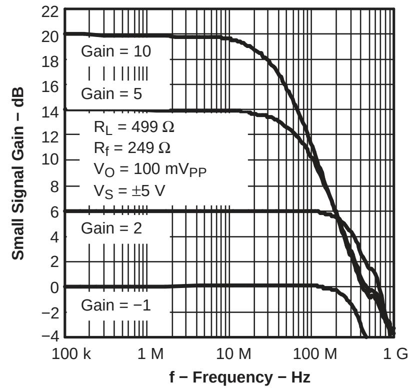


Figure 2.

0.1-dB GAIN FLATNESS FREQUENCY RESPONSE

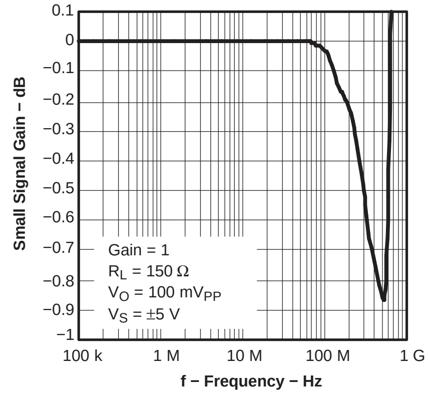


Figure 3.

LARGE-SIGNAL FREQUENCY RESPONSE

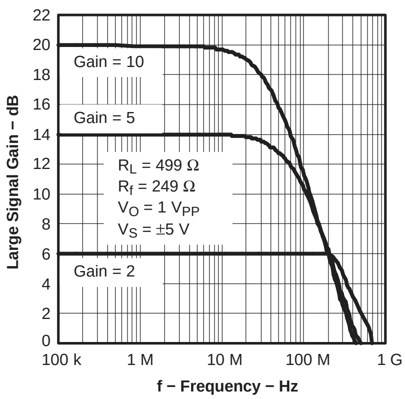


Figure 4.

SLEW RATE vs OUTPUT VOLTAGE

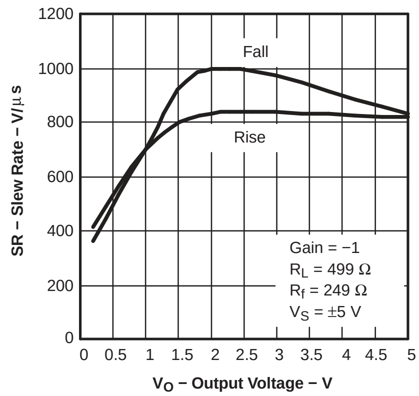


Figure 5.

HARMONIC DISTORTION vs FREQUENCY

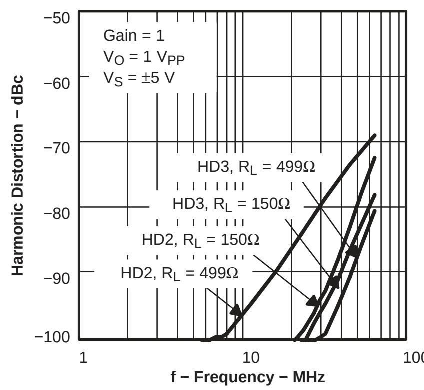


Figure 6.

HARMONIC DISTORTION vs FREQUENCY

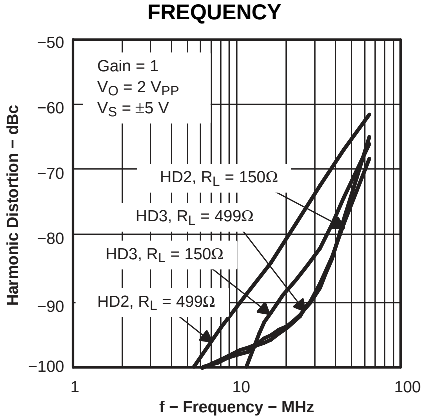


Figure 7.

HARMONIC DISTORTION vs FREQUENCY

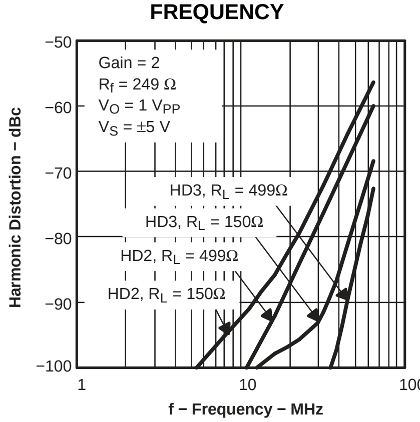


Figure 8.

HARMONIC DISTORTION vs FREQUENCY

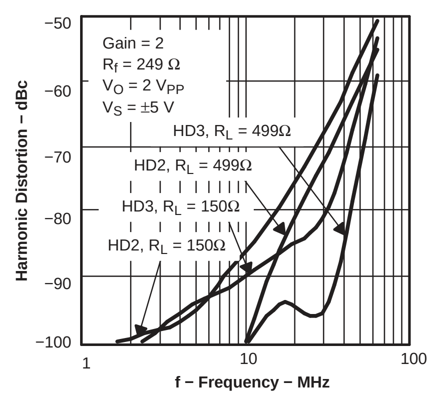


Figure 9.

TYPICAL CHARACTERISTICS: ±5 V (continued)

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

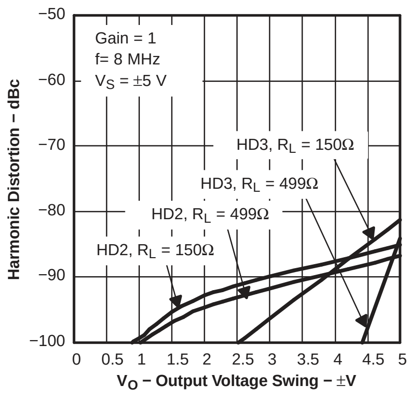


Figure 10.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

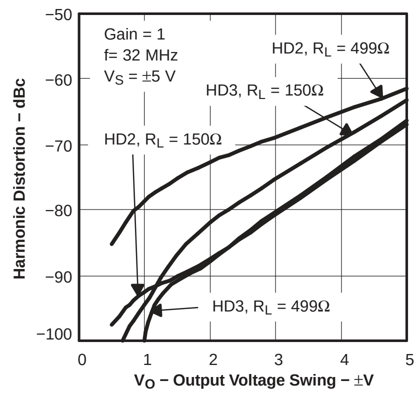


Figure 11.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

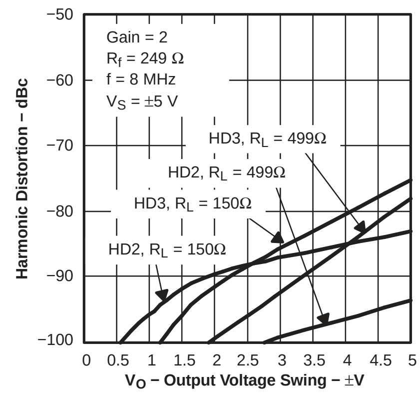


Figure 12.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

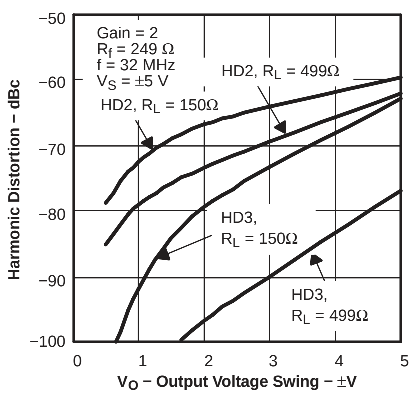


Figure 13.

THIRD-ORDER INTERMODULATION DISTORTION vs FREQUENCY

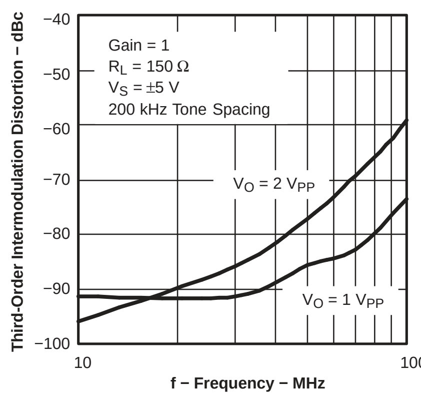


Figure 14.

THIRD-ORDER INTERMODULATION DISTORTION vs FREQUENCY

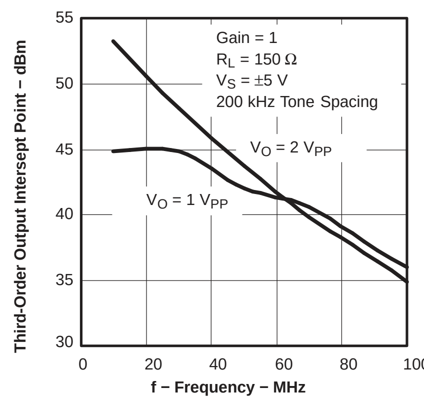


Figure 15.

THIRD-ORDER INTERMODULATION DISTORTION vs FREQUENCY

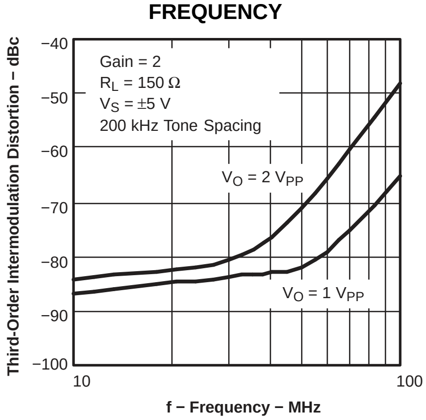


Figure 16.

THIRD-ORDER OUTPUT INTERCEPT POINT vs FREQUENCY

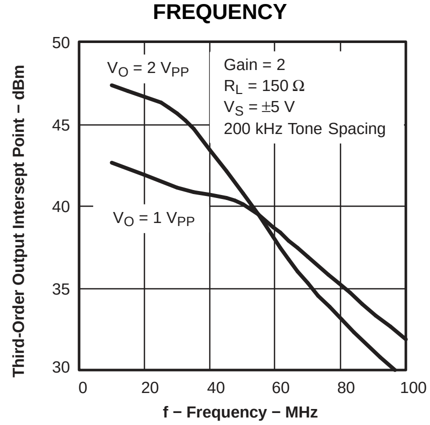


Figure 17.

VOLTAGE AND CURRENT NOISE vs FREQUENCY

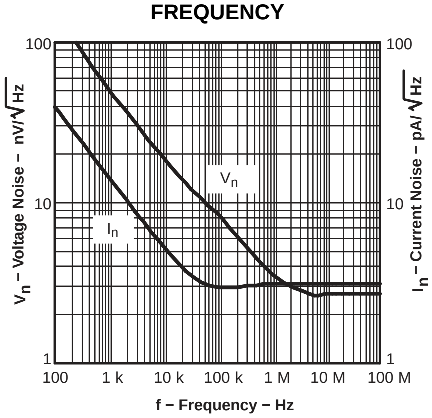


Figure 18.

TYPICAL CHARACTERISTICS: ±5 V (continued)

DIFFERENTIAL GAIN vs NUMBER OF LOADS

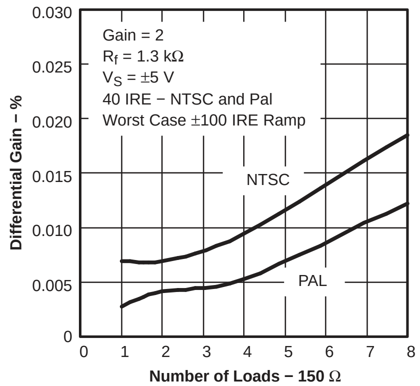


Figure 19.

DIFFERENTIAL PHASE vs NUMBER OF LOADS

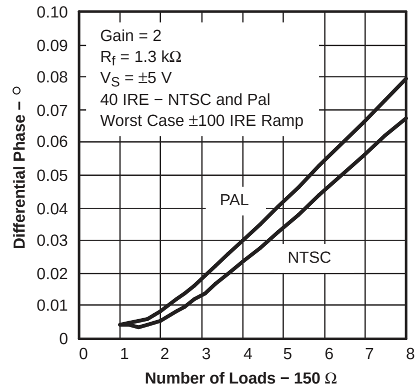


Figure 20.

SETTLING TIME

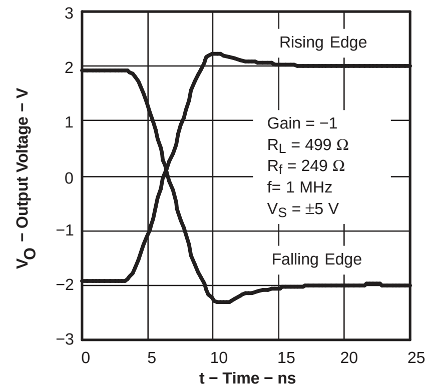


Figure 21.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

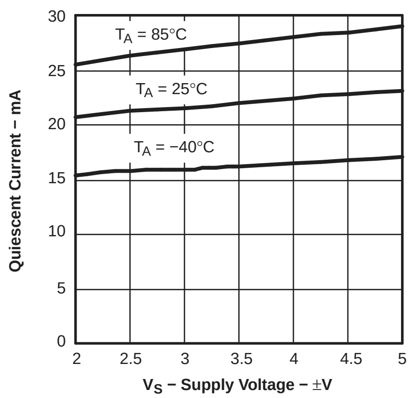


Figure 22.

OUTPUT VOLTAGE vs LOAD RESISTANCE

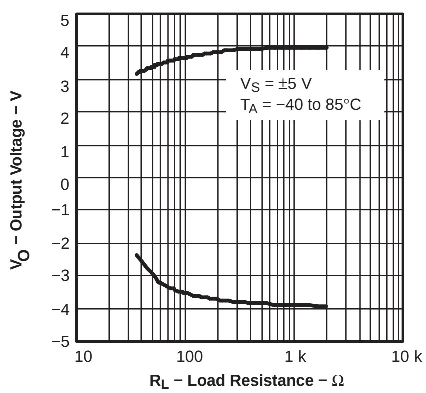


Figure 23.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

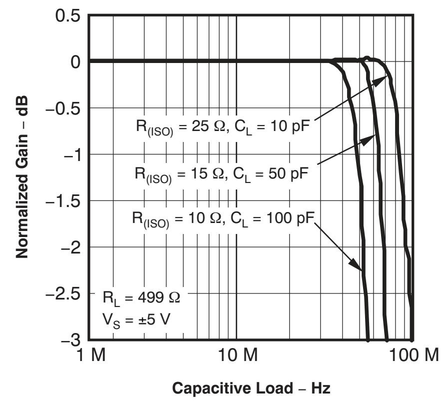


Figure 24.

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

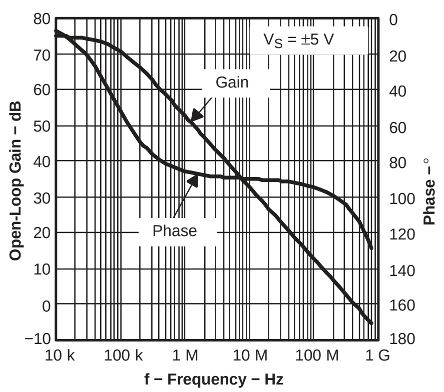


Figure 25.

OPEN-LOOP GAIN vs SUPPLY VOLTAGE

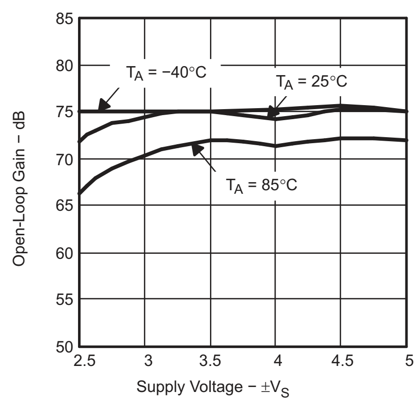


Figure 26.

REJECTION RATIOS vs FREQUENCY

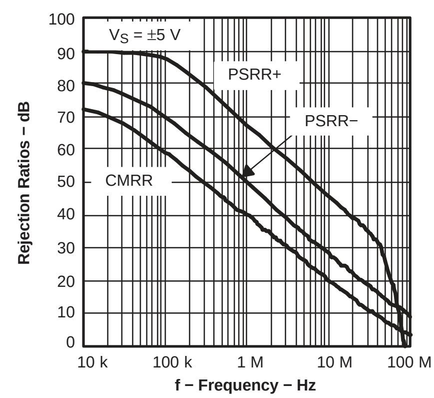


Figure 27.

TYPICAL CHARACTERISTICS: ±5 V (continued)

REJECTION RATIOS vs FREQUENCY

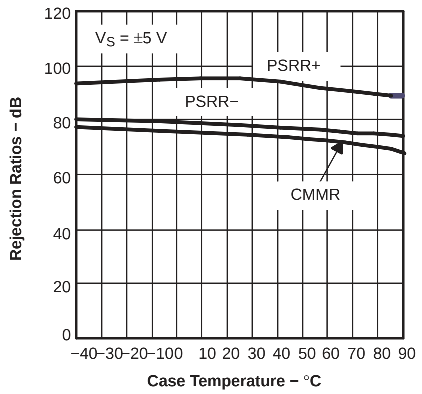


Figure 28.

COMMON-MODE REJECTION RATIOS vs INPUT COMMON-MODE RANGE

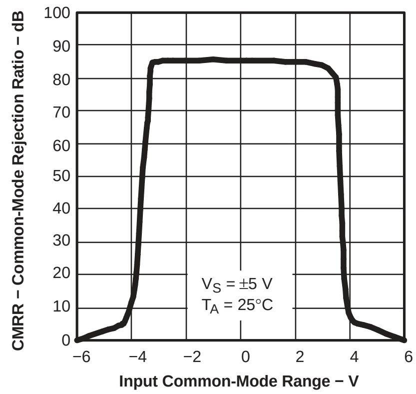


Figure 29.

INPUT OFFSET VOLTAGE vs CASE TEMPERATURE

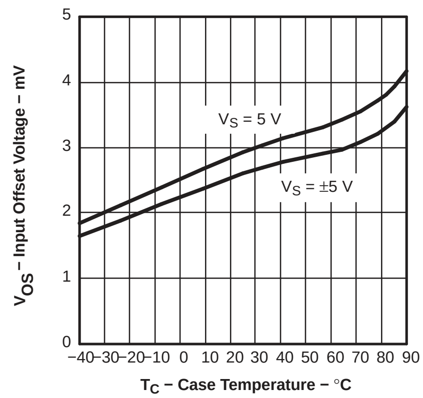


Figure 30.

INPUT BIAS AND OFFSET CURRENT vs CASE TEMPERATURE

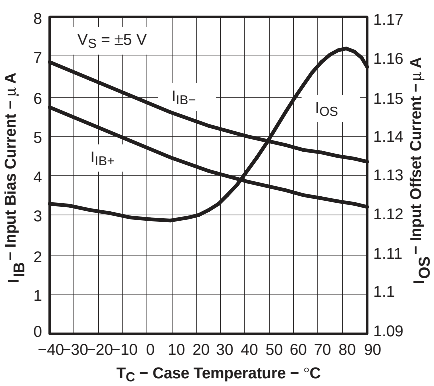


Figure 31.

SMALL-SIGNAL TRANSIENT RESPONSE

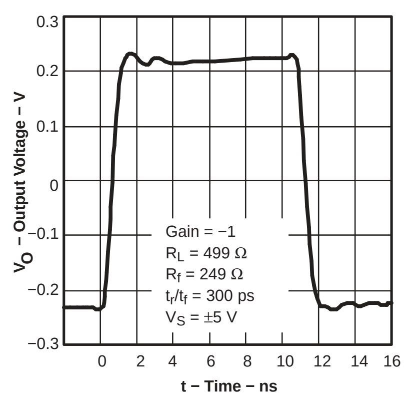


Figure 32.

LARGE-SIGNAL TRANSIENT RESPONSE

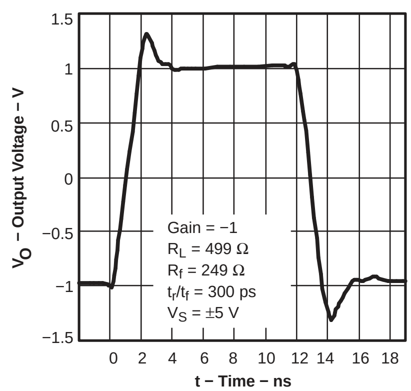


Figure 33.

OVERDRIVE RECOVERY

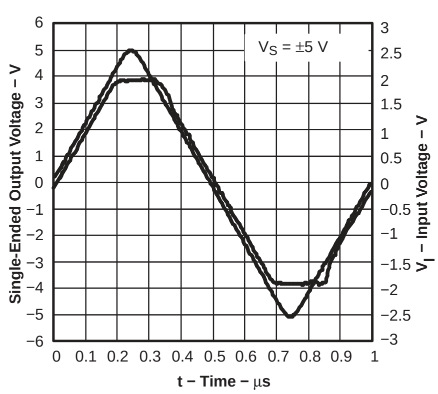


Figure 34.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

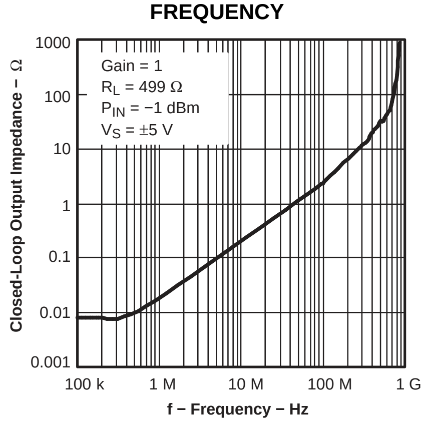


Figure 35.

POWER-DOWN QUIESCENT CURRENT vs SUPPLY VOLTAGE

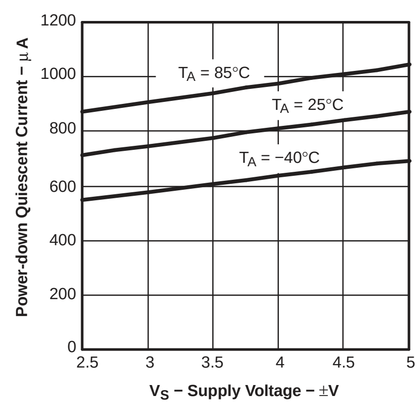


Figure 36.

TYPICAL CHARACTERISTICS: ±5 V (continued)

POWER-DOWN OUTPUT IMPEDANCE vs FREQUENCY

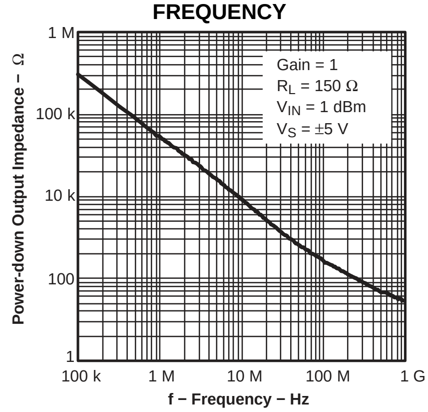


Figure 37.

TYPICAL CHARACTERISTICS: 5 V

SMALL-SIGNAL UNIT GAIN FREQUENCY RESPONSE

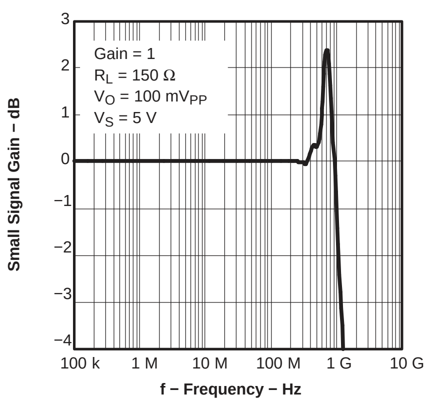


Figure 39.

SMALL-SIGNAL UNIT GAIN FREQUENCY RESPONSE

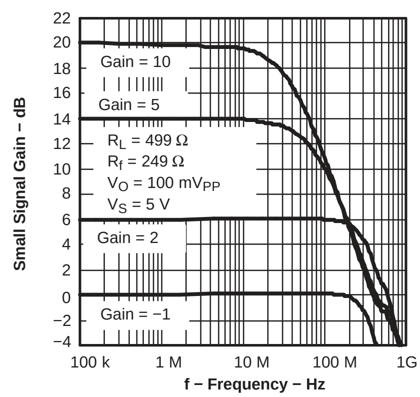


Figure 40.

0.1-dB GAIN FLTANESS FREQUENCY RESPONSE

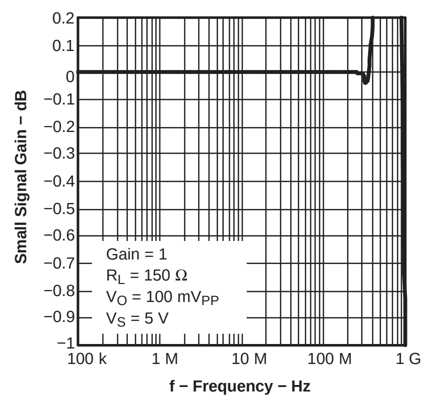


Figure 41.

LARGE-SIGNAL FREQUENCY RESPONSE

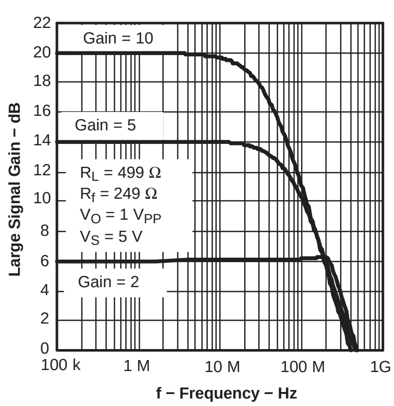


Figure 42.

SLEW RATE vs FREQUENCY

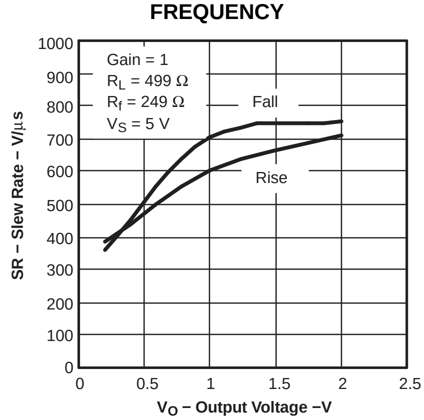


Figure 43.

HARMONIC DISTORTION DISTORTION vs FREQUENCY

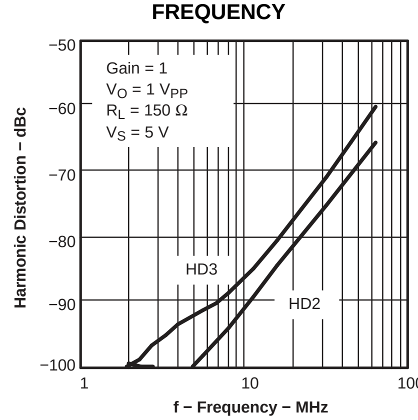


Figure 44.

TYPICAL CHARACTERISTICS: 5 V (continued)

HARMONIC DISTORTION vs FREQUENCY

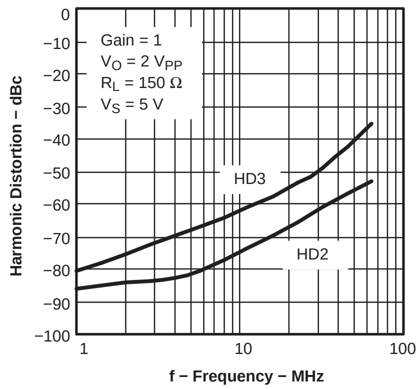


Figure 45.

HARMONIC DISTORTION vs FREQUENCY

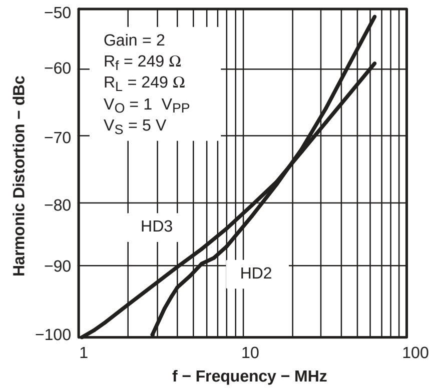


Figure 46.

HARMONIC DISTORTION vs FREQUENCY

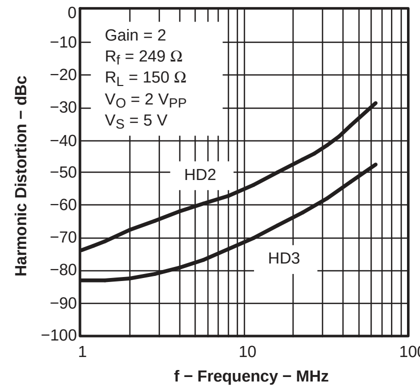


Figure 47.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

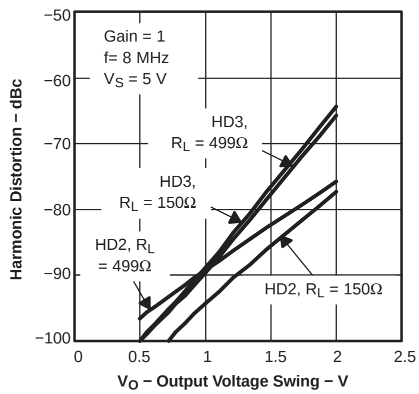


Figure 48.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

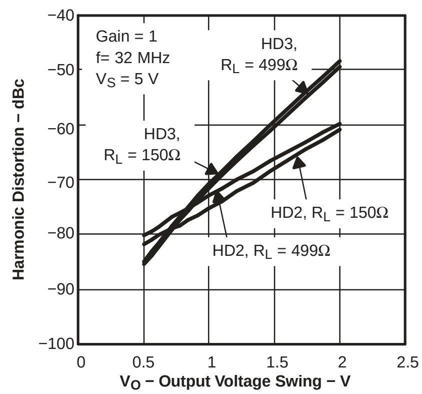


Figure 49.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

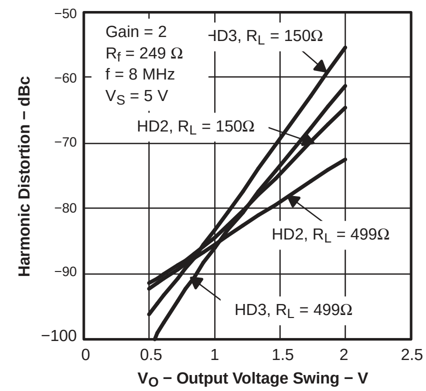


Figure 50.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

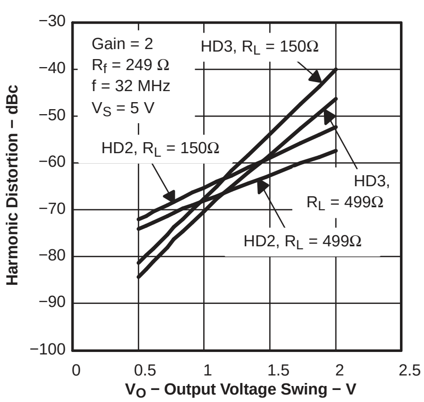


Figure 51.

THIRD-ORDER INTERMODULATION DISTORTION vs FREQUENCY

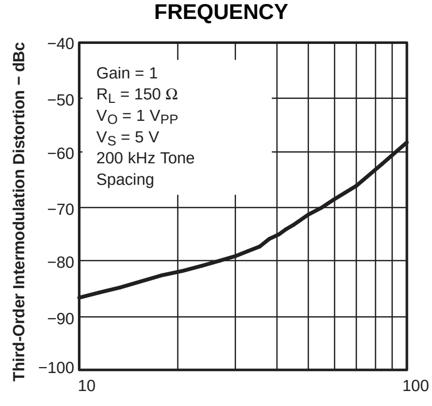


Figure 52.

THIRD-ORDER OUTPUT INTERCEPT POINT vs FREQUENCY

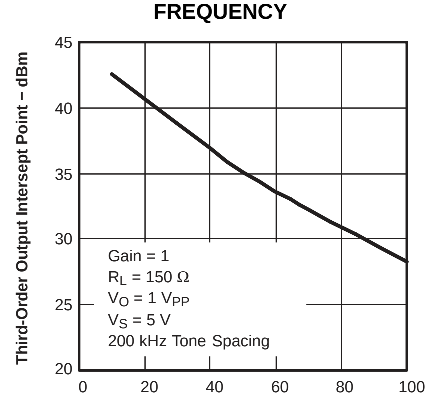


Figure 53.

TYPICAL CHARACTERISTICS: 5 V (continued)

THIRD-ORDER INTERMODULATION DISTORTION vs FREQUENCY

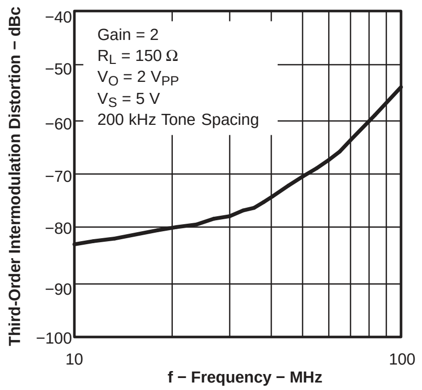


Figure 54.

THIRD-ORDER OUTPUT INTERCEPT POINT vs FREQUENCY

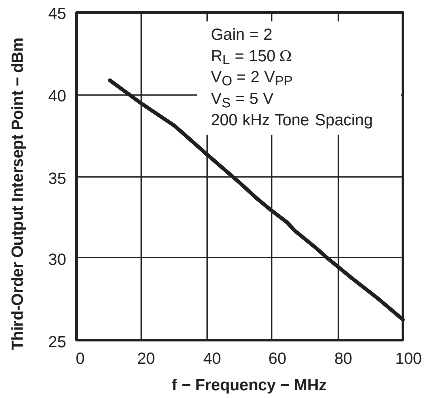


Figure 55.

VOLTAGE AND CURRENT NOISE vs FREQUENCY

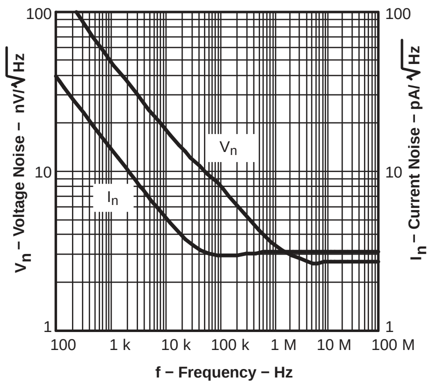


Figure 56.

SETTLING TIME

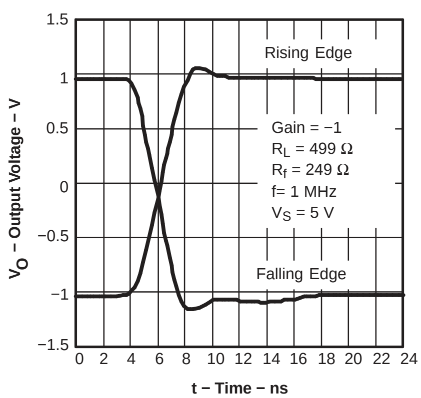


Figure 57.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

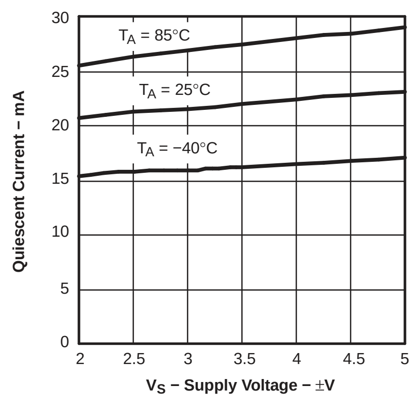


Figure 58.

OUTPUT VOLTAGE vs LOAD RESISTANCE

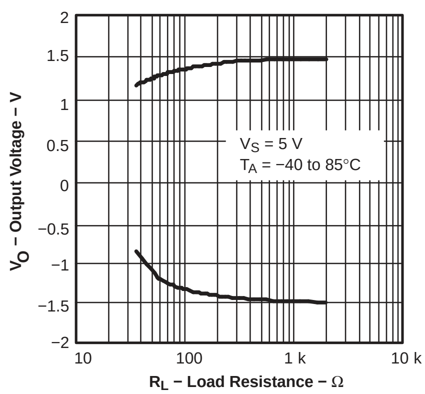


Figure 59.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

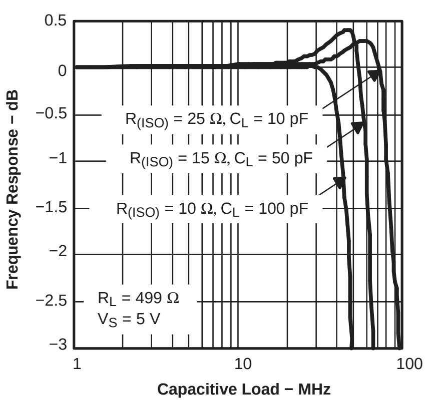


Figure 60.

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

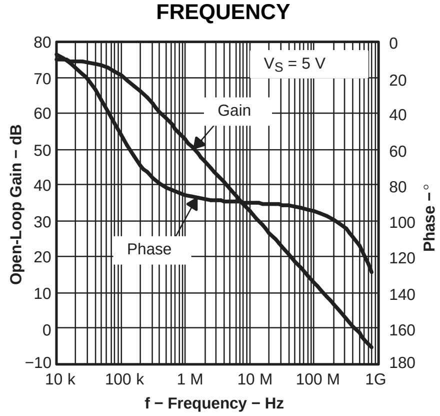


Figure 61.

OPEN-LOOP GAIN vs CASE TEMPERATURE

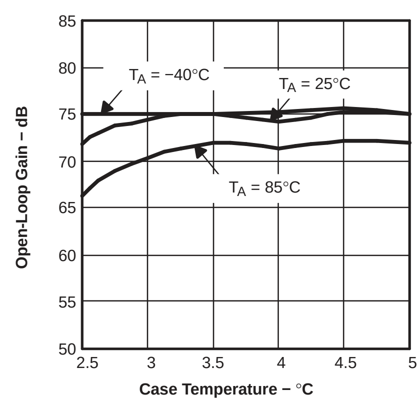


Figure 62.

TYPICAL CHARACTERISTICS: 5 V (continued)

REJECTION RATIOS vs FREQUENCY

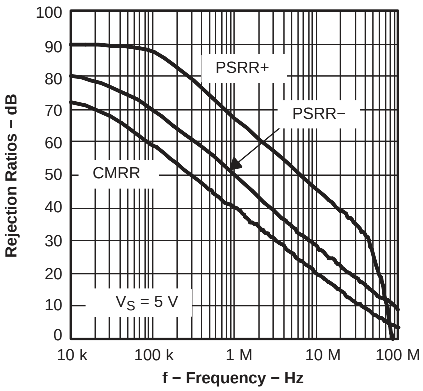


Figure 63.

REJECTION RATIOS vs CASE TEMPERATURE

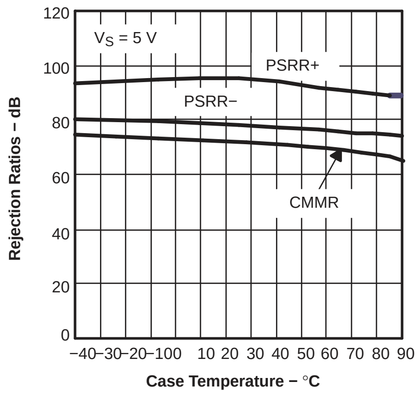


Figure 64.

COMMON-MODE REJECTION RATIO vs INPUT COMMON-MODE RANGE

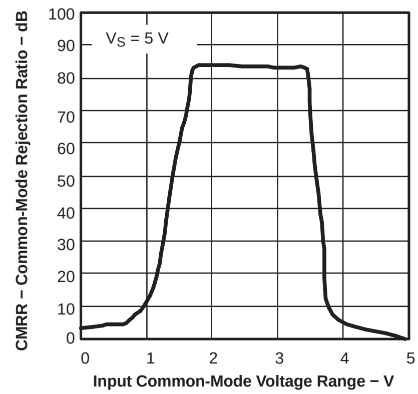


Figure 65.

INPUT OFFSET VOLTAGE vs CASE TEMPERATURE

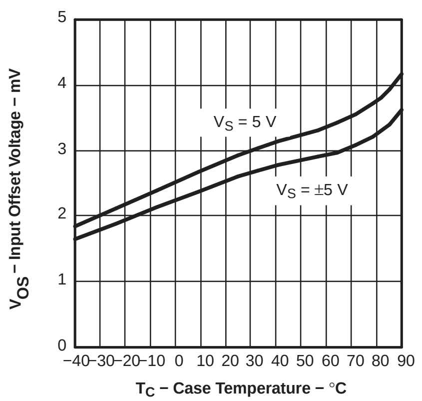


Figure 66.

INPUT BIAS AND OFFSET CURRENT vs CASE TEMPERATURE

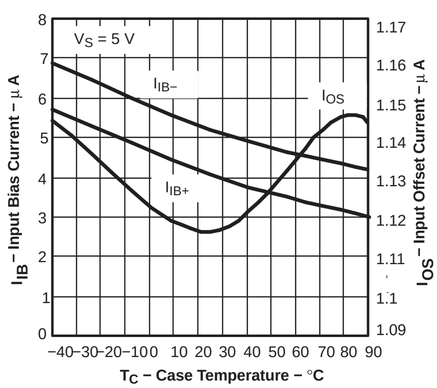


Figure 67.

SMALL-SIGNAL TRANSIENT RESPONSE

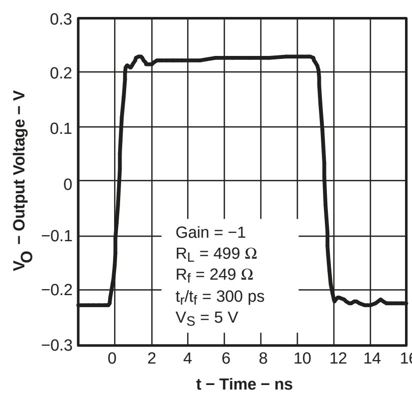


Figure 68.

LARGE-SIGNAL TRANSIENT RESPONSE

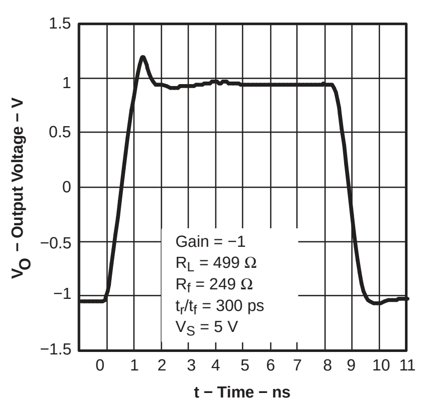


Figure 69.

OVERDRIVE RECOVERY

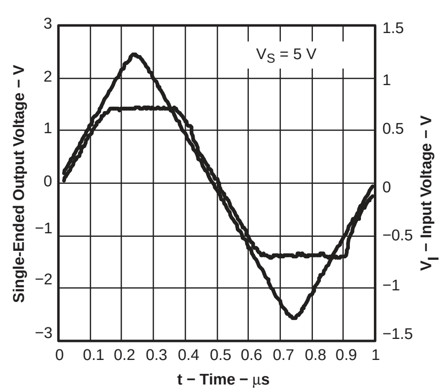


Figure 70.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

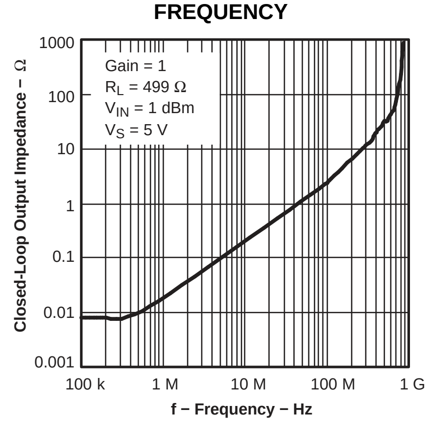


Figure 71.

TYPICAL CHARACTERISTICS: 5 V (continued)

POWER-DOWN QUIESCENT CURRENT vs SUPPLY VOLTAGE

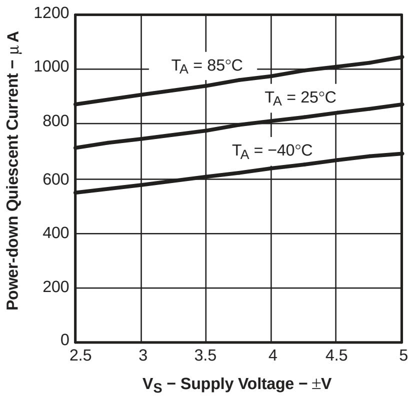


Figure 72.

POWER-DOWN OUTPUT IMPEDANCE vs FREQUENCY

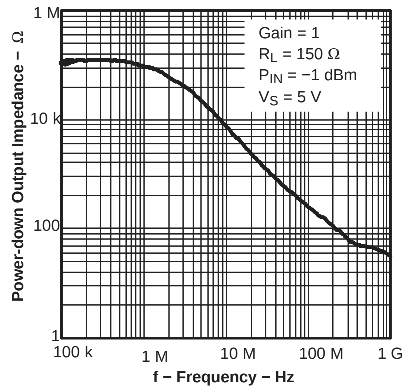


Figure 73.

TURN-ON AND TURN-OFF TIME vs DELAY TIME

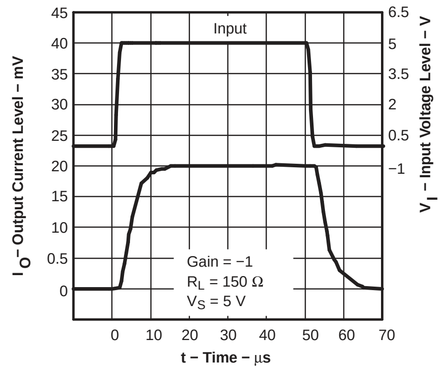


Figure 74.

APPLICATION INFORMATION

MAXIMUM DIE TEMPERATURE TO PREVENT OSCILLATION

The THS4271 and THS4275 may have low-level oscillation when the die temperature (also called *junction temperature*) exceeds +60°C.

The oscillation is a result of the internal design of the bias circuit, and external configuration is not expected to mitigate or reduce the problem. This problem occurs randomly because of normal process variations and normal testing cannot identify problem units.

The THS4211 and THS4215 are recommended replacement devices.

The die temperature depends on the power dissipation and the thermal resistance of the device.

The die temperature can be approximated with the following formula:

$$\text{Die Temperature} = P_{DISS} \times \theta_{JA} + T_A$$

Where:

$$P_{DISS} = (V_{S+} - V_{S-}) \times (I_Q + I_{LOAD}) - (V_{OUT} \times I_{LOAD})$$

Table 1 shows the estimated the maximum ambient temperature (T_A max) in degrees Celsius for each package option of the THS4271 and THS4275 using the thermal dissipation rating given in the Dissipation Ratings table for a JEDEC standard High-K test PCB. For each case shown, R_L = 499 Ω to ground and the quiescent current = 27 mA (the maximum over the 0°C to +70°C temperature range). The last entry for each package option (shaded cells) lists the worst-case scenario where the power supply is single-supply 10 V and ground and the output voltage is 5 V DC.

Table 1. Estimated Maximum Ambient Temperature Per Package Option

PACKAGE DEVICE	V_{S+}	V_{S-}	V_{OUT}	θ_{JA}	T_A max
SOIC	5 V	–5 V	0 V	97.5°C/W	33.7°C
THS4271D			2 V_{PP}		32.4°C
THS4271DR			4 V_{PP}		31.3°C
THS4275D			6 V_{PP}		30.4°C
THS4275DR			8 V_{PP}		29.7°C
Worst Case	10 V	0 V	5 DC		28.8°C
VSON	5 V	–5 V	0 V	45.8°C/W	47.6°C
THS4271DRBT			2 V_{PP}		47.0°C
THS4271DRBR			4 V_{PP}		46.5°C
THS4275DRBT			6 V_{PP}		46.1°C
THS4275DRBR			8 V_{PP}		45.8°C
Worst Case	10 V	0 V	5 DC		45.3°C
PowerPad™ MSOP	5 V	–5 V	0 V	58.4°C/W	44.2°C
THS4271DGN			2 V_{PP}		43.5°C
THS4271DGNR			4 V_{PP}		42.8°C
THS4275DGN			6 V_{PP}		42.3°C
THS4275DGNR			8 V_{PP}		41.9°C
Worst Case	10 V	0 V	5 DC		41.3°C
MSOP	5 V	–5 V	0 V	260°C/W	–10.2°C
THS4271DGK			2 V_{PP}		–13.6°C
THS4271DGKR			4 V_{PP}		–16.5°C
THS4275DGK			6 V_{PP}		–18.9°C
THS4275DGKR			8 V_{PP}		–20.8°C
Worst Case	10 V	0 V	5 DC		–23.2°C

HIGH-SPEED OPERATIONAL AMPLIFIERS

The THS4271 and the THS4275 operational amplifiers set new performance levels, combining low distortion, high slew rates, low noise, and a unity-gain bandwidth in excess of 1 GHz. To achieve the full performance of the amplifier, careful attention must be paid to printed-circuit board (PCB) layout and component selection.

The THS4275 provides a power-down mode, providing the ability to save power when the amplifier is inactive. A reference pin is provided to allow the user the flexibility to control the threshold levels of the power-down control pin.

Applications Section Contents

- Wideband, Noninverting Operation
- Wideband, Inverting Gain Operation
- Single-Supply Operation
- Saving Power with Power-Down Functionality and Setting Threshold Levels with the Reference Pin
- Power Supply Decoupling Techniques and Recommendations
- Using the THS4271 as a DAC Output Buffer
- Driving an ADC With the THS4271
- Active Filtering With the THS4271
- Building a Low-Noise Receiver with the THS4271
- Linearity: Definitions, Terminology, Circuit Techniques and Design Tradeoffs
- An Abbreviated Analysis of Noise in Amplifiers
- Driving Capacitive Loads
- Printed Circuit Board Layout Techniques for Optimal Performance
- Power Dissipation and Thermal Considerations
- Performance vs Package Options
- Evaluation Fixtures, Spice Models, and Applications Support
- Additional Reference Material
- Mechanical Package Drawings

WIDEBAND, NONINVERTING OPERATION

The THS4271 and the THS4275 are unity gain stable, 1.4-GHz voltage-feedback operational amplifiers, with and without power-down capability, designed to operate from a single 5-V to 15-V power supply.

Figure 75 is the noninverting gain configuration of 2 V/V used to demonstrate the typical performance curves. Most of the curves were characterized using signal sources with 50-Ω source impedance, and with measurement equipment presenting a 50-Ω load impedance. In Figure 75, the 49.9-Ω shunt resistor at the V_{IN} terminal matches the source impedance of the test generator. The total 499-Ω load at the output, combined with the 498-Ω total feedback network load, presents the THS4271 and THS4275 with an effective output load of 249 Ω for the circuit of Figure 75.

Voltage feedback amplifiers, unlike current feedback designs, can use a wide range of resistors values to set their gain with minimal impact on their stability and frequency response. Larger-valued resistors decrease the loading effect of the feedback network on the output of the amplifier, but this enhancement comes at the expense of additional noise and potentially lower bandwidth. Feedback resistor values between 249 Ω and 1 kΩ are recommended for most situations.

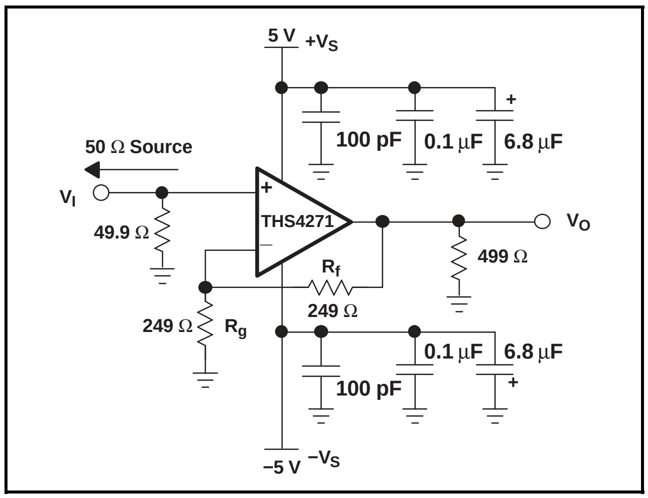


Figure 75. Wideband, Noninverting Gain Configuration

WIDEBAND, INVERTING GAIN OPERATION

Since the THS4271 and THS4275 are general-purpose, wideband voltage-feedback amplifiers, several familiar operational amplifier applications circuits are available to the designer. Figure 76 shows a typical inverting configuration where the input and output impedances and noise gain from Figure 75 are retained in an inverting circuit configuration. Inverting operation is one of the more common requirements and offers several performance benefits. The inverting configuration shows improved slew rates and distortion due to the pseudo-static voltage maintained on the inverting input.

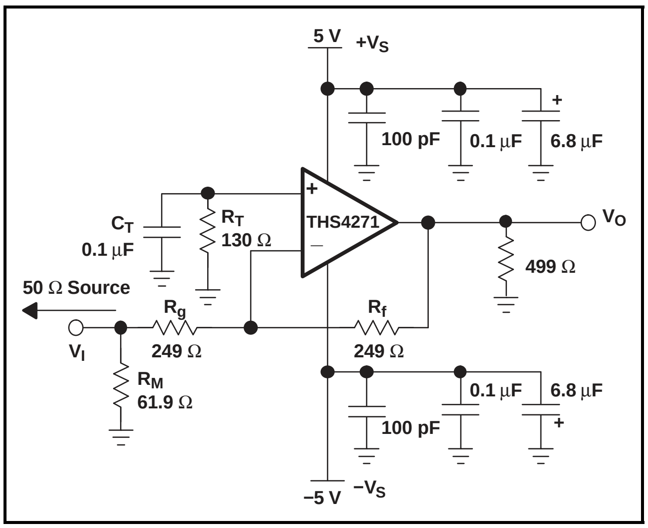


Figure 76. Wideband, Inverting Gain Configuration

In the inverting configuration, some key design considerations must be noted. One is that the gain resistor (R_g) becomes part of the signal channel input impedance. If the input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PCB trace, or other transmission line conductors), R_g may be set equal to the required termination value and R_f adjusted to give the desired gain. However, care must be taken when dealing with low inverting gains, as the resulting feedback resistor value can present a significant load to the amplifier output. For an inverting gain of 2, setting R_g to 49.9 Ω for input matching eliminates the need for R_M but requires a 100-Ω feedback resistor. This has an advantage of the noise gain becoming equal to 2 for a 50-Ω source impedance—the same as the noninverting circuit in Figure 75. However, the amplifier output now sees the 100-Ω feedback resistor in parallel with the external load. To eliminate this excessive loading, it is preferable to increase both R_g and R_f, values, as shown in Figure 76, and then achieve the input matching impedance with a third resistor (R_M) to ground. The total input impedance becomes the parallel combination of R_g and R_M.

The next major consideration is that the signal source impedance becomes part of the noise gain equation and hence influences the bandwidth. For example, the R_M value combines in parallel with the external 50-Ω source impedance (at high frequencies), yielding an effective source impedance of 50 Ω || 61.9Ω = 27.7 Ω. This impedance is then added in series with R_g for calculating the noise gain. The result is 1.9 for Figure 76, as opposed to the 1.8 if R_M is eliminated. The bandwidth is lower for the gain of –2 circuit, Figure 76 (NG=+1.9), than for the gain of +2 circuit in Figure 75.

The last major consideration in inverting amplifier design is setting the bias current cancellation resistor on the noninverting input. If the resistance is set equal to the total dc resistance looking out of the inverting terminal, the output dc error, due to the input bias currents, is reduced to (input offset current) multiplied by R_f in Figure 76, the dc source impedance looking out of the inverting terminal is 249 Ω || (249Ω + 27.7 Ω) = 130 Ω. To reduce the additional high-frequency noise introduced by the resistor at the noninverting input, and power-supply feedback, R_T is bypassed with a capacitor to ground.

SINGLE-SUPPLY OPERATION

The THS4271 is designed to operate from a single 5-V to 15-V power supply. When operating from a single power supply, care must be taken to ensure the input signal and amplifier are biased appropriately to allow for the maximum output voltage swing. The circuits shown in Figure 77 demonstrate methods to configure an amplifier in a manner conducive for single-supply operation.

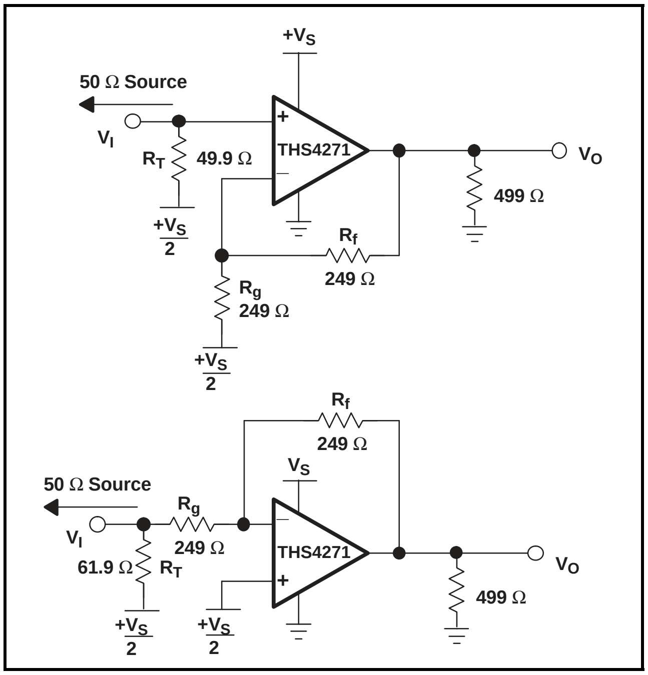


Figure 77. DC-Coupled Single-Supply Operation

Saving Power with Power-Down Functionality and Setting Threshold Levels with the Reference Pin

The THS4275 features a power-down pin ($\overline{PD}$) which lowers the quiescent current from 22 mA down to 700 µA, ideal for reducing system power.

The power-down pin of the amplifier defaults to the positive supply voltage in the absence of an applied voltage, putting the amplifier in the power-on mode of operation. To turn off the amplifier in an effort to conserve power, the power-down pin can be driven towards the negative rail. The threshold voltages for power-on and power-down are relative to the supply rails and given in the specification tables. Above the *Enable Threshold Voltage*, the device is on. Below the *Disable Threshold Voltage*, the device is off. Behavior in between these threshold voltages is not specified.

Note that this power-down functionality is just that; the amplifier consumes less power in power-down mode. The power-down mode is not intended to provide a high-impedance output. In other words, the power-down functionality is not intended to allow use as a 3-state bus driver. When in power-down mode, the impedance looking back into the output of the amplifier is dominated by the feedback and gain setting resistors, but the output impedance of the device itself varies depending on the voltage applied to the outputs.

The time delays associated with turning the device on and off are specified as the time it takes for the amplifier to reach 50% of the nominal quiescent current. The time delays are on the order of microseconds because the amplifier moves in and out of the linear mode of operation in these transitions.

Power-Down Reference Pin Operation

In addition to the power-down pin, the THS4275 also features a reference pin (REF) which allows the user to control the enable or disable power-down voltage levels applied to the $\overline{PD}$ pin. Operation of the reference pin as it relates to the power-down pin is described below.

In most split-supply applications, the reference pin is connected to ground. In some cases, the user may want to connect it to the negative or positive supply rail. In either case, the user needs to be aware of the voltage level thresholds that apply to the power-down pin. Table 2 and Table 3 show examples and illustrate the relationship between the reference voltage and the power-down thresholds.

Table 2. Power-Down Threshold Voltage Levels (REF ≤ MIDRAIL)

SUPPLY VOLTAGE (V)	REFERENCE PIN VOLTAGE (V)	ENABLE LEVEL (V)	DISABLE LEVEL (V)
±5	GND	≥ 1.8	≤ 1
	-2.5	≥ -0.7	≤ –1.5
	-5	≥ -3.2	≤ -4
5	GND	≥ 1.8	≤ 1
	1	≥ 2.8	≤ 2
	2.5	≥ 4.3	≤ 3.5

In Table 2, the threshold levels are derived by the following equations:

REF + 1.8 V for enable

REF + 1 V for disable

Note that in order to maintain these threshold levels, the reference pin can be any voltage between VS_ or GND up to Vs/2 (midrail).

Table 3. Power-Down Threshold Voltage Levels (REF > MIDRAIL)

SUPPLY VOLTAGE (V)	REFERENCE PIN VOLTAGE (V)	ENABLE LEVEL (V)	DISABLE LEVEL (V)
±5	Floating or 5	≥ 4	≤ 3.3
	2.5	≥ 1.5	≤ 0.8
	1	≥ 0	≤ -0.7
5	Floating or 5	≥ 3.3	≤ 3.3
	4	≥ 3	≤ 2.3
	3.5	≥ 2.5	≤ 1.8

In Table 3, the threshold levels are derived by the following equations:

REF - 1 V for enable

REF - 1.7 V for disable

Note that in order to maintain these threshold levels, the reference pin can be any voltage between (V_S+/2) + 1 V to V_S+.

The recommended mode of operation is to tie the reference pin to midrail, thus setting the threshold levels to midrail +1 V and midrail +1.8 V.

NO. OF CHANNELS	PACKAGES
Single (8-pin)	THS4275D, THS4275DGN, and THS4275DRB

Power-Supply Decoupling Techniques and Recommendations

Power-supply decoupling is a critical aspect of any high-performance amplifier design process. Careful decoupling provides higher quality ac performance (most notably improved distortion performance). The following guidelines ensure the highest level of performance.

1. Place decoupling capacitors as close to the power-supply inputs as possible, with the goal of minimizing the inductance of the path from ground to the power supply.
2. Placement priority should put the smallest valued capacitors closest to the device.
3. Use of solid power and ground planes is recommended to reduce the inductance along power-supply return current paths, with the exception of the areas underneath the input and output pins.
4. Recommended values for power-supply decoupling include a bulk decoupling capacitor (6.8 µF to 22 µF), a mid-range decoupling capacitor (0.1 µF) and a high frequency decoupling capacitor (1000 pF) for each supply. A 100-pF capacitor can be used across the supplies as well for extremely high-frequency return currents, but often is not required.

APPLICATION CIRCUITS

Driving an Analog-to-Digital Converter With the THS4271

The THS4271 can be used to drive high-performance analog-to-digital converters. Two example circuits are presented below.

The first circuit uses a wideband transformer to convert a single-ended input signal into a differential signal. The differential signal is then amplified and filtered by two THS4271 amplifiers. This circuit provides low intermodulation distortion, suppressed even-order distortion, 14 dB of voltage gain, a 50-Ω input impedance, and a single-pole filter at 100 MHz. For applications without signal content at dc, this method of driving ADCs can be very useful. Where dc information content is required, the THS4500 family of fully differential amplifiers may be applicable.

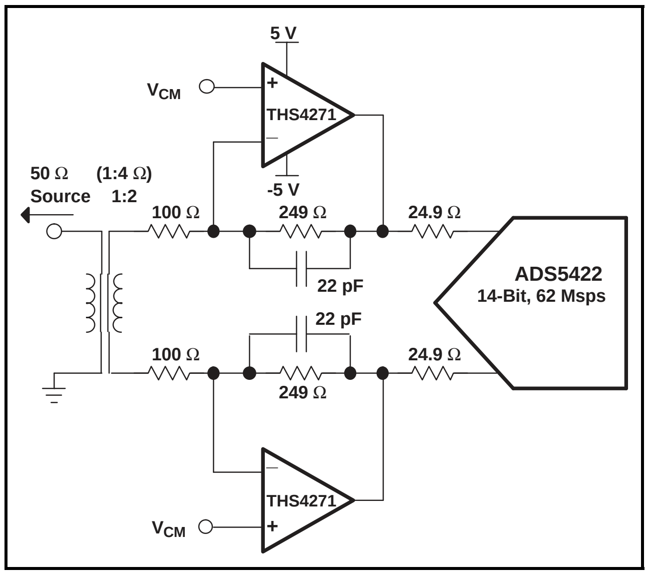
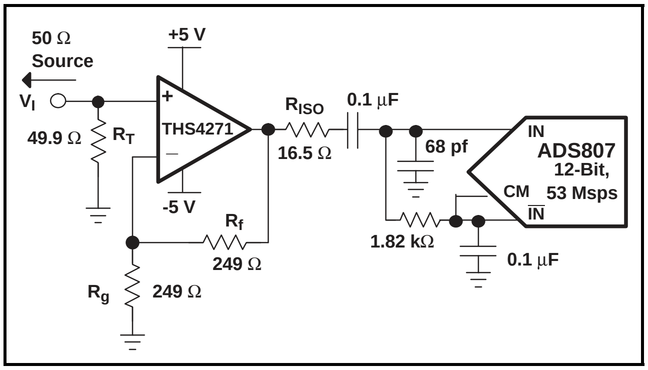


Figure 78. A Linear, Low-Noise, High-Gain ADC Preamplifier

The second circuit depicts single-ended ADC drive. While not recommended for optimum performance using converters with differential inputs, satisfactory performance can sometimes be achieved with single-ended input drive. An example circuit is shown here for reference.



For best performance, high-speed ADCs should be driven differentially. See the THS4500 family of devices for more information.

Figure 79. Driving an ADC With a Single-Ended Input

Using the THS4271 as a DAC Output Buffer

Two example circuits are presented here showing the THS4271 buffering the output of a digital-to-analog converter. The first circuit performs a differential to single-ended conversion with the THS4271 configured as a difference amplifier. The difference amplifier can double as the termination mechanism for the DAC outputs as well.

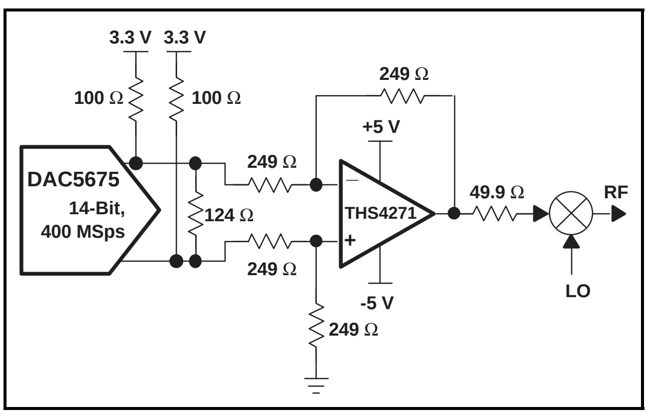


Figure 80. Differential to Single-Ended Conversion of a High-Speed DAC Output

For cases where a differential signaling path is desirable, a pair of THS4271 amplifiers can be used as output buffers. The circuit depicts differential drive into a mixer IF inputs, coupled with additional signal gain and filtering.

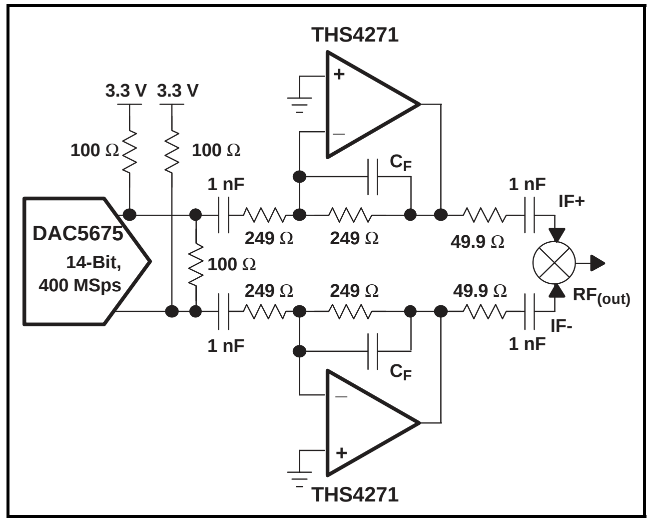


Figure 81. Differential Mixer Drive Circuit Using the DAC5675 and the THS4271

Active Filtering With the THS4271

High-frequency active filtering with the THS4271 is achievable due to the amplifier high slew-rate, wide bandwidth, and voltage-feedback architecture. Several options are available for high-pass, low-pass, bandpass, and bandstop filters of varying orders. A simple two-pole low pass filter is presented here as an example, with two poles at 100 MHz.

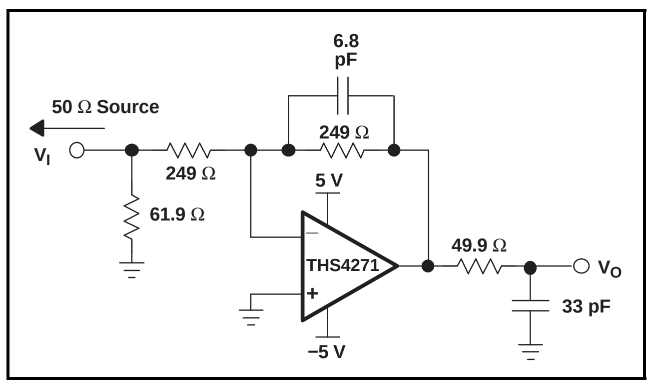


Figure 82. A Two-Pole Active Filter With Two Poles Between 90 MHz and 100 MHz

A Low-Noise Receiver With the THS4271

A combination of two THS4271 amplifiers can create a high-speed, low-distortion, low-noise differential receiver circuit as depicted in Figure 83. With both amplifiers operating in the noninverting mode of operation, the circuit presents a high load impedance to the source. The designer has the option of controlling the impedance through termination resistors if a matched termination impedance is desired.

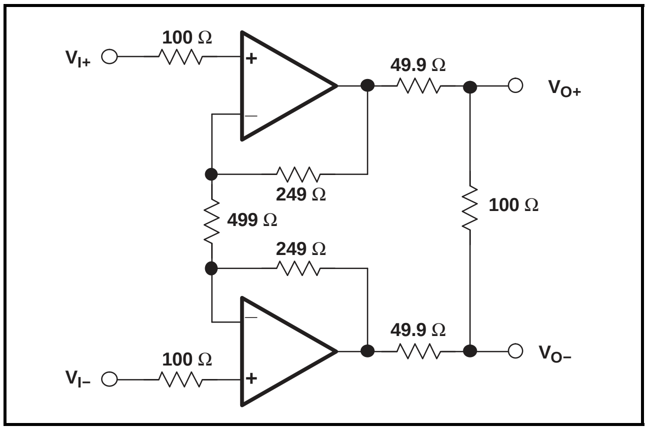


Figure 83. A High Input Impedance, Low-Noise, Differential Receiver

A modification on this circuit to include a difference amplifier turns this circuit into a high-speed instrumentation amplifier, as shown in Figure 84. Equation 1 calculates the output voltage for this circuit.

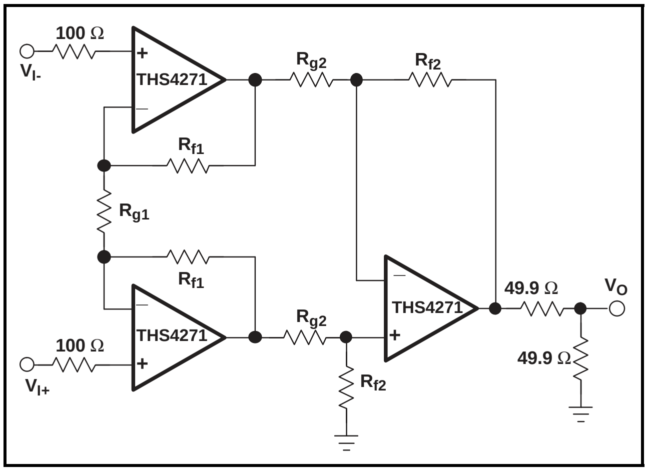


Figure 84. A High-Speed Instrumentation Amplifier

$$V_O = \frac{1}{2}\left(1 + \frac{2R_{f1}}{R_{g1}}\right)\left(V_{i+} - V_{i-}\right)\left(\frac{R_{f2}}{R_{g2}}\right) \quad (1)$$

THEORY AND GUIDELINES

Distortion Performance

The THS4271 provides excellent distortion performance into a 150-Ω load. Relative to alternative solutions, it provides exceptional performance into lighter loads, as well as exceptional performance on a single 5-V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the second harmonic dominates the total harmonic distortion with a negligible third harmonic component. Focusing then on the second harmonic, increasing the load impedance improves distortion directly. The total load includes the feedback network; in the noninverting configuration (Figure 75) this is the sum of R_f and R_g, while in the inverting configuration (Figure 76), only R_f needs to be included in parallel with the actual load.

LINEARITY: DEFINITIONS, TERMINOLOGY, CIRCUIT TECHNIQUES, AND DESIGN TRADEOFFS

The THS4271 features excellent distortion performance for monolithic operational amplifiers. This section focuses on the fundamentals of distortion, circuit techniques for reducing nonlinearity, and methods for equating distortion of operational amplifiers to desired linearity specifications in RF receiver chains.

Amplifiers are generally thought of as *linear* devices. The output of an amplifier is a linearly-scaled version of the input signal applied to it. However, amplifier transfer functions are nonlinear. Minimizing amplifier nonlinearity is a primary design goal in many applications.

Intercept points are specifications long used as key design criteria in the RF communications world as a metric for the intermodulation distortion performance of a device in the signal chain (e.g., amplifiers, mixers, etc.). Use of the intercept point, rather than strictly the intermodulation distortion, allows simpler system-level calculations. Intercept points, like noise figures, can be easily cascaded back and forth through a signal chain to determine the overall receiver chain intermodulation distortion performance. The relationship between intermodulation distortion and intercept point is depicted in Figure 85 and Figure 86.

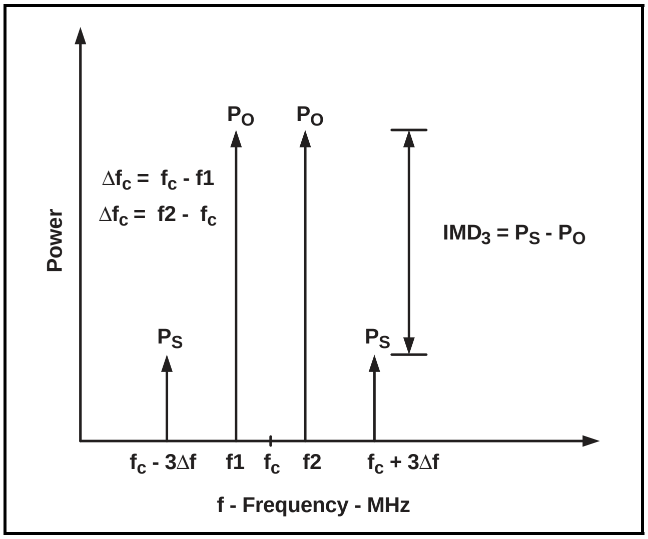


Figure 85.

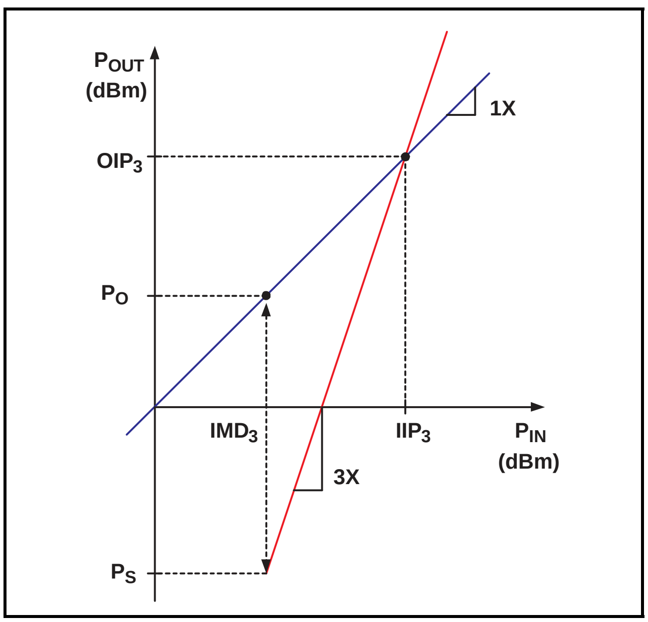


Figure 86.

Due to the intercept point ease of use in system level calculations for receiver chains, it has become the specification of choice for guiding distortion-related design decisions. Traditionally, these systems use primarily class-A, single-ended RF amplifiers as gain blocks. These RF amplifiers are typically designed to operate in a 50-Ω environment. Giving intercept points in dBm, implies an associated impedance (50 Ω).

However, with an operational amplifier, the output does not require termination as an RF amplifier would. Because closed-loop amplifiers deliver signals to their outputs regardless of the impedance present, it is important to comprehend this when evaluating the intercept point of an operational amplifier. The THS4271 yields optimum distortion performance when loaded with 150 Ω to 1 kΩ, very similar to the input impedance of an analog-to-digital converter over its input frequency band.

As a result, terminating the input of the ADC to 50Ω can actually be detrimental to systems performance.

The discontinuity between open-loop, class-A amplifiers and closed-loop, class-AB amplifiers becomes apparent when comparing the intercept points of the two types of devices. Equation 2 and Equation 3 give the definition of an intercept point, relative to the intermodulation distortion.

$$OIP_3 = P_O + \left(\frac{|IMD_3|}{2}\right) \text{ where} \tag{2}$$

$$P_O = 10\log\left(\frac{V_P^2}{2R_L \times 0.001}\right) \tag{3}$$

NOTE: P_O is the output power of a single tone, R_L is the load resistance, and V_P is the peak voltage for a single tone.

NOISE ANALYSIS

High slew rate, unity gain stable, voltage-feedback operational amplifiers usually achieve the slew rate at the expense of a higher input noise voltage. The 3-nV/√Hz input voltage noise for the THS4271 and THS4275 is, however, much lower than comparable amplifiers. The input-referred voltage noise, and the two input-referred current noise terms (3 pA/√Hz), combine to give low output noise under a wide variety of operating conditions. Figure 87 shows the amplifier noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

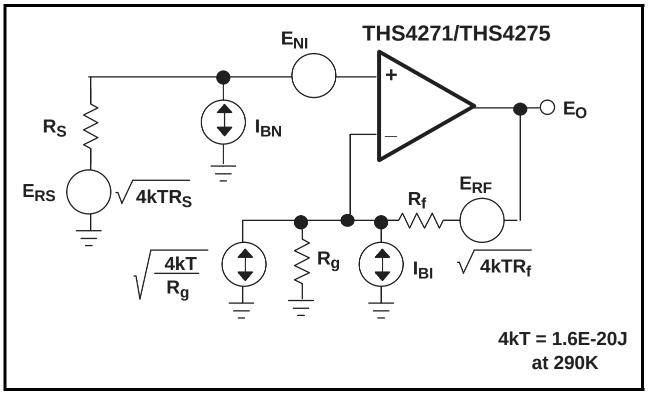


Figure 87. Noise Analysis Model

The total output spot noise voltage can be computed as the square of all square output noise voltage contributors. Equation 4 shows the general form for the output noise voltage using the terms shown in Figure 87:

$$E_O = \sqrt{\left(E_{NI}^{\ 2} + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_f\right)^2 + 4kTR_fNG} \tag{4}$$

Dividing this expression by the noise gain [NG=(1+ R_f/R_g)] gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 5:

$$E_O = \sqrt{E_{NI}^{\ 2} + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_f}{NG}\right)^2 + \frac{4kTR_f}{NG}} \tag{5}$$

Evaluation of these two equations for the circuit and component values shown in Figure 75 will give a total output spot noise voltage of 12.2 nV/√Hz and a total equivalent input spot noise voltage of 6.2 nV/√Hz. This includes the noise added by the resistors. This total input-referred spot noise voltage is not much higher than the 3-nV/√Hz specification for the amplifier voltage noise alone.

Driving Capacitive Loads

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an A/D converter, including additional external capacitance, which may be recommended to improve A/D linearity. A high-speed, high open-loop gain amplifier like the THS4271 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. When the primary considerations are frequency response flatness, pulse response fidelity, or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The *Typical Characteristics* show the recommended isolation resistor vs capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2 pF can begin to degrade the performance of the THS4271. Long PCB traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the THS4271 output pin (see the *Board Layout Guidelines* section).

The criterion for setting this $R_{(ISO)}$ resistor is a maximum bandwidth, flat frequency response at the load. For a gain of +2, the frequency response at the output pin is already slightly peaked without the capacitive load, requiring relatively high values of $R_{(ISO)}$ to flatten the response at the load. Increasing the noise gain also reduces the peaking.

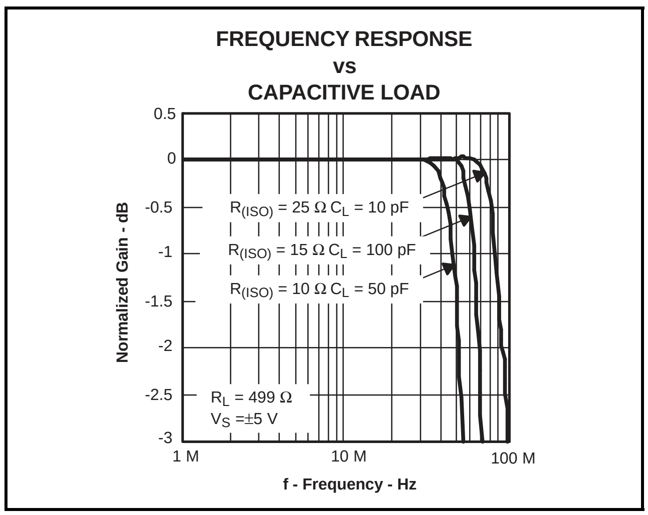


Figure 88. Isolation Resistor Diagram

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the THS4271 requires careful attention to board layout parasitics and external component types.

Recommendations that optimize performance include:

1. **Minimize parasitic capacitance to any ac ground for all of the signal I/O pins.** Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.
2. **Minimize the distance (< 0.25”) from the power supply pins to high frequency 0.1-μF de-coupling capacitors.** At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections should always be decoupled with these capacitors. Larger (2.2-μF to 6.8-μF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.
3. **Careful selection and placement of external components preserves the high frequency performance of the THS4271.** Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wire-wound type resistors in a high frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input-termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values > 2 kΩ, this parasitic capacitance can add a pole and/or a zero below 400-MHz that can effect circuit operation. Keep resistor values as low as possible, consistent with load driving considerations. A good starting point for design is to set the R_f to 249-Ω for low-gain, noninverting applications. Doing this automatically keeps the resistor noise terms low, and minimizes the effect of their parasitic capacitance.
4. **Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines.** For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs capacitive load. Low parasitic capacitive loads (<4 pF) may not need an $R_{(ISO)}$, since the THS4271 is nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an $R_{(ISO)}$ are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is normally not necessary onboard, and in fact, a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS4271 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of $R_{(ISO)}$ vs capacitive load. This does not preserve signal integrity or a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

5. **Socketing a high speed part like the THS4271 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create a troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS4271 onto the board.

PowerPAD™ DESIGN CONSIDERATIONS

The THS4271 and THS4275 are available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 89(a) and Figure 89(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 89(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows both assembly and thermal management in one manufacturing operation.

During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the heretofore awkward mechanical methods of heatsinking.

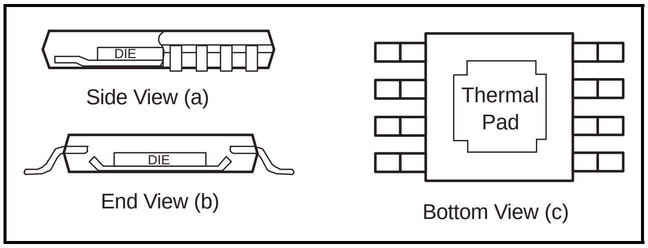


Figure 89. Views of Thermally Enhanced Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

PowerPAD PCB LAYOUT CONSIDERATIONS

1. Prepare the PCB with a top side etch pattern as shown in Figure 90. There should be etch for the leads as well as etch for the thermal pad.

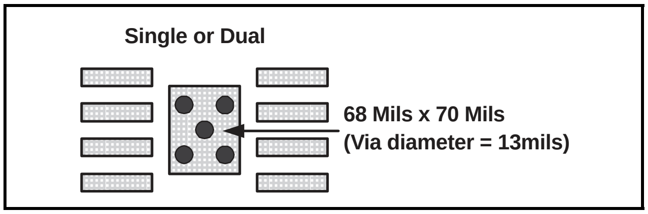


Figure 90. PowerPAD PCB Etch and Via Pattern

2. Place five holes in the area of the thermal pad. The holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. They help dissipate the heat generated by the THS4271 and THS4275 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered, so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This resistance makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS4271 and THS4275 PowerPAD package should make their connection to the internal ground plane, with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

For a given θ_{JA}, the maximum power dissipation is shown in Figure 91 and is calculated by the Equation 6:

$$P_D = \frac{T_{max} - T_A}{\theta_{JA}} \tag{6}$$

where:
P_D = Maximum power dissipation of THS4271 (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to the case
θ_{CA} = Thermal coefficient from the case to ambient air (°C/W).

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multi-amplifier devices. Because these devices have linear output stages (Class AB), most of the heat dissipation is at low output voltages with high output currents.

The other key factor when dealing with power dissipation is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. For a single package, the sum of the RMS output currents and voltages should be used to choose the proper package.

THERMAL ANALYSIS

The THS4271 device does not incorporate automatic thermal shutoff protection, so the designer must take care to ensure that the design does not violate the absolute maximum junction temperature of the device. Failure may result if the absolute maximum junction temperature of +150° C is exceeded.

The thermal characteristics of the device are dictated by the package and the PCB. Maximum power dissipation for a given package can be calculated using the following formula.

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}} \tag{7}$$

where:
P_{Dmax} is the maximum power dissipation in the amplifier (W).
T_{max} is the absolute maximum junction temperature (°C).
T_A is the ambient temperature (°C).
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).
θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).

For systems where heat dissipation is more critical, the THS4271 is offered in an 8-pin MSOP with PowerPAD. The thermal coefficient for the MSOP PowerPAD package is substantially improved over the traditional SOIC. Maximum power dissipation levels are depicted in the graph for the two packages. The data for the DGN package assumes a board layout that follows the PowerPAD layout guidelines referenced above and detailed in the PowerPAD application notes in the *Additional Reference Material* section at the end of the data sheet.

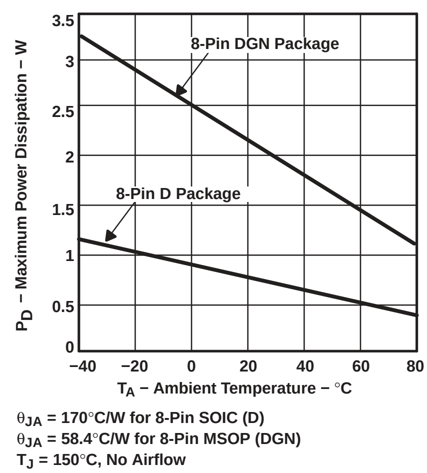


Figure 91. Maximum Power Dissipation vs Ambient Temperature

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to consider not only quiescent power dissipation, but also dynamic power dissipation. Often maximum power is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

DESIGN TOOLS

Performance vs Package Options

The THS4271 and THS4275 are offered in different package options. However, performance may be limited due to package parasitics and lead inductance in some packages. In order to achieve maximum performance of the THS4271 and THS4275, Texas Instruments recommends using the leadless MSOP (DRB) or MSOP (DGN) packages, in addition to proper high-speed PCB layout. Figure 92 shows the unity gain frequency response of the THS4271 using the leadless MSOP, MSOP, and SOIC package for comparison. Using the THS4271 and THS4275 in a unity gain with the SOIC package may result in the device becoming unstable. In higher gain configurations, this effect is mitigated by the reduced bandwidth. As such, the SOIC is suitable for application with gains equal to or higher than +2 V/V or (–1 V/V).

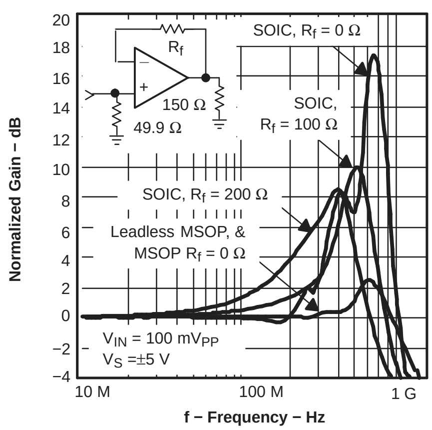


Figure 92. Effects of Unity Gain Frequency Response for DIfferential Packages

Evaluation Fixtures, Spice Models, and Applications Support

Texas Instruments is committed to providing its customers with the highest quality of applications support. To support this goal, evaluation boards have been developed for the THS4271 operational amplifier. Three evaluation boards are available: one THS4271 and one THS4275, both are configurable for different gains, and a third for a gain of +1 (THS4271 only). These boards are easy to use, allowing for straightforward evaluation of the device. These evaluation boards can be ordered through the Texas Instruments web site, www.ti.com, or through your local Texas Instruments sales representative. Schematics for the evaluation boards are shown below.

The THS4271/THS4275 EVM board shown in Figure 96 through Figure 99 is designed to accommodate different gain configurations. Its default component values are set to give a gain of 2. The EVM can be configured in a gain of +1; however, it is strongly not recommended. Evaluating the THS4271/THS4275 in a gain of 1 using this EVM may cause the part to become unstable. The stability of the device can be controlled by adding a large resistor in the feedback path, the performance is sacrificed. Figure 93 shows the small-signal frequency response of the THS4271 with different feedback resistors in the feedback path. Figure 94 is the small frequency response of the THS4271 using the gain of 1 EVM.

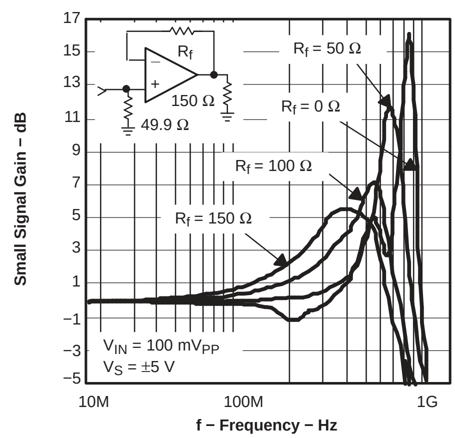


Figure 93. Frequency Response vs Feedback Resistor Using the EDGE #6439527 EVM

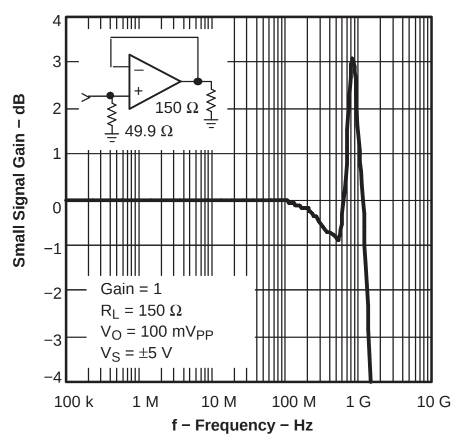


Figure 94. Frequency Response Using the EDGE #6443547 EVM

The peaking in the frequency response is due to the lead inductance in the feedback path. Each pad and trace on a PCB has an inductance associated with it, which in conjunction with the inductance associated with the package may cause peaking in the frequency response, causing the device to become unstable.

In order to achieve the maximum performance of the device, PCB layout is very critical. Texas Instruments has developed an EVM for the evaluation of the THS4271 in a gain of 1. The EVM is shown in Figure 101 through Figure 104. This EVM is designed to minimize peaking in the unity gain configuration.

Minimizing the inductance in the feedback path is critical for reducing the peaking of the frequency response in unity gain. The recommended maximum inductance allowed in the feedback path is 4 nH. This can be calculated by using Equation 8.

$$L(nH) = K\ell\left[\ln\frac{2\ell}{W + T} + 0.223\frac{W + T}{\ell} + 0.5\right]$$

where:
W = Width of trace in inches.
ℓ = Length of the trace in inches.
T = Thickness of the trace in inches.
K = 5.08 for dimensions in inches, and K = 2 for dimensions in cm.

(8)

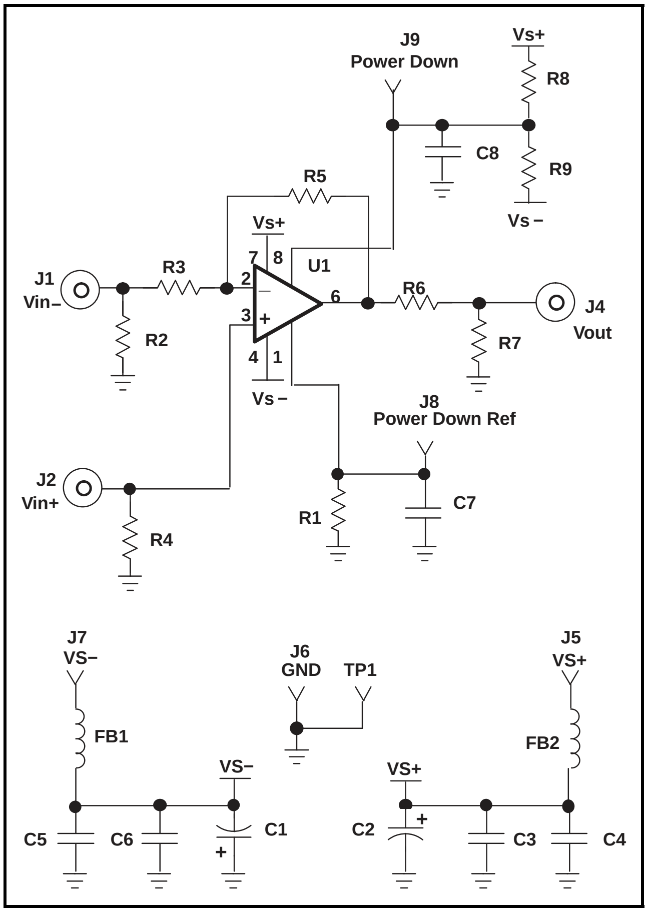


Figure 95. THS4271/THS4275 EVM Circuit Configuration

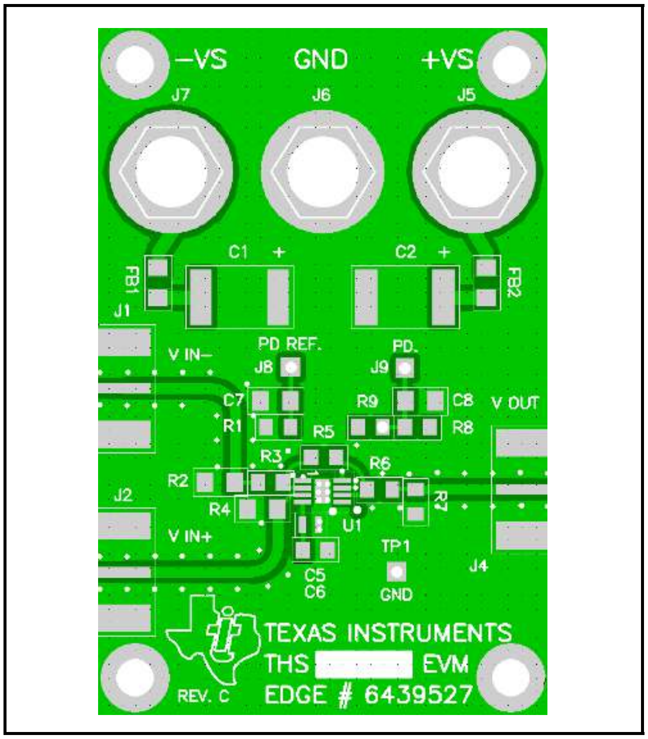


Figure 96. THS4271/THS4275 EVM Board Layout (Top Layer)

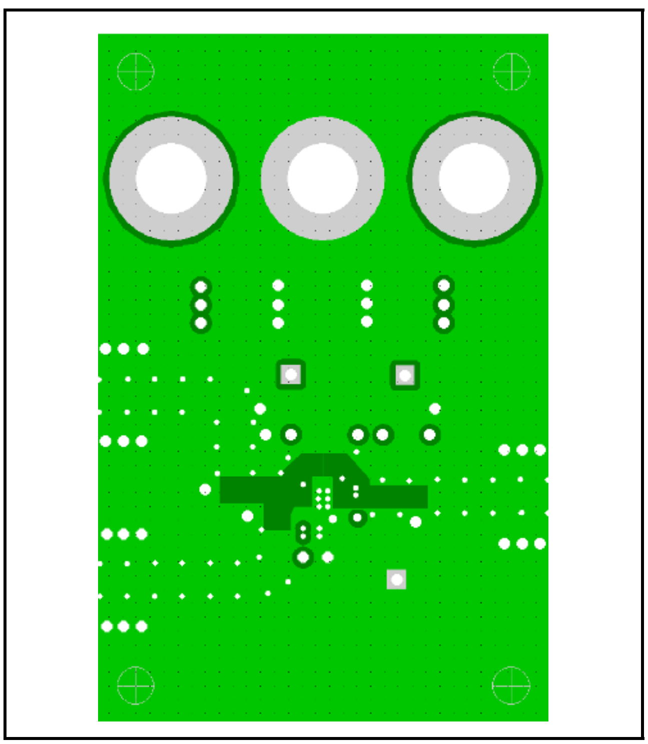


Figure 97. THS4271/THS4275 EVM Board Layout (Second Layer, Ground)

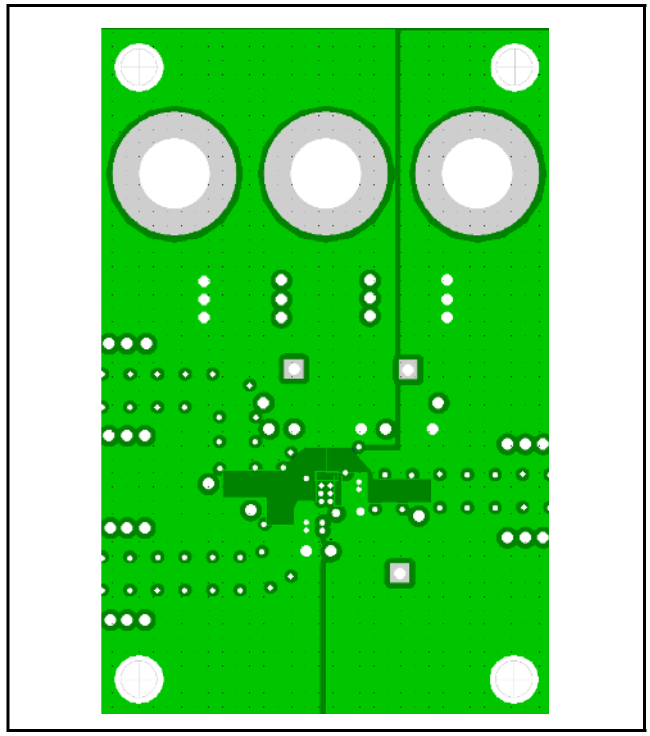


Figure 98. THS4271/THS4275 EVM Board Layout (Third Layer, Power)

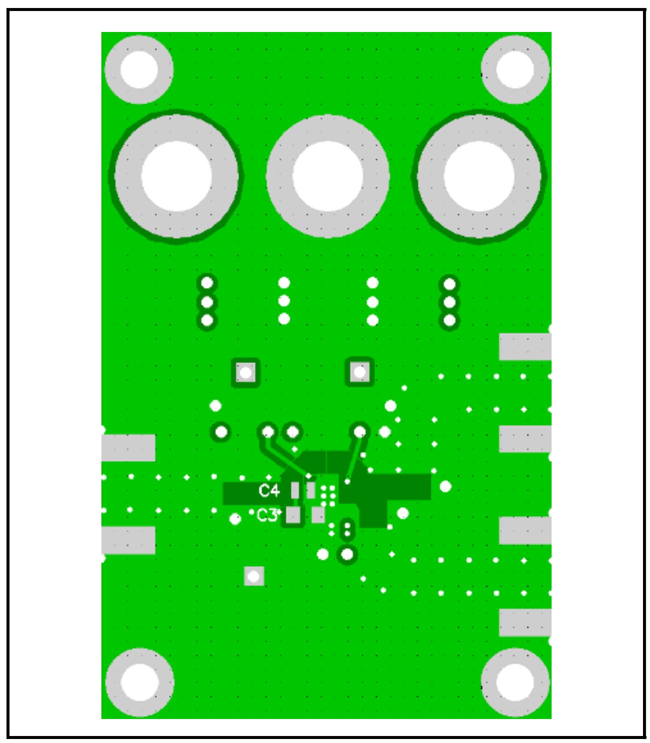


Figure 99. THS4271/THS4275 EVM Board Layout (Bottom Layer)

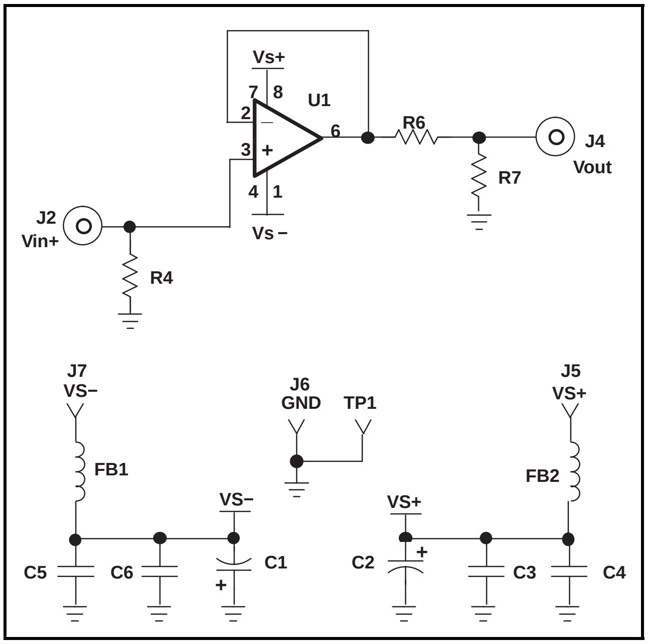


Figure 100. THS4271 Unity Gain EVM Circuit Configuration

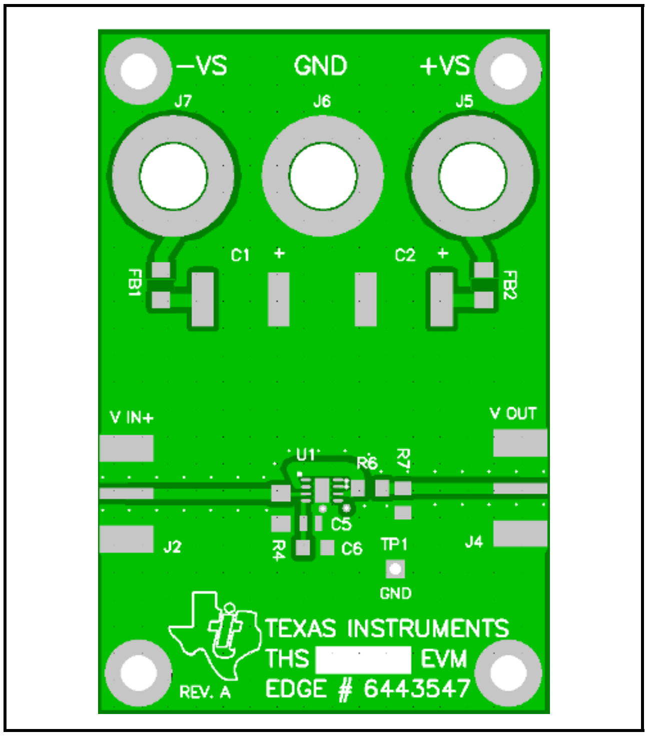


Figure 101. THS4271 Unity Gain EVM Board Layout (Top Layer)

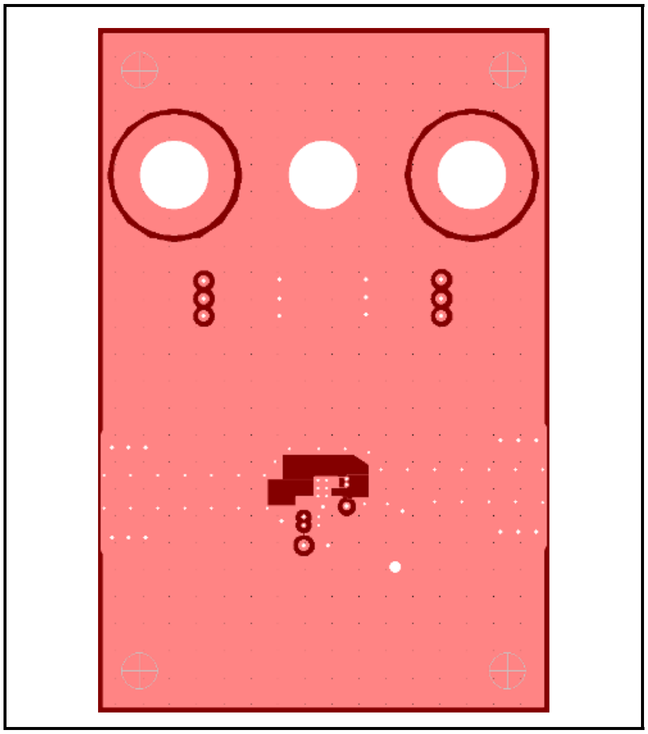


Figure 102. THS4271 Unity Gain EVM Board Layout (Second Layer, Ground)

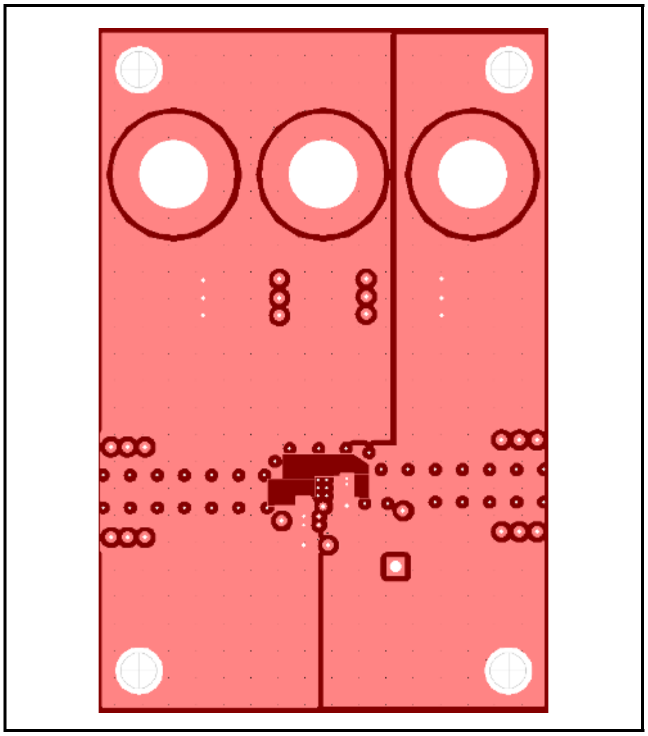


Figure 103. THS4271 Unity Gain EVM Board Layout (Third Layer, Power)

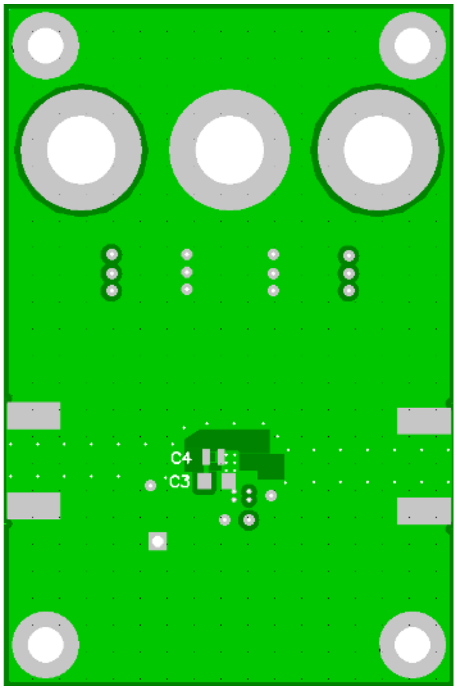


Figure 104. THS4271 Unity Gain EVM Board Layout

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the THS4271 is available through either the Texas Instruments web site (www.ti.com) or as one model on a disk from the Texas Instruments Product Information Center (1-800-548-6132). The PIC is also available for design assistance and detailed product information at this number. These models do a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. They are not intended to model the distortion characteristics of the amplifier, nor do they attempt to distinguish between the package types in their small-signal ac performance. Detailed information about what is and is not modeled is contained in the model file itself.

ADDITIONAL REFERENCE MATERIALS

- *PowerPAD Made Easy*, application brief (SLMA004)
- *PowerPAD Thermally Enhanced Package*, technical brief (SLMA002)

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (January, 2004) to Revision F **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4271D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4271	Samples
THS4271DG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4271	
THS4271DGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BEY	Samples
THS4271DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BFQ	Samples
THS4271DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BFQ	Samples
THS4271DGNRG4	LIFEBUY	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BFQ	
THS4271DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4271	Samples
THS4275D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4275	Samples
THS4275DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BFR	Samples
THS4275DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4275	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF THS4271 :

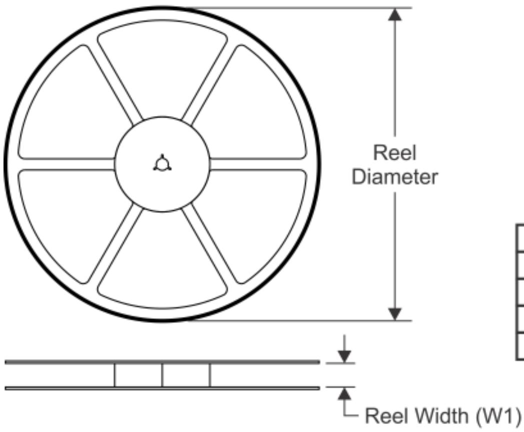
- Enhanced Product : THS4271-EP

NOTE: Qualified Version Definitions:

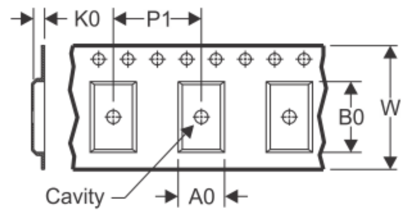
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

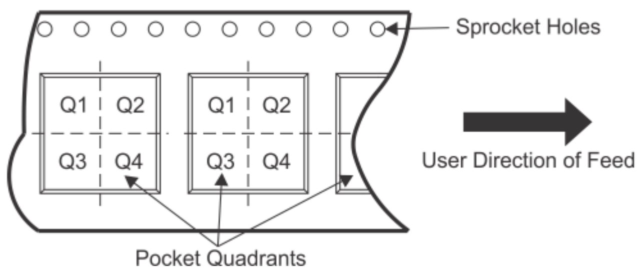


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

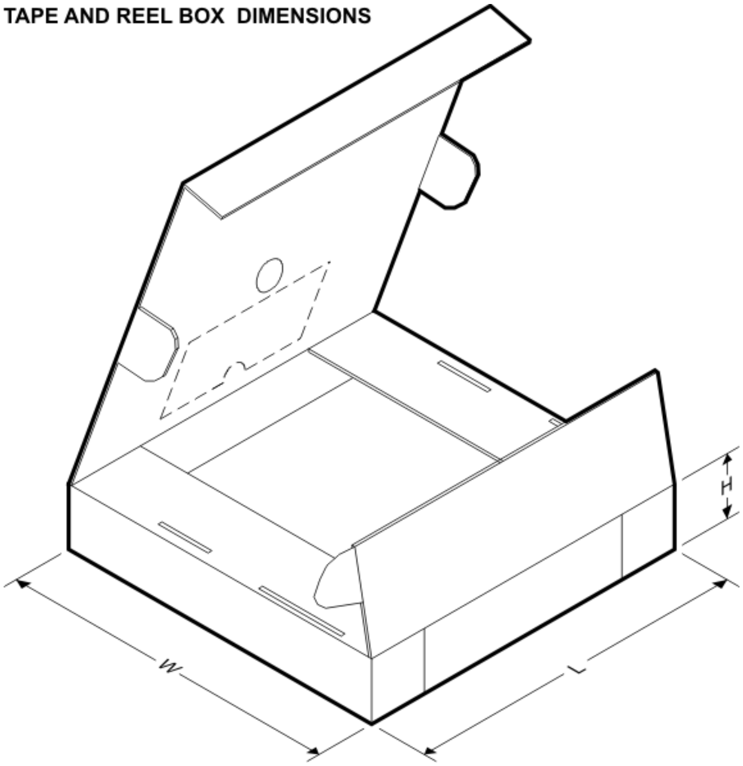
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4271DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

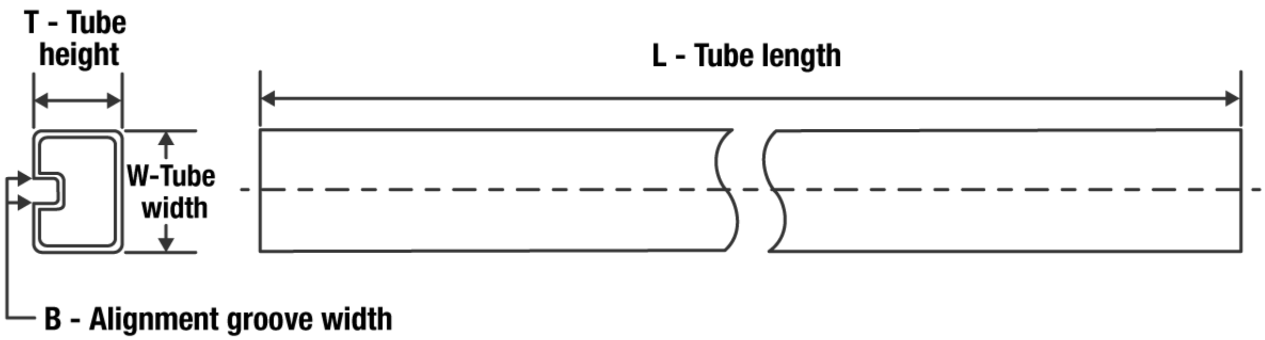
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4271DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0

TUBE



*All dimensions are nominal

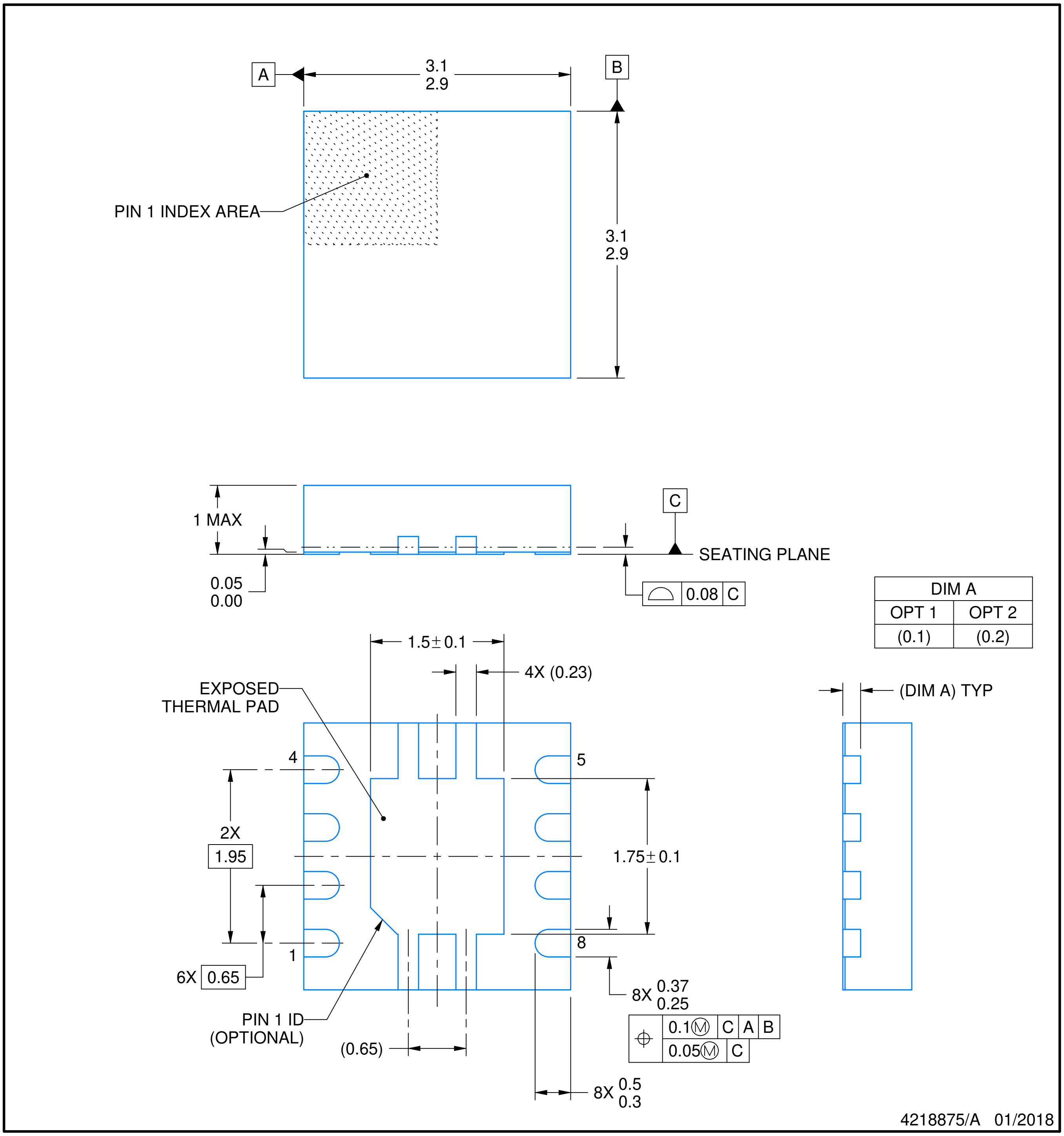
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS4271D	D	SOIC	8	75	505.46	6.76	3810	4
THS4271DG4	D	SOIC	8	75	505.46	6.76	3810	4
THS4275D	D	SOIC	8	75	505.46	6.76	3810	4

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

VSON - 1 mm max height

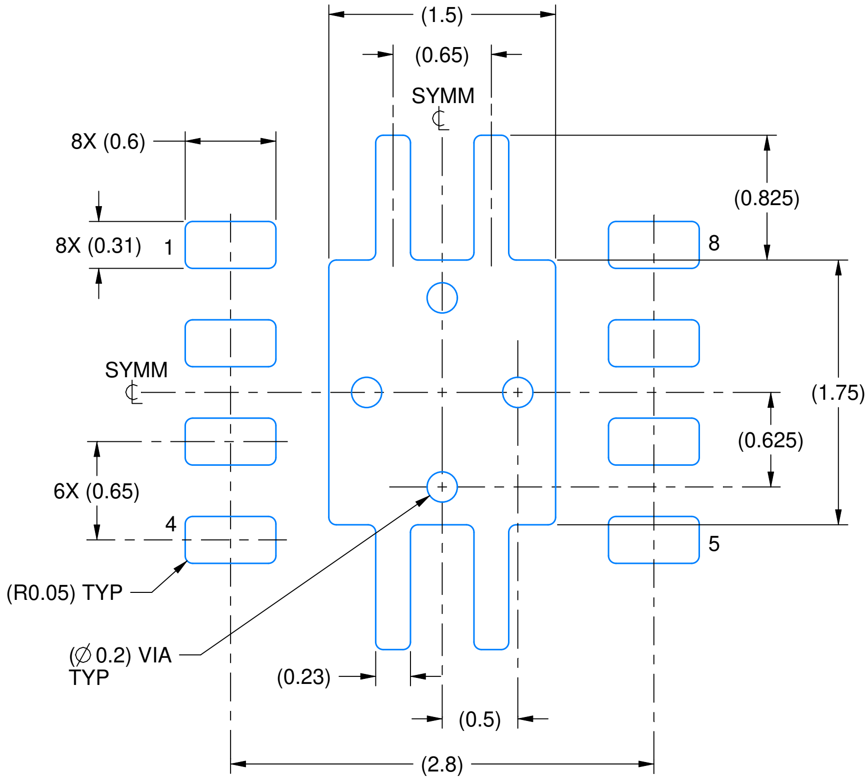
PLASTIC SMALL OUTLINE - NO LEAD



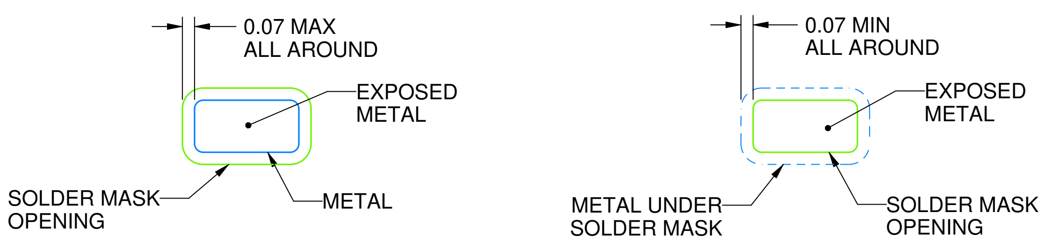
DIM A	
OPT 1	OPT 2
(0.1)	(0.2)

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

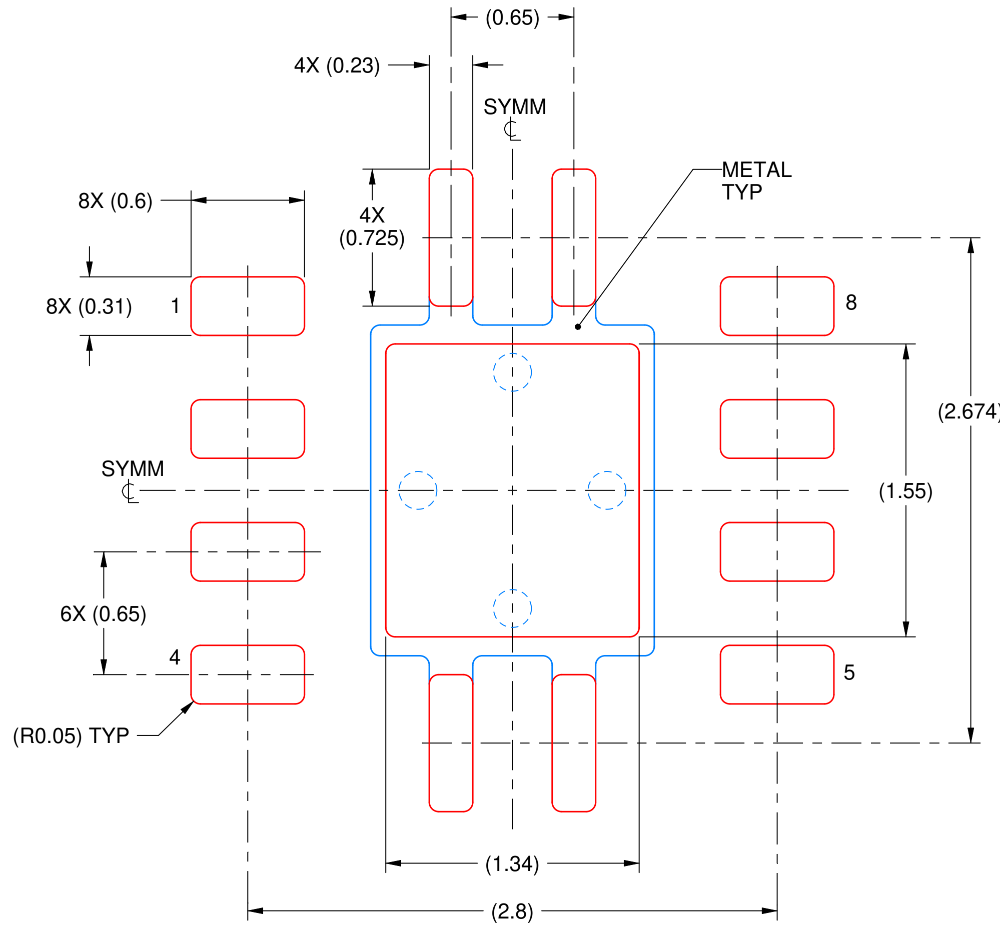
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

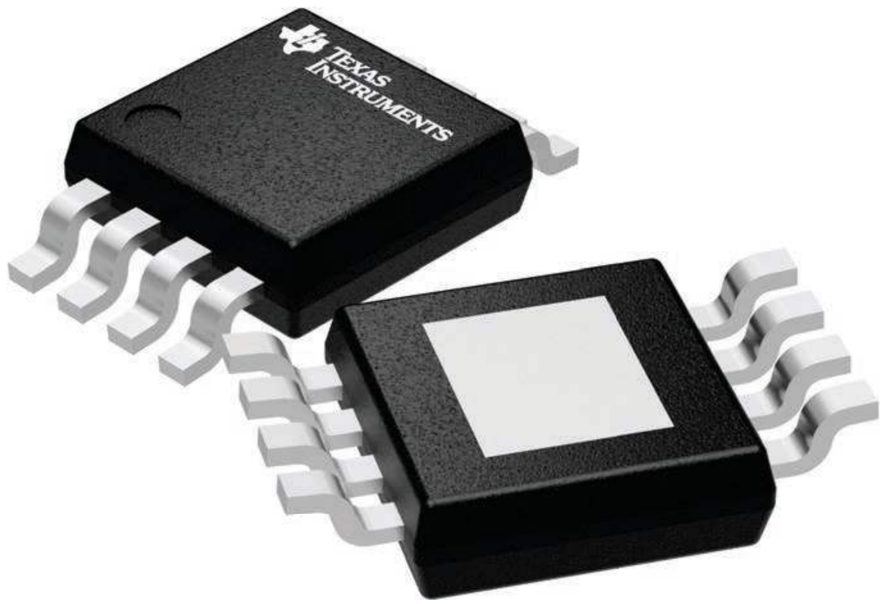
EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



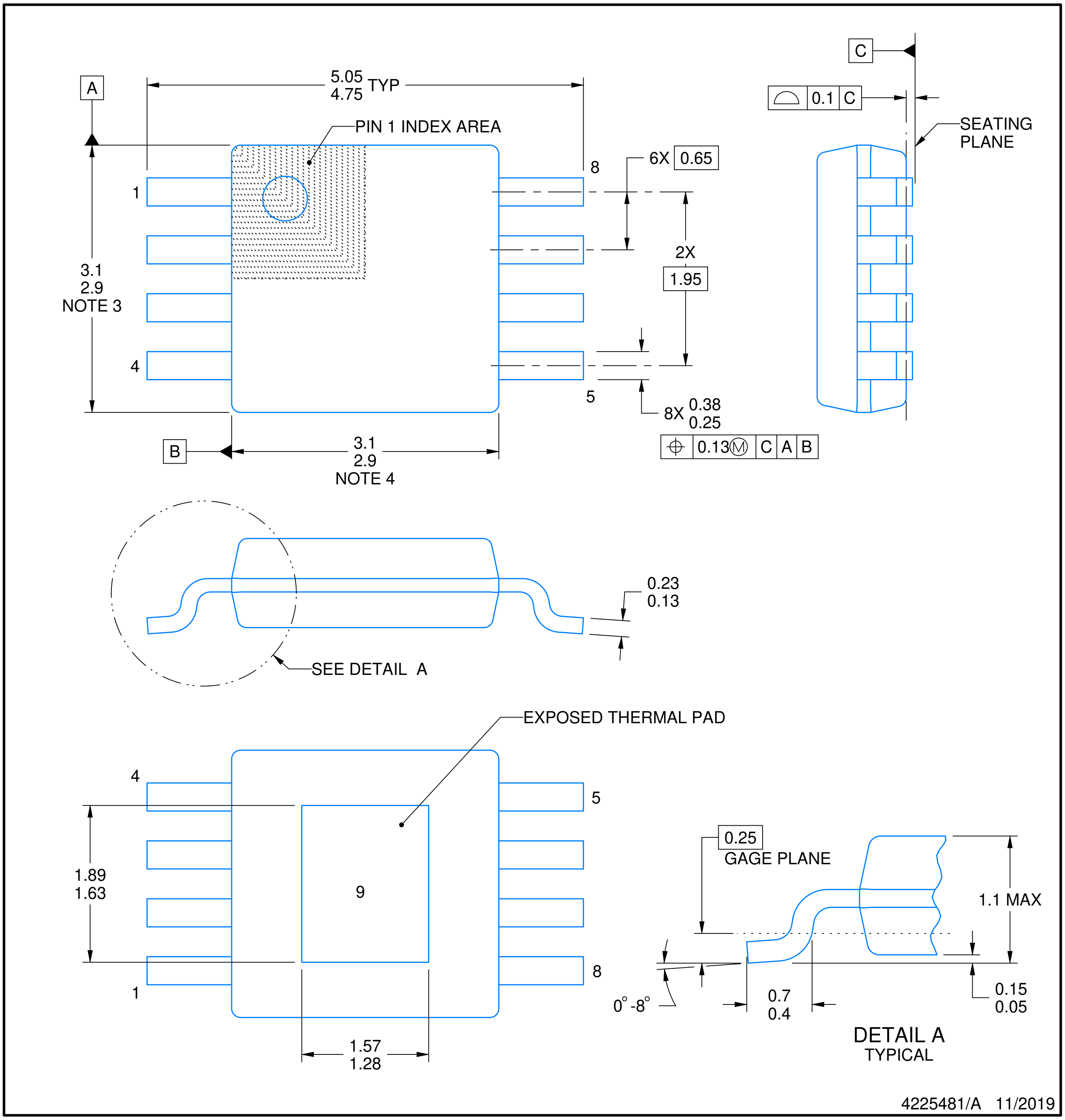
4225482/A

PACKAGE OUTLINE

DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

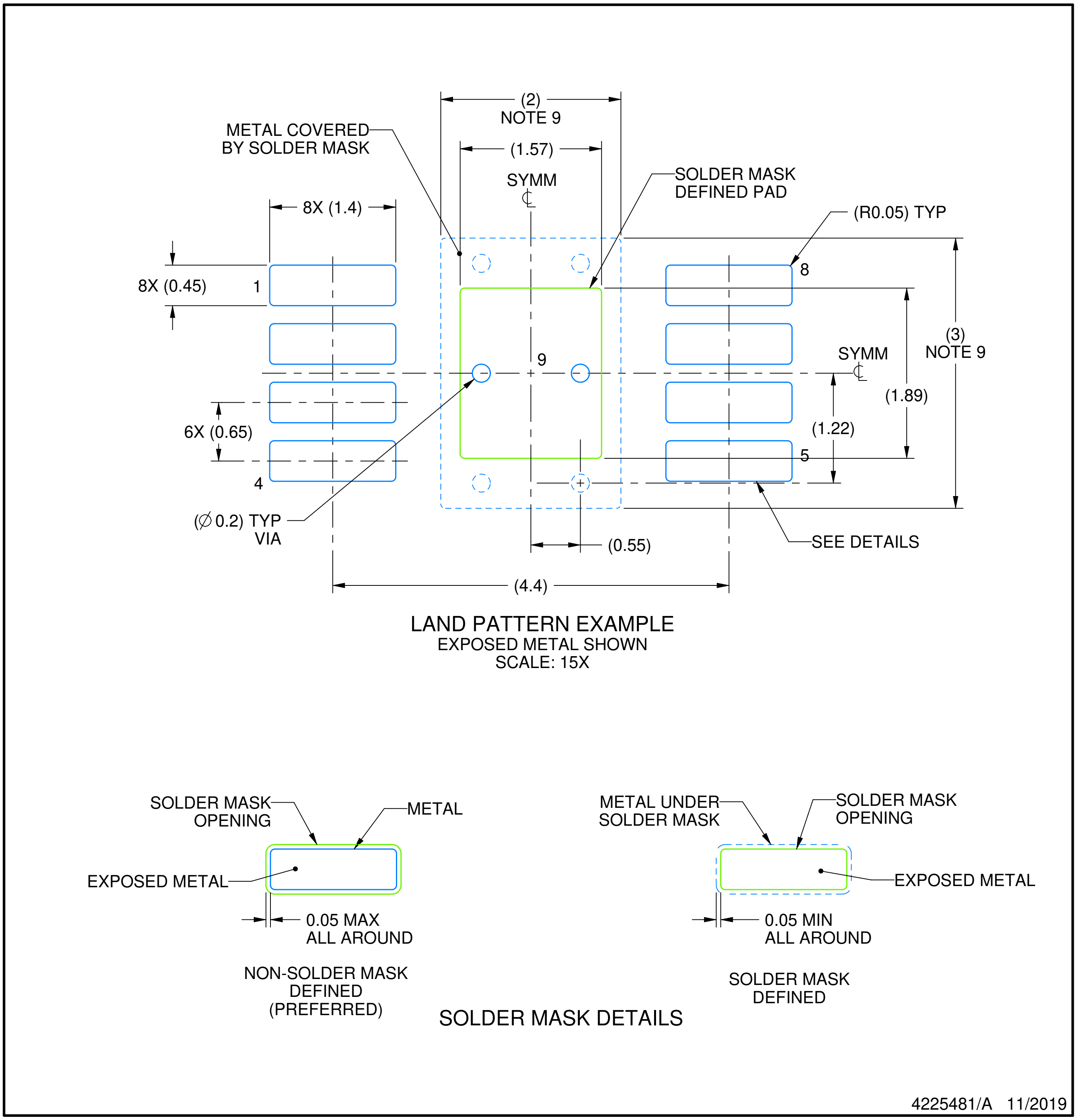


4225481/A 11/2019

PowerPAD is a trademark of Texas Instruments.

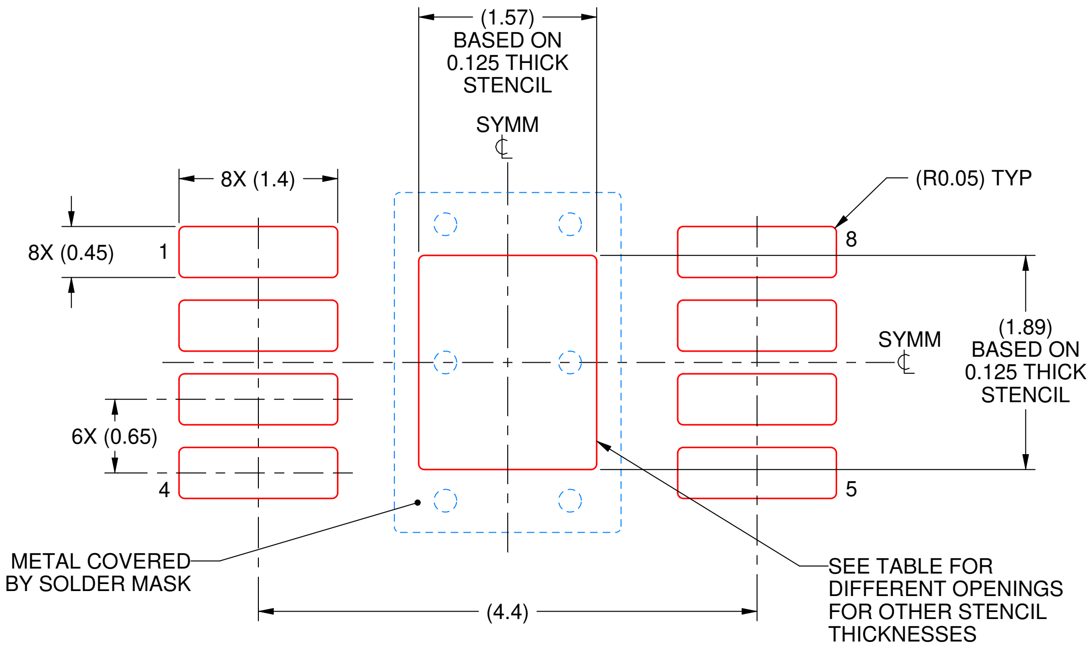
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



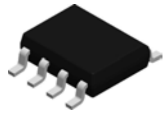
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

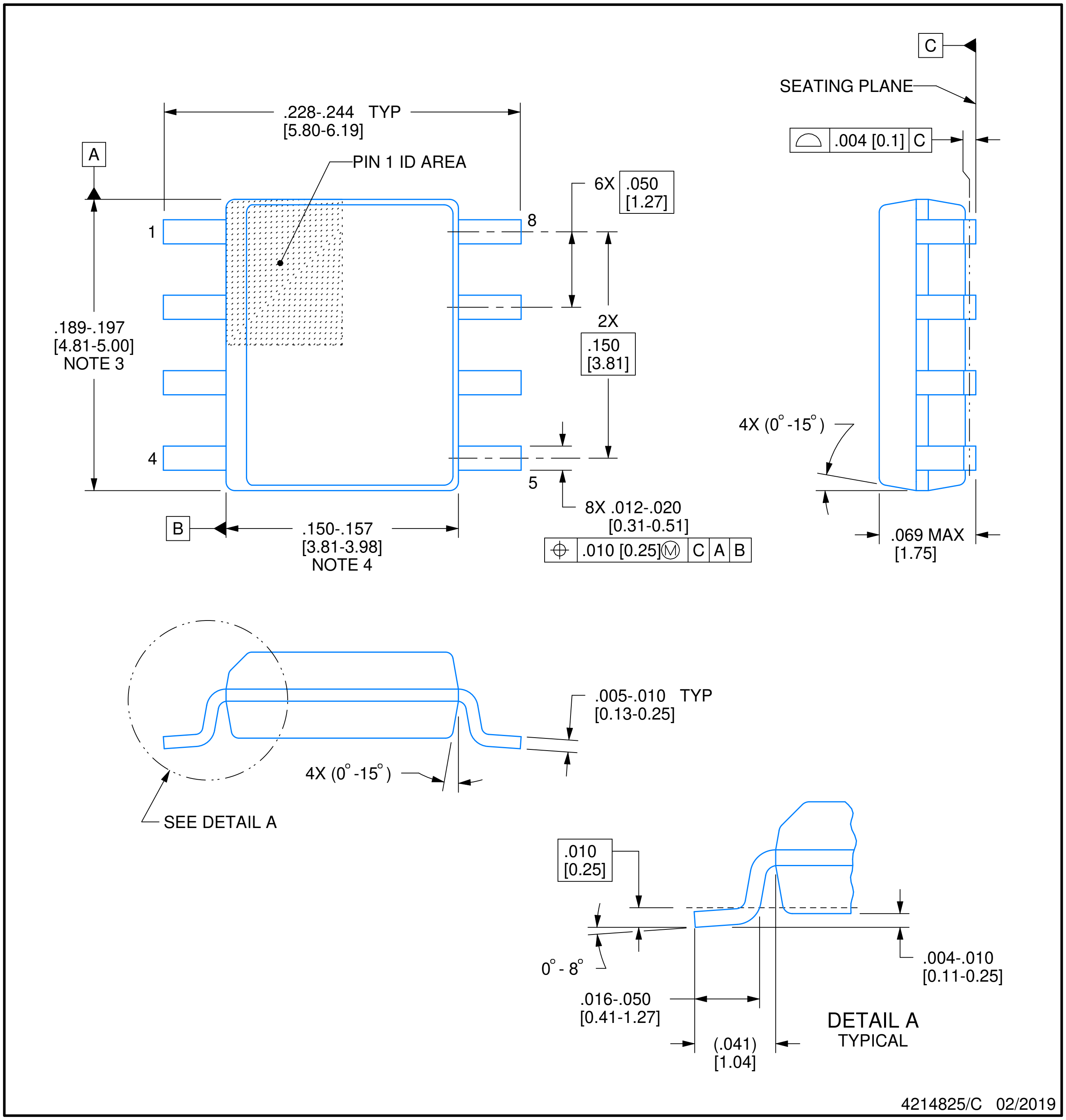
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

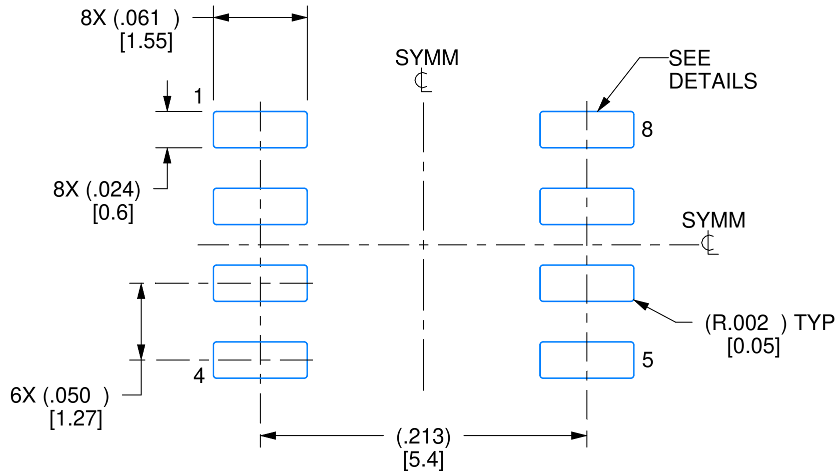




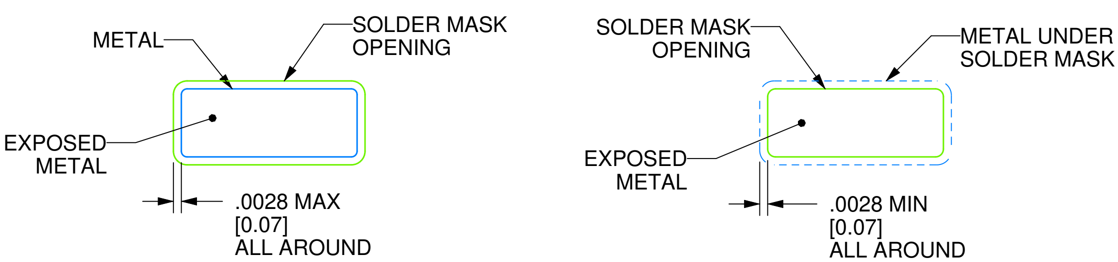
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

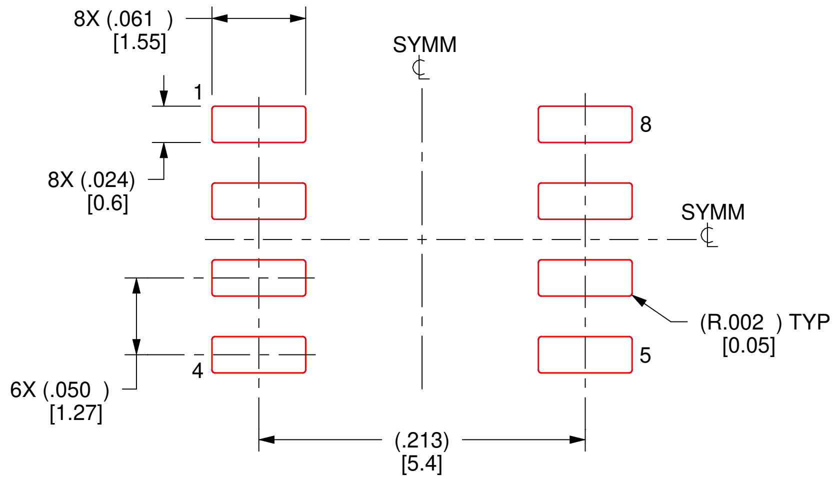
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



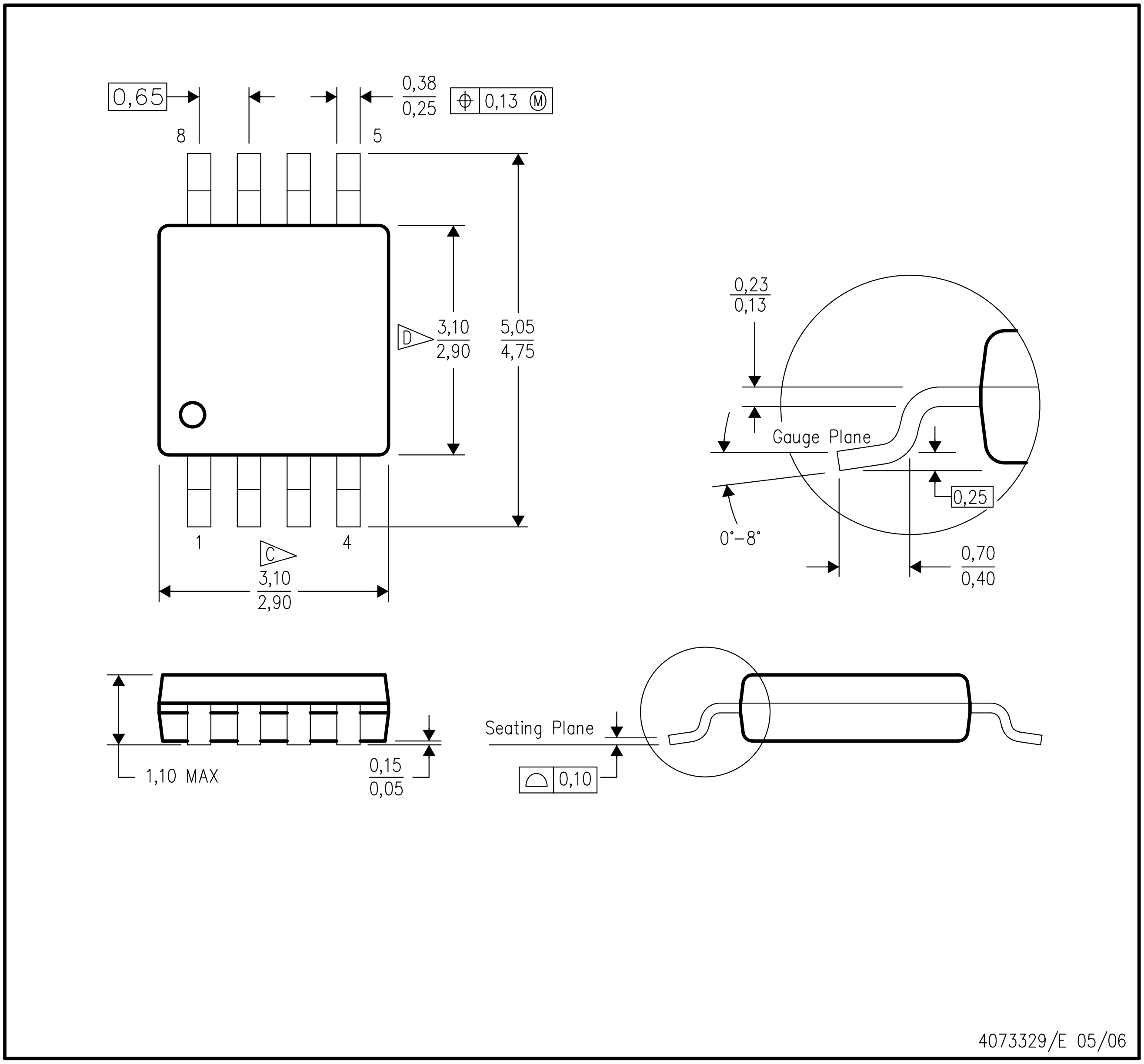
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

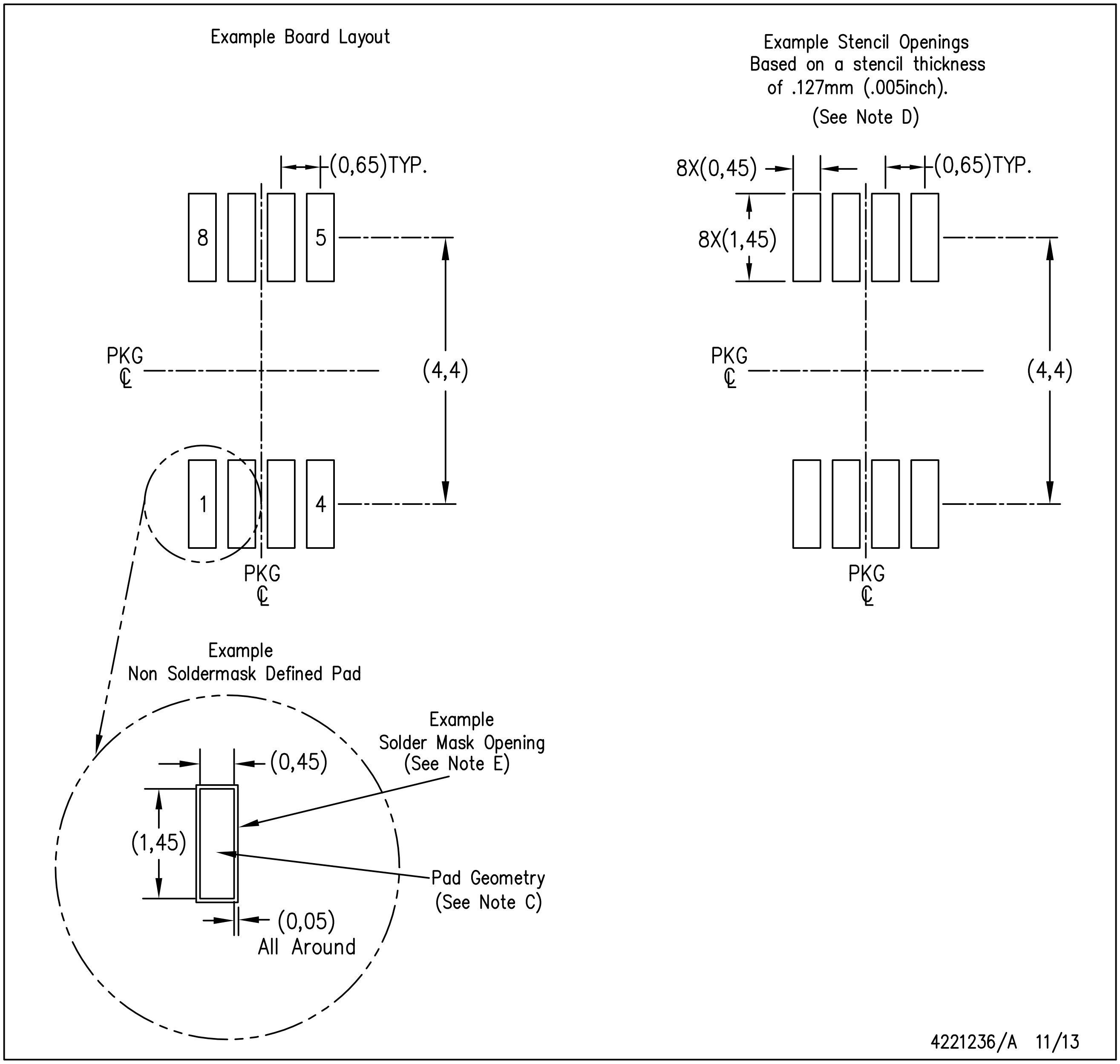
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.