μPA2813T1L

P-channel MOSFET
–30 V, –27 A, 6.2 mΩ

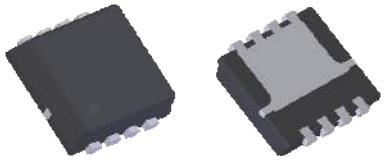
R07DS0763EJ0102
Rev.1.02
May. 28, 2013

Description

The μPA2813T1L is P-channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of portable equipment.

Features

- V_{DSS} = –30 V (T_A = 25°C)
- Low on-state resistance
  — $R_{DS(on)}$ = 6.2 mΩ MAX. (V_{GS} = –10 V, I_D = –27 A)
- 4.5 V Gate-drive available
- Small & thin type surface mount package with heat spreader
- Pb-free and Halogen free



8-pin HVSON(3333)

Ordering Information

Part No.	Lead Plating	Packing	Package
μPA2813T1L-E2-AT *1	Pure Sn	Tape 3000 p/reel	8-pin HVSON (3333) typ. 0.028 g

Note: *1. Pb-free (This product does not contain Pb in external electrode and other parts.)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	∓27	A
Drain Current (pulse) *1	$I_{D(pulse)}$	∓108	A
Total Power Dissipation *2	P_{T1}	1.5	W
Total Power Dissipation (PW = 10 sec) *2	P_{T2}	3.8	W
Total Power Dissipation (T_C = 25°C)	P_{T3}	52	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current *3	I_{AS}	23	A
Single Avalanche Energy *3	E_{AS}	54	mJ

Thermal Resistance

Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	83.3	°C/W
Channel to Case (Drain) Thermal Resistance	$R_{th(ch-C)}$	2.4	°C/W

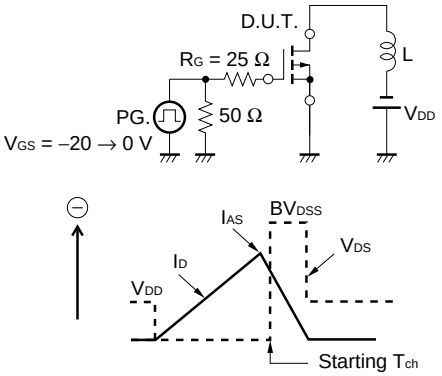
Notes: *1. PW ≤ 10 μs, Duty Cycle ≤ 1%
*2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mmt
*3. Starting T_{ch} = 25°C, V_{DD} = –15 V, R_G = 25 Ω, V_{GS} = –20 → 0 V, L = 100 μH

Electrical Characteristics (T_A = 25°C)

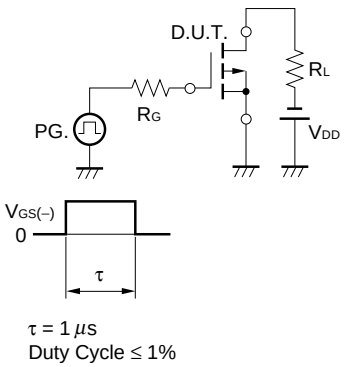
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			−1	μA	V_{DS} = −30 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}			∓100	nA	V_{GS} = ∓20 V, V_{DS} = 0 V
Gate Cut-off Voltage	$V_{GS(off)}$	−1.0		−2.5	V	V_{DS} = −10 V, I_D = −1 mA
Forward Transfer Admittance *1	$\|y_{fs}\|$	8.0			S	V_{DS} = −10 V, I_D = −13.5 A
Drain to Source On-state Resistance *1	$R_{DS(on)1}$		4.8	6.2	mΩ	V_{GS} = −10 V, I_D = −27 A
	$R_{DS(on)2}$		9	13	mΩ	V_{GS} = −4.5 V, I_D = −13.5 A
Input Capacitance	C_{iss}		3130		pF	V_{DS} = −10 V,
Output Capacitance	C_{oss}		1490		pF	V_{GS} = 0 V,
Reverse Transfer Capacitance	C_{rss}		1290		pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$		16		ns	V_{DD} = −15 V, I_D = −13.5 A,
Rise Time	t_r		41		ns	V_{GS} = −10 V,
Turn-off Delay Time	$t_{d(off)}$		196		ns	R_G = 10 Ω
Fall Time	t_f		234		ns	
Total Gate Charge	Q_G		80		nC	V_{DD} = −24 V,
Gate to Source Charge	Q_{GS}		9		nC	V_{GS} = −10 V,
Gate to Drain Charge	Q_{GD}		42		nC	I_D = −27 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.9		V	I_F = 27 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}		173		ns	I_F = 27 A, V_{GS} = 0 V,
Reverse Recovery Charge	Q_{rr}		270		nC	di/dt = 100 A/μs

Note: *1. Pulsed

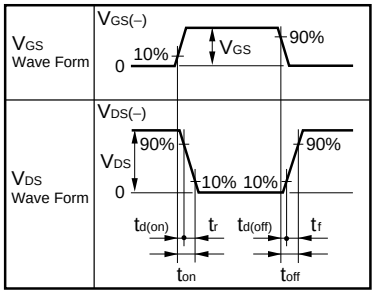
TEST CIRCUIT 1 AVALANCHE CAPABILITY



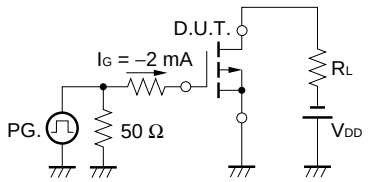
TEST CIRCUIT 2 SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1%

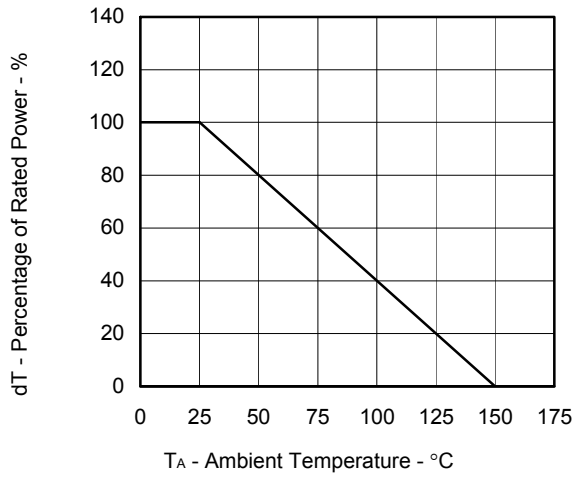


TEST CIRCUIT 3 GATE CHARGE

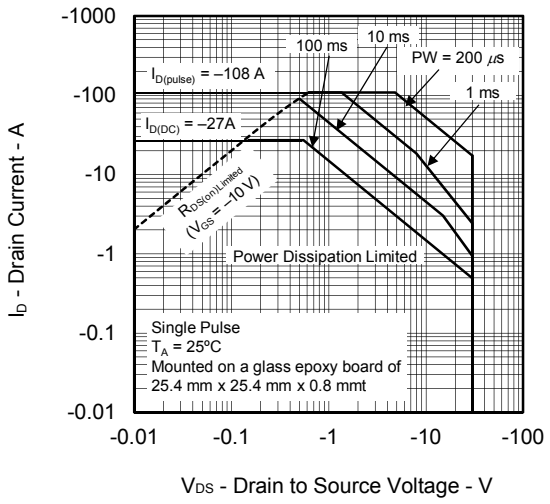


Typical Characteristics (T_A = 25°C)

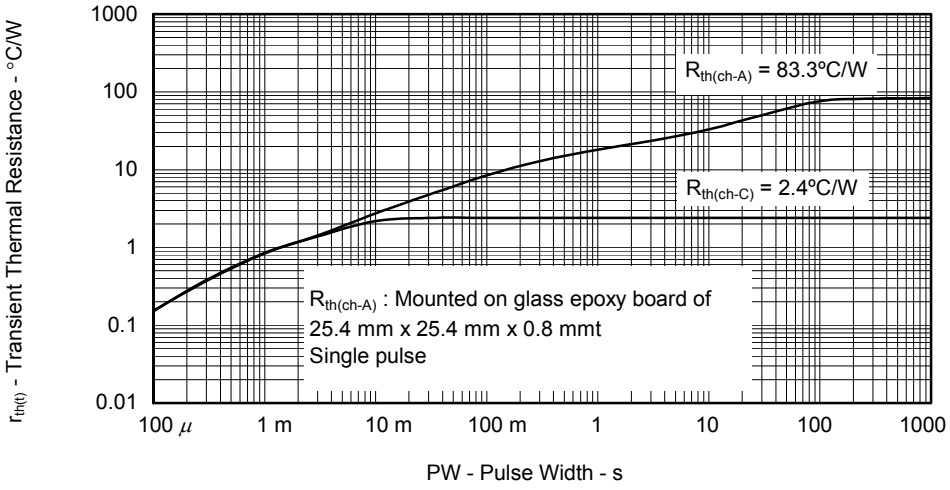
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



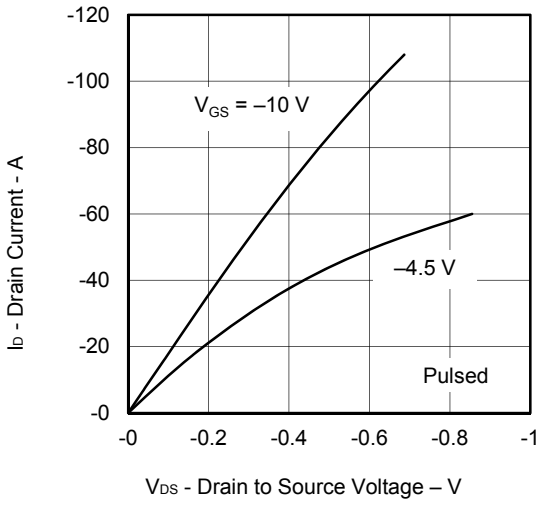
FORWARD BIAS SAFE OPERATING AREA



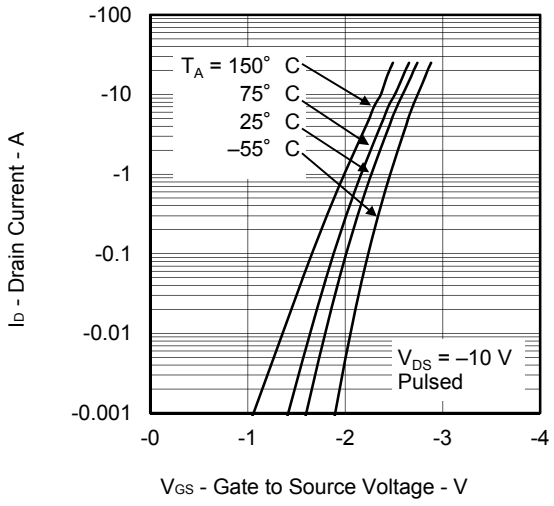
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



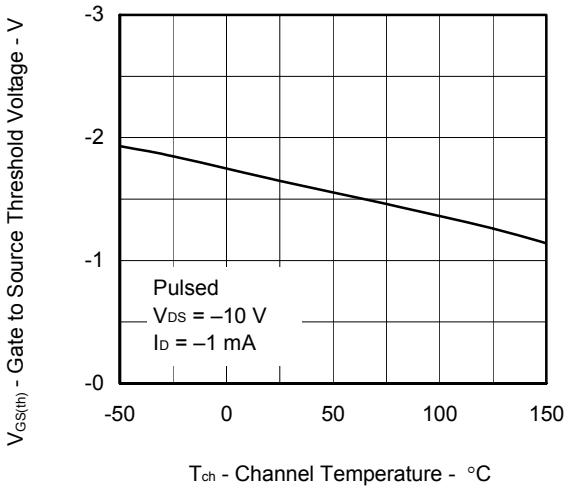
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



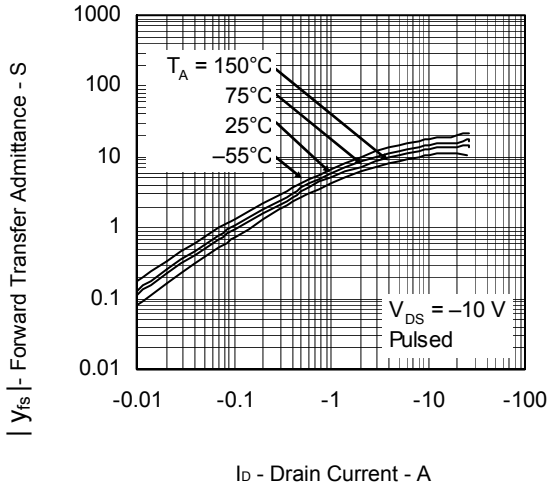
FORWARD TRANSFER CHARACTERISTICS



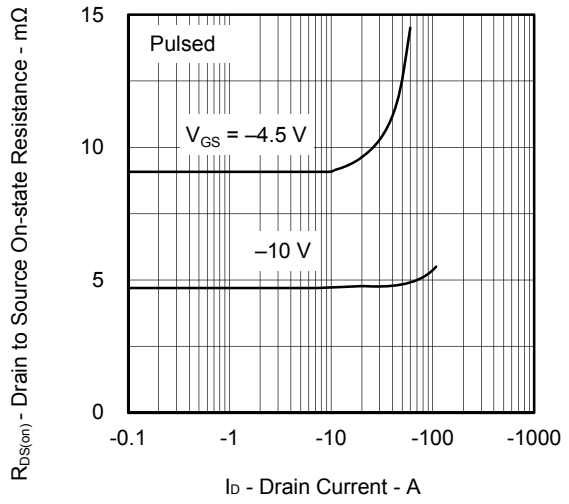
GATE CUT-OFF VOLTAGE vs.CHANNEL TEMPERATURE



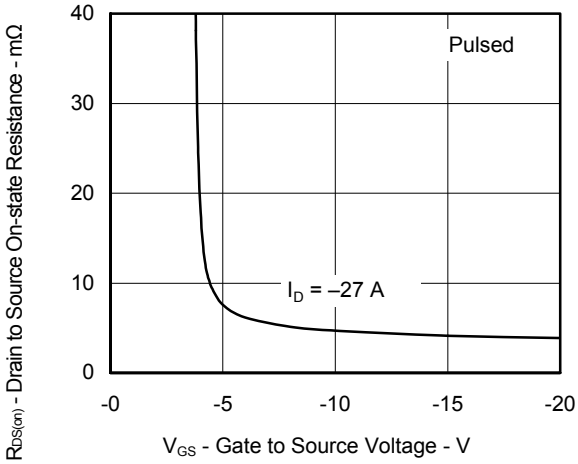
FORWARD TRANSFER ADMITANCE vs. DRAIN CURRENT



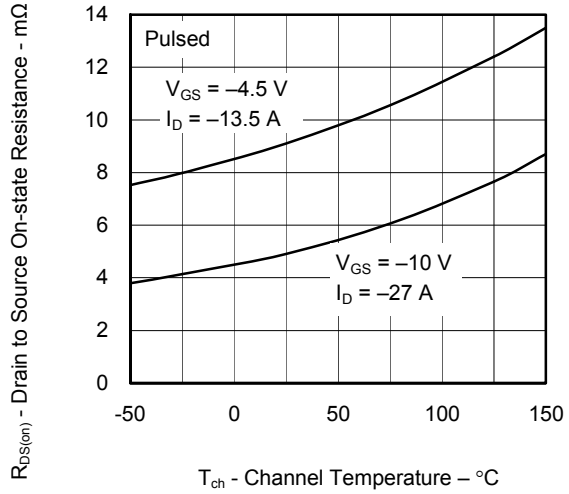
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



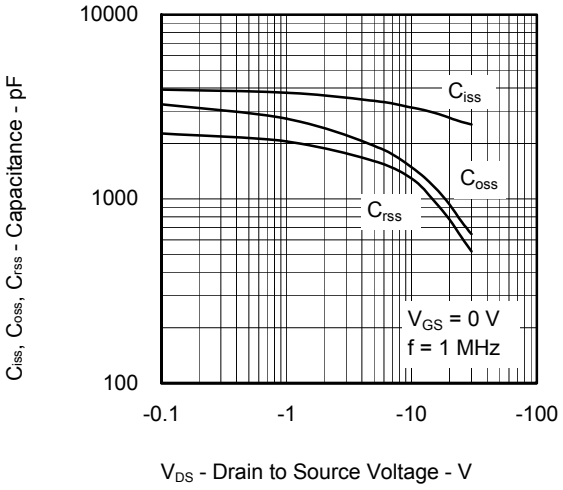
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



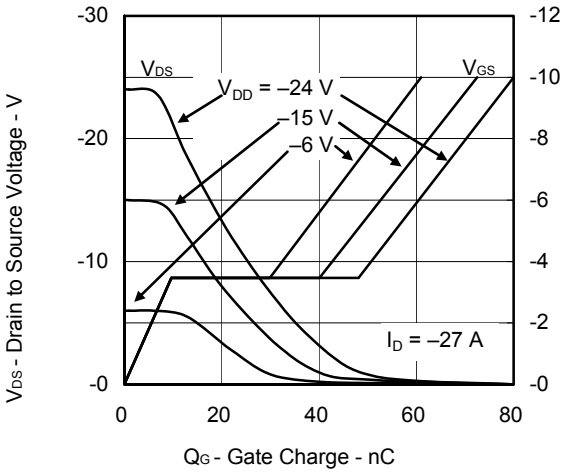
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



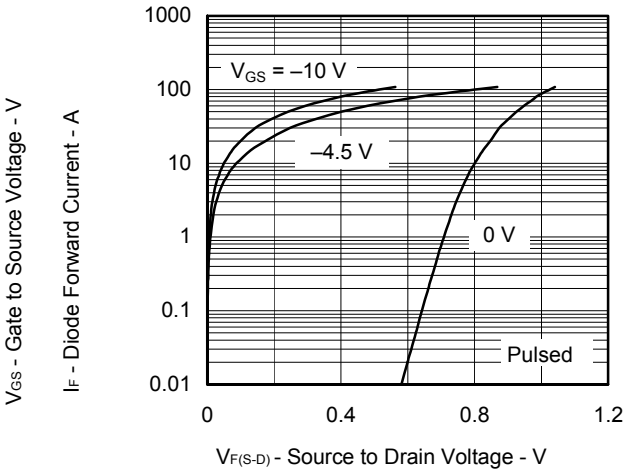
CAPACITANCE vs. DRAIN TOSOURCE VOLTAGE



DYNAMIC INPUT/OUTPUT CHARACTERISTICS

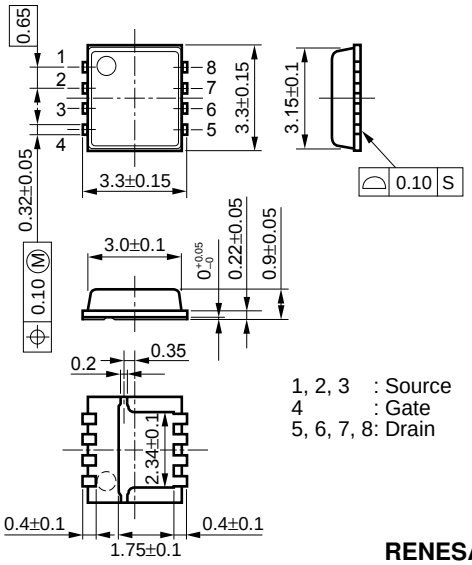


SOURCE TO DRAIN DIODE FORWARD VOLTAGE



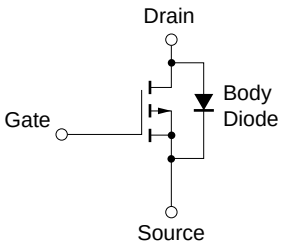
Package Drawings (Unit: mm)

8-pin HVSON (3333)



RENESAS Package code : PVSN0008JD-A

Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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