



COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET

Product Summary

Device	BV _{DSS}	R _{DS(ON)} Max	I _D Max T _A = +25°C	
		1.5Ω @ V _{GS} = 4.5V	0.40A	
0.1	001/	2.0Ω @ V _{GS} = 2.5V 0.35	0.35A	
Q1	30V	3.0Ω @ V _{GS} = 1.8V	0.28A	
		4.5Ω @ V _{GS} = 1.5V	0.23A	
		5Ω @ V _{GS} = -4.5V	-0.22A	
00	001/	6Ω @ V _{GS} = -2.5V -0.2	-0.20A	
Q2	-30V	7Ω @ V _{GS} = -1.8V	-0.18A	
		10Ω @ V _{GS} = -1.5V	-0.15A	

Description and Applications

This MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}) yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

- General Purpose Interfacing Switch
- Power Management Functions
- Analog Switch

Features and Benefits

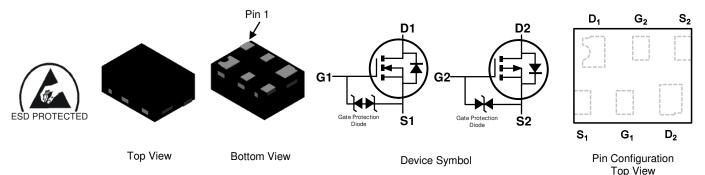
- Low On-Resistance
- Very Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Ultra-Small Surface Mount Package 0.8mm x 0.6mm
- ESD Protected Gate
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen- and Antimony-Free. "Green" Device (Note 3)
- The DMC31D5UDAQ is suitable for automotive applications requiring specific change control; This part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.

https://www.diodes.com/quality/product-definitions/

Mechanical Data

- Case: X2-DFN0806-6
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish Matte Tin Annealed over Copper Lead-Frame.
 Solderable per MIL-STD-202, Method 208 (3)
- Weight: 0.027 grams (Approximate)

X2-DFN0806-6



Ordering Information (Note 4)

ı	Part Number	Case	Packaging	
	DMC31D5UDAQ-7B	X2-DFN0806-6	10,000/Tape & Reel	

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



Top View

B6 = Product Type Marking Code Bar Denotes Pin 1



Maximum Ratings Q1 N-CHANNEL (@ TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit			
Drain-Source Voltage			V_{DSS}	30	V	
Gate-Source Voltage			V_{GSS}	±12	V	
Continuous Dusin Comment (Nata F) V	_ ' H	T _A = +25°C	- I _D	0.4	۸	
Continuous Drain Current (Note 5) V _{GS} = 4.5V		T _A = +70°C		0.32	^	
Maximum Continuous Body Diode Forward Current	(Note 6)	Is	0.8	Α		
Pulsed Drain Current (Note 6)			I _{DM}	0.8	Α	

Maximum Ratings Q2 P-CHANNEL (@ T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit	
Drain-Source Voltage			V _{DSS}	-30	V	
Gate-Source Voltage			V_{GSS}	±12	V	
Ocations Ducis Compat (Nata 5) V		$T_A = +25^{\circ}C$	- I _D	-0.22	^	
Continuous Drain Current (Note 5) V _{GS} = -4.5V		T _A = +70°C		-0.17	A	
Maximum Continuous Body Diode Forward Curren	Is	-0.8	Α			
Pulsed Drain Current (Note 6)			I _{DM}	-0.8	Α	

Thermal Characteristics (@ TA = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P_D	0.37	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	345	°C/W
Operating and Storage Temperature Range		$T_{J_i}T_{STG}$	-55 to +150	°C

Electrical Characteristics Q1 N-CHANNEL (@ TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	30	_	_	V	$V_{GS} = 0V, I_D = 250\mu A$
Zero Gate Voltage Drain Current @ T _C = +25°C	I _{DSS}	_	_	100	nA	$V_{DS} = 24V$, $V_{GS} = 0V$
Gate-Source Leakage	I _{GSS}	_	_	±10	μΑ	$V_{GS} = \pm 10V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(TH)}	0.4	_	1.0	V	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$
		_	1.2	1.5		$V_{GS} = 4.5V, I_D = 100mA$
Static Drain-Source On-Resistance		_	1.3	2.0	Ω	$V_{GS} = 2.5V, I_D = 50mA$
Static Diam-Source On-nesistance	R _{DS(ON)}	_	1.5	3.0		V _{GS} = 1.8V, I _D = 20mA
		_	1.8	4.5		$V_{GS} = 1.5V, I_D = 10mA$
Diode Forward Voltage	V_{SD}	_	0.6	1.0	V	$V_{GS} = 0V$, $I_S = 10mA$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	Ciss	1	22.6	_	pF	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Output Capacitance	Coss	1	2.68	_	pF	$V_{DS} = 15V, V_{GS} = 0V,$ f = 1.0MHz
Reverse Transfer Capacitance	C _{rss}	_	1.8	_	pF	1 - 1.000112
Total Gate Charge	Qg	_	0.38	_	nC	V 45V V 45V
Gate-Source Charge	Qgs	_	0.05	_	nC	$V_{GS} = 4.5V, V_{DS} = 15V,$ $I_{D} = 200mA$
Gate-Drain Charge	Q_{gd}		0.07	_	nC	1D = 20011IA
Turn-On Delay Time	t _{D(ON)}		3.2	_	ns	
Turn-On Rise Time			2.2	_	ns	$V_{DD} = 15V, V_{GS} = 4.5V,$
Turn-Off Delay Time			21	_	ns	$R_G = 2\Omega, I_D = 200 \text{mA}$
Turn-Off Fall Time	t _F	_	7.5	_	ns	1

Notes:

- 5. Device mounted on FR-4 PCB, with minimum recommended pad layout.
 6. Device mounted on minimum recommended pad layout test board, 10µs pulse duty cycle = 1%.
- 7. Short duration pulse test used to minimize self-heating effect.
- 8. Guaranteed by design. Not subject to product testing.



Electrical Characteristics Q2 P-CHANNEL (@ T_A = +25°C, unless otherwise specified.)

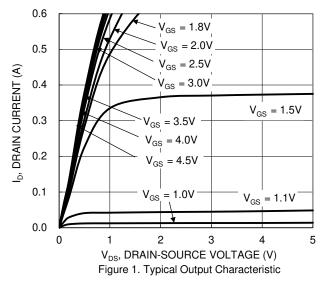
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	-30		_	V	$V_{GS} = 0V, I_D = -250\mu A$
Zero Gate Voltage Drain Current @ T _C = +25°C	IDSS	_	_	-100	nA	$V_{DS} = -24V, V_{GS} = 0V$
Gate-Source Leakage	I _{GSS}	_	_	±10	μΑ	$V_{GS} = \pm 10V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(TH)}	-0.4	1	-1.0	V	$V_{DS} = V_{GS}$, $I_D = -250\mu A$
		_	1.8	5		$V_{GS} = -4.5V, I_D = -100mA$
Static Drain-Source On-Resistance	D	_	2.3	6	Ω	$V_{GS} = -2.5V, I_D = -50mA$
Static Diam-Source Off-nesistance	R _{DS(ON)}	_	3	7		$V_{GS} = -1.8V, I_D = -20mA$
		_	3.4	10		$V_{GS} = -1.5V, I_D = -10mA$
Diode Forward Voltage	V _{SD}	_	-0.6	-1.0	V	$V_{GS} = 0V, I_{S} = -10mA$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	Ciss	_	21.8	_	pF	V 45V V 0V
Output Capacitance	Coss	_	2.82	_	pF	$V_{DS} = -15V, V_{GS} = 0V,$ f = 1.0MHz
Reverse Transfer Capacitance	C _{rss}	_	1.66	_	pF	1 = 1.000112
Total Gate Charge	Qg	_	0.35	_	nC	V 45V V 45V
Gate-Source Charge	Qgs	_	0.05	_	nC	$V_{GS} = -4.5V$, $V_{DS} = -15V$, $I_{D} = -200$ mA
Gate-Drain Charge	Q _{gd}	_	0.10	_	nC	1D = -20011IA
Turn-On Delay Time	t _{D(ON)}	_	3.5	_	ns	
Turn-On Rise Time Turn-Off Delay Time to		_	5.2	_	ns	$V_{DD} = -15V, V_{GS} = -4.5V,$
		_	18.8	_	ns	$R_G = 2\Omega, I_D = -200 \text{mA}$
		_	8.7	_	ns	1

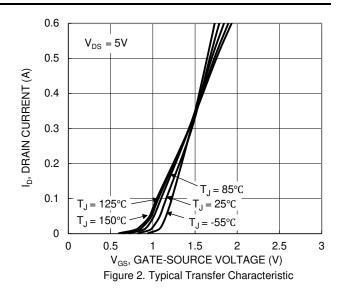
Notes:

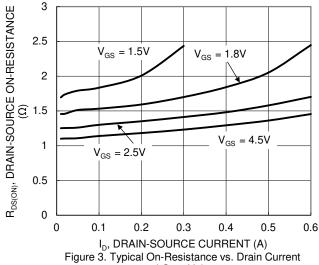
^{7.} Short duration pulse test used to minimize self-heating effect. 8. Guaranteed by design. Not subject to product testing.

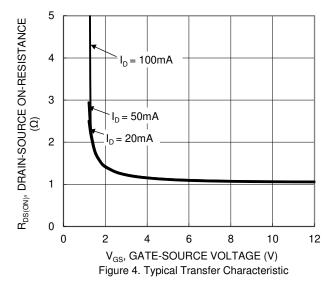


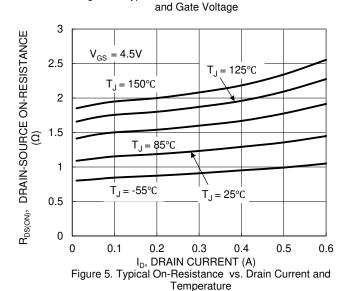
Typical Characteristics - N-CHANNEL

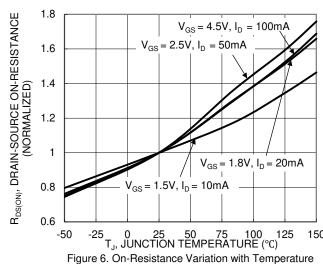












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Typical Characteristics - N-CHANNEL (continued)

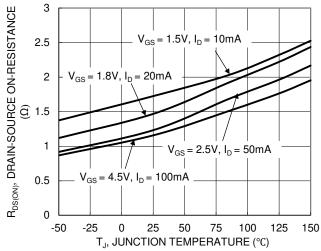
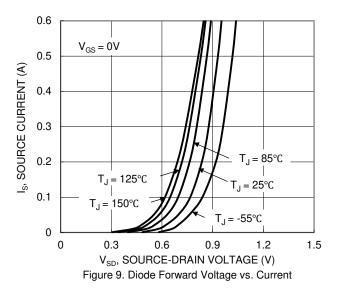


Figure 7. On-Resistance Variation with Temperature



4.5 4 3.5 3 2.5 SS 2 2 1.5 $V_{DS} = 15V, I_{D} = 8A$ 1 0.5 0 0 0.1 0.2 0.3 0.4 0.5 Qg (nC)

Figure 11. Gate Charge

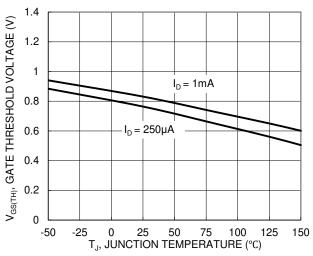
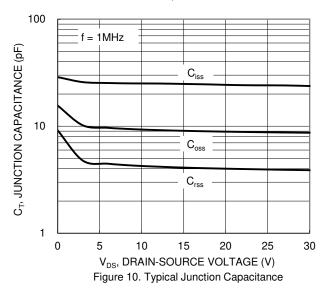
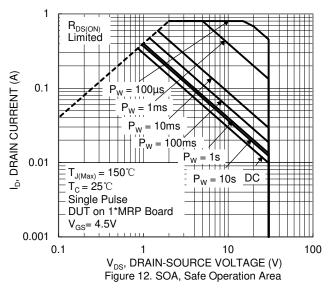


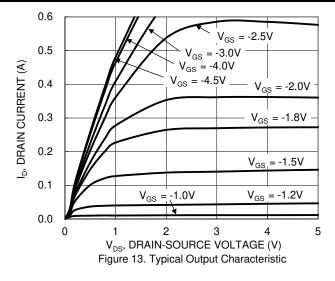
Figure 8. Gate Threshold Variation vs. Junction Temperature

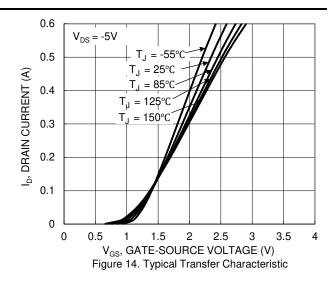


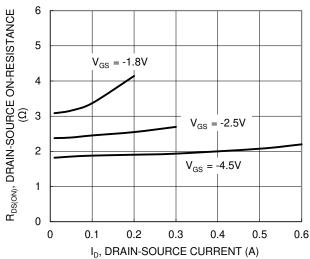




Typical Characteristics - P-CHANNEL







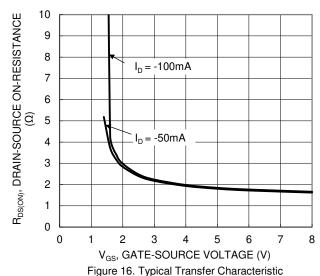
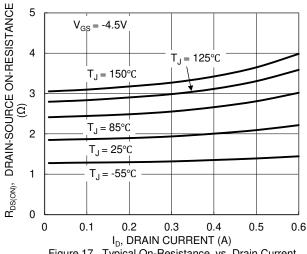


Figure 15. Typical On-Resistance vs. Drain Current and Gate Voltage



1.8 R_{DS(ON)}, DRAIN-SOURCE ON-RESISTANCE (NORMALIZED) $V_{GS} = -4.5V, I_D = -100mA$ 1.6 $V_{GS} = -2.5V, I_{D} = -50mA$ $V_{GS} = -1.8V, I_D = -20m_A$ 1.4 $V_{GS} = -1.5V, I_D = -10mA$ 1.2 1 8.0 0.6 125 -50 25 50 75 100 T_J, JUNCTION TEMPERATURE (°C)

Figure 17. Typical On-Resistance vs. Drain Current and Junction Temperature

Figure 18. On-Resistance Variation with Junction Temperature



Typical Characteristics - P-CHANNEL (continued)

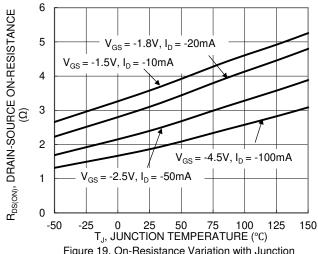


Figure 19. On-Resistance Variation with Junction Temperature

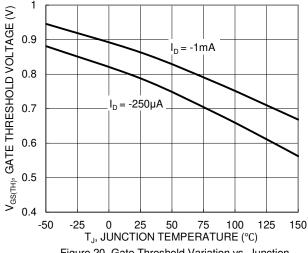


Figure 20. Gate Threshold Variation vs. Junction Temperature

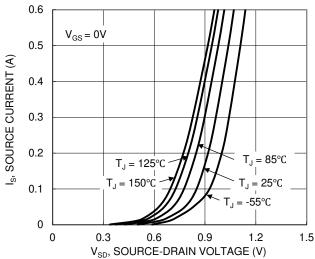


Figure 21. Diode Forward Voltage vs. Current

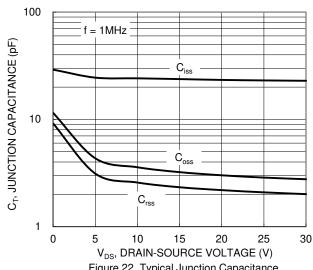
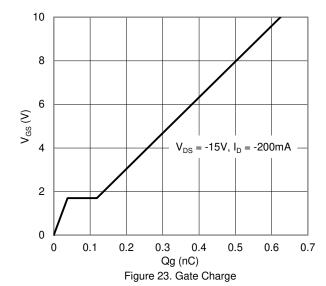


Figure 22. Typical Junction Capacitance

R_{DS(ON)} Limited

0.1



ID, DRAIN CURRENT (A) 0.01 =10s $T_{J(Max)}=150\,{}^{\circ}\mathrm{C}$ DC T_C = 25°C Single Pulse DUT on 1*MRP Board V_{GS}= -4.5V 0.001 0.1 10 V_{DS}, DRAIN-SOURCE VOLTAGE (V)

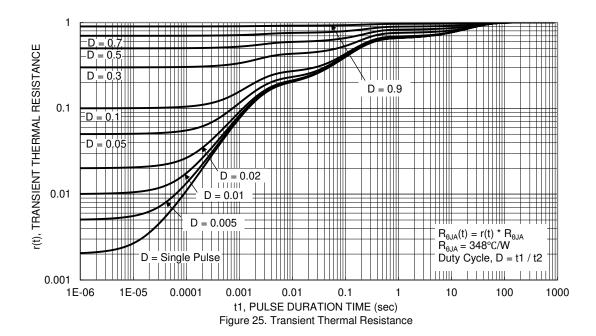
=1ms

=10ms

Figure 24. SOA, Safe Operation Area

100



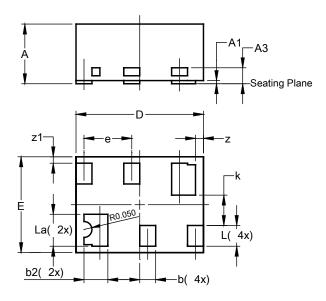




Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

X2-DFN0806-6

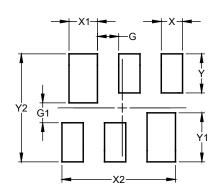


	X2-DFN0806-6						
Dim	Min	Max	Тур				
Α		0.40	0.36				
A1	0.00	0.03	0.02				
A3			0.10				
b	0.07	0.15	0.10				
b2	0.10	0.20	0.15				
D	0.75	0.85	0.80				
Е	0.55	0.65	0.60				
е			0.30				
k			0.19				
L	0.10	0.18	0.13				
La	0.17	0.25	0.20				
Z			0.05				
z1			0.04				
All Dimensions in mm							

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

X2-DFN0806-6



Dimensions	Value (in mm)
G	0.150
G1	0.140
Х	0.150
X1	0.200
X2	0.800
Υ	0.275
Y1	0.345
Y2	0.760



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